A 163-180 GHz 2×2 Amplifier-Doubler Array with Peak EIRP of +5 dBm

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***Abstract*— This paper presents a 2×2 amplifier-multiplier array with on-chip antennas at 163-180 GHz in 45 nm CMOS SOI technology. The measured EIRP is > 2 dBm at 165-175 GHz with a peak value of 5 dBm at 170 GHz meeting the stringiest metal-density rules for antennas. The amplifier-multiplier architecture is scalable to N×M arrays for high EIRP and transmit power.**

***Index Terms*— CMOS, doubler, frequency multiplier, mm-wave, on-chip antenna, THz sources.**

I. Introduction

Silicon systems at > 150 GHz are becoming more popular for active and passive imaging systems, point-to-point communications and wideband spectroscopy [1], [2]. SiGe and CMOS sources have always been a challenge above 150 GHz due to their limited f_t and f_{max}. There are several solutions which have been proposed: 1) Injection-locked or N-push oscillators [3]–[5], and 2) multipliers [6]–[8]. The oscillator approach results in narrowband systems which are not suitable for wideband applications such as active imaging systems with low speckle, THz network analyzers, and spectroscopy. The multiplier approach results in wideband systems which can cover a 20-60 GHz bandwidth and can be easily locked to a W-band reference for low phase noise. Both can be placed in N×M arrays with on-chip antennas so as to increase the power and equivalent isotropic radiated power (EIRP) of the transmitter source.

This paper presents a 2×2 multiplier array at 163-180 GHz with a peak EIRP of +5 dBm in 45nm CMOS technology meeting the stringiest metal-density rules for antennas.

II. Design

Fig. 1(a) presents the architecture of the 2×2 transmitter array where each amplifier-doubler is connected to an on-chip slot-ring antenna. The amplifier-doubler is similar to a design presented in [6] and results in ∼0 dBm of power at 180 GHz (Fig. 1(b)). In order to keep the antenna spacing $0.6\lambda_0$ at 180 GHz, and due to the layout consideration in 45nm CMOS where all the transistors have to be aligned in the same direction, the slot-ring antenna are fed on opposite sides for the left and right sides of the array. This configuration results in a 180° phase difference in the radiated fields from the left and right side antennas, which is not congruent with free-space power combining. Therefore, a branchline coupler is used before the amplifier-doublers at the left and right side antennas, and results in 3-dB power division and a 90° phase difference at 90 GHz. The output of the left and right side doublers are therefore 180° apart and the radiated fields are all in phase. Finally, a wilkinson power divider is used to divide the input signal in equal phase and amplitude between the top and bottom side of the array. This architecture is scalable to a 4×4 array (vertical and horizontal mirror with respect to the input port), using Wilkinson or active power dividers. In fact, the amplifier-multiplier approach is scalable to any N×M array size with no added complexity.

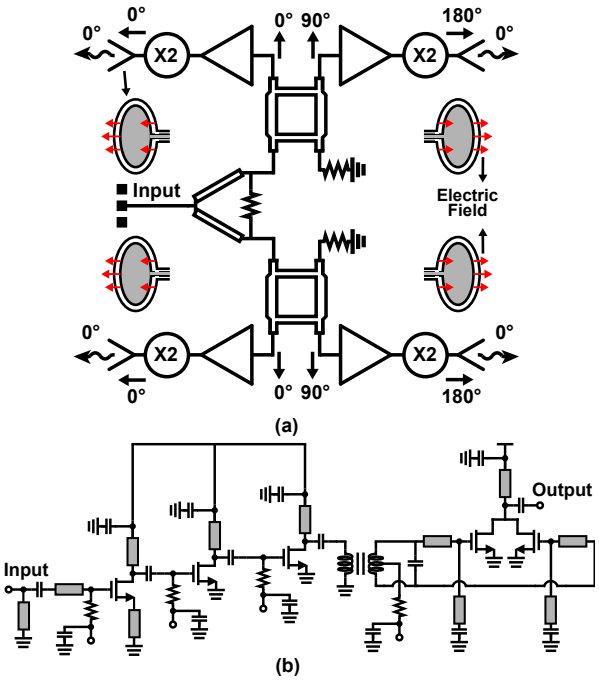

Fig. 1. (a) Block diagram of the 2x2 amplifier doubler array and (b) the amplifier doubler schematic.

The chip is implemented in IBM 45-nm SOI process (IBM12SOI) with 220-230 GHz f_{max} referenced to the

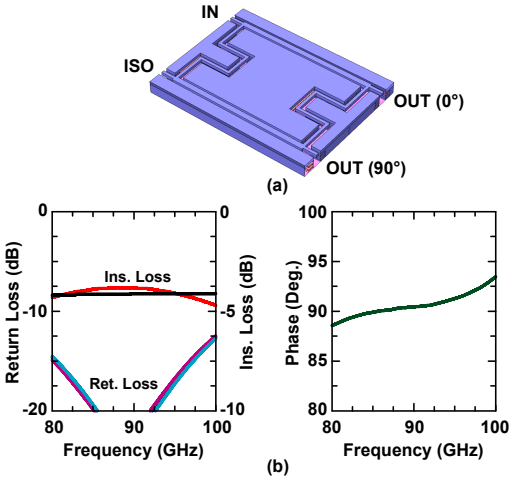

Fig. 2. Branchline (a) sonnet layout and (b) simulated S-parameters.

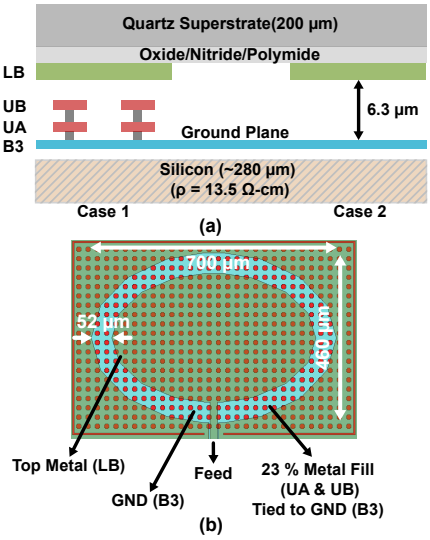

Fig. 3. (a) Metal-fill cases and (b) on-chip single-ended slot antenna with the metal-fill underneath the antenna.

top metal layer [6]. Grounded coplanar waveguide (G-CPW) transmission lines with 9/8/9 μm (Z_0 = 50 Ω) are implemented using LB for the signal line and B3 for the ground plane. The measured loss of G-CPW line is 1.1 dB/mm at 90 GHz and $\sim$2 dB/mm at 180 GHz [6]. The wilkinson and the branchline power dividers are designed using Sonnet 2.5-D EM solver with a simulated loss of 3.7 dB (Wilkinson). The branchline coupler shows an insertion loss of $\sim$4 dB with $<$ 0.3 dB and $<$ 2.5° gain and phase imbalance, respectively, at 80-98 GHz (Fig. 2(b)).

The 180 GHz elliptical slot-ring antenna is designed using a 200 μm quartz superstrate above the silicon chip (Fig. 3) [9]. The antenna is single-ended and placed on the top metal layer (LB), and the ground plane is defined as B3. This creates a parallel-plate condition which channels power away from the antenna and reduces its efficiency. The quartz superstrate is not patterned, and equalizes the propagation constant at the TEM mode in the dielectric layers on top of the silicon substrate, and the TM_0 mode in the quartz superstrate, to λ_d. This results in virtually little spurious radiation coupled to both modes from the two edges of the slot-ring antenna (spaced $\lambda_d/2$).

The slot-ring antenna with a quartz superstrate, and without meeting any metal-density rules, results in a radiation efficiency of 28% and a gain of 1.3 dB at 180 GHz with a 3-dB bandwidth of 165-195 GHz. However, in this work, the antennas are designed to meet the stringiest metal density rules so that no metal exclusion is taken on the wafer, which is congruent with industrial-level designs. The radiation efficiency drop to 13% and the gain drops to -2.3 dB when the metal fill is connected to each other (see Case 1). Still, this is $\sim$4 dB higher than the case without a quartz superstrate, showing the importance of this design technique (Fig. 4).

The 45 nm CMOS has such a high metal density requirement that it provides a severe environment for antennas radiating from the top side of the chip. Better performance can be obtained with the antennas radiating from the bottom side of the chip, but it either requires thinning the wafer to $\sim$100μm [4], or using a dielectric lens [5]. Both are expensive and not congruent with low cost techniques (mounting thick wafers on any standard PCB). It is for this reason that it has been decided to work with antennas with top-side radiation.

The simulated directivity and gain of the 2$\times$2 array is 12.5 dB and 3.6 dB (case 1) at 180 GHz, respectively. The gain drops to 1.6 dB at 170 GHz since the array is electrically smaller and there is the inherent -10 dB bandwidth of the antennas. The mutual coupling between the antennas is very low ($<$ -25 dB) in both E and H planes. The simulated S_{11} for both antennas (with and without metal fill) shows a -10 dB bandwidth of 170-180 GHz (design was done at 180 GHz, more accurate HFSS simulations showed that it shifted to 175 GHz).

The 2$\times$2 array results in a total EIRP of

$$EIRP = P_t \times G_t = 8.6\ dBm$$

where P_t=+5 dBm is the power available at the four antenna inputs (0 dBm/element and -1 dB transmission-line loss between the doubler and the antenna). The EIRP can also be written in terms of the directivity as:

$$EIRP = P_{Radiated} \times D_t$$

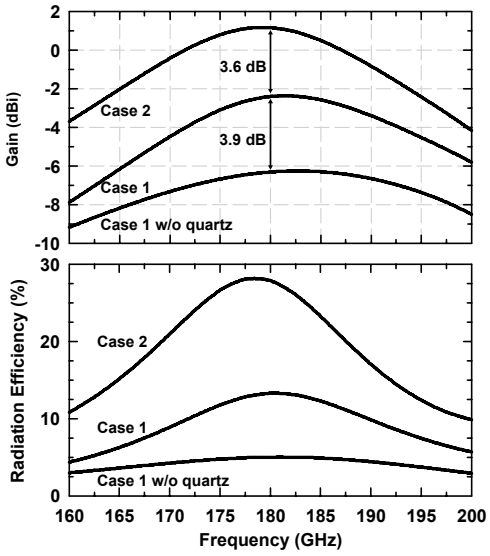

Fig. 4. Simulated elliptical slot-ring antenna gain and efficiency.

an the total radiated power is found to be -3.9 dBm (400 μW) at 180 GHz.

III. Measurements

Fig. 5 presents the chip microphotograph. The total size is 2×2.9 mm^2 including the RF and DC pads.

The current consumption of the W-band amplifier is 30 mA from 1.4 V supply, and the amplifier/doubler delivers $>$ -3 dBm at 170-190 GHz with 0 dBm peak output power at 180 GHz. The 2×2 amplifier-doubler array is characterized for antenna pattern and EIRP measurements using a far-field setup as shown in Fig. 6. The input signal is amplitude modulated at 1 kHz with 50 % duty cycle using an Agilent signal generater (E8257D) followed by a multiplier chain from Virginia Diodes, Inc. (VDI) with $>$ 20 dBm output power at 72-90 GHz [10]. The radiated signal is received by the WR-5 conical horn antenna followed by the zero-biased WR-5 detector with a responsivity of ∼250 V/W (characterized at UCSD using an Erickson Power Meter). The detected envelope of the radiated signal is sent to the SRS-830 lock-in amplifier.

The measured H-plane patterns at 166 GHz, 170 GHz and 180 GHz are shown in Fig. 7 together with the simulated H-plane pattern at 180 GHz. The antenna patterns are measured from -46° to +46° with a 2° step due to the physical limitation of the circular arm setup used over the probe station. The antenna is designed at 180 GHz, but the center frequency shifted to 170 GHz. Still, good agreement is seen between the simulated and measured results. Note the ±1 dB ripple in the measured patterns due to the presence of a large ground plane (metal chuck) below the chip.

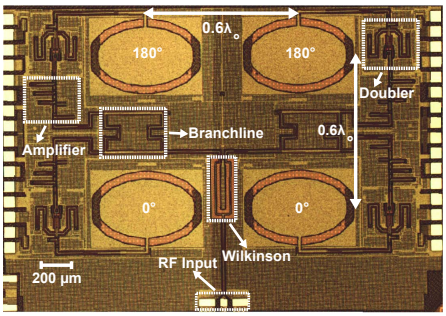

Fig. 5. Microphotograph of the 2×2 amplifier-doubler array (2 x 2.9 mm^2 including pads).

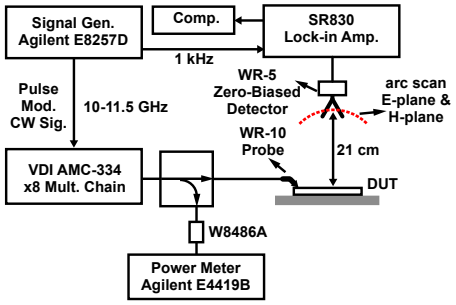

Fig. 6. Measurement setup for antenna patterns and EIRP.

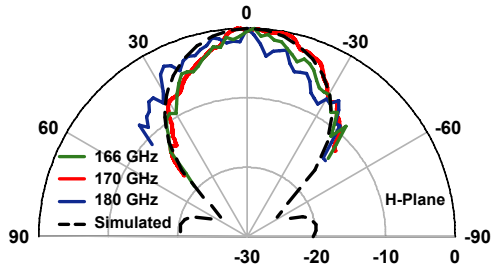

Fig. 7. Simulated (180 GHz) and measured H-plane patterns with a quartz superstrate.

Fig. 8 presents the measured broadside EIRP at 166 GHz, 170 GHz and 176 GHz versus input power. Since the on-chip W-band amplifier has a lower gain at 83 GHz than at 88 GHz, the required input power is higher to saturate the multipliers. The current consumption of the array is 124 mA from 1.4 V supply under quiescent condition, and 191 mA in saturation due to self-biasing.

The measured peak EIRP versus frequency with and without a quartz superstrate is shown in Fig. 9. The measured 3-dB bandwidth is 165-175 GHz with peak EIRP of +5 dBm at 170 GHz with a quartz superstrate. Again, the ripple in the EIRP versus frequency is due to the standing waves in the setup. The quoted EIRP is obtained

TABLE I
SUMMARY OF ANTENNA-COUPLED TRANSMITTERS

Frequency (GHz)	Technology	Design	Antenna Type	P_{rad} (μW)	BW (%)	EIRP (dBm)	Pdc (mW)	Ref.
170	45-nm SOI CMOS	2×2 active doubler array	Slot ring with quartz superstrate	200	8	5	267	This work
280	45-nm SOI CMOS	4×4 oscillator injection-locked	Diff. ring	190	3	9.4	817	[4]
288	65-nm Bulk CMOS	2×1 Triple-push oscillator	Diff. ring with silicon lens*	390	0	16.1	280	[5]

* Silicon lens size is 6.8λ at 300 GHz with 0.55 mm extension length.

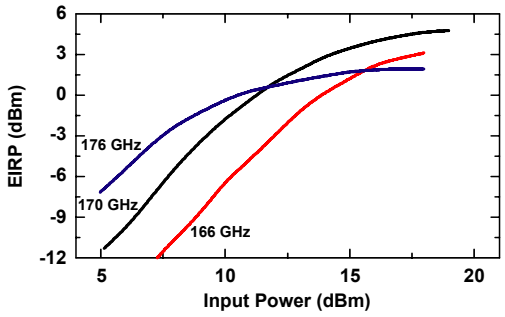

Fig. 8. Measured EIRP versus input power at 166-176 GHz with a quartz superstrate.

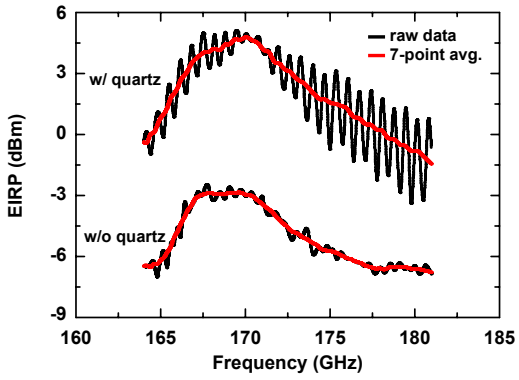

Fig. 9. Measured EIRP versus frequency with and without quartz superstrate. Measurements are taken with 200 MHz steps.

using a 7-point rolling average to reduce the effect of the ripples. The measured (average) EIRP is very close to simulations at 170 GHz (5 dBm versus 5.6 dBm).

IV. CONCLUSION

A 2×2 amplifier-doubler array has been presented at 165-180 GHz. The measured EIRP of the array meeting the metal density rules for the antennas is comparable to the oscillators in this frequency range. It is seen that advanced CMOS technology can result in wideband sources for applications such as low-cost imaging systems and spectroscopy.

V. ACKNOWLEDGEMENT

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