A 62 GHz Inductor-Peaked Rectifier with 7% efficiency

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***Abstract* — This paper presents the first 62 GHz fully on-chip RF-DC rectifier in 65nm CMOS technology. The rectifier is the bottleneck in realizing on-chip wireless power receivers. In this paper, efficiency problems of the mm-wave rectifier are discussed and the inductor-peaked rectifier structure is proposed and realized. By using an inductor-peaked diode connected transistor, self-threshold voltage modulation, and an output filter, the measured rectifier reaches 7% efficiency with 1 mA current load. Compared to previous state-of-art 45 GHz rectifier with 1.2% efficiency [1], our solution achieves a higher efficiency at a higher frequency, providing a better solution for mm-wave wireless power receivers.**

***Index Terms* — RF energy harvesting, wireless power receiver , mm-wave, rectifier, inductor-peaked rectifier.**

I. Introduction

Recently, wireless sensor networks (WSN) based on ultra-low-power radio architectures have received a lot of attention. In order to comply with the small size requirement and overcome the limited battery life time, alternative remote power source techniques such as wireless power transmission have been considered to build independent ultra-low-power systems such as temperature sensors as well as implanted biomedical and radio frequency identification (RFID) devices [2]. If energy would be extracted from electromagnetic radiation, batteries could become obsolete in these applications. This would lead to a longer lifetime, lower maintenance effort and higher safety. Combing on-chip RF energy harvesting with an ultra-low-power radio, future WSNs could operate as follows: monolithic wireless sensors without any external components, receiving energy wirelessly, processing data on chip and transmitting information wirelessly [3].

The most challenging issue for fully integrated sensor nodes is to provide enough power on chip. For RF energy harvesting at mm-wave frequencies, it is possible to integrate the on-chip antenna [4] and rectifier together with the sensor node without any off-chip component. Till now, the state-of-art highest frequency rectifier operates at 45 GHz with 1.2% efficiency with 2 dBm input power [1]. In this work, based on an analysis of the mm-wave rectifier performance, three techniques to improve the efficiency are proposed. In the fabricated rectifier, the efficiency is 7% with -14 dBm input power at 62 GHz. And also with -14 dBm input power, the rectifier provides 100 mV DC output voltage. By using the Villard cascade method, this structure has the potential to provide 1 V output voltage with -4 dBm input power if 10 identical stages [5] are combined.

This paper is organized as follows. In section II, the analysis of the mm-wave rectifier is presented. In section III, based on the analysis of the mm-wave rectifier performance, the inductor-peaked rectifier structure is proposed. In section IV, the measured results of the implemented rectifier are shown. The conclusions are drawn in the section V.

II. Mm-wave Rectifier Analysis

The rectifier is used as an on-chip wireless power converter. The basic half-wave rectifier is composed of a diode and a capacitor. The diode can be realized in CMOS technology as diode-connected MOSFET, or as a Schottky diode [6]. In the 65nm CMOS process used, Schottky diodes are not available as standard library components, and therefore the diode in the rectifier is formed by a diode-connected transistor.

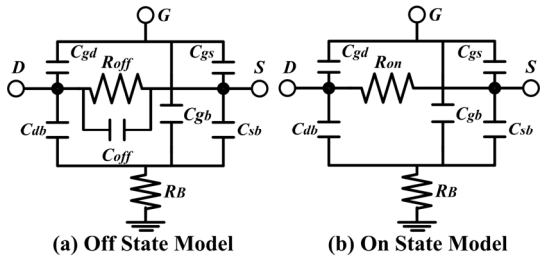

Figure 1: NMOS transistor model.

Figure 1 shows the NMOS transistor model. When the transistor is turned on, the insertion loss at low frequencies is determined by the on-resistance R_{on}, of the NMOS channel. At mm-wave operating frequency, the insertion loss will increase due to the capacitive coupling of the signal through the parasitic capacitances of the transistor to the substrate. When the transistor is turned off, the isolation at low frequencies is determined by the off-resistance R_{off}. For higher frequencies, the isolation becomes worse due to the off-state parasitic capacitances and channel capacitance, therefore the storage capacitor, which is charged by the DC output voltage of the rectifier, is discharged by the signal fed through the parasitic capacitor. To increase the efficiency of the rectifier, the

insertion loss must be minimized and the isolation maximized. In order to obtain minimum insertion loss, one needs to reduce the resistance R_{on}. The on-resistance can be expressed as

$$R_{on} = \frac{1}{\mu C_{ox}\frac{W}{L}(V_{gs}-V_{th})} \quad (1)$$

where μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, V_{th} is the transistor threshold voltage, V_{gs} is the gate-source voltage, W and L are the width and length of the transistor respectively. That suggests the use of transistors with minimum allowable channel length and maximum transistor gate width. However, a larger W will lead to larger parasitic capacitance to the substrate and also increases the gate to source capacitance C_{gs}, which will result in more signal loss in the substrate as well as degradation of the isolation. Furthermore, this phenomenon is magnified as the frequency increases. Also higher overdrive voltage (V_{gs}-V_{th}) is suggested to lower R_{on}. The fundamental difference between the design of MOS transistors as diode at 60 GHz compared to frequencies of 2.4 GHz [7] and HF/UHF [8][9] is the trade-off between insertion loss and isolation. In circuits operating at lower frequencies, the isolation of the MOS switch in the OFF state is not an important consideration. At these frequencies, the design process is entirely focused on minimizing the insertion loss of the switch. On the other hand, at 60 GHz, several low-impedance paths caused by parasitic capacitances lead to a trade-off between isolation and insertion-loss.

III. Inductor-Peaked Rectifier

In this design, inductive input matching, self-threshold modulation, an inductor-peaked diode connected transistor and a low pass output filter are implemented to increase the efficiency as well as the sensitivity of the rectifier.

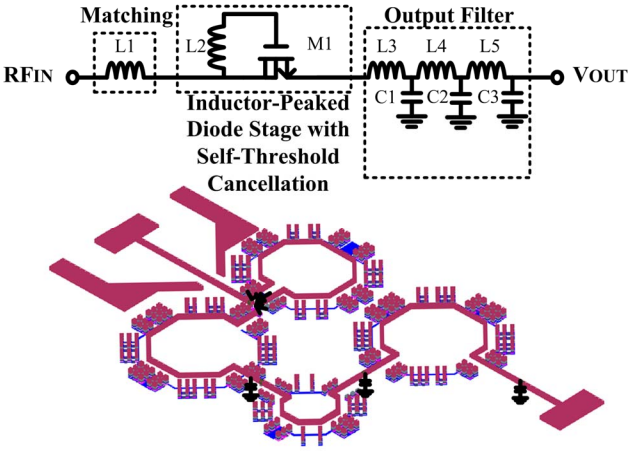

Figure 2: Schematic of the inductor-peaked rectifier and layout model for electromagnetic field simulation.

Figure 2 shows the schematic of the inductor-peaked rectifier and its layout. The inductor L_1 forms the series input matching stage. L_2 and the diode connected transistor M_1 form the inductor-peaked diode. The bulk of M_1 is connected to the input, which forms the self-threshold modulation. L_3, C_1, L_4, C_2, L_5, C_3 form the output filter.

In the normal diode connected transistor the gate and the drain are simply connected using a wire. If this method is applied at high frequency, a low impedance path is formed by this wire and C_{gs} between the input and the output. In the rectifier application, the output is connected via a large capacitor to ground and can thus be treated as RF-ground. Therefore, next to the current path through R_{on}, there is a second path charging and discharging the storage capacitor, which will deteriorate the isolation and lead to low efficiency. Therefore a low-pass output filter is used to prevent that the RF-signal can reach the storage capacitor directly.

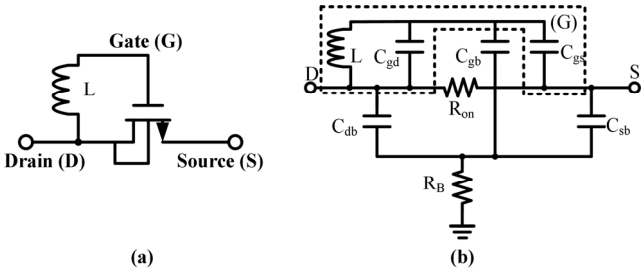

Figure 3: (a) Inductor-peaked diode connected transistor, (b) circuit model in the on-state.

Figure 3 shows the inductor-peaked diode connected transistor and its equivalent circuit model in the on-state. From Eq. 1, R_{on} is decreasing with increasing V_{gs}. The simple short connected wire from gate to drain can be replaced by an inductor L. The inductor L is chosen such that together with the stray capacitances C_{gs} and C_{gd} (Figure 3), an LC-resonator at the input RF frequency is formed. Therefore, the magnitude of voltage across the inductor and the capacitors is Q times higher than the input voltage. Therefore also the voltage swing V_{gs}, at the gate of the transistor is larger than the input voltage. If V_{gs} increases, R_{on} will decrease and bring down the insertion loss which will lead to higher efficiency. In order to choose the value of L, three operational conditions have to be considered: accumulation, depletion and inversion. The different modes of operation cause C_{gs} value variation. The variation of the value of the capacitor under the large signal swing and also turn on and off states will cause distortion of the resonator formed by L ,C_{gs} and C_{gd} In most applications, this situation is not preferred. However, in the rectifier we can take advantage of it. In the on state, the resonator will make it easier for the current to pass through. In the off state, the current will have more

difficulties to pass, which will improve the reverse isolation.

The threshold voltage of the transistor is the bottleneck of the rectifier, because it is related directly to the sensitivity and the efficiency [10]. There are several threshold voltage modulation methods that are used in the HF/UHF range [11]. At 62 GHz, in order to make the design robust to the parasitic capacitors, self-threshold voltage modulation is proposed and implemented by connecting the substrate of the transistor to the input terminal, as shown in Figure 3(a).

The input matching of the rectifier is a dynamic matching because the rectifier input impedance (R_{in}) changes with the output current. In the matched situation, the input voltage V_{in} can be expressed as [5]

$$V_{in} = V_s \frac{R_{in}}{R_{in} + R_s} = 2\sqrt{2R_s P_{AV}} \frac{R_{in}}{R_{in} + R_s}$$

where R_s is the source impedence, P_{av} is the avaialble input power. If the input matching matches to the initial value of the rectifier input impedance, for i_{out}=0, $R_{in|inital}$=$R_{in|max}$, v_{in} will decrease when i_{out} increases because R_{in} will decrease. If the input matching network is matched to the stable value of the rectifier input resistance, that is i_{out}=i_{max}, $R_{in|stable}$=$R_{in|min}$, the magnitude of v_{in} will increase because the input impedance of the rectifier will increase. In the latter case, it can take advantage of the mismatch between $R_{in|stable}$ and $R_{in|inital}$. For high sensitivity, the input voltage v_{in} should be as large as possible. Thus, in order to have a better sensitivity, it is better to match the 50 Ω to the stable phase of the rectifier input impedance. In this design, series inductor matching is used. The series inductor matching can take advantage of the voltage-boosting effect at the input of the rectifier due to the Q-factor of the inductor, which will also improve the sensitivity and efficiency of the rectifier.

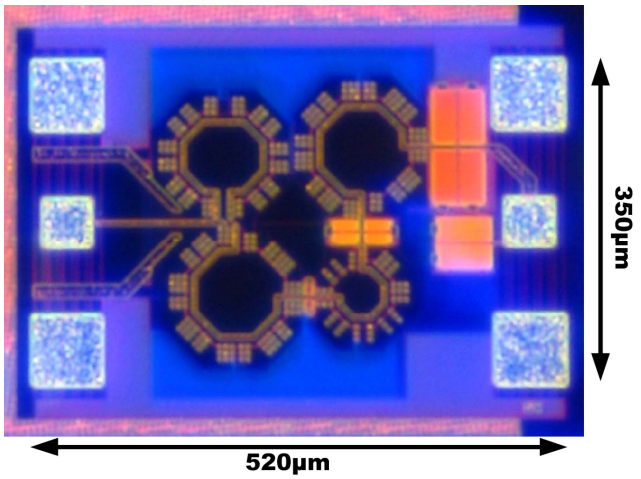

Figure 4: Die micrograph of the 62 GHz inductor-peaked rectifier.

IV. Measurement Results

Figure 4 shows the die photograph of the inductor-peaked rectifier. The input inductor is realized by a metal line inductor with metal strip shielding to achieve a high Q factor and make the design compact. To verify the layout

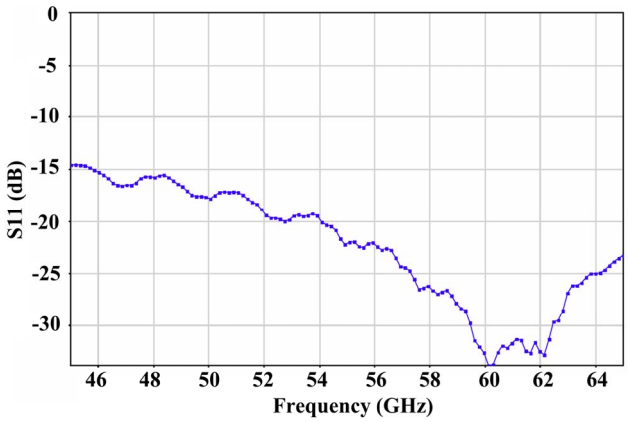

Figure 5: Measured S_{11} of the proposed inductor-peaked rectifier.

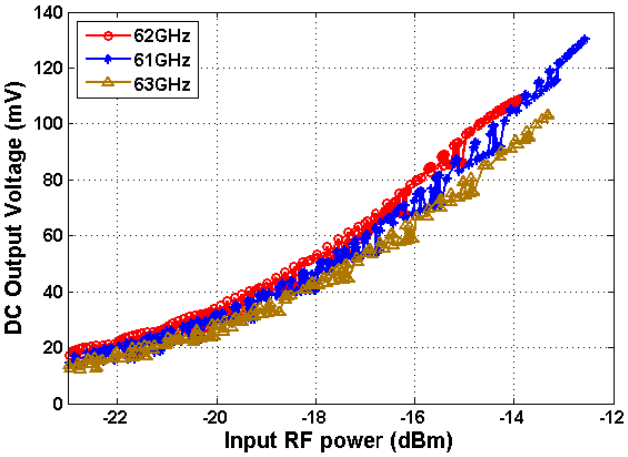

Figure 6: Measured output voltage as a function of the input power.

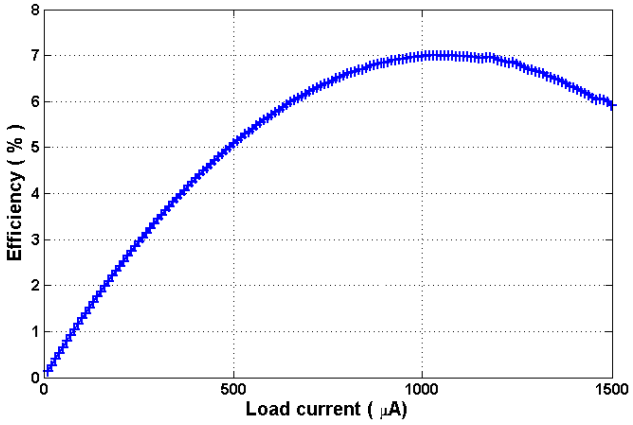

Figure 7: Measured efficiency of the rectifier at 62 GHz as a function of the load current for -14.5 dBm input power.

performance, electromagnetic (EM) software (Agilent Momentum) has been used to simulate all the inductors, the interconnections, the bond pads, and the whole chip. Because all the inductors are close to each other, the return current through the ground metallization will degrade the performance. Therefore, the ground metals around the inductors are cut into small strips and each strip is perpendicular to the inductor line. The total chip area including bond pads is 0.52×0.35 mm^2.

The chip is measured by using on-wafer RF and DC probes. S-parameters are measured with an Agilent N5247A PNA-X network analyzer. Figure 5 shows the measured S_{11} of the inductor-peaked rectifier. At 62 GHz, the S_{11} is -32 dB. In the input power and output voltage (PV) characteristic measurement, the input power is provided by an Agilent E8267D and E8257D PSG signal generator. The input power is measured by a power sensor (Agilent E4491B) through a directional coupler (Agilent 83701E). The output voltage is measured through the Agilent 34401A digital multimeter. Figure 6 shows the measured input power output voltage (PV) characteristic at 61 GHz, 62 GHz and 63 GHz. At 62 GHz, with -14.5 dBm input power, the rectifier provides 100 mV output voltage. In the rectifier efficiency measurement, in order to measure the output power accurately, an Agilent E5270B 8-slot precision measurement mainframe is used as the load for the rectifier. The load current is provided and the corresponding output voltage is measured by the Agilent E5270B 8-slot precision measurement mainframe. Figure 7 shows the measured efficiency of the fabricated inductor-peaked rectifier. The maximum efficiency at 62 GHz is 7% for 1 mA current load.

V. CONCLUSION

In this paper, a 62 GHz inductor-peaked rectifier with 7% efficiencies is presented. The rectifier performance at mm-wave frequency is analyzed, and the impact of the diode-choice on the trade-off between isolation and insertion loss is explained. The inductor-peaked rectifier structure is proposed. An inductor-peaked diode-connected transistor, self-threshold voltage modulation and a low-pass output filter are used to increase the sensitivity and the efficiency of the rectifier. The series input inductor can take advantage of the voltage boost effect. The measured S_{11} of the rectifier is -32 dB at 62 GHz. In the measurement, the designed rectifier reaches 7% efficiency at 62 GHz. With -14 dBm input power, the rectifier provide an output DC voltage of 100 mV. Compared with previous state-of-art rectifier at 45 GHz with 1.2% efficiency, this design achieves a higher efficiency solution at 62 GHz. By using the Dickson structure, this structure has the potential to provide 1 V output voltage with -4 dBm input power with 10 identical stages using the Villard cascade method [5].

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