A 73.9-83.5GHz Synthesizer with -111dBc/Hz Phase Noise at 10MHz Offset in a 130nm SiGe BiCMOS Technology

J.-O. Plouchart, Mark Ferriss, Bodhisatwa Sadhu, Mihai Sanduleanu, Benjamin Parker, Scott Reynolds

IBM T. J. Watson Research Center, Yorktown Heights, NY

***Abstract* — A 73.9-83.5 GHz synthesizer is implemented in a 130nm SiGe BiCMOS technology. The measured phase noise at 10KHz and 10MHz offset of the 82.4GHz carrier are -88.5dBc/Hz and -111dBc/Hz respectively. Reference spurs are -67 dBc. The synthesizer integrates voltage regulators and power management for SoC applications; it consumes 0.51 W from 1.5 V and 2.7 V supplies, and occupies 0.85 mm x 2.9 mm.**

***Index Terms* — mm-wave, ICs, Synthesizer, PLL, VCO, frequency multiplier, W-band, phase noise, SoC.**

I. Introduction

Because they operate in a low atmospheric absorption window, W-band transceivers are ideal for radar, imaging, and long distance communication. For radar applications, a frequency synthesizer with low phase noise close to the carrier is usually required. For example, for 77GHz automotive radar applications a phase noise of less than -80dBc/Hz at 100kHz offset was specified [1]. For communication applications using complex QAM and OFDM modulations, a phase noise of better than -110dBc/Hz at 10MHz offset was key to enabling a 5Gb/s wireless transmission [2]. Although W band silicon PLLs have been reported, none of them can support the phase noise requirements of radar and high-bit rate communication [3]-[5]. In this paper we present a 73.9-83.5 GHz synthesizer for multi-function transceivers [6] that fulfills the specifications for radar, imaging and high-bit rate communication applications, simultaneously achieves low phase noise and a broad tuning range, and is suitable for integration in a mm-wave SoC.

II. Synthesizer architecture

In Fig. 1, a simplified block diagram for the synthesizer including frequency doubler is shown. The PLL generates two sets of outputs, one set at 41.78GHz, to be used in the frequency doubler, and one set at 20.89GHz, intended for use in a baseband mixer. The divider consists of a cascade of 4 bipolar CML stages with division ratios of 2, 2, 5 and 2, with a total division ratio of 40. The dividers are ordered such that the final stage divides by 2 so that the output clock has a 50% duty cycle, making it suitable for use in the downstream AC-coupled CML-2-CMOS converter. The reference clock input passes through a programmable divider, with division ratios of 1, 2 or 4. The programmable divider is added to the reference clock path instead of the feedback clock path, to allow the use of higher reference rates without increasing the sampling rate of the CMOS phase detector. Two identical CML-2-CMOS converters convert the CML reference clock and feedback clock to rail-to-rail CMOS levels. The CMOS phase detector and charge pump operate from a regulated 1.5V supply, which isolates the supply sensitive CMOS elements from the noisier global 2.9V power supply. The relatively high regulated voltage enables the CMOS blocks to run at 1GHz. The CMOS PFD and fully differential charge pump are implemented in 130nm CMOS technology. The fully differential charge pump includes a common mode feedback and a current DAC. The loop filter's resistor and ripple capacitor are programmable to support loop bandwidths from 1MHz to 10MHz. The supply-sensitive VCO is isolated using a dedicated voltage regulator and bandgap. Support circuits needed for integration of the synthesizer into a mm-wave SoC, such as biasing, power-down and digital control, are also included. The PLL also provides a 333MHz clock for digital clocking, and a buffered reference output intended for use in daisy-chained multi-chip systems in scalable phased array applications [6].

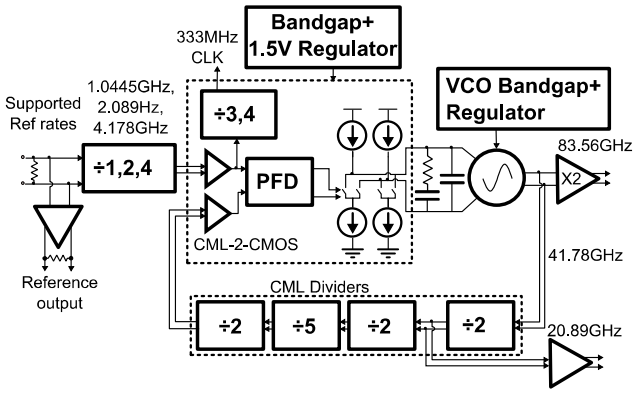

Fig 1. Simplified PLL block diagram.

III. VCO AND DOUBLER ARCHITECTURES

The proposed topology of the 40GHz VCO is shown in Fig. 2. The VCO uses transconductance linearization to achieve superior phase noise performance, as compared to a differential pair topology, based on the principles outlined in [7]. The capacitive transformer network used for achieving the desired linearization along with the capacitor sizes used are shown in Fig. 2. The linearization increases the amplitude of oscillation while reducing the noise injected from the bipolar transistors into the resonating tank, improving the phase noise considerably [7].

Two spiral inductors are used, one for biasing the VCO and providing DC current, and another as the resonating element in the tank. There are two sets of capacitor tuning banks. The 3-bit binary weighted switched capacitor coarse tuning controls and analog varactor controls are placed directly within the tank as shown in Fig. 2. As the VCO frequency is less sensitive to the collector capacitance, the 3-bit fine tuning switched capacitor controls are placed across the bipolar collector nodes. MOSFET based switches and metal-insulator-metal capacitors are used for constructing the switched capacitor varactors. The VCO current is controlled using a resistive current DAC (RDAC) as shown in Fig. 2. The bipolar transistors are biased using a resistive voltage divider.

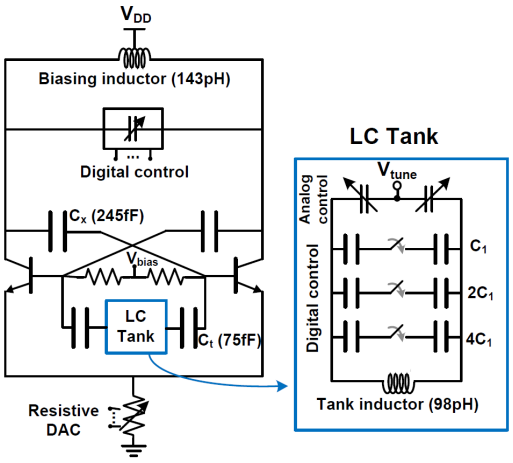

Fig. 2. LiTVCO topology used for the 40GHz VCO

The proposed frequency doubler, shown in Fig. 3, is based on a differential pair (T_1, T_2) with a shared collector node and a shared emitter node. The out-of-phase differential currents in T_1 and T_2 are summed at the collector and emitter nodes, to generate a differential output signal at twice the VCO frequency. The signal is then amplified by a cascoded differential pair ($T_{3..6}$), a two-stage emitter follower ($T_{7..10}$) and a final split cascoded differential pair that can switch between two differential outputs ($T_{11..16}$).

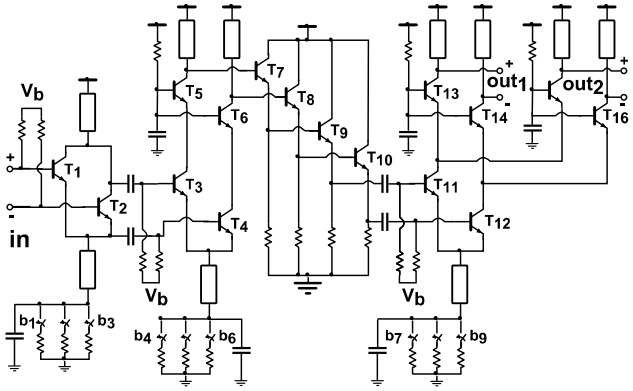

Fig 3. Frequency doubler simplified schematic.

III. MEASUREMENT RESULTS

Fig. 4 shows the measured synthesizer frequency as a function of the varactor voltage, the 8 fine states (3-bit), and the 8 coarse tuning states (3-bit). There is large overlap between bands, and multiple bands can be chosen to generate the same frequency. The varactor tuning overlaps the fine frequency bands by more than 50%. This reduces the probability that the PLL will lose frequency lock as the temperature varies.

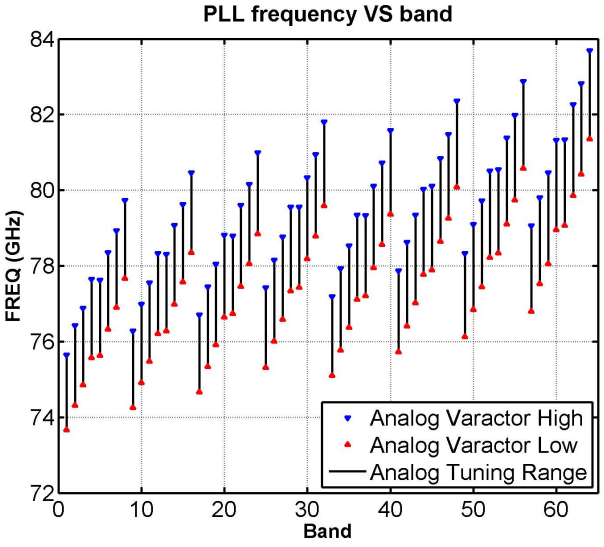

Fig 4. Frequency tuning and band overlap.

We verified that the VCO power is high enough to saturate the frequency doubler by increasing the VCO power (Fig. 5) using the RDAC setting. The 79.2GHz output power is greater than -4dBm.

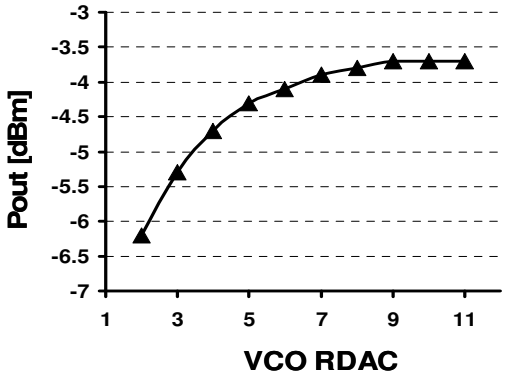

Fig 5. 79.2GHz output power versus RDAC setting.

Phase noise measurement of a W-band PLL is challenging because an external mixer is required for measurements using a spectrum analyzer. This external mixer degrades the phase noise measurement accuracy by increasing the noise floor due to the mixer conversion losses. The mixer can also introduce additional spurs that are hard to distinguish from the intrinsic PLL spurs in the measurement system. As shown in Fig. 6, the sub-harmonic mixer that is usually used to extend the frequency performance of the spectrum analyzer generates large spurs. Therefore, we used a waveguide balanced mixer, which as shown in the black curve in Fig. 6 does not generate large spurs. The drawback of this technique is that a high-purity W-band local oscillator is required.

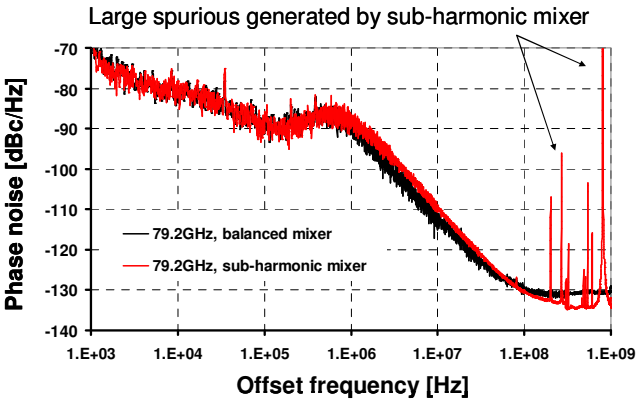

Fig 6. Phase noise measurements with a sub-harmonic and a balanced mixer at 79.2GHz.

Fig. 7 shows phase noise at 10MHz offset from 77.6GHz measured with the balanced mixer as a function of the RDAC setting. More than 12dB of phase noise variation is measured for a variation in VCO power from 18 to 55mW. The VCO consumes 41mW at the minimum phase noise point measured at -114.5dBc/Hz.

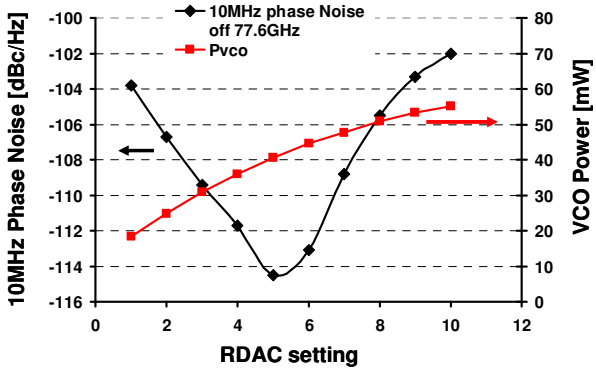

Fig 7. 10MHz offset phase noise measurement from 77.6GHz carrier (black) and VCO power (red) versus RDAC setting.

Fig. 8 shows the phase noise measurements at low, middle and high frequency. The 10MHz phase noise is -113.2, -112.6, and -111dBc/Hz at 74.4, 79.2 and 82.4GHz respectively. There is 2.2dB variation across frequency bands for the 10MHz phase noise. At 100kHz offset from the 82.4GHz carrier the phase noise is only -88.5dBc/Hz. The intrinsic noise of the measurement system was also characterized at 78GHz (Fig. 8). The measurement noise floor is lower than -90dBc/Hz at 10kHz offset and -130dBc/Hz at 100MHz offset, which gives confidence in the synthesizer measurements. Beyond 100MHz offset the system noise floor is reached at -135dBc/Hz.

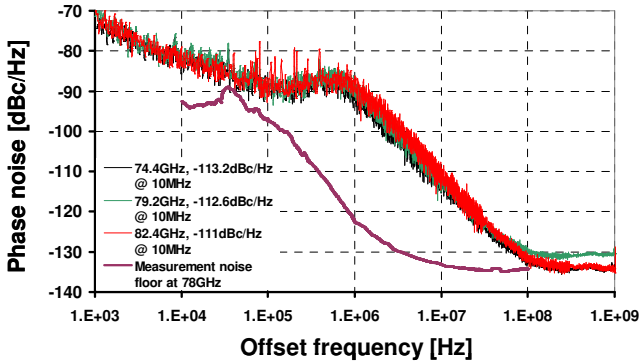

Fig 8. Synthesizer phase noise measurements at 74.4, 79.2 and 82.4 GHz and noise floor system measurement.

Owing to the sensitivity of the measurement system, we were able to measure the impact of the VCO gain variation on the 10MHz phase noise when the varactor is tuned from its highest to its lowest value. As shown in Fig. 9, the 10MHz phase noise variation is 2.8dB within one frequency band. The phase noise degrades as frequency and VCO gain is increased. Since the VCO gain is much smaller for the lowest and highest frequency than in the middle of the varactor tuning range, the phase noise exhibits a maximum (Fig. 9).

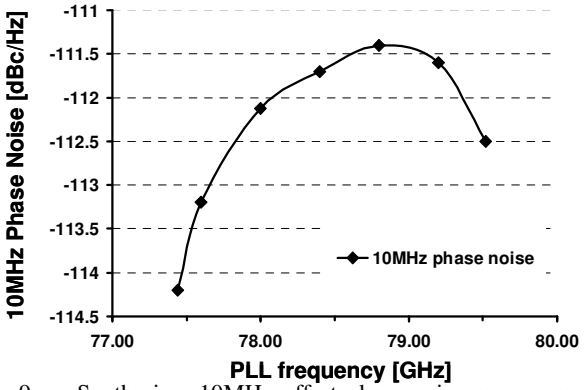

Fig 9. Synthesizer 10MHz offset phase noise measurements across varactor tuning range.

Table I compares the synthesizer with a previously reported state of the art PLL, and demonstrates new state of the art power, frequency tuning, and noise performance for a W-band synthesizer. The break-out of the power consumption is 193, 43, 91, and 184 mW for the PLL, VCO, VCO buffer, and frequency doubler with 50Ω driver respectively.

Table I
COMPARISON TABLE OF STATE OF THE ART W-BAND SYNTHESIZER

	[4]	This work
Frequency	80 - 84.5 GHz	**73.92 - 83.52 GHz**
Tuning range	5.50%	**12.2%**
Phase Noise at 10MHz	-102dBc/Hz @ 84.4GHz	**-111dBc/Hz @ 82.4GHz**
Reference spur	N/A	**-67 dBc**
Output Power	-3 dBm	**-4 dBm**
Supply	1.8V, 2.5V, 3.3V	**1.5V, 2.7V**
Power consumption	1.15 W	**0.51 W**
Regulator	off-chip	**integrated**
Technology	0.13um SiGe BiCMOS	**0.13um SiGe BiCMOS**
Chip area	1.1 mm x 1.7 mm	**0.85 mm x 2.9 mm**

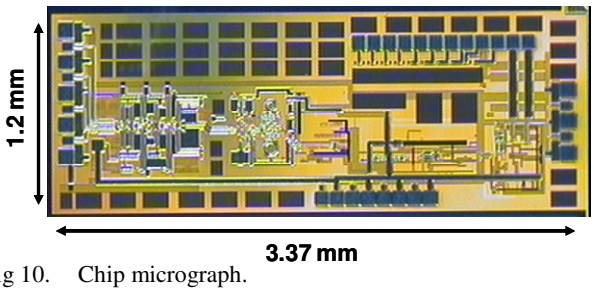

Fig 10. Chip micrograph.

VII. Conclusion

A W-band synthesizer was integrated in a 130nm SiGe BiCMOS technology, and supports multi-function transceivers. With a measured phase noise of -88.5 and -111dBc/Hz at 100KHz and 10MHz offset from the 82.4GHz carrier, respectively, the synthesizer can be used for radar and 5Gb/s wireless communication application. The PLL and VCO voltage supplies are separately regulated to facilitate the synthesizer integration in a SoC. The total power consumption is 0.51W and the synthesizer includes multiple power-down modes to support different operating modes and testing.

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