A low power 60-GHz 2.2-Gbps UWB transceiver with integrated antennas for short range communications

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***Abstract* — A 60-GHz low power fully integrated transceiver including antennas, fabricated in CMOS 65nm SOI and packaged in low cost QFN is described. The circuit achieves 2 Gbps and 500 Mbps rates at 7.5 cm and 22.5 cm transmission ranges respectively. The transceiver energy efficiency is lower than 50 pJ/bit thanks to scalable power consumption using pulse generator and Super Regenerator Oscillator architecture.**

***Index Terms* — UWB, 60 GHz, mm-wave, CMOS, integrated antennas, transceiver, wireless, SRO.**

I. Introduction

Future consumer mobile platforms need high rate wireless connections for data exchange and video streaming. 60-GHz band has been intensively explored for such purpose [1-3, 5]. A first approach consists in using classical coherent architecture with complex modulated signals (QPSK, 16-QAM) and high spectral efficiency. However, such systems exhibit a low energy efficiency resulting in high power consumption that makes them unsuitable for battery powered mobile devices like smart phones [1], [2]. A trade-off between spectral efficiency and transmission range combined to simplified architecture can respond to challenges such as multi-Gbps data rate and sub 100-mW power consumption.

This paper describes a fully integrated 60 GHz low power transceiver, including the antennas, fabricated in a CMOS 65nm SOI high resistivity technology. The chip is packaged in a low cost QFN pre-molded cavity. The circuit targets mobile devices requiring multi-Gbps wireless data transfer for pear-to-pear exchange, data synchronization and kiosk application. It can also be used in chip-to-chip or board-to-board wireless communications where low power consumption is required. For that purpose, very compact and low cost packaging is proposed, with the lowest power consumption compared to other existing 60 GHz transceiver systems [1]-[2], [5]-[8]. It is attained through low complexity in the transceiver architecture and by using On-Off-Keying (OOK) modulation scheme.

II. Transceiver Architecture and Circuit Design

The circuit block diagram is depicted in figure 1(a). The transmitter is based in a switched pulse-injected oscillator that offers fast switching time and high power efficiency [3]. The digital data to be transmitted are injected serially in the transmitter input. The input signal is time-limited by the so called Duty Cycle Controller (DCC), which adjusts the transmitting time between 225 ps and 300 ps with a 25 ps step resolution, as shown in figure 1(b). This duty-cycled data stream acts as a switch on the pulsed oscillator, which is based on the circuit of [3]. When the incoming digital signal toggles to "1", the oscillator is

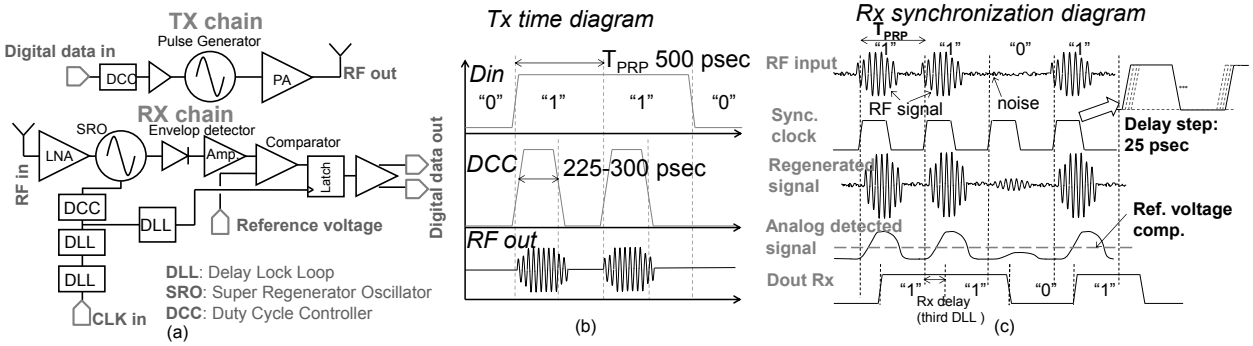

Fig. 1. (a) Transceiver architecture. (b) Time diagram of the transmitted signal. (c) Time diagram of the receiver explaining synchronization between incoming signal, clock and OOK demodulation.

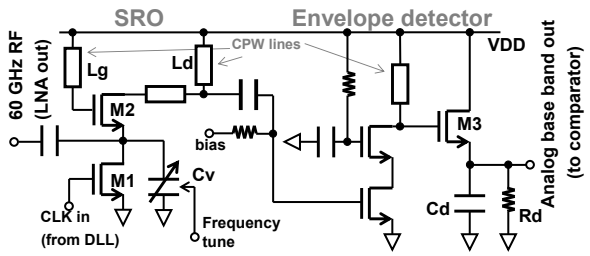

Fig. 2. Super regenerator oscillator and envelop detector schematics.

turned on during a limited time set by the DCC, and a pulsed sine signal with center frequency at 61 GHz is generated. The pulse is next amplified by a single stage power amplifier and radiated by the integrated antenna.

At the receiver side, the system uses a Super Regenerator Oscillator (SRO). It offers many advantages for wideband pulsed oscillating signals in terms of duty cycling capability, sensitivity bandwidth, and instantaneous gain [4]. The integrated on-chip Rx antenna receives the pulsed mmW signal and feeds it to an LNA. After amplification, the signal is injected in the SRO (figure 2). The SRO uses a gyrator architecture: M2 is the negative resistance, L_g and L_d are transmission lines that resonate with the varactor and the M2 gate to source capacitances (C_v and C_{gs}, respectively). The free running oscillation frequency is set to 61 GHz, i.e. at the center of the LNA band. Transistor M1 switches M2 current and it is controlled by the synchronization clock signal that turns on and off the SRO. The RF injected power (coming from the LNA output) is added inside the SRO structure and acts as an in-band accelerator to the oscillator starting time. As illustrated on the time diagram of figure 1(c), the SRO is switched on-and-off by the clock signal, while it integrates the incoming RF signal from the LNA. During the on-time, the SRO generates a small envelop oscillation if the RF energy is small or it consists on noise, and a large envelop oscillation when the incoming energy is high (pulse presence). SRO sensitivity is a compromise between M1 and M2 dimensions and clock on-time width. The SRO output is connected to a cascode amplifier that injects the regenerated signal into the envelop detector. The envelop detector charges and discharges the C_d capacitor. C_d and R_d values are chosen in order to create a large bandwidth low-pass filtered analog signal (>2.5 GHz) that filters out the 60 GHz frequency components. The down-converted signal is compared to a reference voltage for data value decision ("1" or "0"). The pulse duration is short (in the range of 250 ps) and timing accuracy is critical to get the received signal in a good

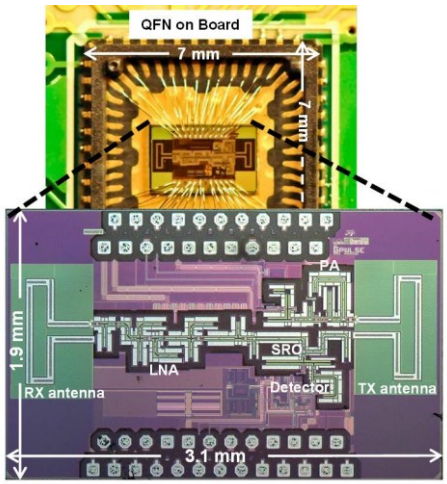

Fig. 3. Chip-in-package photograph (open lid) and details of the chip. Dimensions: 3.1x1.9 mm².

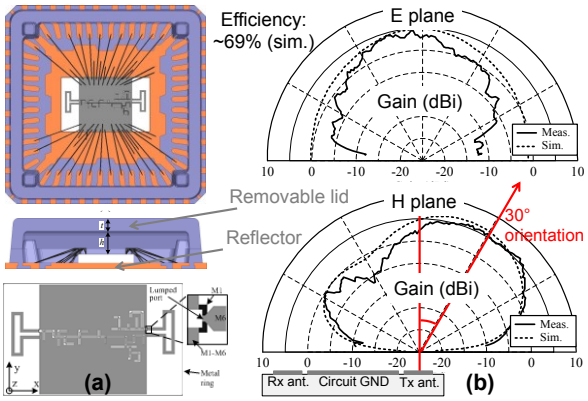

Fig. 4. (a) 3D EM model used for antenna design (top view and cross section) including package, chip, and details of the chip EM model. (b) Antenna diagram pattern in E-plane and H-plane.

phase synchronization condition at the SRO. This is done by three delay lock loops (DLL in figure 1(a)). A reference clock is provided externally and its frequency corresponds to the desired transmission data rate for OOK modulation ($f_{PRP}=1/T_{PRP}$). In order to properly synchronize the receiver, a fine tuning DLL is used with a time step of 25 ps covering up to 550 ps. The second DLL has a coarse tuning with a time step of 514 ps covering up to 11.308 ns. The third DLL is used to compensate the constant circuit delay between the SRO and the latch.

III. Intergrated Antennas

Figure 3 shows a packaged chip photograph with open lid. The chip size is 3.1x1.9 mm². The integrated antennas are folded dipoles and are fabricated with all back-end

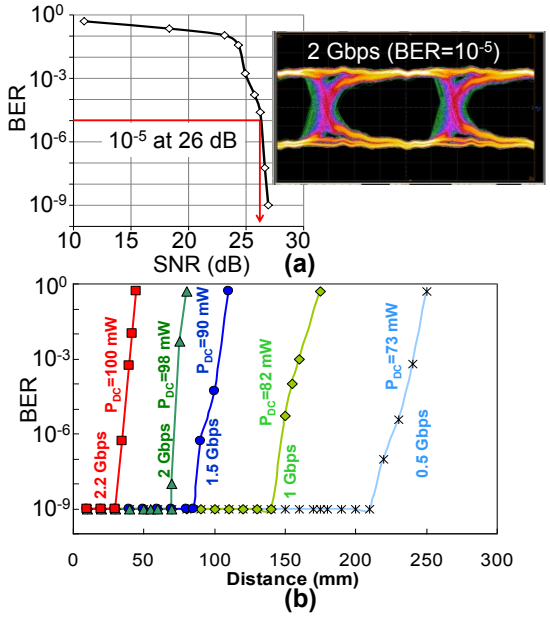

Fig. 5. (a) Measured on-chip bit error rate at the LNA input versus the signal to noise ratio and eye diagram. (b) Experimental wireless link BER versus communication range for various data rates indicating the total transceiver dissipated power for each case.

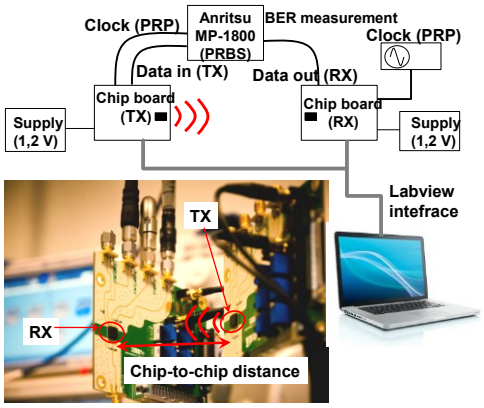

Fig. 6. Experimental setup for wireless link.

metals stacked and connected together (M1 to M6). The antenna design takes into account the packaging environment as illustrated in figure 4(a) (wire bonds, circuit and packaging metallic elements as well as the polymer material properties). The metallic ground plane of the QFN packaging underneath the chip is used as a reflector. Measurements are performed in an anechoic chamber using the Tx as a CW generator (pulse generator in ON-state). The measured antenna diagram pattern shown in figure 4(b) has a maximum gain of 5 dBi and 60° beamwidth. It is tilted 30° away from the z-axis due to

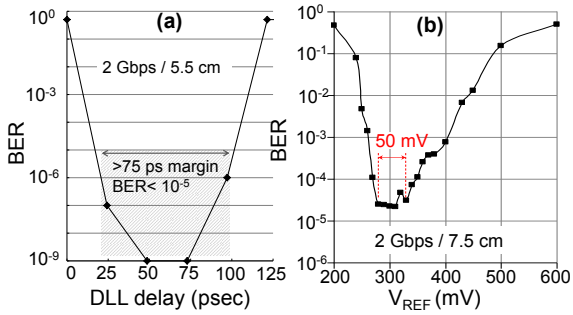

Fig. 7. (a) Receiver sensitivity to the DLL time delay for a wireless link at 5.5 cm distance and 2 Gbps data rate. (b) Receiver sensitivity to the comparison reference voltage for 7.5 cm range and 2 Gbps.

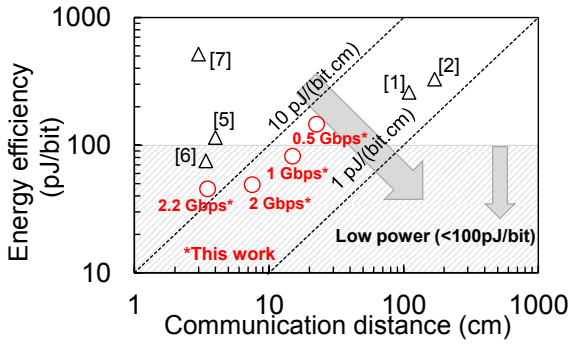

Fig. 8. Comparison with state-of-the-art low-power, high data rate fully integrated CMOS transceivers with antennas.

the presence of the circuit ground plane. All wire-bonded I/Os are ESD protected.

IV. Measured Results and Wireless Link

In order to extract the receiver input sensitivity, on-chip measurements were carried out on a receiver circuit without antenna. A 10^9-1 bit length pseudo random sequence is applied at the LNA input at 2 Gbps throughput. The synchronization is performed using the receiver DLLs. Under these conditions, figure 5 shows the bit error rate (BER) versus the input signal-to-noise ratio (SNR) considering a 5 GHz integration band. The 10^{-5} BER value is reached for 26 dB of SNR at the input of the LNA.

Next, wireless links are tested with two boards containing fully integrated transceivers placed in an office like environment (figure 6). A PRBS signal of 10^9-1 bit length sequence is sent to the transmitter. The maximum communication range achieved for various BER values is plotted as a function of the data rate in figure 5. Duty cycling in the pulse generator, the DLLs and the SRO lead to scalable power consumption with the data rate, as shown in figure 5(b). The wireless link synchronization is

TABLE I
SUMMARY OF RECENT HIGH DATA RATE CMOS TRANSCEIVERS

	This Work	[1]	[2]	[5]	[6]	[7]	[8]
Technology	65 nm CMOS SOI	65 nm CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS	65 nm CMOS	90 nm CMOS
Frequency (GHz)	61 GHz	60 GHz	60 GHz	59 GHz	8 GHz	60 GHz	60 GHz
Modulation	OOK	OFDM 16-QAM	QPSK 16-QAM	OOK	BPSK	OFDM QPSK	OOK
Raw Rate (Gbps)	0.5 to 2.2 Gbps	7 Gbps	3.1 Gbps	2 to 2.5 Gbps	2 Gbps	2.62 Gbps	1.7 to 3.5 Gbps
Power (mW)	**98 mW (2 Gbps)**	1811 mW	1017 mW	286 mW	150 mW	1348 mW	264 mW
Antenna / Packaging	**Integrated on-chip / QFN**	Glass / HTCC	Organic package	Ro4003 / Chip on board	NA	Wire antenna / Plastic BGA	NA
Range (cm)	7.5 to 22.5 cm	110 cm	170 cm	4 to 5 cm	3.4 cm	3 cm	NA
Energy efficiency (pJ/bit)	**48.5 pJ/bit (2 Gbps)**	259 pJ/bit	328 pJ/bit	114.4 pJ/bit	75 pJ/bit	514 pJ/bit	76 pJ/bit

achieved using a Labview interface that sets the receiver DLLs state to the optimum BER. Both receiver and transmitter use not synchronized external reference clocks. For a BER $\leq 10^{-5}$, a 7.5 cm distance is achieved for 2 Gbps rate and up to 22.5 cm distance for 500 Mbps. The circuit sensitivity to synchronization accuracy is shown in figure 7. It is shown that less than 10^{-6} BER is obtained within a margin of 4 DLL time steps. This ensures for the overall link to correctly synchronize within ±2 DLL time steps from the optimal time synchronization. Changes in the decision threshold (reference voltage) do not impact the data value decision significantly, as soon as the deviation does not exceed ±25 mV (figure 7(b)).

Figure 8 and table I summarize the transceiver performances and compare them to recent high data rate CMOS transceivers with antennas. This work shows an excellent trade-off between wireless transmission range, data rate and power consumption achieving better than 50 pJ/bit total energy efficiency, which is the best to our knowledge and sets the state-of-the art for this type of transceivers. The proposed circuit provides a fully integrated and low-cost solution for high data rate, low power, and short range wireless data exchange chipsets.

VII. CONCLUSION

This paper shows a fully integrated solution for wireless low power high throughput data exchange. Low power consumption is attained thanks to low modulation and architecture complexity with OOK modulation. Moreover, scalable consumption with throughput is realized thanks to super regenerator oscillator at the Rx side. Finally, integrated antennas offer very compact and low cost packaging solution.

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