A 0.7V Intermittently Operating LNA with Optimal On-Time Controller for Pulse-Based Inductive-Coupling Transceiver

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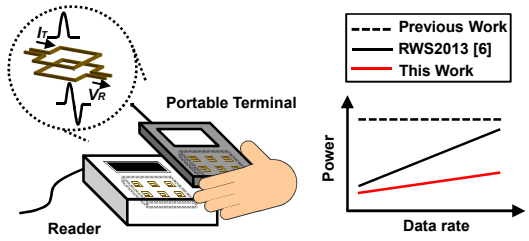
***Abstract* — This paper presents a low-power LNA for a inductive-coupling tranceiver. Intermittently operating technique to turn on LNA only at the moment when the pulse signal appears is used to reduce power consumption. To optimally control the On-time of LNA, pulse width detector based on self-oversampling TDC is used and compensate the PVT variations of On-time witdh and of pulse signal width. The fabricated test chip in 65nm CMOS occupies 0.06mm^2 and achieved the intermittently operating frequency at the range from 60 to 400Mbps. The power consumption is 0.42mW at 400Mbps and the supply voltage of 0.7V which corresponds to 37% power reduction from the power consumption without optimal On-Time Controller.**

***Index Terms* — inductive-coupling, Low Noise Amplifier, proximity communication, intermittent operation, pulse width detector, oversampling TDC.**

I. INTRODUCTION

In recent years higher-speed wireless interfaces are demanded with the increase of the content's size. TransferJet [1] is one of the standards for high-speed wireless proximity interface. Although, its communication range is relatively long (~3cm), the speed is not enough (357 Mbps) and the power consumption is still large (222mW) [2]. Our group have developed the low-power and high-speed proximity interfaces [3-6] using pulse-based inductive coupling technique as shown in Fig.1 (a). At [5] we already achieved 1.2Gbps with power consumption of 5.6mW. The data rate can be easily increased by arranging the inductive coupling channels.

To further reduce the power consumption, in our previous work, intermittently operating technique is proposed and demonstrated [6]. This technique is to turn on Low Noise Amplifier (LNA) only at the moment of pulse signal appearing. The power consumption of analog circuit can be reduced as well as digital circuit with the data rate decreasing as shown in Fig.1 (b). However in [6], the On-time of LNA is not controlled but is pre-determined. Therefore On-time can be too long or short because the received signal width can change by the channel characteristic or the slew rate of transmitter current as shown in Fig.2. Too long On-time causes the extra power consumption and shortage of On-time causes incorrect intermittent operation. Also On-time itself is critically affected by Process Voltage Temperature (PVT) variation



(a) (b)

Fig.1 (a)High-speed wireless proximity communication
(b)The power of LNA in variation of data rate

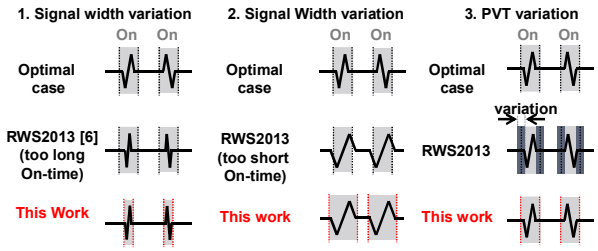


Fig.2 Effect of signal width and PVT variation

under the low supply voltage. In this work the optimal on-time controller is newly added to compensate those variations and set On-time optimally. In the On-time controller, multi-phase clocks are used to generate On-time clock. In addition the clocks are shared with self-oversampling Time to Digital Converter (TDC) which is used to detect the received pulse signal width and On-time clock width. On-time could be set optimally and automatically as the pulse width varying.

II. PROPOSED TRANCEIVER

A. *Inductive-Coupling Transceiver*

Fig.3 shows the block diagram of inductive-coupling transceiver. In transmitter data (TXD) is converted into pulse current (I_T). At the rising edge of CLK if TXD is high positive pulse current will feed into a transmitter coil. If TXD is low, negative pulse current will. In a receiver coil, voltage (V_R) which is proportional to dI_T/dt is induced. The receiver consists of LNA, hysteresis comparator, clock and data recovery circuit (CDR), and On-time controller. V_R becomes double pulse and is amplified by the LNA. An asynchronous data (V_{hys}) is recovered by hysteresis

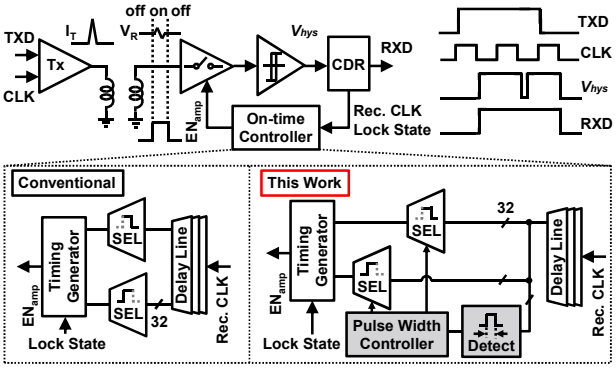


Fig.3 Block diagram of proposed transceiver

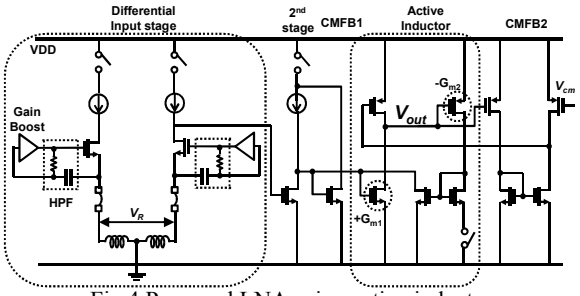


Fig.4 Proposed LNA using active inductor

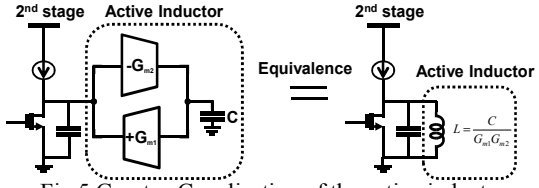


Fig.5 Gyrator-C realization of the active inductor

comparator. Since the V_{hys} contains glitch like pulse, complete Non Return to Zero (NRZ) data is restored by latching the V_{hys} with the recovered clock (Rec.CLK) which is internally generated from V_R. LNA is turned on only at the moment when received pulse signal appears. The On-time of LNA is controlled by On-time Controller. Compared with conventional work, the proposed On-time controller newly has pulse width detector and pulse width controller. The width of Rec.CLK is same as that of received pulse signal because Rec.CLK is generated from received pulse signal. In addition, timing of rising edge of both the Rec.CLK and received pulse signal are nearly simultaneous. This feature is used to detect the pulse width in this work.

B. Low Noise Amplifier using active inductor

Proposed two stage LNA with active inductor (AI) is shown in Fig.4. First stage consists of a gain boosted common gate topology which can be used at low power supply voltage. The second stage is the common source amplifier. The switches above the current source are used to control intermittently.

The AI is connected after 2nd stage to enhance the bandwidth. In this work, a gyrator-C based AI [7] was employed. Its equivalent model is shown in Fig.5. Note that

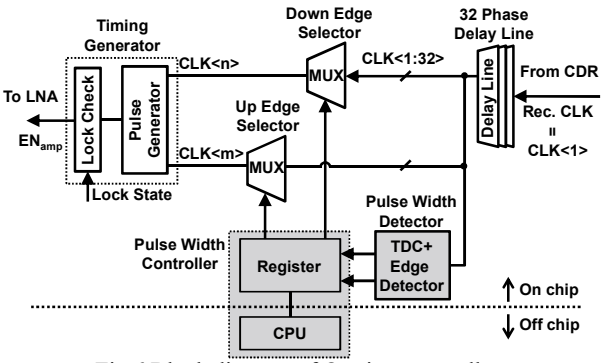


Fig.6 Block diagram of On-time controller

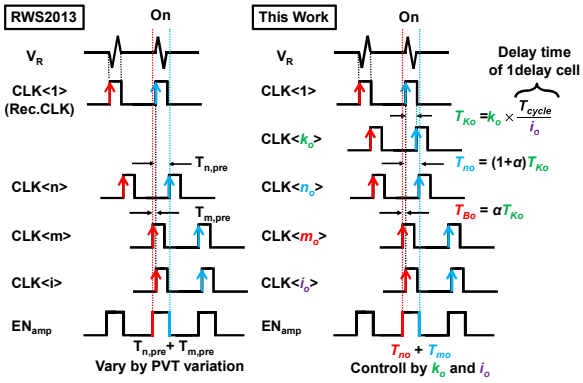


Fig.7 Timing chart at fast corner

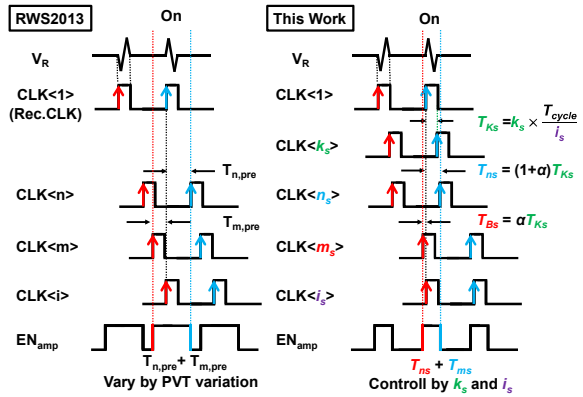


Fig.8 Timing chart at slow corner

L depends on the bias current because the G_m depends on the bias current. The current is adjusted by the reference voltage V_{cm} of CMFB2 so as to realize an optimum peaking. In our design, the chip area is reduced by sharing the capacitor used in AI and succeeding S/H circuit.

C. Proposed Optimal On-time Controller

Fig.6 shows the detail of the proposed On-time controller. Its operating timing chart at fast corner and slow corner are shown in Fig.7 and Fig.8 respectively. The enable signal of LNA, EN_{amp}, is generated here. The input (CLK<1>) is Rec.CLK which has same width and timing as received signal. Firstly multi-phase clocks are created from CLK<1> in delay line. Then two clocks, CLK<*n*> and CLK<*m*>, are selected in MUX to generate EN_{amp}, which have margin

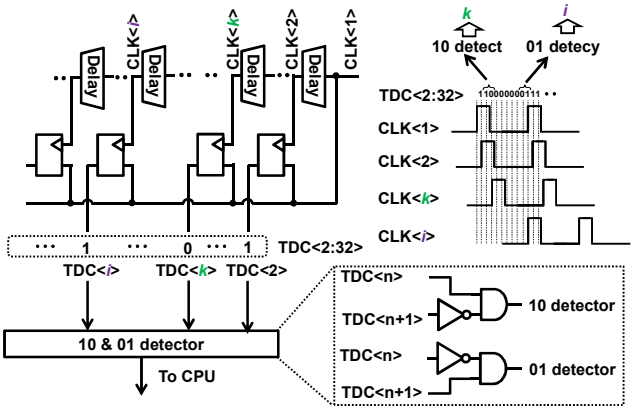


Fig.9 TDC based Pulse width detector

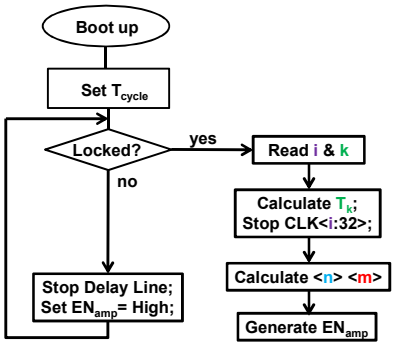


Fig.10 Flow chart of intermittent operation

$T_{n,pre}$ and $T_{m,pre}$ before and behind the rising edge of CLK<1> respectively. In conventional work, these two clocks are pre-selected. Therefore the width of EN_{amp}, T_{ENamp}, can vary by PVT variation of delay amount of delay cell. For example when the process changes from fast corner to slow corner, T_{ENamp} becomes unnecessary margin and LNA consumes extra power. Same effect occurs when the supply voltage changes from high to low.

In this work T_{ENamp} can be controlled optimally by tracking the width of received pulse signal and the delay amount of the delay cell. Pulse width detector and pulse width controller are newly added to compensate the variations. First the delay amount of one delay cell is calculated as T_{cycle} / i_o. T_{cycle} is one cycle of Rec.CLK. i_o is the number of the clock index which corresponds to the one cycle delay. Then the received signal width T_{ko} is calculated by the formula in Fig.7. According to T_{ko}, T_{no} and T_{mo} which have margin (1+)T_{ko} and T_{ko} respectively are decided. Then T_{ENamp} which has T_{no} + T_{mo} is decided. For example when the process changes from fast corner to slow corner, i_o changes to i_s. Then T_{ENamp} can be optimally controlled by following i_s.

D. Self-Oversampling TDC based Pulse Width Detector

Fig.9 shows the pulse width detector used in optimal On-time controller to calculate received signal width and delay amount of delay cell. It is realized by self-oversampling TDC. The multi-phase clocks used in TDC are generated in the delay line in Fig.6. By using simple D-Flip Flop (DFF)

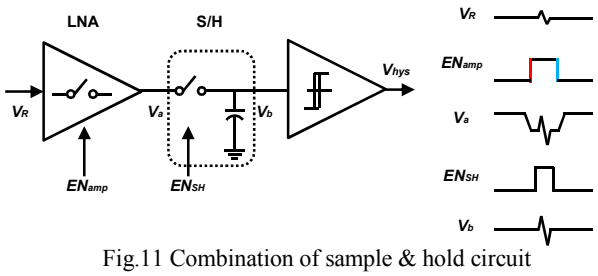


Fig.11 Combination of sample & hold circuit

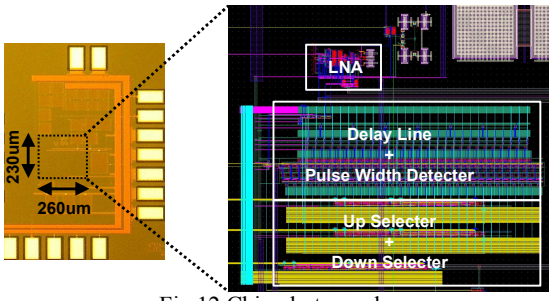


Fig.12 Chip photography

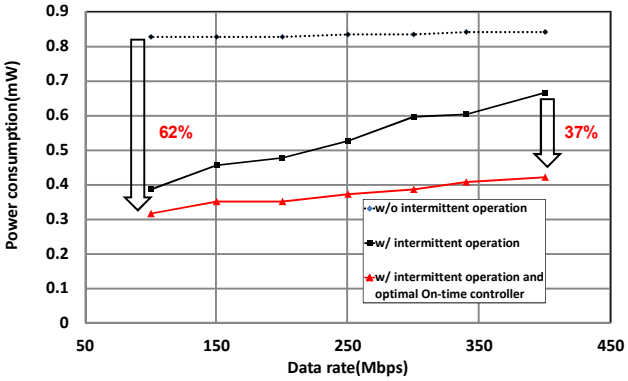


Fig.13 Power consumption of LNA

to oversample CLK<1> by itself, 31 TDC output can be obtained. Then CLK<*k*> and CLK<*i*> are detected where TDC output changes from 1 to 0 and from 0 to 1 respectively. After detecting CLK<*k*> and CLK<*i*>, the signal width, T_k, and the delay amount, T_{cycle} / i, can be calculated in CPU by the formula in Fig.7.

E. Flow of Intermittent Operation

Fig.10 shows the flow chart of intermittent operation. After booting up the transceiver, T_{cycle} should be set firstly. Next the Lock sate of CLK against data is checked. If not locked, EN_{amp} is always set high and the intermittent operation is disabled. If locked, the result of pulse width detector is read and the width of received pulse signal is calculated. Then the clock behind CLK<*i*> is stopped to reduce the power consumption. Finally CLK<*n*> and CLK<*m*> which are optimal margin are automatically selected to generate EN_{amp}.

When the LNA is turned on, the output common mode of the LNA (V_a) drops as shown in Fig.11. Because this common mode voltage drop brings false operation of the succeeding hysteresis comparator, S/H circuit is inserted between the LNA and hysteresis comparator. The S/H

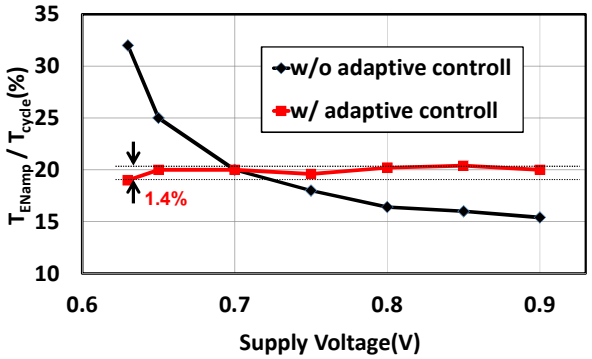


Fig.14 Pulse width vs. supply voltage

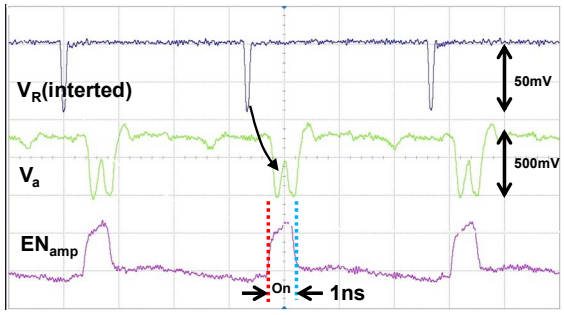


Fig.15 Waveform at intermittent operation

circuit is controlled by EN_{SH} whose high state is shorter than EN_{amp}. EN_{SH} is generated in On-time Controller as well as EN_{amp}.

III. MEASUREMENT RESULTS

Fig.12 is a photograph of the fabricated chip. The area of core chip is 0.06mm^2. Fig.13 shows the power consumption of LNA against data rate. As the scalability of power is maintained, the power consumption is reduced by 62% comparing with non-intermittent operation and by 37% comparing with intermittent operation not using optimal on-time controller. The offset power is caused by CFMB2 in Fig.4. It can be easily reduced by set several switches there. Fig.14 shows T_{ENamp} / T_{cycle} against the supply voltage. At the range from 0.63V to 0.9V, the rate of change can be suppressed less than 1.4%. Fig.15 shows the waveform of the intermittent operation. The input signal V_R is amplified only at the moment when EN_{amp} is high. Fig.16 shows the T_{ENamp} / T_{cycle} against code number of the MUX. The monotone and linearity can be maintained. The performance summary is shown at TABLEI.

IV. CONCLUSION

Intermittently operating LNA which operates at 0.7V has been developed in 65nm CMOS. The power consumption of LNA is reduced by 62% at maximum by using intermittent operation with optimal on-time controller. In addition, the pulse width variation could be suppressed less than 1.4% at the range of supply voltage from 0.6V to 0.9V.

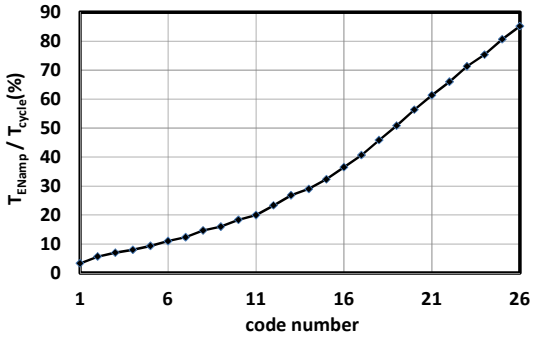


Fig.16 Pulse Width vs. code number

TABLE I. Performance Comparison

Refernce	RWS2013 [6]	This Work
Technology	65nm CMOS	65nm CMOS
Supply voltage	0.8V	0.7V
Intermittent operation frequency range	20Mbps-150Mbps	60Mbps-400Mbps
Energy efficiency (@400Mbps)	3pJ/bit	1.5pJ/bit
Chip core size	0.035mm^2	0.06mm^2

ACKNOWLEDGMENT

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