A 32-Gbps 4×4 Passive Cross-Point Switch in 45-nm SOI CMOS

Donghyup Shin and Gabriel M. Rebeiz

University of California, San Diego, La Jolla, CA 92093-0407, USA

***Abstract* — This paper presents a passive 4x4 cross-point switch in 45-nm SOI CMOS technology for LVDS systems with near-zero power consumption. The CMOS switch dimensions and layout structures are optimized using full-wave electromagnetic simulations for the highest 3-dB bandwidth in order to maximize the data-rate for digital signal transmission. Also, a novel series switch is used between the cells to enhance the bandwidth. The 4x4 switch matrix results in a measured 3-dB bandwidth of ~ 20 – 25 GHz (depending on the path) and an isolation > 40 dB at 26.5 GHz. The group delay variation is < ±5 psec, and results in very low jitter as seen from eye measurements (< 1.3 psec). Good eye-openings are obtained at 26 Gbps and up to 31.5 Gbps. The design is readily scalable to an 8x8 cross-point switch matrix.**

I. Introduction

Switch matrices are commonly used in various communication systems providing signal routing in servers, multi-core processing units, and fast memory interfaces. In silicon technology, there were several demonstrations of switch matrices for optical and digital networks [1-3]. However, since they are all based on active switching using CML multiplexers, they consume significant DC power and the maximum data-rate of the switching matrix is dependent on the multiplexer design.

In this paper, a 4x4 switching matrix in 45nm CMOS SOI is presented which is capable of passing digital signals with data-rates of up to 32 Gbps while consuming almost no DC power. The design was optimized to achieve maximum bandwidth and isolation considering all the parasitics and electromagnetic effect of interconnects. Also, a high degree of scalability is obtained by having a novel series switch after each 2x2 cell. This series switch minimizes the bandwidth drop as N increases by isolating the desired signal path from the open-ended transmission lines, which are capacitively loaded and degrade the bandwidth.

II. Architecture

Most of commercial cross-point switches today are based on multiple of N:1 multiplexers (Fig. 1b). Although this architecture provides fast switching and regeneration of signal waveform, the CML multiplexers consume significant DC power.

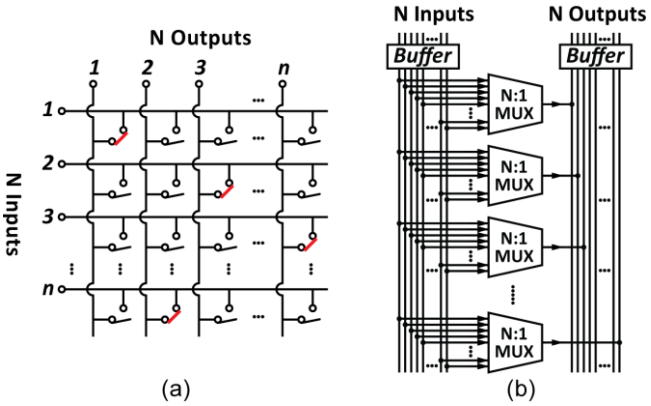


Fig. 1. Simplified block diagram of switch matrices in (a) cross-point and (b) multiplexer-based architecture

In contrast, a cross-point architecture shown in Fig. 1a using passive switches has the advantage of near-zero power consumption, bi-directionality, and easy scalability. Advanced CMOS technology such as 45nm SOI passive switches offers a high 3-dB bandwidth, which is directly related to the maximum data-rate of the transmitted digital signal. As a result, cross-point architectures using passive CMOS switches can achieve data-rates comparable to multiplexer-based designs, and are a promising candidate for low-power applications.

II. Design

Fig. 2 presents the block diagram of the proposed differential switch matrix which is suitable for LVDS systems. A 4x4 switch matrix is implemented for this work but can be scaled to larger dimensions. Switching cells are placed at every cross-point between the vertical and horizontal differential transmission-lines. The key design parameters are the 3-dB transmission bandwidth and the isolation between the ports, which correspond, respectively, to data-rate and cross-talk performance.

The 45-nm SOI process (IBM12SOI) provides advanced switch performance for high frequency operation. The 45nm CMOS transistors have low on-resistance and low off-state capacitance CMOS and also a buried-oxide (BOX) layer underneath which results in high isolation between the active layer and the low-resistivity substrate. Therefore, the substrate resistance

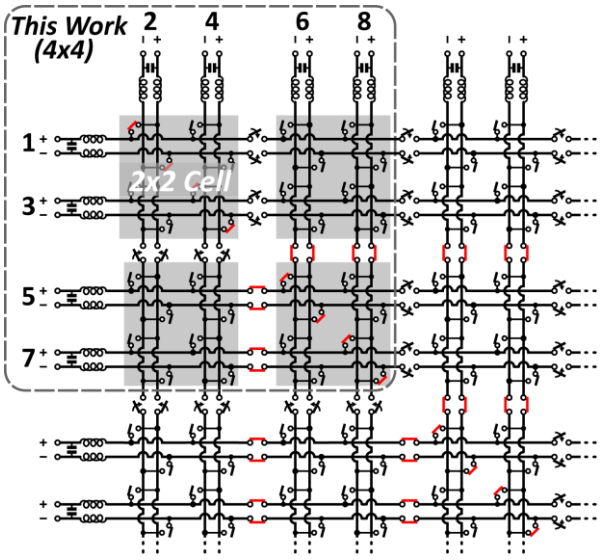


Fig. 2. Block diagram of the 4x4 switch matrix. Amplifiers can be placed at the input and output to equalize the (relatively) low loss of the switch matrix.

network which degrades the insertion loss and isolation of switch is no longer present in the SOI CMOS process.

The unit switching cell either "passes" or "isolates" the overlapped vertical and horizontal differential lines using a series-shunt-series switch in a differential configuration

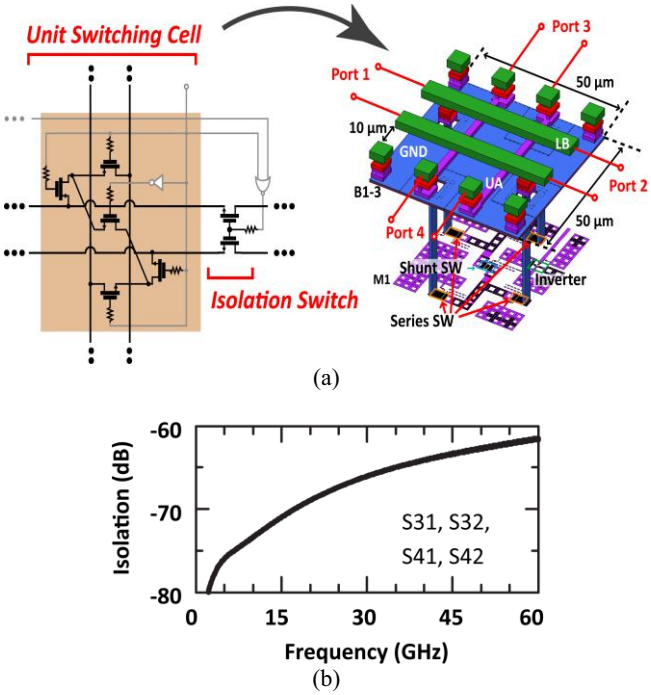


Fig. 3. (a) Schematic and 3-D geometry of the unit switching cell and (b) Sonnet simulations for the transmission line cross-overs.

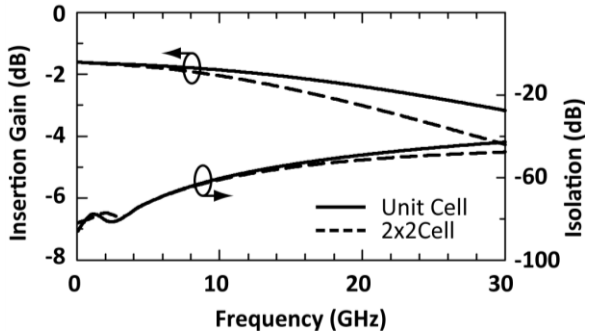
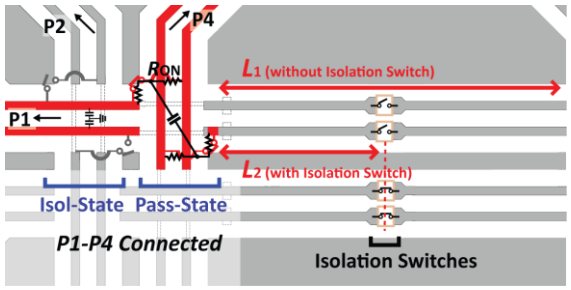


Fig. 4. Simulated insertion gain and isolation of a unit cell and a 2x2 cell.

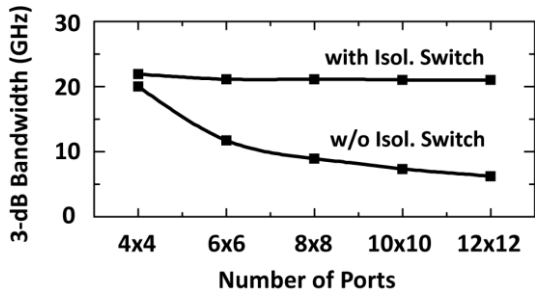
(Fig 3a). This configuration is chosen since it achieves a much higher isolation (~40 dB at 50 GHz) as compared to a simple series switch. The penalty is only ~0.5 dB increase in the insertion loss at 24 GHz, which is the required 3-dB bandwidth for 32 Gbps operation. The overlapped transmission lines are also modeled in a 3-D electromagnetic solver (Sonnet) in order to ensure that the "input" and "output" transmission lines have enough isolation. Simulations show an isolation > 65 dB between the four ports (S31, S32, S41, and S42) up to 30 GHz (Fig. 3).

Since the series-shunt-series configuration and cross-over lines provide a very high isolation up to 50 GHz, the CMOS switch dimensions can be optimized to achieve the best 3-dB insertion-loss bandwidth. A parameterized sweep was done to find the optimum nFET width with a setup including the 4x4 switch units, EM-simulated interconnects, and matching networks. A unit series-shunt-series switching cell with series switch width of 40 µm and shunt switch width of 7 µm result in a 3-dB bandwidth > 30 GHz and an insertion loss of < 3.2 dB while maintaining isolation of > 45 dB up to 30 GHz. A 2x2 cell shows a simulated insertion loss and isolation of < 4.3 dB and > 45 dB, respectively, up to 30 GHz (Fig. 4). In both cases, the 3-dB bandwidth is > 35 GHz since the DC insertion loss is 1.8 dB.

The simplicity of the cross-point architecture makes the design highly scalable once a 2×2 unit cell is designed. A 4x4 cross-point switch can be implemented using an array of 2×2 unit cells with proper biasing and control lines. However, care must be taken in order to maintain the bandwidth of the 2x2 cell as N increases. This is because the off-state switch capacitances are always present and load the signal line, but more importantly, the transmission lines which are not connected to the output ports effectively become short open-stubs which add significant capacitance as N and their lengths increase.



(a)



(b)

Fig. 5. (a) Top metal layout and parasitic components when P1 is connected to P4 and (b) simulated 3-dB bandwidth of switch matrix with different number of ports, with and without the series isolation switches.

This effect can be overcome by using an isolation switch after each 2x2 cell as shown in Figs. 2 and 5. After a unit switching cell is turned on to become a "pass-state" (horizontal and vertical lines connected), the isolation switch following this unit cell is turned off such that the open-ended transmission line after the "pass-state" switch becomes very short. Each cell is therefore loaded by a very short open-stub as a capacitive load (L_2 in Fig. 5a) irrespective of the size of the switching matrix. This greatly increases the bandwidth and scalability of the design as shown in Fig. 5b. Note that the 3-dB bandwidth remains the same even for a 12x12 matrix (or even a 16x16 matrix) using the series isolation switch. The only penalty paid is insertion loss which can be compensated using external wideband amplifiers.

II. Measurements

Fig. 6 presents the microphotograph of the 4x4 cross-matrix switch in 45-nm SOI CMOS. Inductors are used at the input and output ports in order to match the off-state capacitance of the un-used cross-point switches on each line. The overall chip dimension is 1.4x1.4 mm^2 but is dominated by the 100 µm pitch GSSG differential RF pads. The core matrix occupies only 0.69×0.69 mm^2 including the matching networks.

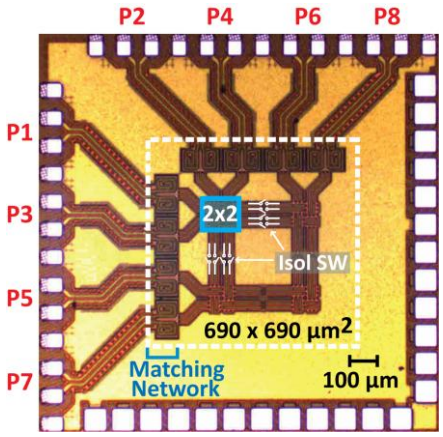


Fig. 6. Microphotograph of the 4x4 cross-point switch matrix. The dimensions are 1.4×1.4 mm^2 including pads.

The small-signal S-parameters were measured using Agilent N5242A PNA-X 4-port network analyzer up to 26.5 GHz. A short-open-load-thru (SOLT) calibration is done to define the reference planes at the GSSG probe tips. Fig. 7 presents the measured results when P1-P2, P3-P4, P5-P6, and P7-P8 are connected. The measured return loss for four different paths is < 8.5 dB up to 26.5 GHz. The measured insertion loss at 20 GHz is 4.7 - 6.2 dB for the four different paths, and the 3-dB bandwidth is ~20-25 GHz depending on the path. Paths S_{65} and S_{87} show higher insertion loss compared to S_{21} and S_{43} because they are passing by an isolation switch (~1 dB loss at 20 GHz).

The isolation plot shows S_{41}, S_{61} and S_{81} when P1-P2 are connected, and the measured isolation is > 40 dB up to 26.5 GHz regardless of the path. However, since it is not possible to terminate port 2 with 50 Ω when measuring the isolation at ports 4, 6, or 8, the isolation measurement shows some ripple as a result of reflection from the open circuit port. This effect and a slightly inaccurate switch model account for the discrepancy between simulation and measurement. Group delay measurement shows very low variation (±5 psec) from DC to 26.5 GHz, which results in low horizontal variation in the eye diagram.

In order to verify the signal integrity of the signal passing through the switch matrix, an eye diagram is measured at different data rates. A differential 15-44 Gb/s pseudo-random binary sequence (PRBS) pattern of 2^{31}-1 signal generated from Centellex TG1P4A pulse pattern generator is injected into the switch matrix and the output of the matrix is connected and analyzed using an Agilent 86100A DCA sampling oscilloscope. The resulting eye diagrams show good eye opening at the maximum data-rate of 31.5 Gbps (47 mV and 23.7 psec eye height and width respectively when the input waveform is 230 $mV_{peak\text{-}to\text{-}peak}$) with an rms jitter of 1.6 psec (Fig. 8). The

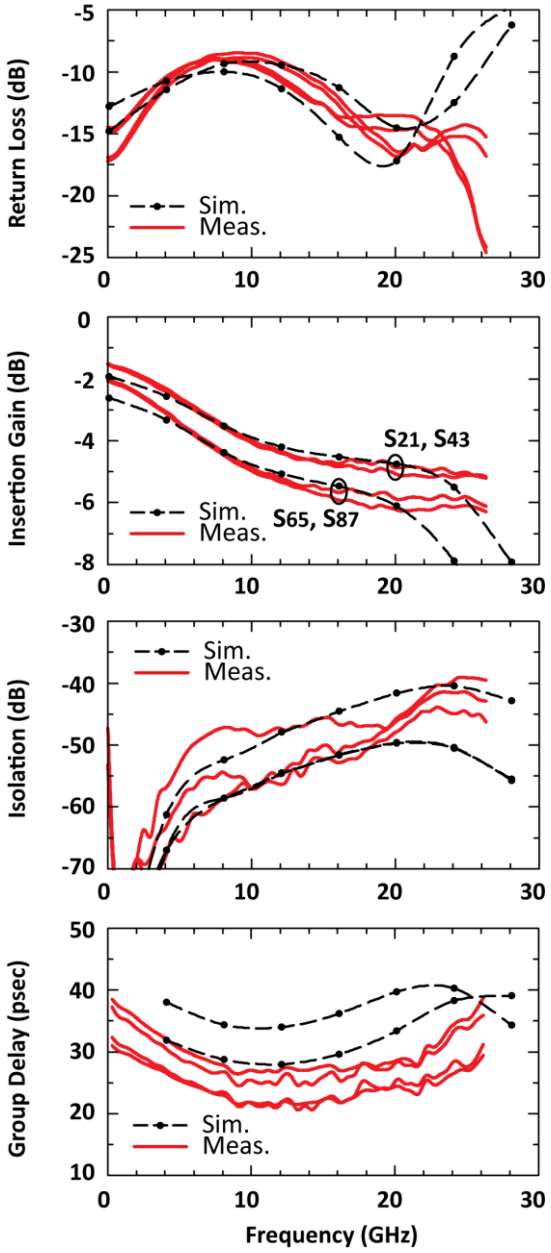


Fig. 7. Measured and simulated S-parameters of 4x4 switch matrix when P1-P2, P3-P4, P5-P6, and P7-P8 are connected.

measured rms jitter includes the jitter from the measurement setup (bias tee, attenuators, cables, etc.), which is determined to be 0.84 psec from measuring a THRU standard on the calibration substrate. Therefore the jitter contribution from switch matrix itself is < 1.3 psec.

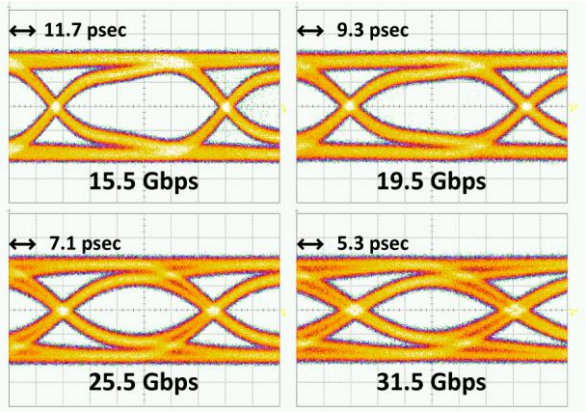


Fig. 8. Eye diagrams of 4x4 switch matrix with different data-rates when the input swing is 230 $mV_{peak\text{-}to\text{-}peak}$.

V. Conclusion

This work shows that a 4x4 cross-point switch matrix with a data-rate of > 30 Gbps and no DC power consumption is achievable using passive switches in 45-nm SOI CMOS. This design is a good candidate to replace the existing CML-multiplexer switch matrices in optical and digital networking applications.

Acknowledgement

This work was supported by Intel Corp., Portland, Oregon, and the US-Army Research Laboratories, Maryland, USA.

References

[1] H. Veenstra, P. Barre, E. van der Heijden, D. van Goor, N. Lecacheur, B. Fahs, G. Gloaguen, S. Clamagirand, and O. Burg, "A 20-input 20-output 12.5Gb/s SiGe cross-point switch with less than 2ps RMS jitter," in *Proc. Int. Solid State Circuits Conf., 2003*, pp. 174–176.

[2] A. G. Metzger, C. E. Chang, K. D. Pedrotti, S. M. Beccue, K.-C. Wang, and P. M. Asbeck, "A 10-Gb/s high-isolation 16_16 crosspoint switch implemented with AlGaAs/GaAs HBT's," *IEEE J. Solid-State Circuits*, vol. 35, pp. 593–600, Apr. 2000.

[3] K. S. Lowe, "A GaAs HBT 16_16 10-Gb/s/Channel crosspoint switch*," IEEE J. Solid-State Circuits*, vol. 32, pp. 1263–1268, Aug. 1997.

[4] D. Shin, D-W Kang, and G. M. Rebeiz, "A 0.01-8-GHz (12.5 Gb/s) 4x4 CMOS switch matrix," *IEEE Trans. Microw. Theory Tech.*, vol. 60, pp. 381–386, Feb. 2012.