A 36GHz/mW Single-Phase Prescaler using Implication Logic in 0.13μm CMOS

Elkim Roa, Wu-Hsin Chen and Byunghoo Jung
School of Electrical and Computer Engineering - Purdue University
elkim,jungb@purdue.edu

***Abstract*— This paper presents a non-Boolean digital logic technique used in the design of a high-speed and low-power frequency prescaler. Maximum achievable frequency input of prescalers is limited by the number of devices connected in cascade to the high-speed signal path. In this work, a reduced number of devices is obtained in the prescaler by realizing implication logic operators with a single-phase digital-based flip-flop. The prescaler is implemented in 0.13μm CMOS with a 1.2V supply. A measured efficiency of 36GHz per mW is achieved which represents 3X power consumption reduction compared to prior art in the same technology node, and the highest efficiency reported.**

I. Introduction

Multistandard SOC radios require on-the-fly reconfigurable frequency plans to mitigate VCO pulling issues caused by SOC-CPU clock interference. Reconfigurable fractional frequency dividers enable the on-the-fly adjustment by changing the VCO frequency and divider ratio by inverse factors, such that synthesized channel remains unchanged [1]. Closely spaced fractional division ratios would afford the use of just one VCO for different standards. However, fractional frequency dividers may exceed power budget and therefore they must be implemented using low power techniques. Fractional frequency division is typically implemented by mixing or phase rotation techniques that require inductors or stringent timing constraints. A compact solution is to use integer frequency prescalers in quadrature [1]. Frequency prescalers must be able to work in a large tuning range and at high operating frequency because, for some standards, the synthesized VCO frequency can be 4X larger than required radio band. Furthermore, in clock generation synthesis the energy consumption depends strongly on VCO and frequency dividers. In an energy saving strategy, the first frequency prescaler after the VCO is a key block to be considered to decrease overall power.

In this paper, we have demonstrated a simplified digital divider-by-2/3 operating at 17.1GHz in 0.13μm as a successor to Current Mode Logic (CML) in relative high-speed applications. We propose a new dual-modulus prescaler scheme using extended true single-phase-clock (ETSPC) [2] logic-style with a reduced number of transistors allowing high-frequency division. A non-Boolean-logic-based technique is proposed to extend the maximum achievable input frequency (f_{max}) while providing low-power and low-area. The energy consumption is reduced 3X and the f_{max} is increased by 20%, both compared to prior art in same technology process [3].

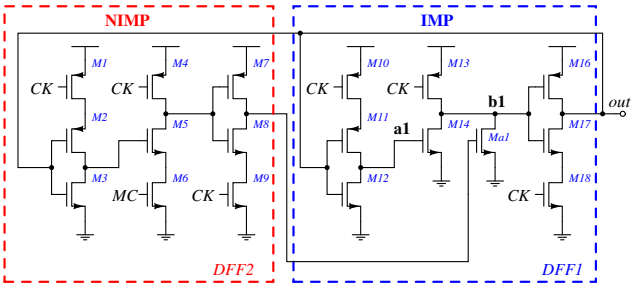

Fig. 1. Dual modulus prescaler presented in [3].

II. Compact and High-Speed Frequency Prescaler

A common approach to implement frequency prescalers in the lower half of the centimeter-wave band is to use TSPC logic structures [3], [4], whereby a single clock is required to drive the logic. This removes the need for differential clock generation as in CML, and skew/overlapping issues [5]. Recently, different TSPC-based topologies have been proposed to include the logic gates that select the divider mode within the Flip-Flops (FFs) in order to reduce the number of stages in cascade. Nonetheless, capacitance loads increase at the nodes, requiring greater drive capability in internal nodes. In [4], a divider-by-2/3 with TSPC and ETSPC cells includes the OR and AND gates in the same branch, with an inverter placed between the FFs adding a stage to the logic chain. Additionally, in divide-by-2 mode, two branches of the three non-used FF are still switching.

A divider-by-2/3 in TSPC logic that achieves 14GHz in a 0.13μm CMOS is reported in [3]. Figure 1 presents the prescaler in [3] which is based on implication logic cells to achieve more power efficiency. Although there is no additional inverter or logic gate between the FFs, the logic operation is realized in the critical path. Transistor Ma1 loads the node b1, reducing the maximum frequency achievable. In addition to using three transistors for branch, the transistor Ma1 forces to increase the size of M13 which

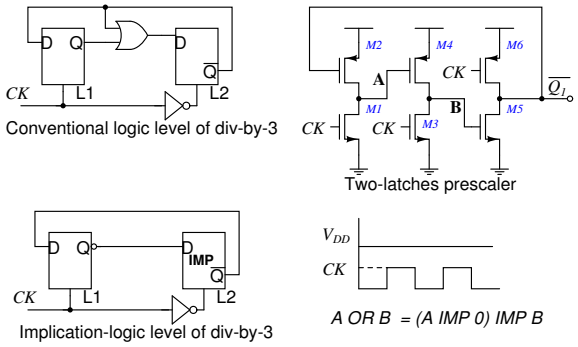

Fig. 2. Proposed two latches dual-modulus prescaler using implication logic.

A	B	B'
0	0	1
0	1	1
1	0	0
1	1	1

TABLE I
TRUTH TABLE FOR IMP, $A \rightarrow B$.

implies more load capacitance to nodes a1 and b1.

Instead of using the conventional logic concept, we rely on a new logic concept that allows us to minimize the number of elements in the critical path of the divider. The compact design is the result of using the implication logic concept [6]. In place of using the basic logic cells AND and OR to operate the selection mode, the flip-flop in Fig. 2 intrinsically executes the material implication operation IMP. The truth table of the IMP operator is shown in Table I. A latch or flip-flop that can execute the implication operation would be able to synthesize Boolean logic operations. Recursive logic gates can be synthesized with implication operators that have the ability to store a variable. For instance, the flip-flop (master-slave latches) in Fig. 2 has the capacity to execute the IMP operation by replacing the OR operation in the classical divider-by-3. Considering the inputs of the cell as the gate of M4 and the gate of M5, and checking each combination of the inputs with the truth table of the IMP operation, the flip-flop executes the IMP operation.

As a result, the operation of the simplified prescaler shown in Fig. 2 is as follows. In divide-by-2 mode, the FF is connected as a Mobius counter. The FF can be seen as two-latches, where the first latch is high-level active and the second latch is low-level active. By placing an OR gate between the two-latches, the circuit is setup as a divider-by-3. The operation OR is substituted by the operation IMP, where the second latch executes the IMP operation between

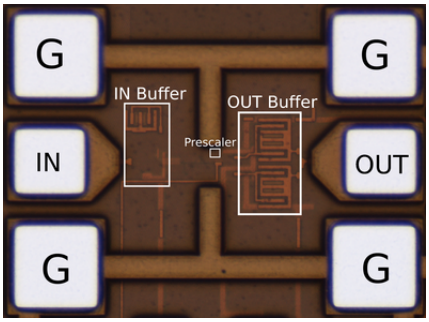

Fig. 3. Chip micrograph.

the input and the output if the offset-level of the clock signal is shifted down. In other words, the operation performed at node B is (A IMP 0) IMP B, which is the same as A OR B. The complete performed operation is explained in Table II, where 0- and 1- indicate the new logic values with the clock level shifted down. Therefore, by shifting down the clock level, the circuit goes from divide-by-2 to divide-by-3 mode. This configurable behavior can leverage an automatic adjustment of closely spaced ratios.

The flip-flop is transparent at the negative-edge instead of the positive-edge, decreasing the load capacitance driven by the clock. In the case of positive-edge flip-flop as in [3], [4], Fig. 1, the clock is driving two gates of PMOS transistors. In the case of negative-edge DFFs Fig. 2, the clock is driving 2 gates of NMOS transistors and 1 gate of a PMOS transistor. Therefore, the load capacitance to the clock is lower in the NMOS case considering that NMOS transistors are smaller for a given load, resulting in a power consumption reduction and a lower path delay.

TABLE II
RESULT IN NODE B FOR LOWER DC LEVELS AT CK.

A	B	$A_{CK=0}$	$A_{CK=1}$	$A_{CK=1-}$	$A_{CK=0-}$
0	0	1	0	1	1
0	1	1	0	1	1
1	0	0	0	0	0
1	1	1	0	1	1

III. MEASUREMENT RESULTS

The dual-modulus prescaler was fabricated using 0.13μm CMOS and have an active area of 10μm $\times$ 7μm. Figure 3 shows a micrograph of the test chip. The test setup is shown in Fig. 4. Notice that voltage supplies of the prescaler and output driver are separated to measure independently the power consumption. However, the power consumption of the first buffer seen by the output of the prescaler, is included in the reported consumption. For testing the two-latches prescaler, a bias tee was used at the input

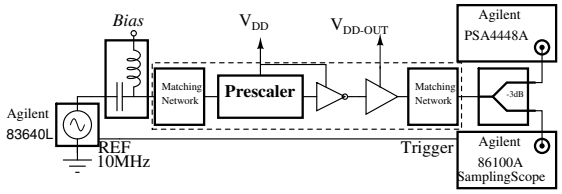

Fig. 4. Block diagram of the test setup.

TABLE III
PERFORMANCE COMPARISON.

Design	Tech.	Div.	f_{min}/f_{max} [GHz]	Efficiency [GHz/mW]
CML dyn. [5]	65nm	4	20/70	10.86
IL [7]	65nm	2	79/81.6	30.3
TSPC [8]	0.13μm	2/3	8GHz	6.8
TSPC [3]	0.13μm	2/3	5/14.1	11.66
TSPC [4]	65nm	2/3	6.2/16GHz	35.71[!]
ETSPC [4]	65nm	2/3	8/18GHz	28.5
This work	0.13μm	2/3	6/17.1	36.3

[!] Measured in divide-by-2 mode.

in order to shift the offset-level of the clock signal in conjunction with the supply voltage of the input buffer. Table III summarizes and compares the performance of the state-of-the-art frequency prescalers. The two-latches prescaler consumes only 471μW from a 1.2V supply at f_{max} of 17.1GHz in divide-by-2. In divide-by-3 mode, the consumption is 444μW.

Figure 5 shows the output waveforms measured with a sampling scope (Agilent 86100A) at f_{max}. In Fig. 6, the mean measured input power level sensitivity plots are presented. For the supply sweeps, the input power is fixed to 12dBm. For the input power sweeps, the voltage supply is fixed to 1.2V. The locking range at an input power of 12dBm is from 6GHz to 17.1GHz with a 1.2V supply. Figure 6 indicates an operation of 6GHz with a 0.55V supply voltage. Out of four measured chips, all are fully functional with variations of f_{max} in a range below 200MHz for different supply voltages and worst-case temperature. These results indicate the feasibility of using the frequency prescaler in a wide frequency range with a low voltage supply settled to the required f_{max} to decrease power consumption.

Figure 7 shows the measured phase noise at the input (top-curve) for a 17.1GHz input. The middlemost-curve is the measured phase noise at the output in divide-by-2 mode. The phase noise in divide-by-2 mode is 6dB lower (up to 1MHz offset) than the input, as theoretically expected from a division-by-2. A similar result is obtained from the output phase noise in divide-by-3 mode (bottom-curve), which is 9dB lower compared to the input. The results indicate that the proposed dual-modulus frequency prescaler introduces a negligible degradation. Measured spectrum plots at the

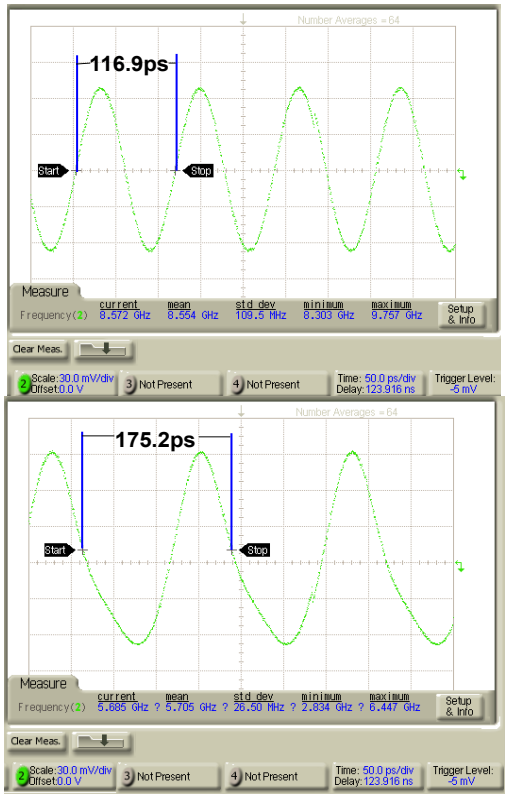

Fig. 5. Measured output waveforms in div.-by-2 mode (upper) and div.-by-3 (lower) for a 17.1 GHz input.

output of the prescaler are shown in Fig. 8 for divide-by-2 mode, and for divide-by-3 mode in Fig. 9 with an input of 17.1GHz.

IV. CONCLUSION

The performance comparison in Table III indicates that the proposed prescaler provides the highest power-efficiency among the previous reported designs. We demonstrate sub-1mW compact prescaler working in frequencies above 15GHz with 3X lower power consumption compared to prior art in same technology node. The applied design strategy is a radical departure from conventional approaches. This technique enables digital-based prescalers to operate at significantly improved speed performances.

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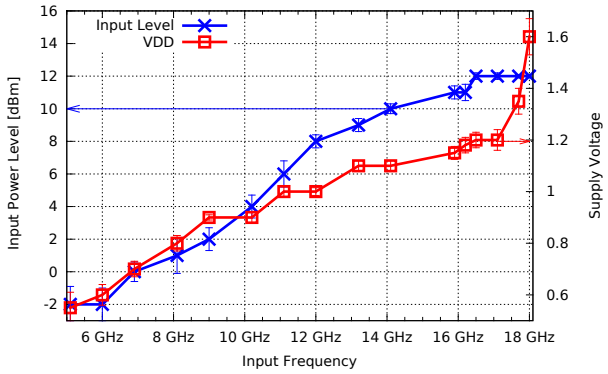

Fig. 6. Measured input power level and voltage supply sensitivity in divide-by-3 operation mode.

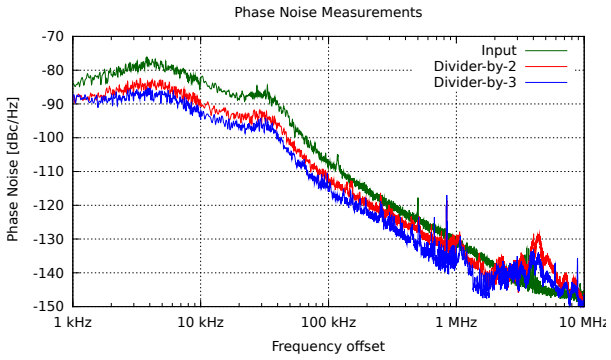

Fig. 7. Measured phase noise at the input @ 17.1GHz (top curve), at the output in divide-by-2 mode (middlemost curve) and -3 operation mode (bottom curve).

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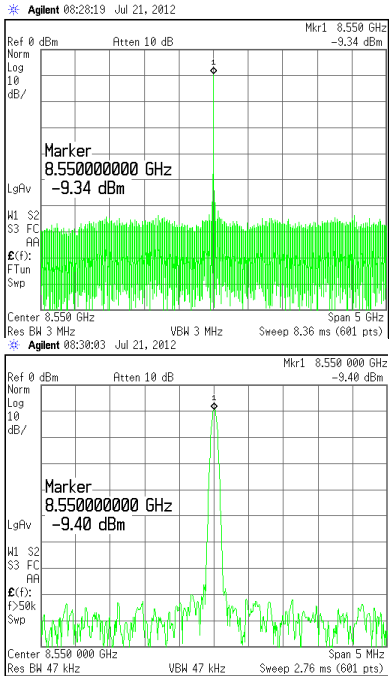

Fig. 8. Measured spectrum output in divide-by-2 mode at 17.1GHz input.

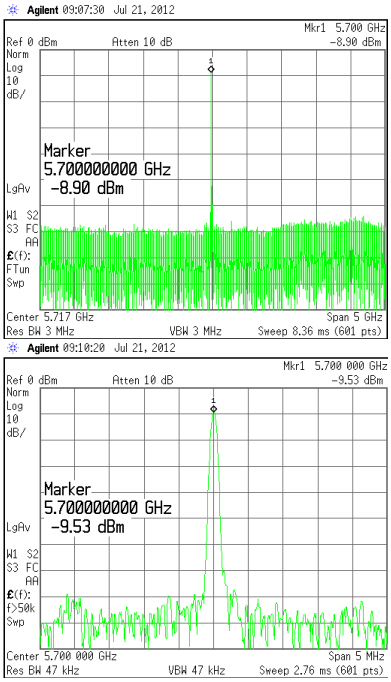

Fig. 9. Measured spectrum output in divide-by-3 mode at 17.1GHz input.