A Sub-GHz Low-Power Wireless Sensor Node with Remote Power-Up Receiver

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***Abstract* — A fully integrated low-power sub-GHz sensor node is presented for wireless sensor networks (WSN). The sensor node features a sensor IC and a RF transceiver IC, vertically assembled in a single QFN package. A unique remote power-up scheme is configured to supply the power to a sensor node from power-down state. It features a technique of centralized remote power-up scheme combined with local broadcasting power-up sequence to achieve ultra-low standby current, fast power-up time, and extended coverage. It proposes a time division switch to separate power-up message from data information, both propagated at the same frequency band. The standby current in power-down state draws less than 450nA. The sensitivity of power-up receiver is -24dBm, while the sensitivity of data receiver is -103dBm. The Sensor and RF transceiver ICs were fabricated in 0.25μm CMOS and 0.18μm RF CMOS, respectively.**

***Index Terms* — Wireless sensor network, low-power RF transceiver, sensor, remote power-up receiver, sensitivity.**

I. Introduction

In a wireless sensor network (WSN) design, radio transceiver and communication protocol are mainly tailored to provide high power efficiency. One way to increase the lifespan of sensor networks takes advantage of duty cycle control, leaving radio transceiver off and waking it up asynchronously only when needed to access data. Periodically wake-up receiver or dedicated wake-up receiver [1, 2] have been used for high power saving, but their standby current would not be tolerable in some applications such as transportation or automotive, where a number of sensor nodes should be powered down while the engine is off. Putting the sensor networks into long-time hibernation is more efficient to conserve power by shutting down the sensor nodes which are not used or in active for a long time. This scheme enables a sensor node to have extremely low standby current (< 1μA), but the power-up scheme becomes significant. Furthermore, if the applications require fast power-up time and wide power-up coverage at the same time, conventional approaches are hard to accomplish those system specifications.

This paper presents a fully integrated low-power sub-GHz sensor node for densely distributed sensor network. It features a technique of centralized remote power-up scheme combined with local broadcasting power-up sequence to achieve fast power-up time and extended power-up coverage. The sensor node utilizes a type of time division multiplexing scheme for receiving data and power-up commands that operate at the same frequency band. The power-down current in a sensor node only draws approximately 450nA. The power-up time of a WSN where more than 100 sensor nodes are distributed within a 5m radius is less than 100 ms.

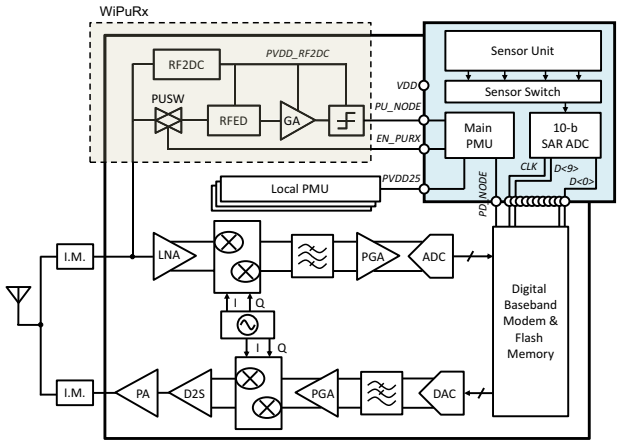

Fig. 1. Block diagram of the sub-GHz sensor node including an RF transceiver and a sensor unit.

II. Sensor Node Architecture

Fig. 1 shows a simplified block diagram of a sensor node. It consists of two ASICs, an RF radio and a Sensor. The fully integrated RF radio consists of transceiver (TRx), power-up receiver (WiPuRx), LO synthesizer, 8-b data converters, and a digital baseband. The architecture of the transceiver is based on a 2MHz low-IF receiver and a direct modulation transmitter. The single-ended input differential output LNA has two gain mode settings. The differential downconverted signal by the double-balanced passive switched I/Q mixers is fed into a differential TIA. A complex 4th-order band-pass filter centered at 2MHz incorporated with programmable gain stages can adjust its bandwidth up to 4MHz and baseband gain up to 65dB.

Transmitter supports a direct up conversion transmit mode with an active-RC biquard filter. The variable-gain driver amplifier (DA) provides output power in the range of -11dBm to +3dBm. The DA has an extra turbo mode with +10dBm output power to perform local broadcasting power-up sequence. The digital baseband includes ASK/FSK modulation processor, Gaussian pulse-shaping filter, automatic gain control, and a 1024byte Flash memory. The quadrature LO signal is generated on-chip using a fractional-N frequency synthesizer to obtain fine frequency resolution and fast lock time. An 18-b ΔΣ modulator controls the divider modulus, steps as small as 61Hz can be achieved from a 16MHz reference over a synthesizable range from 850 to 990MHz. The target phase noise of the synthesizer is -108dBc/Hz at 1MHz offset from the carrier, and lock-up time is less than 25μs.

Sensor ASIC consists of three on-chip analog sensors including voltage, temperature and current, a main power management unit (M-PMU), an analog 3:1 multiplexer, and a 10-b SAR ADC. The M-PMU includes a power control unit that configures the power-up sequence and a main LDO that generates 2.5V regulated supply voltage (*PVDD25*) from a single battery. The regulated 2.5V is supplied to local LDOs at RF radio IC to generate 1.8V regulated supply voltages (*PVDD18_i*).

III. Wireless power-up receiver

Wireless power-up receiver (WiPuRx) is designed to generate a self-powered power-up enable signal (PU_NODE) that alerts the transition to power-up mode from power-down state. The WiPuRx has a RF-to-DC converter (RF2DC) to supply DC power to WiPuRx. It also includes a power-up switch (PUSW), an RF envelope detector (RFED), a 3-stage amplifier (10 x 10 x 5.5) and a hysteresis comparator. Antenna on a sensor node is a printed PCB-type that is LC-matched to the average input impedance of TRx and WiPuRx. The WiPuRx shares the antenna with TRx to reduce the system overhead. The PUSW is placed in between the antenna and WiPuRx to isolate TRx path from power-up path. Since RF packet data and power-up command are propagated at the same frequency band of 915MHz, impedance matching network should be taken carefully to achieve excellent NF and the sensitivity. From impedance matching analysis, it becomes clear that the maximum sensitivity of Rx and WiPuRx do not occur at the same impedance. In Rx mode, the PUSW is turned off, so high input impedance of WiPuRx is added to that of Rx. The matching network is designed so that the input impedance is about 50 Ω at 915MHz. In power-up mode, the PUSW is 'on' state while TRx is turned off. On-board matching network is designed to make high-power input impedance of WiPuRx less than 200Ω with input power of -10dBm at 915MHz.

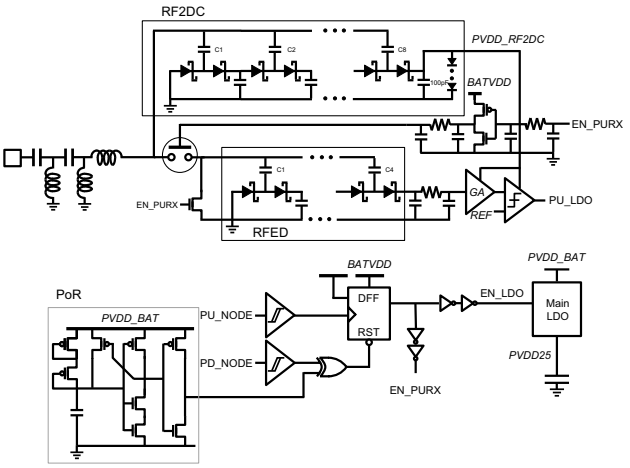

Fig. 2. Circuit schematics of the WiPuRx and the M-PMU.

A. Circuit Design

Fig. 2 shows the simplified circuit schematics of WiPuRx and M-PMU. RF2DC provides DC supply voltage (*PVDD_RF2DC*) to the WiPuRx from incident RF power-up message at 915MHz. Power-up message consists of adjustable 8~64 packet-length 'H' signal in OOK format. It is followed by a 16-b Power-Up Identification (PUID) to avoid false power-up sequence. Eight parallel Schottky barrier diode (SBD) based rectifier [3, 4] is chosen to enhance RF2DC input sensitivity and power conversion efficiency. The unit size of Schottky diode is 2 x 4 μm^2. *PVDD_RF2DC* has a five-stage diode clamp in parallel with a 100pF on-chip capacitor to limit accumulated voltage less than 3.1V. The PUSW is controlled by a signal EN_PURX that is generated at M-PMU. When WSN is downed, base-station delivers power-down message to all sensor nodes, by using either command packets or broadcasting. Then, the main LDO is shut down (EN_LDO = 'L') and the PUSW is 'on' state to detect power-up message (EN_PURX = 'L'). When the network is opened, base-station broadcasts power-up message to all sensor nodes. The power-up message is converted to DC voltage *PVDD_RF2DC* so that WiPuRx becomes "on" state. At the same time, the message is delivered to RFED through on-state PUSW. The single-ended RFED output is fed into a hysteresis comparator to generate power-up enable signal, PU_NODE. The structure of RFED is the same as the RF2DC except deploying only four parallel rectifiers. The reference voltage of a comparator is determined to around 0.5V by the ratio of pull-up to pull-down device conductance.

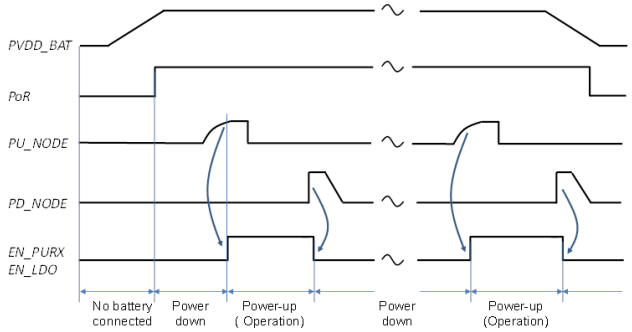

Fig. 3. Timing diagram of the power-up sequence.

B. Self-Power-Up Sequence

Main power management unit (M-PMU) at Sensor ASIC manages power-up sequence of a sensor node. It consists of a power control unit (PCU) and a main LDO. The PCU generates EN_PURX and EN_LDO signals to decide the state sequence. The control signals are synchronized to power-up enable signal PU_NODE and power-down enable signal PD_NODE. When a sensor node is connected to a Li-Ion battery with sufficiently high voltage, the power-on-reset (PoR) detects and generates a reset pulse signal to initialize the sensor node into a known state. As power-up sequence is initiated, PU_NODE triggers EN_LDO and turn the PUSW off, pushing the Sensor and RF radio into operation mode. The operation mode is ended with power-down command that is encoded to generate PD_NODE at digital baseband. These two signals are combined with the PoR output to reset the D-F/F, putting the sensor node into power-down state. Fig. 3 depicts the timing diagram of power-up sequence in a sensor node. The WSN is initially power-off state and starts its operation by accepting System-On signal (power-up message) from base-station. After power-up sequence is completed, the sensor node initiates the local power-up operation so that the node broadcasts local power-up message to neighboring nodes. Base-station can continuously monitor and configure the nodes' power-up state, commanding a local power-up sequence and asking for power-up completion.

C. Local Power-Up Sequence

Fig. 4 shows the circuit schematics of a variable-gain DA. It is composed of four cascaded CMOS inverter-type stages and a bias control circuitry. Slightly lower linearity performance is compensated with relatively simple design, reliable driving of (external) PA with non-negative voltage swing, and improved power efficiency of PA.

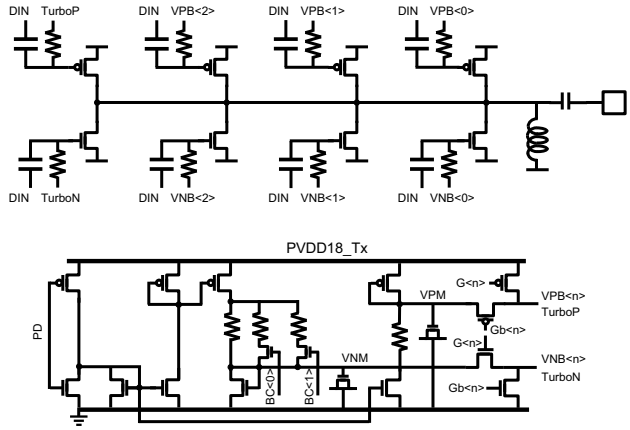

Fig. 4. Circuit schematic of DA for local power-up sequence.

Careful design of the inverter-stage sizes, digitally controlled driver transconductance (G<2:0>), and programmable bias current (BC<1:0>) achieve excellent DA gain and linearity performance. The DA has additional control bit of TurboP(N) to turn a turbo inverter driver on. It can boost the output power of the DA up to +10dBm during local power-up sequence. The simulation results of DA gain versus output power under given conditions of G<2:0> = <111> and Turbo = 'L' are shown the estimated output power and output P1dB of +5dBm and 3.5dBm, respectively.

IV. Measurement Results

The measurement results of the sensor node are shown in Fig. 5. WiPuRx achieves the sensitivity of -24dBm at 915MHz. The S11 of WiPuRx is -7dB at 915MHz, while the input return loss of Rx is about -18dB. The input matching is emphasized on Rx path over WiPuRx because of barely enhanced sensitivity of WiPuRx even with improving S11 of -18dB from -7dB. It is noted that similar sensitivity performance is observed with a large-signal impedance matching plot. The larger-signal S11 is measured -7dB until input power up to -24dBm, where WiPuRx is 'ON' state and enters a power-up mode. The S11 becomes -20dB when input power is beyond -13dBm. It means that Rx is turned on. The power-up distance between a sensor node and base-station is measured up to 4.5 meters when base-station uses external PA with Pout,max of +28dBm. The local power-up sequence enables the neighboring sensor nodes to be power-up mode, and the power-up distance is about 0.3 meters.

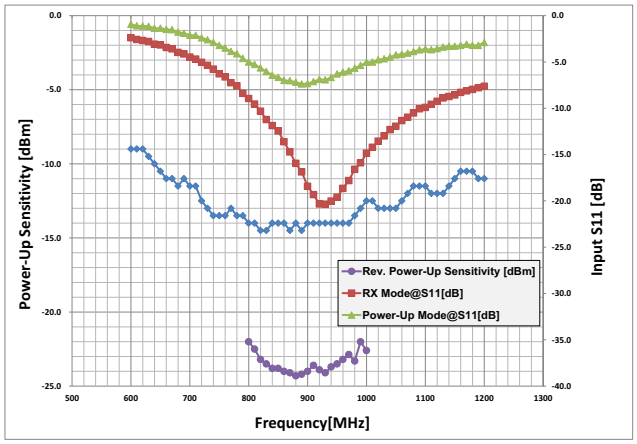

Fig. 5. Input matching versus sensitivity of WiPuRx.

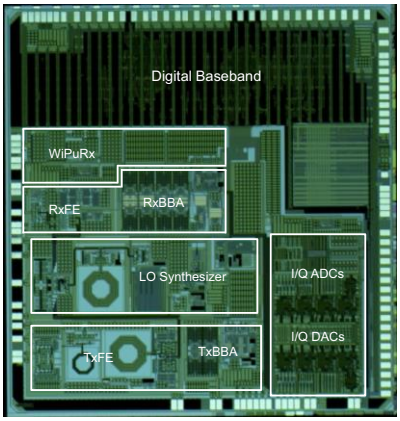

Fig. 6. RF transceiver micrograph.

The performance comparison of a sensor node is summarized in Table 1. The receiver sensitivity is about -103dBm at 1Mb/s in ASK, while the sensitivity is -87dBm in FSK. The DA delivers +3.1dBm maximum output power and OP1dB is +2.1dBm. The operating current of Rx, Tx, LO synthesizer, and data converters are 9.5mA, 13.5mA, 9.8mA, and 13mA, respectively. The Sensor ASIC consumes 2.3mA operating current. The power-down current of a sensor node draws less than 450nA. The sensor node is fabricated in 0.18μm CMOS for RF radio ASIC and 0.25μm CMOS for Sensor ASIC. The RF radio ASIC occupies 19.74mm^2, and the Sensor ASIC occupies 6mm^2. The die micrographs are shown in Fig. 6. Two ASICs are vertically assembled in a single 68-pin QFN package.

Table 1. Performance comparison of a sensor node

	Parameters	This Work	[3]
General	Frequency Band	868/915MHz for Data 868/915MHz for Power-Up	2.4GHz for Data 5.8GHz for Power-Up
	Data Rate	1Mb/s	
	PER at 5meters	< 0.13%	
	Technology	0.18μm RF CMOS	0.13μm CMOS
	Standby Current	450nA for both ASICs	
RX	S11	-20dB	-10dB
	Total RX NF	8dB	
	Sensitivity	-103dBm in ASK	
	Supply Current	9.5mA	
Tx	Output Power (Max/Turbo)	+3.1dBm/+9.6dBm	
	Supply Current	13.5mA at Pout,max	
LO	VCO Frequency	1620MHz ~ 1980MHz	
	Phase Noise	-100dBc/Hz at 1MHz	
WiPuRx	S11	-7dB	-11dB
	Sensitivity	-24dBm at 915MHz	-13dBm at 5.8GHz
	Power-up time	< 100ms	

VII. Conclusion

A fully integrated low-power sub-GHz single-package sensor node has been presented for densely distributed wireless sensor network. A sensor node consumes 83mW operating power, and its power-down current draws less than 450nA. Ultra-low standby current is attributed to a self-power-up receiver that features remote central power-up incorporated with local power-up sequence. Since the self-power-up receiver utilizes the same RF spectrum with data transmission, it achieves simple and area-efficient design. The self-power-up receiver can cover more than 3 meters radius distribution of sensor network with less than 100ms power-up transition time.

Acknowledgement

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