A mm-Wave FMCW Radar Transmitter Based on a Multirate ADPLL

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***Abstract* — We present a 60-GHz FMCW radar transmitter based on an all-digital phase-locked loop (ADPLL) with ultra-wide linear frequency modulation. Multirate, two-point modulation generates an ultra-linear programmable frequency ramp. A novel, closed-loop DCO gain linearization method employing 24kb of SRAM realizes a GHz-level triangular chirp with high sweep linearity, and enables hitless modulation through multiple DCO tuning banks. Measured frequency error (i.e., nonlinearity) in the FMCW ramp is only 117-kHz$_{rms}$ for a 62-GHz carrier with 1.22-GHz bandwidth. The synthesizer is transformer-coupled to a 3-stage neutralized power amplifier that delivers +5 dBm to a 50-Ω load. Implemented in 65-nm CMOS, the transmitter prototype consumes 89 mW from a 1.2-V supply.**

I. Introduction

Frequency-modulated continuous-wave (FMCW) radar at mm-wave frequencies is used in high-resolution radar and imaging applications. Range and velocity resolutions of an FMCW radar depend on the transmitter bandwidth (BW) and the period (T_{mod}) of the linear frequency sweep, i.e., the linear chirp. For short-range detection indoors at 60 GHz, a wideband triangular modulation BW of up to several GHz is required to obtain range resolution <10 cm. In addition, a fast chirp is desired to keep the resulting beat frequency in the receiver far enough from the 1/f noise region. By contrast, a slow chirp, e.g., modulation period of ~10 ms, is required for high-resolution velocity detection in a long-range scenario. Nonlinearity in the ramp further degrades radar resolution [1]. Therefore, a wideband, ultra-linear modulation with programmable T_{mod} covering a large range (>10x) is desired for FMCW radar ICs.

A charge-pump (CP) phase-locked loop (PLL) is typically employed to linearize a voltage-controlled oscillator (VCO) tuning curve [2][3] to generate the FMCW chirp. Two analog FMCW synthesizer examples are shown in Fig. 1. Frequency modulation applied via ΔΣ modulation of a multi-modulus divider in a fractional-N PLL is shown in Fig. 1a. Fig. 1b employs an integer-N PLL with a direct digital frequency synthesizer (DDFS) as a reference to control the modulation period T_{mod} and the bandwidth BW. To overcome the difficulty of achieving a linear ramp for long modulation periods using analog techniques, the mixed-mode FMCW synthesizer of Fig. 1c was proposed in [4]. The majority of the PLL blocks are digital, but the DAC, integrator and VCO still

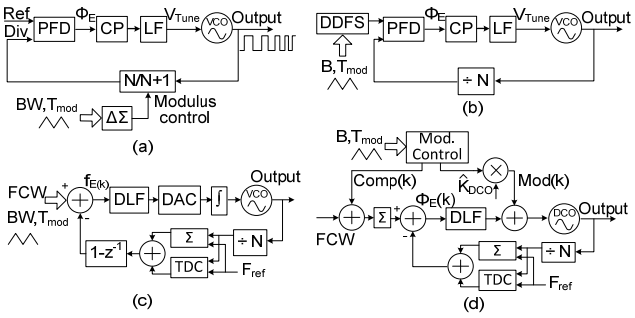

Fig. 1. FMCW synthesizers: (a) fractional-N divider [2]; (b) with DDFS [3]; (c) mixed-mode [4]; and (d) the proposed all-digital scheme.

operate in the continuous-time analog domain due to the unavailability of a high-performance digitally-controlled oscillator (DCO) at mm-wave in the past. Moreover, building a high-precision analog integrator that tracks the ever-changing output of a zero-order-hold (ZOH) is difficult. In addition, the fastest chirp achievable via indirect VCO modulation (as in Figs. 1a, b, and c) is limited by the PLL's closed-loop bandwidth. For a triangular modulation with 100-μs period, the PLL bandwidth should be >100x10 kHz in order to pass 100 harmonics through the loop filter and achieve a 0.01% sweep linearity [1]. Thus, to accommodate the modulation, the required PLL loop bandwidth of ~1 MHz appears much higher than the desired modulation BW for optimum synthesizer phase noise.

To solve these problems elegantly, we propose a 60-GHz FMCW transmitter with a new multirate two-point wideband frequency modulation scheme that also incorporates the ADPLL reported in [5]. The inherent signal processing capability of this digitally-intensive architecture ensures linearity of the triangular chirp. The two-point FM modulation features a direct path to the DCO, and a compensation path to the reference, as shown in Fig. 1d. Therefore, the maximum extent of the modulation triangular frequency is not limited by the PLL loop bandwidth. In contrast to the simple two-point FM shown in [5], the direct modulation path here operates at a much higher clock-rate than the reference frequency to further improve the chirp linearity. An ultra-linear chirp of several GHz in range is realized via the proposed DCO gain calibration and linearization, which compensate for process, voltage and temperature (PVT) variations. These new techniques also enable hitless modulation by

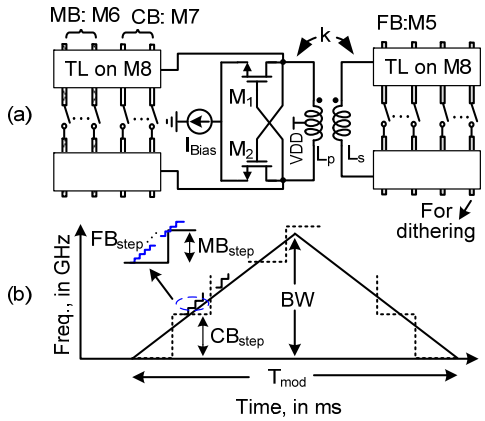

Fig. 2. (a) 60-GHz multi-bank DCO; (b) wideband triangular modulation traversing all three tuning banks.

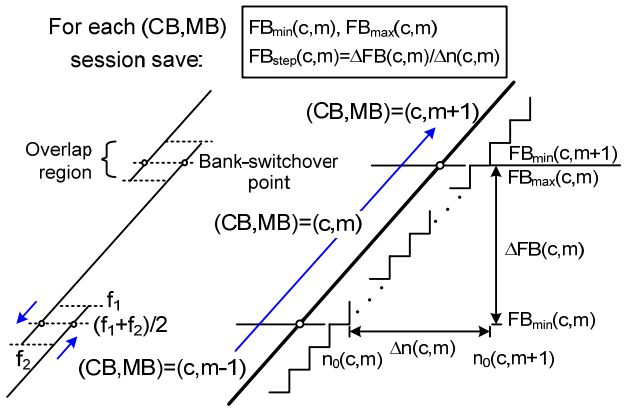

Fig. 3. Proposed DCO gain calibration and linearization algorithm.

traversing all three tuning banks of the DCO. The measured FMCW slope is programmed between 300 and 5000 GHz/s. The measured frequency error is only 117 kHz_{rms}, and degrades to 384 kHz for ultra-fast chirps. Fabricated in 65-nm CMOS, the total power consumption of the proposed 60-GHz FMCW transmitter is 89 mW from a 1.2-V supply.

II. Gain Linearization of a Multi-bank DCO

To achieve a wide-tuning range and good phase noise performance, switched-capacitor tuning of an oscillator using multiple tuning banks is employed. Traversing multiple banks, each with distinct tuning characteristics, is unavoidable across multi-GHz modulation bandwidths. Novel DCO gain calibration and linearization techniques proposed in this paper are therefore essential for linear FMCW generation.

A. Frequency tuning nonlinearity in a multi-bank DCO.

The 60-GHz DCO in the FMCW synthesizer employs reconfigurable distributed metal capacitors and transformer coupling to attenuate the frequency step size [5][6]. It has a multi-GHz tuning range and ~1-MHz raw resolution at 60 GHz. The DCO gain (oscillation frequency change per tuning bit, K_{DCO}) characterizes its tuning behavior. Ideally, a single tuning bank with constant K_{DCO} across the modulation range would be desired. However, in practice, the DCO tuning must be segmented into coarse-tuning (CB), mid-coarse-tuning (MB), and fine-tuning (FB) banks (with different K_{DCO}) to realize both high resolution and the overall wide tuning range. Integer bits in FB are matched to within 1% [6]. One fractional bit in FB (for ΔΣ modulation) is located at the edge of the tuning bank (see Fig. 2(a)), and suffers a larger mismatch compared to the integer bits. Mismatch of the dithering bit is digitally calibrated to further minimize frequency error during modulation. Tuning step mismatches in MB and CB are much larger than in FB (~15% [6]) due to the larger unit capacitor size, and parasitic coupling between adjacent tuning capacitors at 60 GHz. Moreover, the K_{DCO} in MB and FB varies with the CB tuning word. The non-linearity in the DCO tuning curve must therefore be calibrated and compensated in real-time to implement the wideband triangular modulation shown in Fig. 2(b).

B. Automatic DCO gain calibration for wideband modulation.

Correcting K_{DCO} via a look-up table for each bit in CB, MB, and FB from an open-loop DCO gain calibration [7] requires a long calibration time (up to hours) and an unacceptably large lookup table for a wide chirp BW. Therefore, a new closed-loop DCO gain calibration and linearization technique is developed in this work.

For a triangular modulation of slope $k_m=2\cdot BW/T_{mod}$, the output frequency change within each CKM is k_m/f_{CKM}, where f_{CKM} is the modulation frequency. In the proposed calibration scheme, accurate DCO tuning words (OTW) are determined only in the vicinity of the bank-switchover points (see Fig. 3), instead of finding and storing accurate OTWs for each frequency along the chirp trajectory. To ensure monotonic tuning against PVT, the total FB tuning range is set to 1.5 times the frequency step size in MB. Thus, bank switchover may be performed at any frequency located in the overlap region shown in Fig. 3. The mid-point of the overlap region is chosen for robust switchover. When the upper and lower boundaries of the tuning word in FB are determined for CB=c and MB=m, i.e., FB_{max}(c, m) and FB_{min}(c, m), the normalized tuning step value FB_{step}(c, m) is calculated, as shown in Fig. 3. Thus, only 3 variables: FB_{max}(c, m), FB_{min}(c, m), and FB_{step}(c, m) need to be saved in SRAM for each index (c, m). Note that two sets of DCO tuning words are saved for each switchover point to implement hitless modulation, e.g., FB_{max}(c, m) and FB_{min}(c, m+1). The required power-on calibration time before starting the wideband modulation is reduced to only 4 seconds by employing this new closed-loop DCO gain linearization.

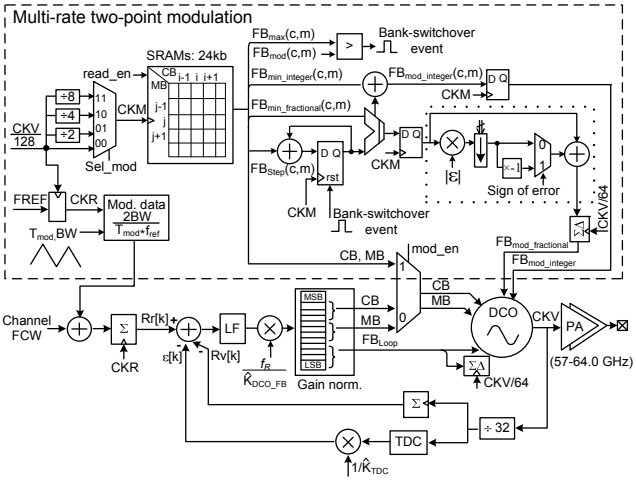

Fig. 4. Multi-clock domains of the 60-GHz FMCW transmitter.

III. Multirate, Two-point Modulation for the FMCW Transmitter

A block diagram of the 60-GHz FMCW transmitter is shown in Fig. 4. The FB bank is divided into two parts: one for modulation and one for loop drift tracking that doesn't require an accurate K_{DCO}. Therefore, an approximate tuning-step ratio of 16 is employed between CB and MB, as well as between MB and FB to simplify the gain normalization logic in the loop.

A. Synchronization in a multirate system

Fig. 4 elaborates on the multirate two-point modulation. The direct modulation path operates at a high rate of clock CKM, which is a divided-down DCO output to obtain high sweep linearity. It can be reduced from CKV/128 to CKV/1024 for a slow modulation slope to minimize power consumption. The compensation path is applied to the frequency reference and operates at the retimed reference clock (CKR) of rate f_R. During FM, CKV varies linearly with time and so does CKM. Clock CKR is always synchronized with CKM via re-sampling of FREF by CKV/128. The DCO FB is separated into two independent parts for the modulation and drift tracking. Thus, no sampling rate conversion is required for the DCO tuning word. Upon modulation, a state-machine controls the access to SRAMs and reads out the proper data before bank switchover. Operation at high-speed is simplified to an accumulation of FB_{step} and a comparator to generate the bank-switchover event. Meanwhile, a frequency change of $k_m/f_R/32$ is added as compensation to the reference at every CKR to obtain the wideband FM modulation. The lithography-related mismatch of the dithering bit in FB, ε, is obtained via an open-loop calibration [7] and compensated in the direct path (highlighted by the dotted line in Fig. 4).

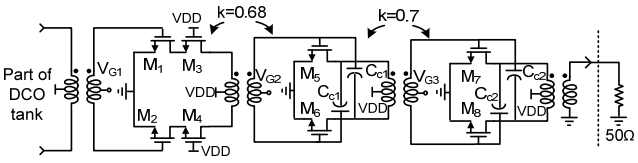

Fig. 5. Schematic of the 60-GHz power amplifier.

B. Output power amplifier

The synthesizer output is transformer-coupled to the 3-stage power amplifier (PA) of Fig. 5. The cascode-first stage minimizes loading on the DCO tank and improves the reverse isolation. The 2nd and the 3rd common-source stages use neutralization [8] to achieve higher gain and greater stability. An on-chip output balun provides a single-ended output to drive a 50-Ω antenna or test instrument input for characterization.

IV. Experimental Results

The 60-GHz FMCW radar transmitter is implemented in TSMC 65-nm CMOS (see Fig. 6). The synthesizer and PA consume 40 mA and 34 mA from a 1.2-V supply, respectively, and occupy 0.72 mm^2 core area. The chip is wire-bonded to a PCB to provide DC and low-frequency connectivity, while the 60-GHz output is measured via on-die probing. DCO gain calibration and linearization require only a few seconds, and the results are stored in 24kb SRAMs. The FMCW signal is measured using an R&S®FSUP signal source analyzer with FM demodulation firmware. Both slow and fast modulation slopes are used to characterize the chirp linearity by programming various values of modulation range (BW) and period (T_{mod}).

Fig. 7 (inset) shows the FMCW chirp spectrum measured at the PA output for a 1.22-GHz modulation BW centered at 62.1 GHz. The T_{mod} is 8.2 ms, forming a slow, triangular chirp. CKM is configured at CKV/1024 to reduce power consumption. The instantaneous output frequency of the FMCW synthesizer and the frequency error compared to the ideal chirp are also plotted in Fig. 7. The frequency error is only 117 kHz_{rms}. Fig. 8(a) shows the results when the modulation slope is 4 times faster, where the rms error is 148 kHz. An ultra-fast chirp (1-GHz change in 210 μs) is plotted in Fig. 8(b), where the frequency error degrades to 384 kHz_{rms} and the power consumption increases to 42 mA.

The performance of the 60-GHz all-digital FMCW synthesizer is summarized in Table 1. Compared to state-of-the art FMCW generators, the proposed all-digital technique features wider modulation range, higher sweep linearity for varying modulation slopes, and achieves better phase noise, all with less power consumption. The measured chirp frequency error remains less than 400 kHz when the modulation slope increases by a factor of 16.

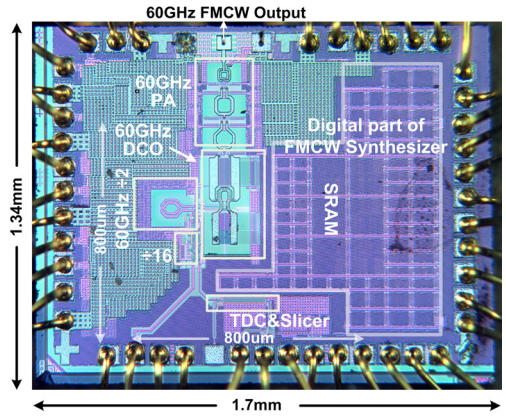

Fig. 6. Chip microphotograph.

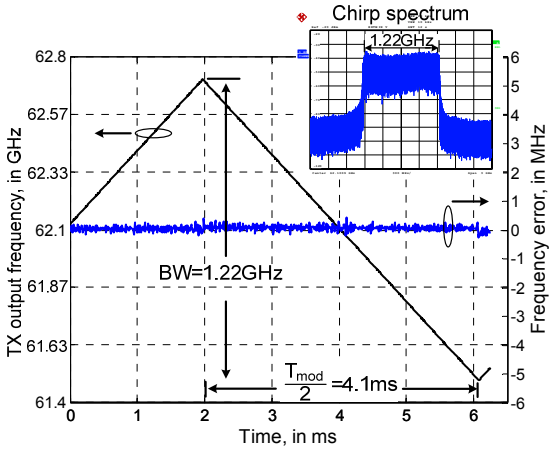

Fig. 7. Measured chirp spectrum and time-domain frequency characteristics for BW=1.22 GHz and T_{mod}=8.2 ms.

V. Conclusion

A 60-GHz frequency-modulated continuous-wave (FMCW) radar transmitter based on an all-digital multirate synthesizer with two-point modulation is implemented in 65-nm CMOS. Compared to analog and mixed-mode topologies, the all-digital architecture can calibrate and linearize the DCO tuning curve to less than 10-kHz of frequency granularity. Multirate, two-point modulation ensures sweep linearity for various FM slopes. The proposed closed-loop DCO gain linearization algorithm calibrates the DCO gain against PVT in only 4 seconds. The calibration results are saved on-chip in 24kb SRAM and are applied to the DCO directly without the need for gain normalization. Mismatch between the fractional (dithering) and integer bits of the fine-tuning bank is also calibrated via an open-loop method. The high-speed modulation clock can be configured to optimize power consumption for various chirp slopes. Compared to analog-intensive designs, the proposed FMCW transmitter achieves much smaller frequency error (117-kHz_{rms}) for slow chirp. It also demonstrates fast linear chirp generation capability and >40% power reduction in consumption, making it an excellent choice for mm-wave FMCW radar IC implementations.

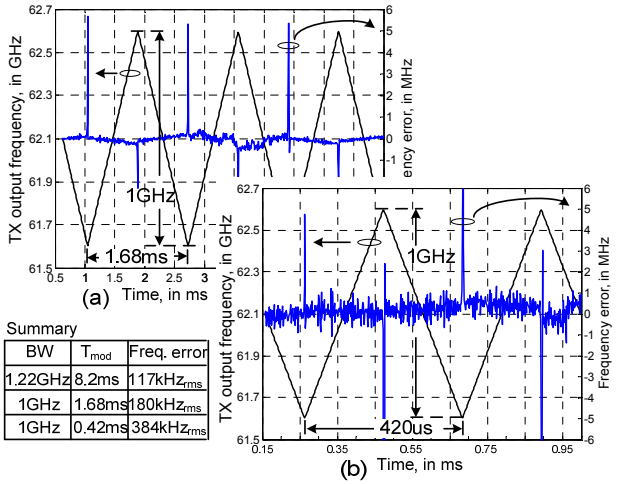

Fig. 8 Measured frequency characteristics of FMCW signal for (a) T_{mod}=1.68 ms, BW=1 GHz; (b) T_{mod}=0.42 ms, BW=1 GHz.

TABLE I. FMCW synthesizer performance comparison

	This Work	ISSCC'11 [4]	JSSC'10 [3]	ISSCC'10 [2]
Architecture	ADPLL + multi-rate 2-point mod.	Mixed-mode	DDFS+PLL	Fractional-N
Frequency (GHz)	56.4-63.4	82.1-83.8	78.1.4-78.8	75.6-76.3
CMOS	65nm	65nm	90nm	65nm
Reference	40MHz	26MHz	77MHz	700MHz
Modulation slope (k_m)	Fast:1GHz/ 0.21ms Slow:1.22GHz/ 4.1ms	Fast:1.5GHz/ 1ms Slow: 0.5GHz/ 5ms	700MHz/ 0.22ms	500MHz/ 0.5ms
Frequency error, rms	Fast: 384kHz Slow:117kHz*	Fast: 179kHz Slow:170kHz	1.05MHz*	<300kHz*
PN @ 1MHz	-90dBc/Hz	-84dBc/Hz	-85dBc/Hz	-84.6dBc/Hz
Supply	1.2V	1.2V	1.2V	1.2V
P_{DC} (mW)	48+41 (PA)	152 with buffer	101+305(TX)	73+115(PA)
Output power (50Ω)	+5dBm	NA	-2.8dBm	+10.5dBm

* Includes turn around point

Acknowledgements

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