Power Handling Capability of an SOI RF Switch

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***Abstract* — In this study, we define and investigate the maximum power handling capability (Pmax) in an SOI RF shunt branch switch. One of the critical factor in the Pmax is the non-uniform voltage division across an OFF shunt branch. In this study we provide a simple analytical method to determine the stack voltage imbalance. The Pmax is characterized as a function of various parameters, such as, switch stack height, channel length, Gate and Body bias, and process parameters. Overall, we find that the Pmax can be improved by reducing stack imbalance as well as device leakage currents, namely, GIDL.**

***Index Terms* — SOI, RF switch, front-end-module.**

I. Introduction

During the recent past, the high-resistivity SOI technology has become the mainstream solution for the transmit-receive (T/R) switch in the RF front-end section of the wireless radio [1]. With the 3G/4G high data rate standards for mobile users, recent smart phones needs to support highly complex RF T/R switch (known as Antenna Switch Module) that needs to meet very stringent performance and reliability standards. Smart phones with upwards of 12 throws that switch to multiple antennas are becoming increasingly common.

The T/R switch is designed with each branch being able to support the maximum voltage seen at the antenna. In SOI technology, where the device breakdown is much lower than the peak RF voltage, a series of stacked device is utilized to withstand the voltage. In this work, we study some of the key factors that influence the maximum voltage handling capability of a SOI technology that has been previously discussed [2].

II. PMAX Definition

In an RF switch, while one branch is transmitting, the rest of the branches are turned OFF. The peak voltages at the antenna need to be withstood by all the OFF branches. Under worst case antenna impedance mismatch while transmitting a GSM signal, there could be peak voltages in excess of 40V! If shunt branches are not designed to withstand such high peak voltages, one would expect a pre mature shunt branch breakdown. Shifrin et al. [3] had defined the Pmax of an off-state switch branch to be proportional to the square of the product of maximum gate-drain breakdown voltage and number of stack. While this is valid for an ideal shunt branch where voltages are equally divided, one needs to make adjustments based on other variations in an SOI technology to determine the Pmax. Tinella et. al have characterized the power handling as P1dB of a series-shunt branch, which while meaningful, does not isolate the limitations of a shunt branch [4].

We define the Pmax of a shunt branch as the input power that cause harmonics to abruptly increase, ie., over 10dB, under a 6:1 VSWR. In this study, we have kept the fundamental frequency of interest to be 900MHz. While this abrupt harmonics increase is not destructive for the stack switch, we consider it as a limiting factor in the maximum power that the switch can handle, hence, called as Pmax.

Figure 1 shows the Pmax characterization for various FET stack shunt branch configuration. As expected the 2nd and 3rd harmonics rise with Pin, but, at certain power the harmonics abruptly rise, which we identify as the Pmax of the shunt branch. As expected, the results indicate that the Pmax reduces with a shorter stack height. In this particular case, we observe a 6 dB reduction in Pmax when one cuts the stack height from 8 to 4.

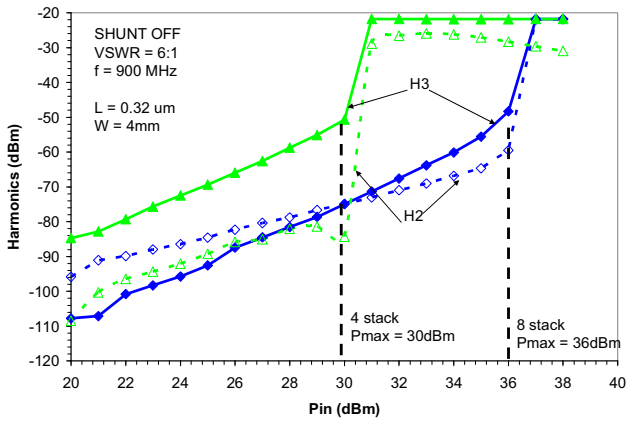

Fig. 1. Pin vs. harmonics for 3 different shunt branch stack height configuration.

III. Analytical Estimation of Stack Voltage Division

In the OFF state, a shunt branch is assumed to be a series of capacitors that is each equal to the OFF capacitance (Coff) of the unit cell in the branch. Due to the parasitic coupling to the substrate, in reality one needs to consider the device to the substrate through BOX capacitance (Cbox). This coupling is expected to create a non-linear voltage division on the stack. Previous work by Lee et al had investigated the BOX coupling effects in accurate harmonic and distortion modeling in an SOI technology [5].

Here we provide an analytical method to estimate the voltage division, with impedance Z being assigned to the OFF branch and admittance Y being assigned to the parasitic coupling through BOX. For simplicity, here the capacitances are assumed to be bias independent.

$$dI = VYdx \quad \text{..... (1)}$$

$$dV = IZdx \quad \text{..... (2)}$$

$$\frac{d^2V}{dx^2} - VZY = 0 \quad \text{..... (3)}$$

$$V = V_{rf}\frac{\sinh \lambda i}{\sinh \lambda n} \quad \text{..... (4)}$$

We can solve the stack voltage division as a continuous structure of arbitrary length in frequency domain. Equation (1) determines the voltage distribution across the stack as a function of the current through the stack. Equation (2) determines the current through the stack. One can then solve the 2nd order differential equation (as in eqn. 3) with a boundary condition of the top drain of the FET stack having the peak voltage of Vrf and the source of lowest stack at 0V.

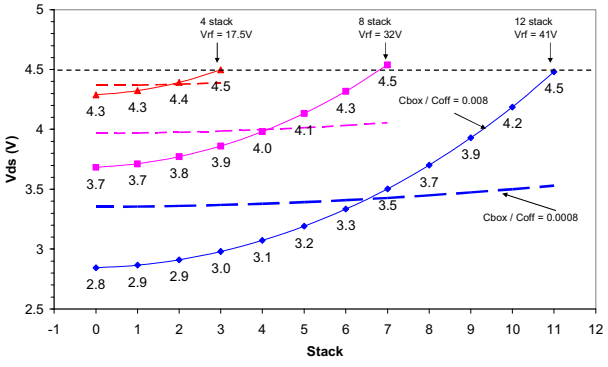

Fig. 2. Voltage seen by each FET in a 12, 8, and 4 shunt stacks with a (Cbox/Coff) ratio of 0.008 is shown. Overlaid as dashed lines for each of the stacks are the voltage when the Cbox/Coff ratio is lowered by 10x.

Equation (4) gives the voltage on the drain of the i-th FET in an n-stack shunt OFF branch. Here lambda is the sqrt of (Cbox/Coff). In ideal case, when Cbox is very low compared to Coff, one can observe that there will be more equal voltage division across the stack.

In Fig. 2, the voltage scaling based on eqn. (4) is shown for a case with Cbox/Coff = 0.008. Three different stacks are shown for comparative purposes. The Vrf for each stack is scaled to keep the Vds of the top FET at roughly the same, i.e., in this case 4.5V. As one observes, the higher the stack number, more voltage imbalance will be observed. On the other hand for a shorter stack, the Vds voltages for each FET are closer to each other (better balance), and stays higher across the branch.

Overlaid on these curves for each stack is the case when the Cbox/Coff is reduced by 10x. In this case, one can see that the voltage is well balanced across the stack as well as a reduction in the Vds for the top FET. One should expect to see improvements in Pmax under such a circumstance.

IV. Device Aspects and PMAX

The voltage imbalance in itself is not considered a problem unless the voltages seen by each individual FETs results in high non-linearity, resulting in a Pmax limit.

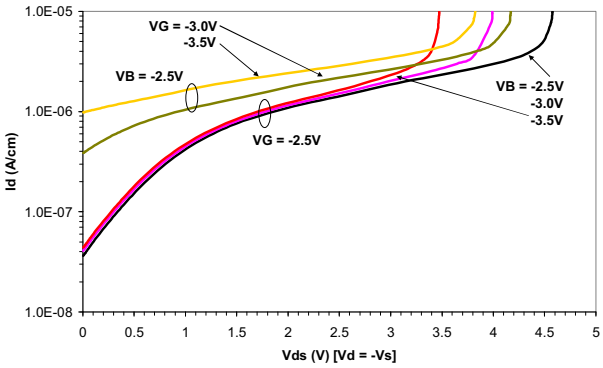

Fig. 3. TCAD simulation of a nominal channel length device under OFF condition with a DC bias, showing the exponential dependence of drain current with VG and VB.

Many authors have studied the OFF state leakage and breakdown mechanisms in a PD-SOI device [6, 7] and will not be dealt here. For an OFF fet, typically the gate and body is biased negative, i.e., -2.5V, while the RF voltage will ac couple through the floating gate and body nodes to divide equally. Under these circumstances, one can determine that the peak G-D (and D-B) is equal to the

magnitude of (Vdmax/2+VG). This causes higher leakage currents through D-S and D-B, thereby modulating the OFF impedance (Zoff = Roff || Coff) with bias and hence the harmonics of the shunt branch.

In Figure 3, we show a TCAD based electrical simulation of the leakage current for a nominal SOI device with various VG and VB bias. In this simulation, the Vd = -VS is swept and drain and body currents are monitored. As one can observe, with higher body and/or gate OFF bias, one observe an exponential increase in drain (or body current not shown).

Overall, for Pmax limit it is important to understand both the stack imbalance induced by the Cbox/Coff and the voltage dependence of leakage currents in the OFF device.

V. SWITCH DESIGN VARIABLES AND PMAX

Typical switch design parameters, such as, stack height reduction, channel length and width variations, and gate OFF bias condition were studied to see the influence on Pmax.

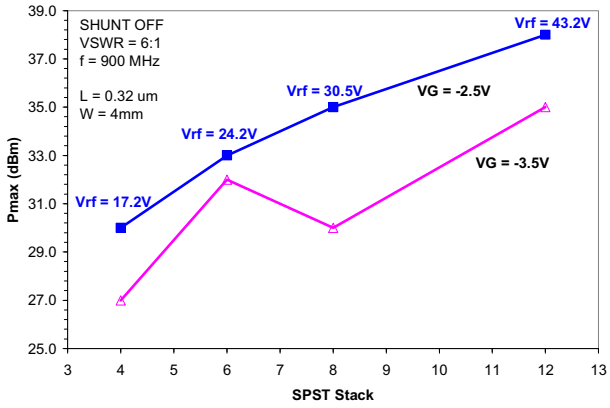

Fig. 4. Pmax variation with shunt stack height and OFF gate bias voltage. Estimated Vrf voltage seen by each stack at the Pmax condition is labeled for VG=-2.5V case.

As discussed in the previous sections, the Pmax scaling with stack height will be influenced by both the stack imbalance and the "breakdown" conditions seen by the stack FET. Fig. 4 shows the Pmax scaling with shunt branch stack that use a 4mm wide FET unit cell. Data for both OFF bias of VG = -2.5V and -3.5V are shown. Other than the Pmax of 6-stack at VG=-3.5V, the data looks to well behaved.

Pmax of the 4-stack FET is 30dB and the peak Vrf is roughly 17.2V. Based on the analytical study in section II, we expect roughly equal voltage division for a 4-stack, along with an assumption of Cbox / Coff = 0.008 we see that the stack can support a peak of 17.5V with a Vdsmax of 4.5V. This is within reasonable estimation of what is measured for the 4-stack.

Higher shunt branches support higher peak voltage, as one expects, even under the imbalance. The peak voltage estimations are in close proximity to that projected in Fig.2 for the stack imbalance assuming a Cbox/Coff=0.008 and the Vdsmax of the top FET at 4.5V. As shown in Fig. 4, a higher VG OFF bias drops the Pmax considerably. We have monitored the body current and observed an exponential increase in leakage with the increased gate bias and the rf power, leading to a lower Pmax. Thus we conclude that the additional factor in this case (beyond stack imbalance) is the reduction in Zoff due to voltage induced leakage current of the device.

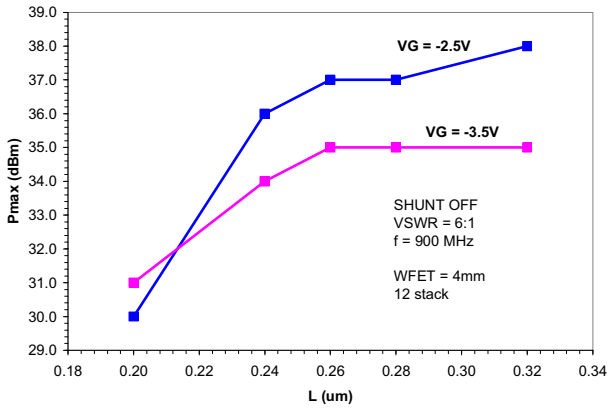

Fig. 5. Pmax variation with Lg for 12stack shunt and OFF gate bias voltage.

Device channel length and width can be modulated in the design for one to optimize the switch performance. Figure 5 shows the Pmax variation with channel length scaling. As the Lg is reduced, we expect Coff to not vary as much, however, the coupling to the BOX (Cbox) will be reduced proportionally to the channel length. Thus one would expect the stack imbalance to improve with Lg reduction.

The Pmax is marginally reduced for shorter Lg from the 0.32um case, more likely due to competing factors from the improved imbalance reducing the peak voltages, but more OFF state leakage currents at the reduced channel lengths. Decreasing channel length beyond 0.24um worsens the Pmax much strongly. Also observe that higher VG reduces the Pmax for all channel lengths. Overall, one can see that the stack imbalance and the voltage induced leakages (GIDL, which does not scale strongly with Lg, but the BVdss which does reduce strongly with Lg) play an important role in determining the Pmax of the shunt stack.

V. FET Process Experiments and Pmax

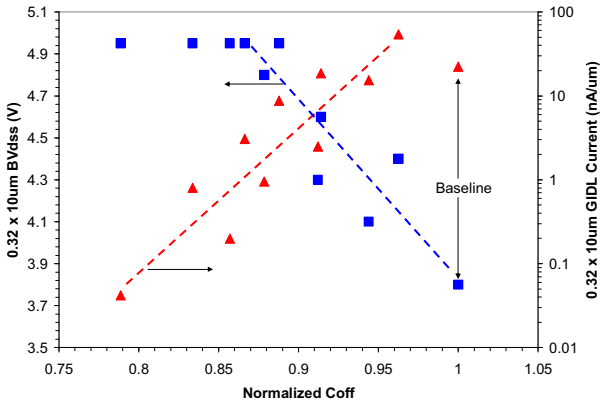

Fig. 6. Drain-Source DC Breakdown voltage at VG=0V and GIDL current at VG=-1.8V as a function of the Coff modulation obtained by implantation splits.

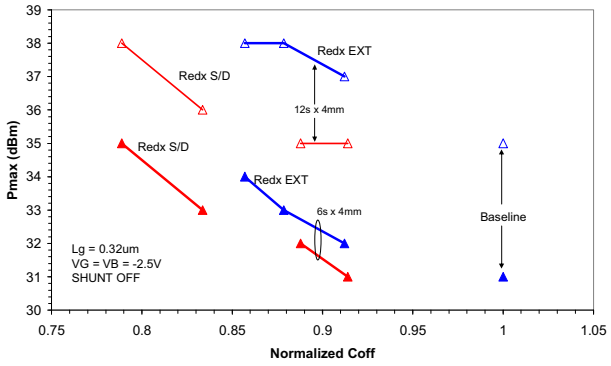

Fig. 7. Pmax scaling with Coff variation obtained by implant splits.

An experiment to modulate the Coff and its influence on Pmax was studied by implantation in the extension and Source-Drain regions of the nFET. Since the splits are not expected to modulate Coff independently, there are several device parameters that vary in dependence to the Coff. For example, the ON resistance (Ron) worsens with reduced Coff. For the various splits run, the normalized Ron (to the value of the nominal process) varies well over 8x while the Coff varies by 20% or so. Predictably, the implant variation that modulates the overlap of the FET by either reducing the extension or s/d implants increases the Ron.

With the implant variation we expect to modulate the electric field under the gate coupling to the source and drain. This will improve the GIDL and BV as shown in Fig. 6. In the extreme case of implant variation, we observe that the GIDL can be reduced to well over 3 orders of magnitude and gaining over 1.2V in BVdss for roughly 20% improvement in Coff.

Pmax was characterized for 3 cases in these splits that represented the range of variations observed for device parameters from the splits. One can obtain a 3-4 dB improvement in Pmax within the experimental range (See Fig. 7). In these experimental cases, even though the stack imbalance is expected to be slightly worse, the Pmax improvement is obtained by keeping the device leakages low.

VI. Conclusion

We have investigated the power handling capability of the SOI device. A simple analytical calculation reveals that the voltage stack imbalance in the shunt branch can cause the Pmax limitation due to relative ratio of Cbox/Coff. Beyond this, optimizing the device leakage currents and breakdown is important for higher Pmax.

Acknowledgement

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