# A Low-Current Digitally Predistorted 3G-4G Transmitter in 40nm CMOS

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***Abstract* — To create a wide-band transmit path with high current efficiency a single-balanced passive modulator is combined with a class-B single-ended resonant driver. The linearity of such configuration is limited by a strong 3rd harmonic response of the modulator combined with a strong third-order intermodulation in the driver. A novel digital pre-distortion approach is presented to enable good linearity under these highly non-linear conditions. Implemented in 40nm CMOS, the modulator and driver combined consume only 45mW to deliver a +3dBm Release 99 WCDMA signal with 1.1% EVM, -54dBc ACLR and -160dBc/Hz noise in the RX band. The ACLR remains below -50dBc over temperature, frequency and TX-power without adjustment of the predistortion coefficients. The transmitter delivers +0dBm 10MHz LTE with -51dBc ACLR.**

***Index Terms* — CMOS, digital, driver, linearity, modulator, passive, predistortion, transmitter.**

## I. Introduction

Current consumption and silicon area reduction have been the predominant driving forces behind the development of new wireless transceiver circuits. In this context, the direct conversion I/Q transmitter with 25% duty-cycle passive mixer as presented in [1] and analyzed in [2] allows for significant power savings compared to current-mode mixers.

A known drawback of passive voltage-sampling mixers is the generation of strong LO harmonics. The combination of a passive mixer followed by a very efficient but very non-linear driver creates inter-modulation products that cannot be corrected with traditional PA digital predistortion (DPD) approaches as the ones used in [3]. In this paper we present a DPD algorithm that overcomes the LO harmonic problem. This allows for the combination of a passive mixer with a very efficient driver while achieving very good ACLR and EVM performance.

## II. Transmitter Architecture

Fig. 1 shows a simplified circuit schematic of the transmitter architecture. It is a similar line-up as used in [1]. The analog baseband signals are directly coupled to an RC low-pass filter which suppresses both out-of-band noise and D/A replicas. Next, a passive mixer with 25% duty-cycle is used to up-convert the I/Q signals to RF. Finally a cascode $g_m$ stage loaded with a tunable tank is used as driver for the off-chip PA. The modulator and driver are sliced to achieve a large power control range. Differently from [1], the tank includes a resistor load to offer a good 50Ω termination. Moreover, the driver is biased in class B, providing very low current consumption at the expense of linearity. Also differently from [1], a single path is used to cover both low and high bands and switches after the driver are included to provide multiple output ports. The switches contribute to the non-linearity of the overall system, but more importantly introduce losses that reduce the transmitter efficiency.

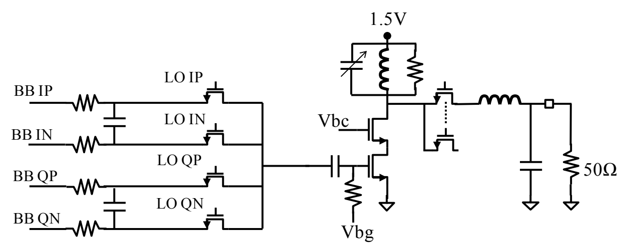


Fig. 1. Simplified schematic of the single-ended transmitter circuit.

## III. Digital Predistortion Approach

In [3] a strategy to derive DPD coefficients to compensate for PA non-linearity taking into account memory effects is explained. In our case the output power is significantly lower and memory effects are negligible. However, simplifying the memory polynomial or the generalized memory polynomial used in [3] to the memoryless case is insufficient to achieve acceptable ACLR for the architecture shown in Fig. 1.

Note that the input to the non-linear driver consists of the baseband signal up-converted around the LO frequency, plus the mirrored spectrum of the BB signal up-converted around 3LO, plus the BB signal up-converted around 5LO, etc. The passive mixer effectively multiplies the BB signal with a square wave, and given the wideband nature of the transmitter, this translates into strong LO harmonics (e.g. 3LO -9.5dBc, 5LO -14dBc …). Due to non-linearity in the mixer, distortion products

around 2LO are also present. Moreover, because the mixer load impedance changes with frequency, the phase of each LO harmonic is not exactly the same as what the Fourier decomposition of the 25% duty-cycle signals predicts.

As in [3], the DPD concept used here is based on the assumption that the baseband I/Q products necessary to accurately model the non-linearity are the same products that need to be included in the predistortion polynomial. Careful study of the I/Q products generated by a passive mixer in combination with a non-linear driver shows that the I/Q distortion model can be written as:

$$I_o = a_1 I_i + a_3 I_i^3 + a_{12} I_i Q_i^2 + a_5 I_i^5 + a_{14} I_i Q_i^4 + a_{32} I_i^3 Q_i^2 + \ldots \\ + a'_1 Q_i + a'_3 Q_i^3 + a'_{12} Q_i I_i^2 + a'_5 Q_i^5 + a'_{14} Q_i I_i^4 + a'_{32} Q_i^3 I_i^2 + \ldots \quad (1)$$

$$Q_o = b_1 Q_i + b_3 Q_i^3 + b_{12} Q_i I_i^2 + b_5 Q_i^5 + b_{14} Q_i I_i^4 + b_{32} Q_i^3 I_i^2 + \ldots \\ + b'_1 I_i + b'_3 I_i^3 + b'_{12} I_i Q_i^2 + b'_5 I_i^5 + b'_{14} I_i Q_i^4 + b'_{32} I_i^3 Q_i^2 + \ldots \quad (2)$$

The I/Q predistortion polynomial is identical to (1)-(2) but with different coefficient values. It has to be clarified that even if a particular circuit non-linearity can be correctly modeled with an $M^{th}$-order polynomial, the predistortion polynomial might require a higher order to achieve satisfactory performance. During a calibration phase, a training sequence with characteristics similar to a WCDMA signal is transmitted without predistortion. A loopback path to the main receiver is used to down-convert the transmit signal and allow comparison to the original data. Attention to the alignment between the loopback path samples and the original data has to be paid not to degrade accuracy. The DPD coefficients can be found by storing N samples of the received distorted training sequence and solving the following least-squares problem (**Ii** and **Qi** denote Nx1 input data vectors, and **Io** and **Qo** are the corresponding Nx1 output data vectors)

$$(\mathbf{Y_o}^T\ \mathbf{Y_o})\,\mathbf{a} = \mathbf{Y_o}^T\,\mathbf{I_i} \quad (3)$$

$$(\mathbf{Y_o}^T\ \mathbf{Y_o})\,\mathbf{b} = \mathbf{Y_o}^T\,\mathbf{Q_i} \quad (4)$$

where the matrix $\mathbf{Y_o}$ is

$$\mathbf{Y_o} = [\mathbf{I_o\ Q_o\ I_o^3\ Q_o^3\ I_oQ_o^2\ Q_oI_o^2\ I_o^5\ Q_o^5\ I_oQ_o^4} \ldots \\ \mathbf{Q_oI_o^4\ I_o^3Q_o^2\ Q_o^3I_o^2} \ldots ] \quad (5)$$

and the arrays of coefficients are

$$\mathbf{a} = [a_1\ a'_1\ a_3\ a'_3\ a_{12}\ a'_{12}\ \ a_5\ \ a'_5\ \ a_{14}\ \ a'_{14}\ \ a_{32}\ \ a'_{32} \ldots]^T \quad (6)$$

$$\mathbf{b} = [b'_1\ \ b_1\ \ b'_3\ \ b_3\ \ b'_{12}\ \ b_{12}\ b'_5\ b_5\ b'_{14}\ b_{14}\ b'_{32}\ b_{32} \ldots]^T \quad (7)$$

Besides non-linearity, the coefficients in (6) and (7) along with the predistortion polynomials (1) and (2) also fully compensate for I/Q mismatch. In the absence of I/Q mismatch or if compensated in a step previous to the DPD, the coefficients in (6) and (7) are related as follows

$$a_k = b_k \quad (8)$$

$$a'_k = -b'_k \quad (9)$$

and consequently only one of the equations (3) or (4) needs to be solved. Alternatively, the solutions of (3), (4) could be combined to reduce coefficient estimation noise.

The calibration has to be done only once at power-up and therefore can be implemented in software. After calibration, the DPD coefficients are stored, ready to be used during transmission. The only operations that need to run continuously are those in (1) and (2).

| DPD case | OFF | 3rd | 5th | 7th | [3] 3rd | [3] 5th | [3] 7th |
|---|---|---|---|---|---|---|---|
| ACLR5 (dBc) | -36.9 | -44.3 | -53.8 | -55.8 | -41.7 | -42.5 | -41.9 |
| ACLR10 (dBc) | -62.3 | -58.3 | -63.7 | -66.6 | -58.2 | -60.5 | -57.7 |
| BB PAR (dB) | 3.3 | 4.4 | 5.6 | 6.3 | 4.0 | 4.9 | 5.4 |
| BB BW (MHz) | 2.3 | 4.5 | 8.5 | 10 | 4.5 | 8.5 | 13 |

Fig. 2. WCDMA R99 ACLR performance versus digital predistortion case at Pout = 3dBm.

| | LTE 5MHz, Po = 1dBm | | | | LTE 10MHz, Po = 0dBm | | | |
|---|---|---|---|---|---|---|---|---|
| **DPD case** | **OFF** | **3rd** | **5th** | **7th** | **OFF** | **3rd** | **5th** | **7th** |
| ACLR1 (dBc) | -38.9 | -44.8 | -52.8 | -53.6 | -39.8 | -44.8 | -50.7 | -52.2 |
| ACLR2 (dBc) | -62.3 | -59.2 | -60.7 | -61.4 | -58.7 | -57.3 | -58.1 | -58.3 |
| BB PAR (dB) | 6.5 | 7.6 | 9.4 | 9.5 | 7.5 | 8.5 | 10.4 | 10.5 |

Fig. 3. LTE ACLR performance versus digital predistortion. LTE 5MHz modulation at Pout = 1dBm and LTE 10MHz modulation at Pout = 0dBm.

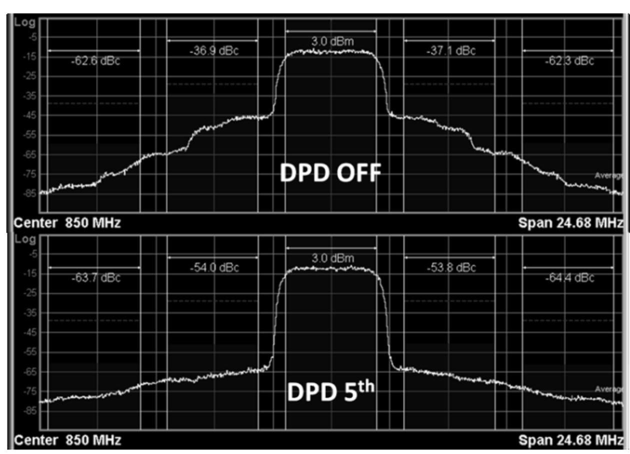


Fig. 4. WCDMA R99 output spectrum comparison.

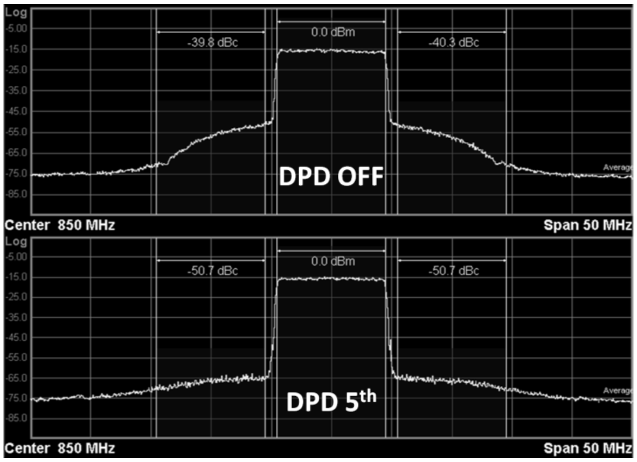


Fig. 5. LTE 10MHz output spectrum comparison.

## IV. MEASUREMENTS

In this wideband transmitter implementation, the LO harmonics are strongest at the lowest frequency. This is the worst scenario for the predistortion algorithm. In the following we show the measurement results in band V.

Fig. 2 summarizes the measured WCDMA R99 ACLR at 5MHz and 10MHz offset versus DPD polynomial order. The raw ACLR achieved by the transmitter without predistortion is shown in the first column. An order 3 polynomial improves ACLR5, but it is detrimental to ACLR10. DPD order 5 gives good ACLR5 and ACLR10 performance. DPD order 7 offers some small ACLR improvements with respect to $5^{th}$ order, but the improvements are too small to justify the additional complexity. Changing the DPD order does not change the transmitter current consumption, but it does change the BB signal bandwidth and the peak-to-average power ratio as shown in the last two rows. The original 3.3dB PAR of the complex baseband signal increases to 5.6dB for DPD order 5 while the baseband bandwidth expands from 2.3MHz to 8.5MHz. In the same figure the result using the PA DPD technique in [3] is included. It is clear that for this transmitter architecture, the memory polynomial model in [3] is insufficient and it cannot achieve an ACLR5 much lower than -42dBc. Actually ACLR degrades for DPD order 7, as the problem of finding the DPD coefficients becomes less numerically stable, due to the poor fit of the model. The output wide-spectrum emissions show a $2^{nd}$, $3^{rd}$ and $5^{th}$ LO harmonic suppression of -24, -27.5 and -42dBc, respectively. Both LO feed-through and I/Q mismatch are lower than -55dBc.

Fig. 3 shows the E-UTRA ACLR1 and ACLR2 performance for two LTE signals: 5MHz QPSK and 10MHz 16QAM. Due to a measurement set-up limitation

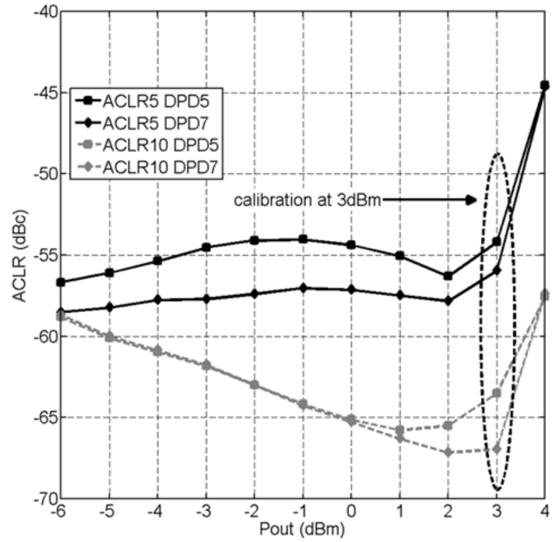


Fig. 6. ACLR variation with output power at 25°C, 850MHz.

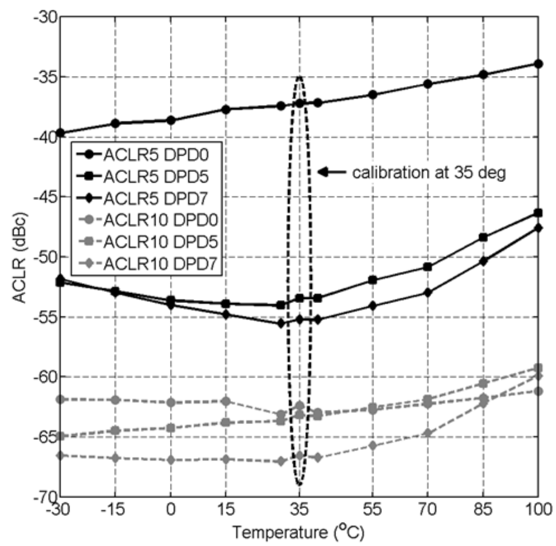


Fig. 7. ACLR variation with temperature at 3dBm, 850MHz.

in the maximum input peak power, the RMS power had to be decreased for these higher PAR modulations. Focusing in the 5MHz LTE signal measurement, the lower RMS output power translates in a starting ACLR1 value better than before (-38.9dB in place of -36.9dB). As in the WCDMA case, DPD order 5 is sufficient to achieve very good ACLR1 and ACLR2 values: -52.8dB and -60.7dB, respectively. The 10MHz LTE signal measurement shows a similar trend. The maximum allowed PAR expansion due to DPD is clipped to 3dB. This limits the improvements achieved by DPD 7 for both LTE modulations. The power consumption is 44mW for 5MHz LTE at 1dBm, and 42mW for 10MHz LTE with 0dBm.

Fig. 4 and Fig. 5 compare the WCDMA (LTE 10MHz) output spectrum for the system without predistortion and with 5$^{th}$ order DPD for an output power of 3dBm (0dBm). In the LTE 10MHz case, the ACLR improvement due to DPD although still significant, is smaller than in the WCDMA case. This is partly due to the frequency response of the transmitter, which has a 1-dB bandwidth of 35MHz. This problem could be circumvented by increasing the RC-pole frequency or by using digital pre-emphasis after the predistortion polynomial.

The DPD calibration is intended as a one-time-only calibration. It is therefore paramount that the DPD coefficients provide stable performance versus frequency, power and temperature variations. Fig. 6 shows the measured WCDMA ACLR5/10 variation with RMS output power. In this test the power is varied by changing the baseband signal level before DPD. The DPD calibration was performed at 3dBm. The ACLR10 degradation at low output powers is due to the test equipment noise floor. Fig. 7 shows the measured WCDMA ACLR5/10 variation with temperature. In this test the baseband signal level was adjusted to keep the output power equal to 3dBm, as would be the case with transmit power control active. A similar measurement sweeping the carrier frequency from 824MHz to 915MHz was performed while keeping both temperature and output power constant. The DPD coefficients were calibrated only once at 850MHz. For a DPD order 5 (7) system, the ACLR5 variation was less than 6dB (8dB). The ACLR10 variation was within 1dB for all DPD orders. ACLR performance will also vary with output load, however load variations are less pronounced for a TX than for a PA.

Fig. 8 shows the die micrograph of the transmitter chip as implemented in 40nm CMOS. The area of the LDO, LO divider, LPF, passive mixer and driver is 0.53mm$^2$.

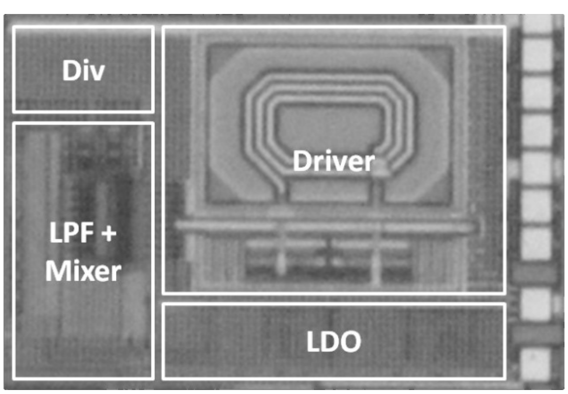


Fig. 8. Die micrograph of the TX chip in 40nm CMOS.

| | [1] | [4] | [5] | [6] | this work |
|---|---|---|---|---|---|
| Process [nm] | 45 | 65 | | 90 | 40 |
| Output Power [dBm] | 1 | 0 | 6 | 4 | 3 |
| ACLR5 [dBc] | -52 | -42 | -50 | -44 | -54 |
| ACLR10 [dBc] | -74 | -58 | | | -64 |
| RMS EVM [%] | 1.0 | 2.9 | 3.5 | 1.5 | 1.1 |
| Noise @45MHz [dBc/Hz] | -159 | -159 | -160 | -156 | -160 |
| Power Dissipation [mW] | 22 1) | 144 | 73 3) | 151 2) | 45 1) |
| Area [mm$^2$] | 0.8 1) | 0.7 | 2 | 3.7 | 0.53 1) |

1) Excluding synthesizer, DAC and digital

2) Excluding synthesizer

3) RFDAC only

Fig. 9. WCDMA performance summary of the transmitter.

## V. Conclusion

Fig. 9 summarizes the performance of the digitally predistorted transmitter in WCDMA band V and compares the result with previously published transmitters. This work shows best in class ACLR, EVM and noise in Rx band with a very competitive current consumption and die area. Only [1] has a lower current consumption but that design is not multi-band, does not support multiple outputs and is not terminated on-chip for good S22. The same DPD concept has been successfully demonstrated for LTE 5MHz and 10MHz signals.

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