Nano Switching Crossbar Array ESD Protection Structures

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***Abstract* — We report a new nano-switching ESD protection mechanism and dual-polarity Cu/$Si_xO_yN_z$/W nano crossbar array ESD structures. Experiments show full ESD protection featuring fast response of 100pS, ultra low leakage of <2pA and ESD protection of >9A. New dispersed local ESD tunneling model and CMOS integration are reported.**

***Index Terms* — ESD protection, nano switching array.**

I. Introduction

ESD protection design becomes challenging for sub-90nm ICs. For decades, traditional ESD structures utilize PN-junction-based ESD discharging mechanism, which is inherently very leaky and introduces significant parasitic effects due to active conduction mechanisms that seriously affect analog and RF IC performance [1]. Further, conventional PN turn-on type ESD triggering may cause mis-triggering in RF ICs dealing with high-frequency signals [2]. As technologies continue advance, novel ESD protection mechanisms and concepts are in urgent demands [3]. In this paper, we report a non-traditional nano phase switching ESD discharging mechanism and the first nano switching crossbar array ESD circuit.

II. Nano Switching Esd Protection

Fig. 1 depicts the new nano phase switching crossbar array ESD protection concept. The nano ESD switch can be turned on by an incoming ESD pulse for ESD discharging. Fig. 2 shows cross-section for a single-node nanowire crossbar ESD device consisting of a nano switching dielectric and two metal electrodes (A & K). Unlike a traditional PN-based ESD device, this nano insulator ensures very low leakage (I_{leak}). When an ESD surge appears at I/O, electric field instantly triggers the nano phase switch, resulting in the required ESD discharging. After ESD surge, it returns to OFF state. Prior reports on phase switching memories (CuTCNQ, SiO, etc.) [4] cannot be used for high-current transient ESD discharging in practical. We recently discovered a new Cu/$Si_xO_yN_z$/W single-node nano crossbar ESD switching mechanism [5]. This paper reports design of novel nano phase switching crossbar array ESD protection mechanism and new nano crossbar array ESD structures.

III. Experiments and Discussions

Based on our preliminary result on single-node nano

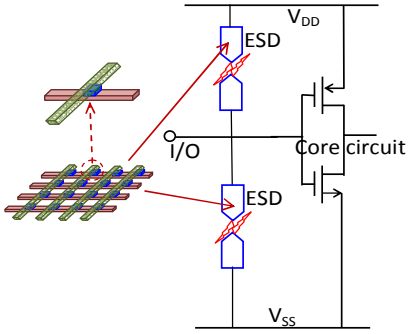

Fig. 1. New ESD protection scheme using novel nano phase switching crossbar array ESD structures.

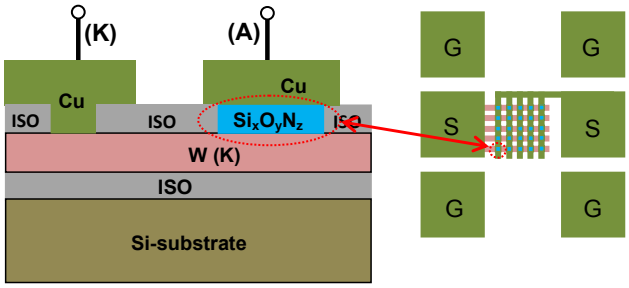

Fig. 2. Conceptual cross-section and layout for the new nano phase switching crossbar array ESD structures.

crossbar ESD protection concept, novel nano phase switching crossbar array ESD structures were designed in this work because single-node device cannot be used in practical designs. A new CMOS-compatible process was developed to fabricate nano crossbar array ESD devices including the following fabrication steps: First, a thin tungsten (W) film OF 100nm was deposited on SiO_2/Si wafer, which is followed by lithography and RIE etching to define the cathode (K). Next, a $Si_xO_yN_z$ nano phase switching layer was deposited by PECVD and tuned by reactive gas ratio of N_2O/SiH_4. Via is then formed for bottom connection. Finally, a Cu film was formed by PVD and lift-off to define device size, anode (A) and K pads. For design optimization, a large set of Cu/$Si_xO_yN_z$/W nano crossbar array ESD structures with varying design parameters were fabricated with the design split matrix given in Table I, including devices with different single-node areas and array sizes. Different $Si_xO_yN_z$ thickness (e.g., 50nm and 20nm) and composition ratios were used to adjust the critical ESD triggering voltage (V_{t1}). TCAD simulation was done to predict nano phase switch ESD

Table I Nano switching Array ESD Protection Design Matrix

Nano Insulator	$Si_xO_yN_z$		
Insulator Thickness	50nm		
	20nm		
Top Metal Contact	Cu		
	Pt		
Device Layout			
Single-Node ESD Devices: Node area		Array ESD Devices: Node area	Array size
1μmX1μm		2μmX2μm	8X8
2μmX2μm		5μmX5μm	5X5
5μmX5μm		10μmX10μm	3X3
10μmX10μm		20μmX20μm	2X2
20μmX20μm			
40μmX40μm			
60μmX60μm			
80μmX80μm			

discharging as shown in Fig. 3. A new *dispersed local ESD tunneling model* is proposed for as depicted in Fig. 3. Porous $Si_xO_yN_z$ is formed with low-temperature annealing to pre-diffuse and disperse Cu ions into $Si_xO_yN_z$ where Cu is trapped by Oxygen and Nitrogen atoms inside, yet remains in OFF state. Under ESD stress, a strong ESD electric field causes local electron tunneling between neighbor Cu ions dispersed throughout $Si_xO_yN_z$, resulting in low-R (R_{ON}) ESD discharging. After ESD pulse, ESD tunneling stops and the device returns to OFF state. Fig. 4 shows a die photo for fabricated nano crossbar array ESD devices. Full ESD function was verified by transmission line pulsing (TLP) testing. Fig. 5 shows full ESD I-V for a 1μmX1μm single-node nano crossbar ESD device by TLP

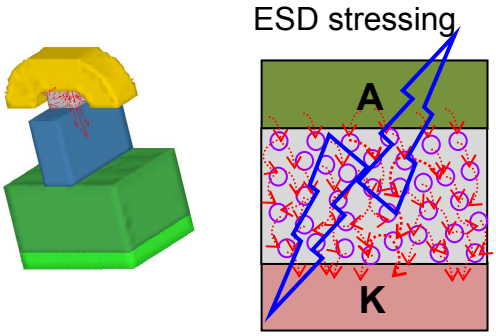

Fig. 3. Simulated ESD discharging (L) and dispersed local ESD tunneling model (R) for new nano switch array ESD structure.

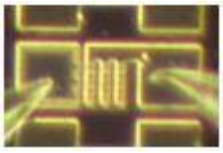

Fig. 4. Die photo for a sample 3x3 nano array ESD structure.

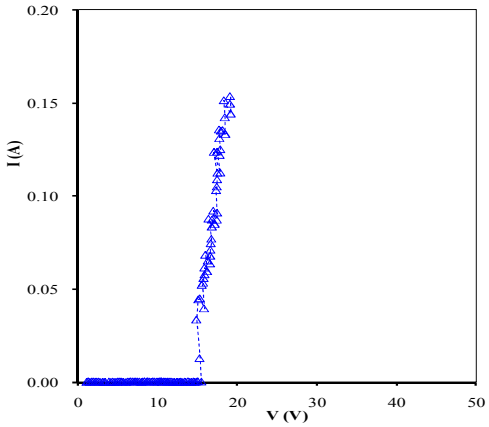

Fig. 5. Measured I-V by TLP for a 1μmX1μm single-node ESD.

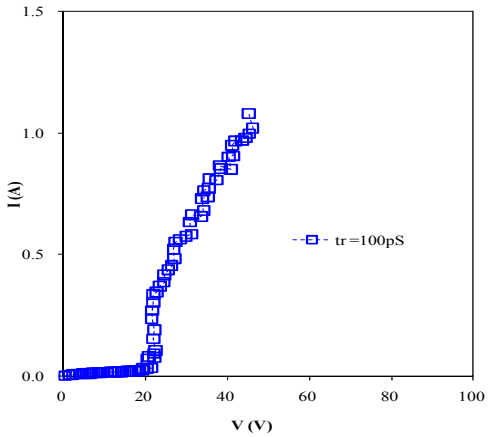

Fig. 6. Measured I-V *vs.* t_r by VF-TLP for a 20μmX20μm single-node ESD.

test (with pulse rising time t_r~10nS for HBM model). Fig. 6 gives I-V curve for a 20μmX20μm single-node crossbar ESD device by very-fast TLP (VF-TLP) confirming very fast ESD triggering at t_r~100pS (for CDM and IEC ESD models). Figs. 7, 8 & 9 depict full ESD I-V curves for both nano switch single-node and array ESD structures by TLP for the structure crossbar node areas of 5, 10μm and20μm in dimension. The array ESD device sizes are given in Table I. It is noticed that the single-node ESD device has one single ESD triggering as suggested by the new ESD tunneling model. However, all nano crossbar array ESD structures show multiple ESD triggering points associated with the crossbar nodes within the nano crossbar array ESD structures. The more array cross-nodes (2X2, 3X3 & 5X5 for node areas of 20, 10 & 5μm), the more multiple ESD triggering points observed (i.e., 2, 4 & 5 times) because local ESD tunneling may trigger one or more cross-nodes each time and sequentially within an ESD array structure. Hence, the numbers of multiple ESD triggering points may not be the same as the numbers of

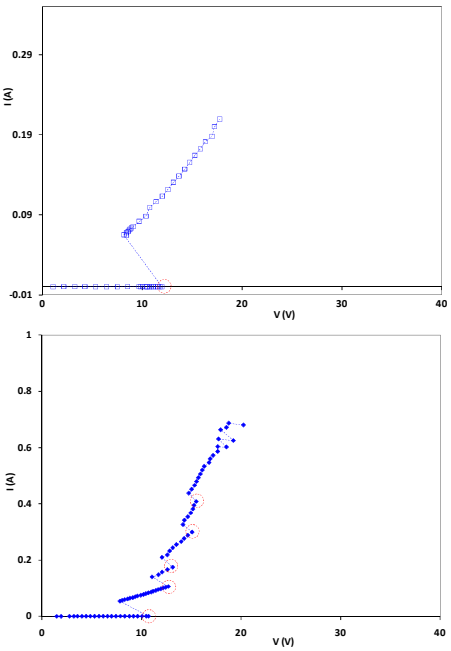

Fig. 7. Measured I-V curves by TLP for 5μmX5μm ESD devices: Single-node (Up) and 5X5 Array (Down).

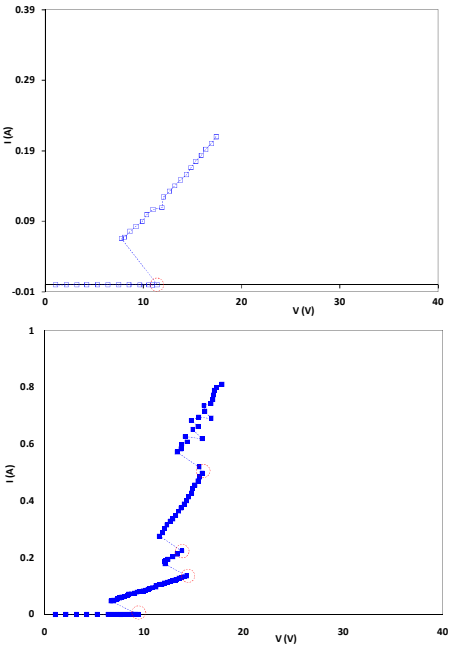

Fig. 8. Measured I-V curves by TLP for 10μmX10μm ESD devices: Single-node (Up) and 3X3 Array (Down).

cross-node units within an array. However, a monolithic relationship does exist. The new nano crossbar ESD device features fully dual-polarity ESD discharging function as shown in Fig. 10, highly desired in practical RF IC designs to reduce ESD parasitic effects [1]. Fig. 11

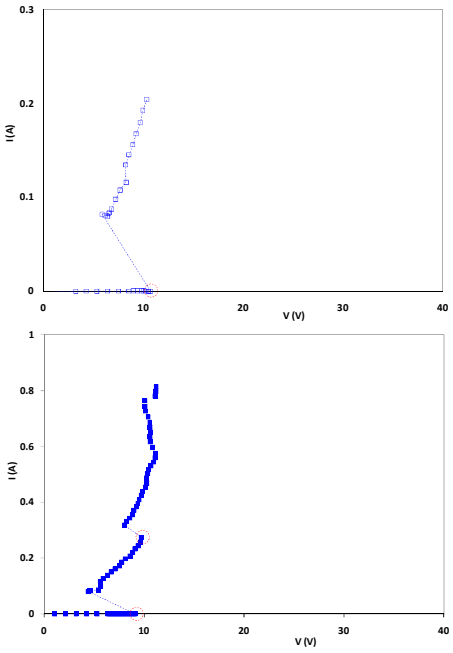

Fig. 9. Measured I-V curves by TLP for 20μmX20μm ESD devices: Single-node (Up) and 2X2 Array (Down).

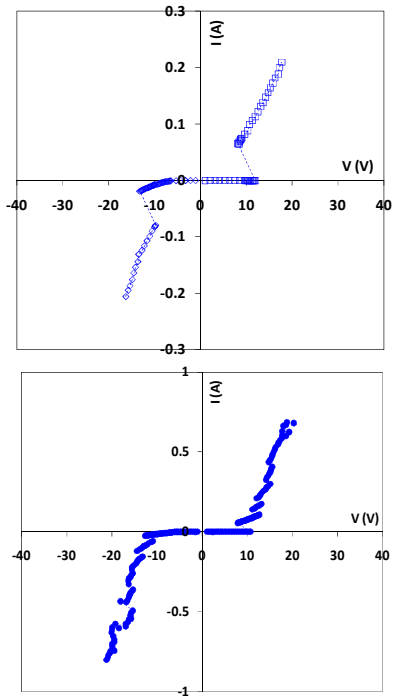

Fig. 10. TLP shows dual-polarity ESD discharging I-V curves for sample 5μmX5μm nano crossbar ESD protection devices: Single-node device (Up) and 5x5 Array ESD structures (Down).

shows that new ESD structure achieves ultra-low leakage of I_{leak}<2pA. The new dispersed local ESD tunneling model is different from reported phase changing memory

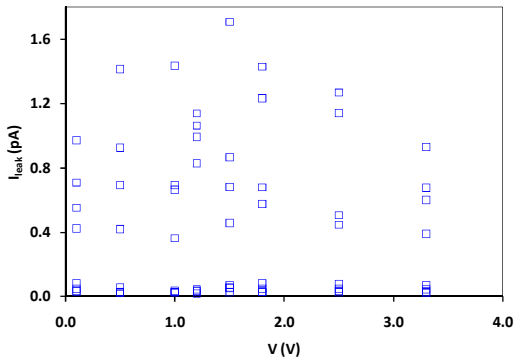

Fig. 11. Measured I_{leak} for single-node and array ESD structures at typical biasing of 0.1V to 3.3V.

model and verified by testing in two ways: very fast switching of t_r~100pS (5-50nS in phase memories) and monolithic R_{ON} against device sizes as shown in Fig. 12 (versus fixed R_{ON} in memories due to limited numbers of conducting filaments) [6, 7]. Fig. 13 shows ESD V_{t1} reduction by TLP testing as its pulse t_r reduces from 10nS to 0.2nS, because displacement current increases for faster TLP pulse [1]. We found that ESD triggering is greatly affected by $Si_xO_yN_z$ ratio and thickness, which allows flexible ESD V_{t1} by design splits. This work shows a wide ESD V_{t1} tuning range from 1.26V to 28.3V by varying $Si_xO_yN_z$ ratio and thickness as shown in Fig. 14. It is also found that Cu contact is better than Pt, due to more efficient local ESD tunneling effect for Cu. In addition, TLP testing shows that our array ESD devices can handle ESD transient of up to 9A without clear damages.

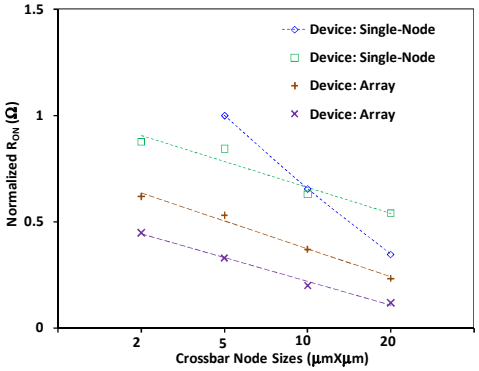

Fig. 12. Measured normalized ESD discharging R_{ON} for sample single-node and array devices.

IV. Conclusion

We report a new dual-polarity nano phase switching ESD protection mechanism and the first nano switching crossbar array ESD structure, which was verified experimentally and by a new model. Testing shows excellent ESD protection features including ultra fast response time t_r~100pS, ultra low leakage I_{leak}<2pA and high ESD protection level. The new design is compatible to CMOS process flows and can be used for RF ICs.

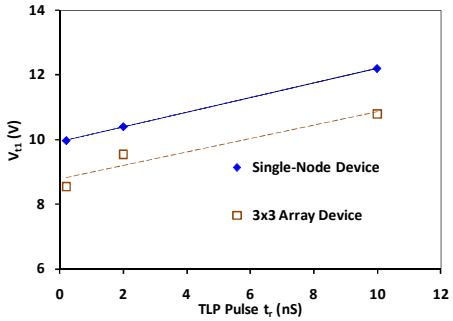

Fig. 13. Measured ESD V_{t1} decreases as TLP pulse rising time becomes shorter.

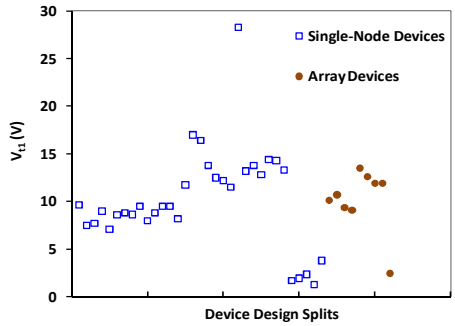

Fig. 14. Measurement shows a wide range adjustable ESD triggering by ESD device design splits.

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