A 12ps True-Time-Delay Phase Shifter with 6.6% delay variation at 20-40GHz

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***ABSTRACT* — A fully integrated 2-channel Ka-band True Time Delay (TTD) phase shifter with 12ps continuous changing delay time has been realized in a 0.25μm SiGe:C BiCMOS technology. A delay variation cancellation technique is proposed, resulting in less than 0.8ps delay variation over a 20-40GHz frequency span, meanwhile maintaining a constant input impedance. In the high (low) power mode, the measured input 1dB compression point and input IP3 are +9.7dBm (+3.6dBm) and +18dBm (+13dBm) at 30GHz with an averaged power consumption per channel of 145mW (33mW) for the same TTD performance. The size of the core phase shifter is less than 0.1mm^2.**

Keywords – Ka-band, True Time Delay, Phase Shifter, SiGe:C BiCMOS technology.

I. Introduction

Phased array technique is widely used in mm-wave frequencies to compensate for high path loss and to suppress interference from the undesired direction. Wideband phased array receivers not only meet the need for high speed data transfer but facilitate a generic solution for multi-applications operating in different frequencies. As an example, 10GHz bandwidth is necessary for a full coverage of the main applications in Ka-band, i.e. VSAT, LMDS and Ka-band radar. Classical phase shifters, which can only be used to approximate the required delay in a narrow bandwidth, will in this case result in the beam-squinting phenomenon, which degrades the performance of the beamformer.

To extend the bandwidth of a beamforming system, true-time-delay (TTD) phase shifters are needed to provide the constant time delay independent of signal frequency. Switched delay lines are extensively used in RF TTD circuits [1-4], where the variable delays are realized by changing the inserted length of a transmission line (TL). A general disadvantage of this solution is that the delay settings are discrete, limiting the delay setting resolution. A varactor loaded TL offers continuous delay settings feature, however, by tuning the capacitor over a large range, the characteristic impedance (Z_0) of the TL changes, resulting in a varying input and output impedance as well as in gain variation. Besides the mentioned limitations, all these TL-based solutions tend to consume large chip area. Employing LC-based artificial TL [5] and meander TL [1] implementations can, in general, help to reduce the dimension of the delay lines. However, more than 10% delay variation over frequencies can be observed for these techniques. There are also TTD solutions proposed based on RC all-pass filters [6, 7], which achieve large variable delay within small area. So far, they are only explored for frequencies below 10GHz.

In this work, a delay variation cancellation technique will be introduced, which enables a flat delay response over 20-40GHz with only 6.6% delay variation. The paper is organized as follows: Section II introduces and explains the delay variation cancellation. Section III discusses the design of TTD blocks. Section IV presents the measurement results and benchmarking, which will be followed by conclusions in Section V.

II. Delay Variation Cancellation

Most of the TTD circuits implementations can be considered as a kind of low-pass filter (LPF). They are either based on LC-LPF, i.e. lumped LC π-networks and distributed LC networks (transmission line), or based on RC-LPF. Due to the limited cut-off frequency, their phase response can only approximate the TTD up to a limited frequency, beyond which delay variations will be present. Equations (1) and (2) present the absolute delay generated by ideal single stage LC π-network and G_m-RC cell (Figure 1):

$$\tau_{LC} = \frac{1}{\omega}\tan^{-1}\frac{2\omega L_A}{R_L(2-L_AC_A\omega^2)} \quad (1)$$

$$\tau_{RC} = \frac{1}{\omega}\tan^{-1}\omega R_BC_B \quad (2)$$

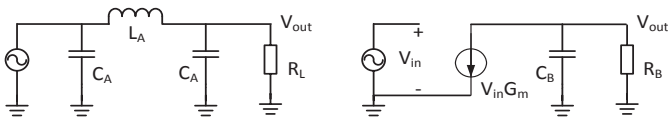

Figure 1. Simplified LC π-network (left) and G_m-RC cell (right)

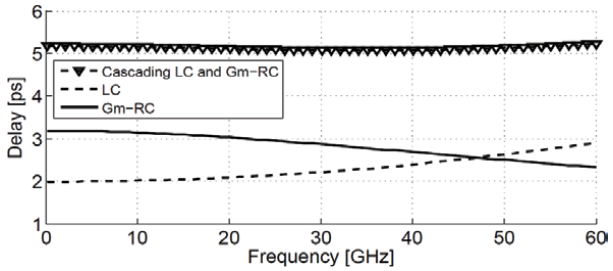

Figure 2. Mechanism of delay variation cancelation

in which ω is the angular frequency and R_L is the load impedance of the LC network, which is assumed resistive for simplicity. Figure 2 shows the delay responses generated by G_m-RC cell and LC networks as a function of frequency. The delay of the former compressed as the frequency increases mainly due to the nonlinear nature of $\tan^{-1}$ function, while the delay of the latter can offer an expansive feature by properly adjusting its parameters. As a result, by cascading the two types of LPF in a proper way, the expansion and compression behavior will cancel each other and a flat delay response will be achieved over a large frequency band (Figure 2, triangular line).

III. Design of TTD phase shifter

A. Architecture Choice

Figure 3 shows the block diagram of the proposed fully differential TTD phase shifter (figure shows single-ended implementation for simplicity). To perform a delay variation cancellation, the required delay is generated by cascading varactor-loaded LC-networks with G_m-RC delay cells. The N-stage G_m-RC cells, each with a fixed delay τ_D and unit-gain, perform the coarse delay tuning. Switches k_1, k_2… k_N are acting as path selectors to control the coarse delay with a time step τ_D. G_m-RC cells that are bypassed by the switches are turned off to reduce power consumption. Since the first G_m-RC cell has to be turned-on all the time, the N-stage G_m-RC cells generate a variable delay (N-1)τ_D. The LC-delay cell, composed by the M-stage cascaded LC π-networks, performs a continuous fine tuning with a total variable delay of τ_f ($\tau_f \geq \tau_D$). As a result, the total continuously variable delay is $\tau_f + (N-1)\tau_D$. As the G_m-RC cells are inductorless, the maximal variable delay of the proposed structure can be extended by cascading more G_m-RC cells in a compact way. Signals from different channels are summed in current domain at node RF_{out}.

The target total variable delay is 12ps, i.e. the relative delay between two receiver channels will then range from -12ps to 12ps. This enables a 2-channel beamformer to perform a beam steering from -45 to 45 degree, enough for most Ka-band applications. With the fixed total variable delay, increasing the number of stages cascaded in the LC and G_m-RC cells, i.e. M and N, will reduce gain variation and input impedance variation during the delay settings. However, larger N and M will result in larger power consumption and chip area. A trade-off has been achieved by choosing M=N=3, which yields $\tau_f = \tau_D =$ 4ps, assuming the fine tuning range can just cover the gap between two coarse settings.

B. Design of the delay cells

The G_m-cell is implemented by a common-based (CB) differential amplifier (Figure 4). RF chokes are realized by resistors R_1 and R_2 instead of inductors to keep the structure compact. Each path-selecting switch $k_{1,2,...N}$ (Figure 3) is implemented as differential pair Q_2 and Q_3 (Figure 4), which at 30GHz present an insertion resistance of 2.5Ω in the on-state and have more than 10dB attenuation when turned off. Capacitance C_{dc} acts as a DC blocking capacitor. To generate 4ps delay per stage, the equivalent parallel resistance R' and capacitance C' at the output node of G_m-cell should satisfy $R'C'$=4ps. As shown in Figure 5, this $R'C'$ is mainly composed out of the output capacitance of G_m cell (C_{out}), series resistance of switches (R_{ON}) and the input impedance of next G_m-RC stage (Z_{CB}). The G_m-RC cells are able to operate at different supply voltage, i.e. from 1.5V to 2.7V, without degrading of TTD performance. Each differential G_m-RC stage in high power mode (2.7V) draws 27mA, and in low power mode (1.5V) consumes 11mA. The simulated worst-case delay variations of the complete G_m-RC cells are 1.3ps and 1.5ps respectively in high and low power modes over 20-40GHz frequency band. The input impedance of G_m-RC cells, due to the CB structure, is only 6Ω. To ease the impedance matching, the LC networks are designed also with low characteristic impedance.

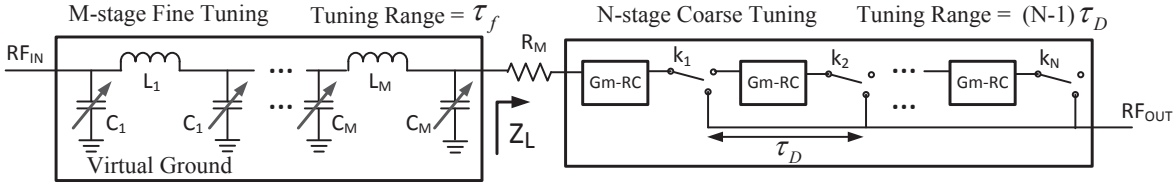

Figure 3. Block diagram of differential proposed TTD phase shifter (plotted in single-ended form for simplicity)

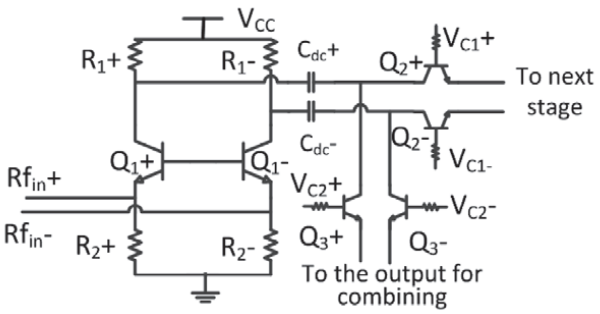

Figure 4. Schematic of G_m-Cells (bias not shown)

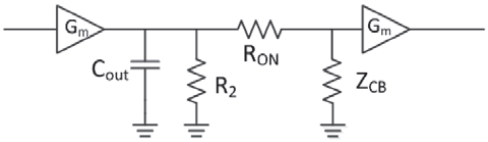

Figure 5. Composition of R'C' at the output of G_m-cell

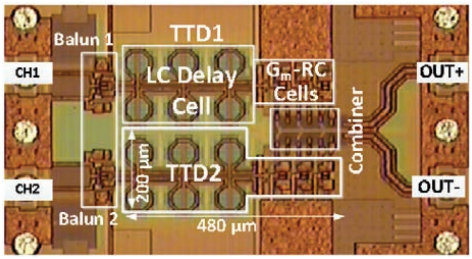

Figure 6. Die photo of the 2-channel TTD beamformer

As shown in Figure 3, by combining the fixed MIM capacitance and the varactor, the equivalent single-ended capacitance $C_{1,2...M}$ varies from 130fF to 190fF. To perform delay-variation cancellation, the single-ended Z_L is chosen as 17Ω, with which the LC-delay cell almost cancels the 1.3ps delay errors coming from the G_m-RC cells. To provide such Z_L, an 11Ω series resistor R_M is added in series with the G_m-RC cells. The complete LC delay cell offers 5.1ps variable delay, enough to cover the 4ps gap between the 2 successive coarse settings.

IV. Measurements

The proposed TTD phase shifter has been realized in a single-channel and two-channel version, using a 0.25µm SiGe:C BiCMOS technology with a peak f_T/f_{max} of 216/177 GHz [8]. The power dissipation (P_{diss}) of the phase shifter depends on the amount of realized delay. Denote P_D as the power consumed by each G_m-RC cell. The maximum P_{diss} of the 2-channel beamformer is $4P_D$, i.e. with one channel activating three G_m-RC cells and the other channel turning on one G_m-RC cell. This leads to an effective P_{diss} per channel of $2P_D$, which in high power mode equals to 146mW, i.e. 2×27mA×2.7V, and in low power mode equals to 33mW, i.e. 2×11mA×1.5V.

S-parameters measurement of single-channel phase shifter has been performed with different supply voltage. With V_{CC} from 1.5V to 2.7V, the realized phase shifter presents similar performance regarding S_{11}, delay and gain variation. Taking V_{CC}=2.7V as an example, Figure 7 shows the measured relative delay response for different delay settings. To evaluate the flatness of the achieved delay response, Figure 8 shows the fitted Gaussian distribution function of the worst-case delay variations over 13 circuit samples. The results show an average delay variation of 0.77ps ($\sigma < 60fs$) within a 20GHz frequency band, and of only 0.36ps ($\sigma < 35fs$) within a 10GHz frequency band. The gain variation (S_{21}) of the phase shifter, across different delay settings, is less than ±0.9dB at 30GHz. The core of the phase shifter presents an available gain G_a of -10.5dB at 30GHz and almost constant input impedance, i.e. $|S_{11}|$< -15dB for all delay settings. The large signal performance of the phase shifter, as expected, changes as a function of supply voltage, i.e. power dissipation. As shown in Figure 9, the measured worst-case input 1dB compression point (ICP_{1dB}) and IIP3 at 30GHz are +9.7dBm and +18dBm in high power mode and are +3.6dBm and +13dBm in low power mode.

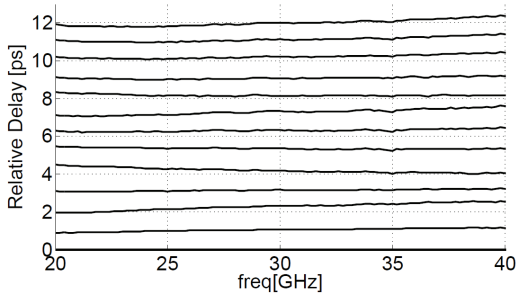

Figure 7. Relative delay response for different delay settings

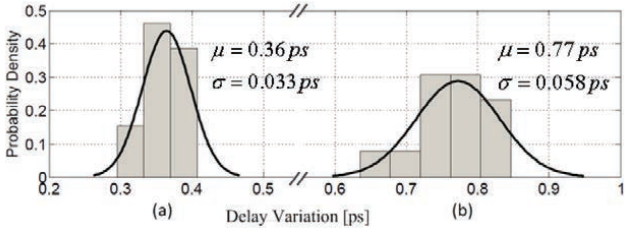

Figure 8. Fitted Gaussian distribution of worst-case delay variation over 13 samples within (a) 25-35GHz (b) 20-40GHz

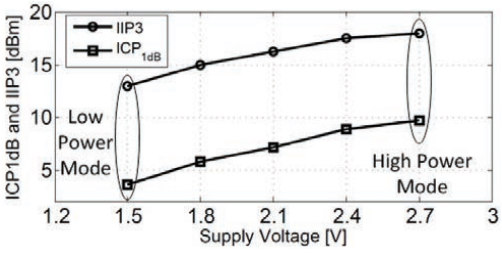

Figure 9. Measured ICP_{1dB} and IIP3 with different supply voltage

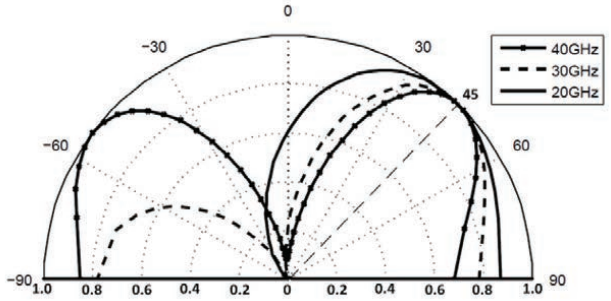

Figure 10. Normalized beam pattern of 2-channel beamformer

The two-channel TTD beamformer (Figure 6) consists of two identical TTD phase shifters as in the single-channel version. On-chip active baluns are used to perform single-to-differential conversion from the two single-ended channel input. At the output, signals from two channels are summed in current domain via a microstrip-line based passive combiner which also acts as a part of output matching network. To evaluate the beam pattern of the 2-channel beamformer, taking into account of the coupling between channels, a full 3 ports S-parameters measurement is performed for different delay settings, i.e. single-ended port 1 and 2 for two channel input and differential port 3 at the output. Figure 10 shows the normalized array pattern for the 2-channel beamformer for maximal delay setting (in high power mode), which is synthesized from the measured 3-port S-parameters. It is seen that signals with 20GHz frequency difference simultaneously reach their optimum at a signal angle of 45° without obvious beam-squinting.

Table I shows the benchmark with other fully integrated TTD phase shifters. The proposed work has an improved performance regarding delay/gain variation (in percentage of total variable delay), flat delay bandwidth, and delay resolution.

V. Conclusion

A compact Ka-band TTD phase shifter has been realized using 0.25µm SiGe:C BiCMOS process. With the proposed delay-variation cancellation technique, a flat delay response is achieved from 20GHz to 40GHz with only 6.6% delay variation. A constant input impedance, i.e. $|S_{11}|$< -15dB, is maintained for all delay settings within 20-40GHz frequency band.

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Table I. The benchmarking with other fully integrated TTD phase shifter

	[1]	[2]	[3]	[5]	[6]	[7]	[9]	This Work (2.7V supply)		This Work (1.5V supply)	
Technology	0.18 µm SiGe	0.13 µm SiGe	0.13 µm SiGe	0.13 µm CMOS	0.14 µm CMOS	0.8 µm SiGe	90 nm CMOS	0.25 µm SiGe		0.25 µm SiGe	
Gain variation [dB]	±1	N.A.	N.A	±3	±0.4	±0.7	±3	±0.9		±1.4	
Max. delay [ps]	64	16	54	225	550	25	26	12		12.5	
Frequency [GHz]	1-15	55-65	31-41	1-15	1-2.5	3-10	0-8	20-40	25-35	20-40	25-35
Delay variation**	~16 %	N.A.	N.A.	~14 %	3.6 %	40 %	10%	6.4*%	3*%	6.6%	3.2%
P_{DC} per channel [mW]	87.5	Passive	104	78	90	38.8	Passive	146		33	
Resolution [ps]	4	1.2	18	15	Cont.	Cont.	13	Cont.		Cont.	
Size*** [mm^2]	0.82	0.35	1.44	1.5	0.07	0.23	N.A.	0.1		0.1	

*Based on 13 samples ** The absolute delay variation in percentage of total variable delay, values with '~' are estimated from the given delay response
*** Estimated size of core TTD size only