A Passive Mixer-First Receiver Front-End without External Components for Mobile TV Applications

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***Abstract* — This paper describes a passive mixer-first receiver front-end (RFE) for mobile TV covering 100MHz to 800MHz without any external components. The proposed input matching technique with RC discharging circuit achieves a simple topology with a low noise. The out-of-band linearity is enhanced using the low pass filtering of sampling capacitor, delivering an outstanding out-of-band linearity. The out-of-band IIP3 and IIP2 are 7dBm and 36dBm, respectively at the maximum gain setting of 36dB. The third and fifth harmonic rejection ratios (HRR) are 49dB and 42dB, respectively. The power consumption is 23mW and the maximum NF is 3.6dB. The active area occupies 0.33mm^2 in 65nm CMOS technology.**

***Index Terms* — Direct conversion, mobile TV, front-end, receiver, passive mixer, low-pass filter, harmonic mixing, impedance matching.**

I. Introduction

Various frequency bands are used for mobile TV among several countries and the unified mobile TV tuner should have a wideband input matching. Moreover, it requires good linearity and low noise across the broad band for multistandard operation [1, 2]. A passive mixer-first receiver can achieve the wide input matching using transparency characteristic of the mixer with simple topology, small power consumption and good out-of-band linearity [3].

This paper describes a passive mixer-first receiver front-end (RFE) in 65nm CMOS process for the mobile TV applications. The proposed RFE is consisted of passive mixers with 8-phase LO pulses, transconductance (gm) stages, current-mode Biquad LPFs and frequency divider with clock buffers as shown in Fig. 1.

The detailed descriptions of the blocks will be introduced in the next session. The passive mixer and input matching blocks are controlled by the clock. The clock circuit is consisted of the frequency divider (divided-by-8) and the clock buffer, which generates a non-overlapping clock. The proposed RFE covers 100MHz to 800MHz, which is limited by the clock circuit with an external single LO. Using a differential LO or phase corrector, the operation frequency range can be easily extended [2, 3].

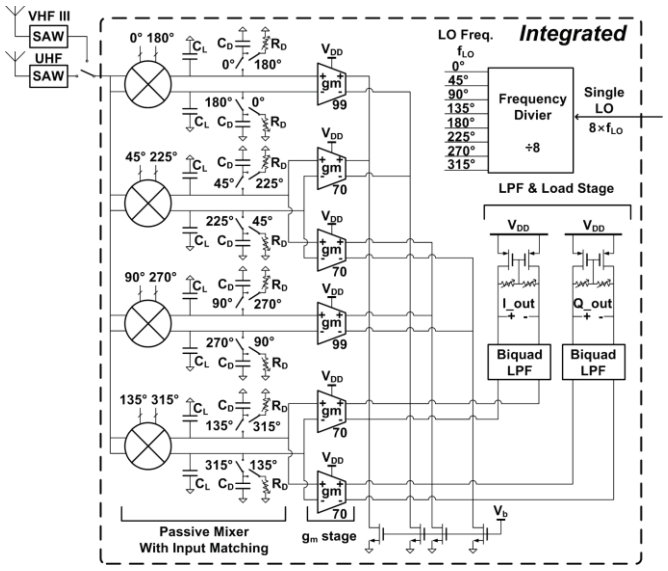

Fig. 1. Block diagram of the proposed passive mixer-first RFE.

II. Topology and Implementation

A. Input Matching

The passive mixer has a transparency property, presenting the impedance of their baseband port to the RF port. Therefore, the passive mixer-first receiver can achieve wideband input matching using tunable baseband resistors [3]. The baseband resistors generate significant noise and the noise can be minimized using a feedback loop. However, the loop reduces the gain and generates the stability problem, and buffer stages and additional capacitors are required to alleviate the problems. These extra circuit components increase power consumption and chip area. To solve the problem, we proposed a very simple circuit with discharging resistor R_D and switched capacitor C_D. Figure 2 shows the charging step and discharging step of the mixer where the input capacitor C_L functions as a storage of the sampled signal from the RF port for the input of the following gm stage. This technique separates the charging and discharging steps

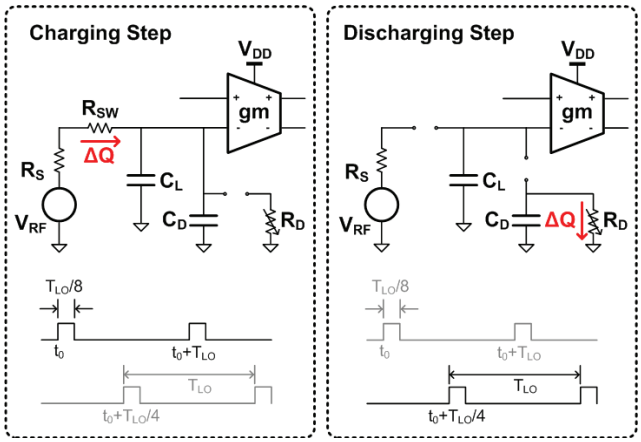

Fig. 2. Charging and discharging steps of the proposed input matching technique.

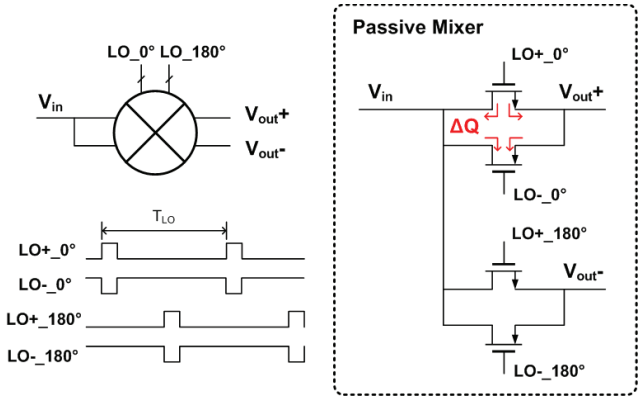

Fig. 3. Complementary Switches of the passive mixer.

using the opposite phase LO pulse and the switch isolation. During the charging step, the C_L and C_D are connected to one node by the switch and charged by the down-converted signal from the RF port. During the discharge step, a portion of the signal in the C_D is discharged to R_D.

The R_D is always opened from the signal path and its noise has no effect. Using the tunable R_D for adjusting an amount of the discharge, we can tune the impedance of the baseband port and also achieve the input matching through the transparency property. The capacitor sizes are determined by the operation frequency range and the required bandwidth, and the proposed technique does not increase the total capacitor size and the chip area. The impedance matching can affect the noise performance, and there is a tradeoff between the input matching and the noise performance. From the optimum R_D for the input matching, we can reduce noise by increasing R_D, while the matching is degraded.

B. Noise performance

For a low noise, the on-resistance of the passive mixer switch R_{SW} should be small but the switch size has a limit because the operation frequency is limited by the parasitic capacitance of the switches. To minimize the R_{SW} without increasing the parasitic capacitance, we use higher bias voltage of 1.6V for the clock buffer than the voltage of 1.2V for the rest of the circuits. In the simulation, the total RFE without the LPF has a small NF, under 2dB over the operation frequency. Due to this low noise, we can implement an additional current-mode Biquad LPF [4] for out-of-band signal rejection and still can achieve the total NF of under 3.6dB without using an additional gain stage to suppress noise from the LPF.

C. External components

The conventional RFEs for mobile TV require external components for the wideband input matching and biasing. Due to the transparency property, the passive mixer-first receiver does not require any external component for the wideband input matching. In the proposed RFE, the input bias of the gm stage is supplied through an internal resistor instead of a RF choke, eliminating the external components. As the operation frequency increases, the input bias variation, due to the charge injection from the switch of the passive mixer, becomes large. To reduce the charge injection, we implement complementary switches for the passive mixers as shown in Fig. 3. For the complementary switches, the clock buffers generate the differential LO pulses. Compared to NMOS-only or PMOS-only switches, the total capacitance of the switches remains almost the same, and an additional power consumption for the clock buffers is negligible.

D. Folded cascode

In the conventional passive-mixer first topology, the baseband LNA amplifies the down-converted baseband signal with a sufficient gain for a reduced total noise figure. However, as the gain of the baseband LNA increases, the linearity requirement of the following blocks as gm stage and load stage for a harmonic rejection (HR) also increases. In the proposed topology, thanks to the proposed input matching technique, the RFE does not require an additional gain stage. The gm stage and load stage in a folded cascode form functions as the baseband LNA as well as HR and it relaxes the linearity requirement by reducing the gain stages (Fig. 1). Two types of the different gm (99/70) stages are used for the third and fifth HR [5]. Through the Biquad LPF, the out-of-band signal is rejected, and the current signal is converted to the

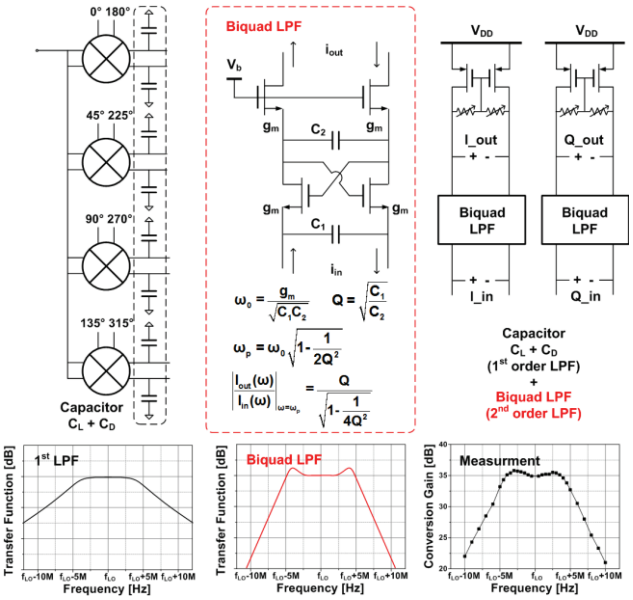

Fig. 4. Transfer characteristic of two LPFs and measured conversion gain of the RFE.

voltage in the load stage. For a high gain and low noise, the gm stages should have a large current. However, the load stage with the active load and the Biquad LPF should have a small current for a large output load and low cutoff frequency using small capacitors, respectively. The folded cascode topology is designed to function as a current divider, driving a large current to gm stages and a small current to the Biquad LPF and load stage at the same time. Moreover, the folded cascode topology solves the stacking problem with a low supply voltage of 1.2V.

E. Linearity requirements

Linearity requirement is one of critical issues to design a RFE for the mobile TV. The input capacitor C_L and switched capacitor C_D can be used as a first order LPF on the baseband port to reject out-of-band signals and relax the linearity requirement [3]. As C_L+C_D increases, the in-band loss becomes significant while the out-of-band reject is increased. Overshoot of the second order Biquad filter is utilized to compensate the in-band loss (Fig. 4). The frequency and magnitude of the overshoot can be controlled by current and capacitance of the Biquad LPF. Using the two filtering characteristics, the proposed RFE has a flat gain, fluctuation of less than ±0.5dB within the ±4MHz channel bandwidth and 3dB cutoff frequency of ±5MHz away from LO frequency f_{LO}. This filtering method can reject the out-of-band signal effectively and minimizes the in-band fluctuation at the same time.

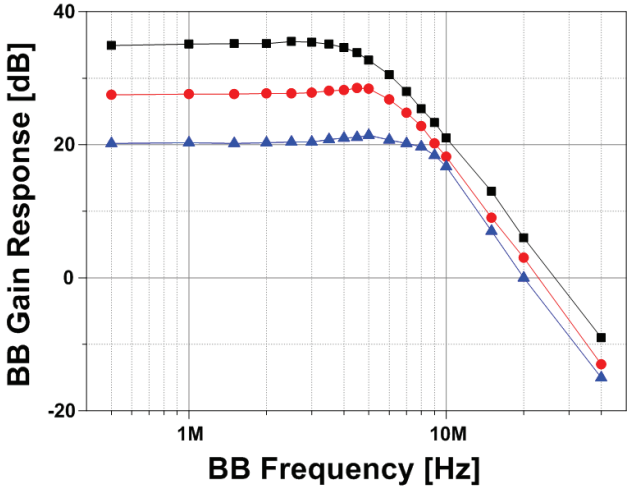

Fig. 5. Measured RFE's baseband gain responses with variable gains.

III. Measurements

The RFE fabricated in 65nm CMOS measures the maximum conversion gain of 36dB±0.5dB and the different gain steps of over 16dB are shown in the Fig. 5. The total power consumption is 23mW at 800MHz with 1.2V and 1.6V (clock buffers) supply voltages. The maximum noise figure is 3.6dB over the operating frequencies. The out-of-band IIP3 and IIP2 versus various operation frequencies for the two-tone signals at [f_{LO}+16MHz/f_{LO}+28MHz, f_{LO}+16MHz/f_{LO}+20MHz] are shown in Fig. 6. The out-of-band IIP3 and IIP2 are 7dBm and 36dBm, respectively at the maximum gain of 36dB. The minimum third and fifth harmonic rejection ratios

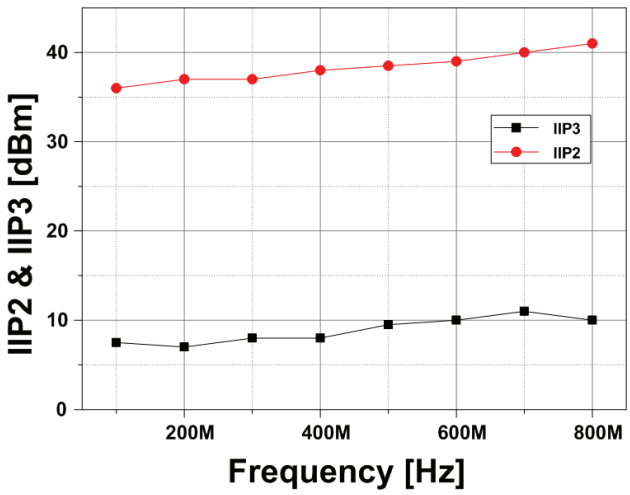

Fig. 6. IIP3 and IIP2 measurements versus frequencies.

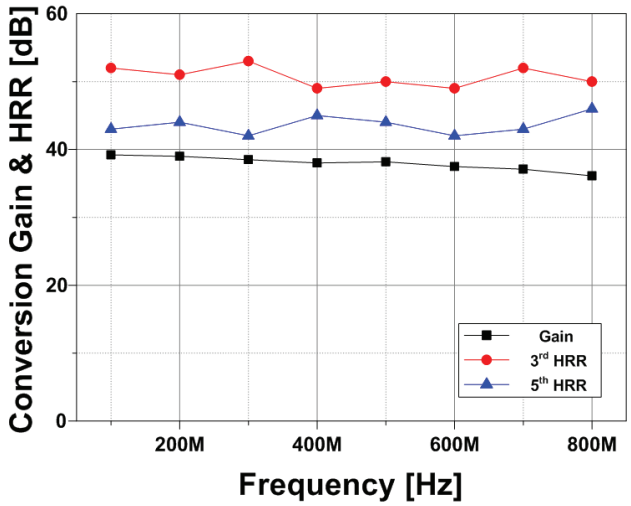

Fig. 7. Measured harmonic rejection ratio and conversion gain versus frequencies.

(HRR) are 49dB and 42dB, respectively (Fig. 7), relaxing the rejection profile of the off-chip SAW filter [5]. The measurement results are summarized in Table I. The active area of the RFE occupies 0.33mm^2 and the die photo is shown in Fig. 8.

IV. Conclusion

The proposed passive mixer-first RFE for mobile TV covers frequency band of 100MHz to 800MHz while eliminating external components and has outstanding linearity performance, low noise and small chip area.

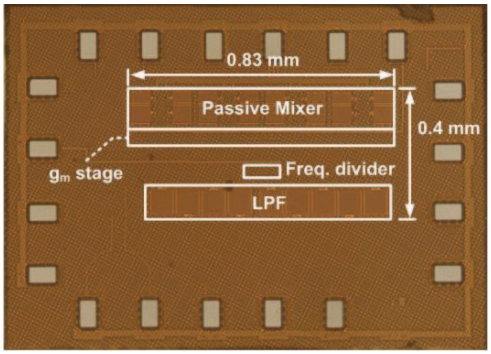

Fig. 8. Die Photograph of the RFE.

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TABLE I
Summary of Measured Performance and Comparison

Parameters	This Work	JSSC11' [2]	JSSC10' [6]
Frequency (GHz)	0.1 to 0.8	0.17 to 1.7	0.3 to 0.8
Gain (dB)	20 to 36	17 to 35	22 to 28
Ext. Components	None	1 Inductor	2 Inductors
Area (mm^2)	0.33	0.46	0.5
DSB NF (dB)	3.6*	4	0.8 to 4.3
IIP3/IIP2 (dBm)	7*/ 36*	-3.4 / 32	-14 / 38
Power (mW)	23	55	18
Input Matching	Matched	Matched	Unmatched
3rd / 5th HRR (dB)	49 / 42	35 / 39	60 / 60
Supply (V)	1.2 / 1.6	1.2 / 2.5	1.2
Process (nm)	65	65	65

(*) – Reported value is for the maximum gain setting of 36dB.

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