Effect of Drift Region Resistance on Temperature Characteristics of RF Power LDMOS Transistors

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***Abstract* — In this work, we investigated the effects of drift region resistance on the temperature behaviors of RF power LDMOS transistors. Devices with various implant doses in the drift region were fabricated. Owing to the quasi-saturation effect, the transconductances at high gate voltages are less dependent on the temperature for low-drift-dose device. In addition, the maximum oscillation frequency exhibits different temperature coefficients for devices with different drift doses. We derived an expression of unilateral power gain with 4th-order frequency term, and found that the drift resistance has a large influence on the device temperature characteristics at high frequencies.**

***Index Terms* — Power transistor, radio frequency, resistance, temperature, transconductance.**

I. Introduction

The rapid growth of wireless communication product markets has created a huge demand for low-cost, high-efficiency, and good-linearity RF power amplifiers. Among power devices, laterally diffused metal-oxide-semiconductor (LDMOS) transistors are the most attractive in cost and potential for improvements in performance and integration. LDMOS transistors have been widely used in RF power amplifier modules for a high frequency range up to 3.8 GHz [1]-[3]. Since the power devices are operated at high power densities, the device will suffer a high channel temperature due to self-heating effect. Besides, for high-temperature applications, the temperature behavior of devices needs to be investigated and well modeled for circuit design. Therefore we are interested to know the temperature effect on RF characteristics of LDMOS transistors.

The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) are critical figures of merit for evaluating the performance of RF transistors. For low-voltage CMOS transistors in RF applications, the temperature dependences of f_T and f_{max} are related to the transconductance and substrate resistance [4]-[6]. Owing to the present drift region in LDMOS, the temperature effects on the LDMOS performance might be different from those on the CMOS device performance. Previously, we investigated the temperature effect on f_T and f_{max} of LDMOS and found that the variations of f_T and f_{max} with temperature were not only affected by the change in transconductance but also affected by the drain resistance [7]. In this work, we explored the temperature behavior of RF LDMOS transistors with various implant doses in the drift region. Low-drift-dose device exhibits larger drift resistance and more severe quasi-saturation effect. Owing to the effects of the drift region resistance, different temperature behaviors in RF characteristics are presented for devices with different drift doses.

II. Experiments

The n-channel LDMOS transistors in this work were fabricated on 6-inch (100) silicon wafers with a gate oxide thickness of 135 Å. The schematic cross section of the device is shown in Fig. 1(a). This device has a lightly doped n-well drift region under the field oxide to achieve a breakdown voltage higher than 50 V. The effective channel length and drift-region length are about 0.6 μm and 3 μm, respectively. Devices with the same process condition except for different implant doses in the drift region were investigated. The devices under test (DUT) have a multifinger gate configuration featuring 40 fingers with a total width of 400 μm [Fig. 1(b)]. The S-parameters of devices were measured on chip using an Agilent 8510 network analyzer from 100 MHz to 20 GHz.

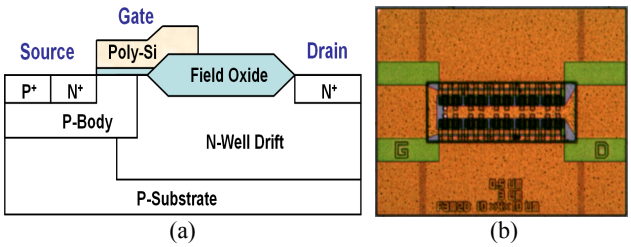
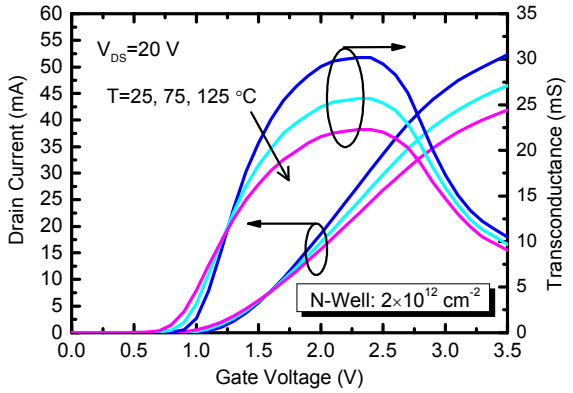


Fig. 1. (a) Schematic cross section of an LDMOS transistor. (b) Photography of the DUT.

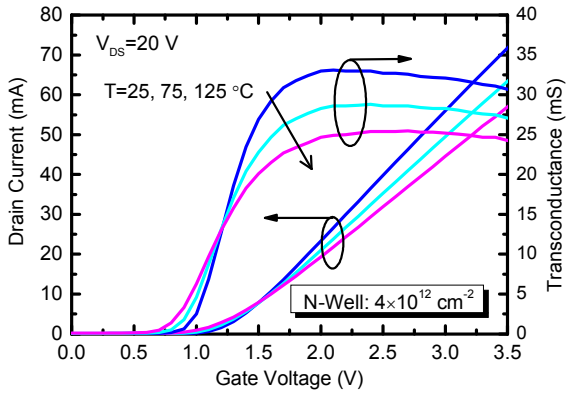
III. Results And Discussion

A. DC Characteristics

Fig. 1 shows the transfer characteristics of LDMOS with different n-well drift doses. At low gate voltages (V_{GS}<1.2 V), the transconductance (g_m) and drain current increase with increasing the temperature owing to the decrease in the threshold voltage [8]. At high gate voltages, because the channel mobility decreases with increasing temperature, the g_m and drain current decrease [8]. Because of the negative temperature coefficients of the effective mobility and threshold voltage, the drain current and g_m have zero-temperature-coefficient biases near V_{GS}=1.5 and 1.2 V, respectively. For low-drift-dose device, the g_m decreases rapidly when the gate voltages are higher than 2.5 V, which is not observed in the high-drift-dose device. It indicates that the quasi-saturation effect in the low-drift-dose device is more significant.



(a)



(b)

Fig. 2. Transfer characteristics of LDMOS with drift doses of (a) 2×10^{12} and (b) 4×10^{12} cm^{-2}.

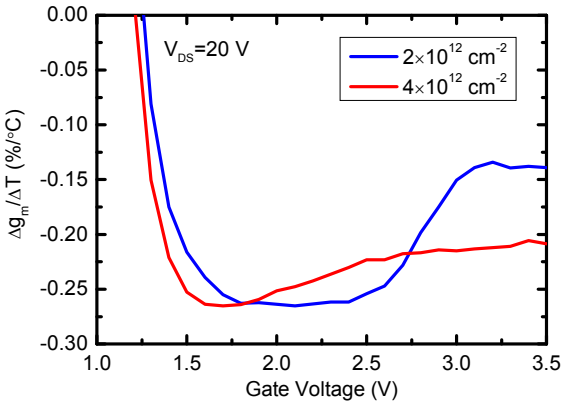


Fig. 3. Temperature coefficients of transconductance as a function of gate voltage. The values of $\Delta g_m/\Delta T$ have been normalized to g_m at 25ºC.

The quasi-saturation effect will influence the temperature coefficients of transconductance ($\Delta g_m/\Delta T$). As shown in Fig. 3, the $\Delta g_m/\Delta T$ in quasi-saturation region (V_{GS}>2.5 V) is much lower than that in medium gate bias region for device with a drift dose of 2×10^{12} cm^{-2}. For LDMOS transistors, the drain current is dominated by the channel current at low gate voltages, while it is dominated by the drift region resistance at high gate voltages. When the device operates in quasi-saturation, the carrier velocity in drift will reach saturation. Since the temperature coefficient of saturation velocity is smaller than that of mobility [4], the $\Delta g_m/\Delta T$ in quasi-saturation region will become smaller. For high-drift-dose device, $\Delta g_m/\Delta T$ is less changed (-0.26 to -0.21 %/ºC) when the device operates from medium gate voltages to high gate voltages.

B. f_T and f_{max}

After de-embedding the parasitic pad effects from measured S-parameters, the ac current gain (H_{21}) and unilateral power gain (U) were calculated to extract f_T and f_{max}, respectively. The extracted f_T and f_{max} of LDMOS with different n-well drift doses are shown in Fig. 4. The temperature coefficients of cutoff frequency ($\Delta f_T/\Delta T$) at V_{GS}=2 V are -0.22 and -0.23%/ºC, respectively, for device with 2×10^{12} and 4×10^{12} cm^{-2} drift doses. These values close to the $\Delta g_m/\Delta T$. Besides we found that the gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}) are nearly unchanged by the temperatures [9]. For LDMOS, the drain resistance is an important component and has to be taken into account in the expression of the cutoff frequency [10]

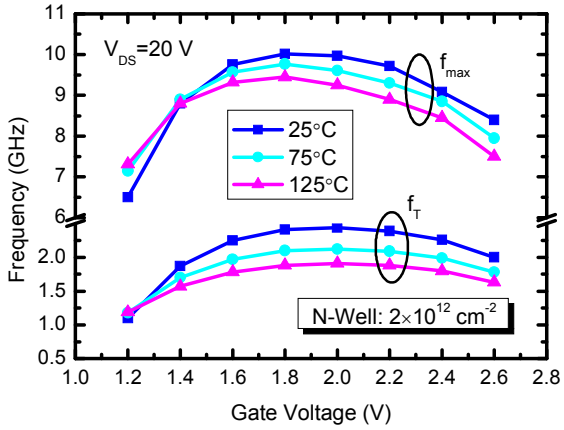
$$f_T = \frac{g_m}{2\pi\left\{\left(C_{gs}+C_{gd}\right)\left[1+g_{ds}\left(R_s+R_d\right)\right]+C_{gd}g_m\left(R_s+R_d\right)\right\}}, \quad (1)$$

where g_{ds} is the channel conductance, R_s is the source resistance and R_d is the drain resistance containing the drift resistance and drain contact resistance. Therefore, the temperature behavior of f_T is mainly influenced by g_m.

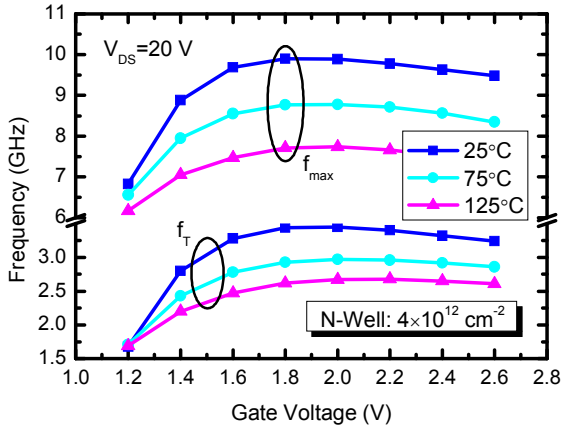
For high-drift-dose device, the temperature coefficient of maximum oscillation frequency ($\Delta f_{max}/\Delta T$) at V_{GS}=2 V is -0.22%/ºC. The f_{max} is expressed approximately as [10]

$$f_{\max} = \frac{f_T}{\sqrt{4g_{ds}R_g + 8\pi f_T C_{gd}\left(R_g + \alpha R_d\right)}}, \quad (2)$$

where R_g is the gate resistance and α is the ratio of drain capacitance (C_{dd}) to gate capacitance (C_{gg}). Similar temperature coefficients of f_{max} and f_T indicate that the variation of f_T with temperature in the denominator is cancelled by those of R_g and R_d.

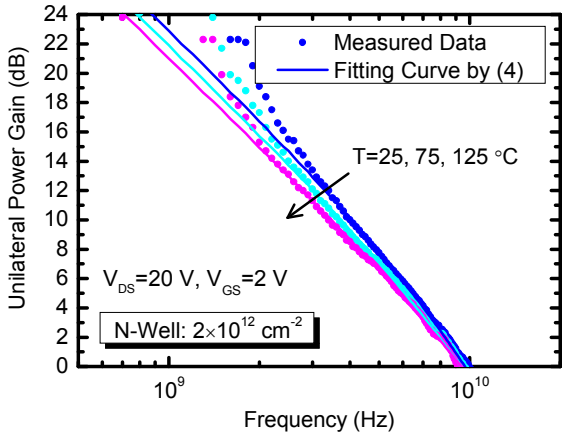


(a)

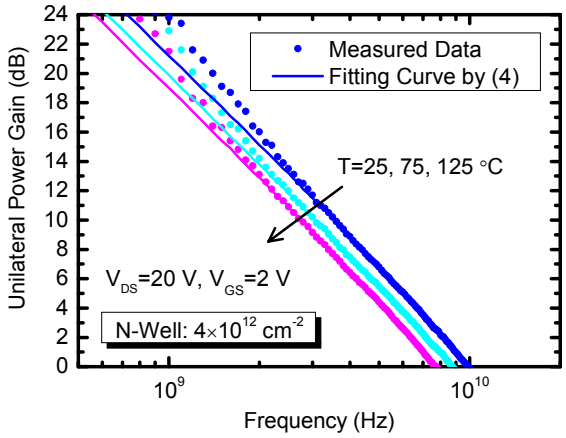


(b)

Fig. 4. Cutoff frequency and maximum oscillation frequency of LDMOS with drift doses of (a) 2×10^{12} and (b) 4×10^{12} cm^{-2}.



(a)



(b)

Fig. 5. Unilateral power gain of LDMOS with drift doses of (a) 2×10^{12} and (b) 4×10^{12} cm^{-2}.

However, we observed that f_{max} of the low-drift-dose device is less dependent on the temperature compared to f_T. The $\Delta f_{max}/\Delta T$ at V_{GS}=2 V is -0.072%/ºC, which is much lower than $\Delta f_T/\Delta T$. Because the device operates near the quasi-saturation region, as illustrated in Fig. 2(a), the temperature sensitivity of drift resistance might become less. According to (2), when R_g is negligible compared to αR_d and the temperature coefficient of R_d is lower than $\Delta f_T/\Delta T$, $\Delta f_{max}/\Delta T$ will be lower than $\Delta f_T/\Delta T$. However, $\Delta f_{max}/\Delta T$ should be higher than $0.5\times(\Delta f_T/\Delta T)$, which is not correspondent with the experimental results. Hence the low $\Delta f_{max}/\Delta T$ in low-drift-dose device cannot be explained adequately by using (2). For this reason, we consider a 4th-order frequency term in the derivation of unilateral power gain to demonstrate this phenomenon.

B. Unilateral Power Gain

Fig. 5 shows the unilateral power gain of LDMOS with different drift doses. The slope of the gain versus frequency decreases with increasing temperature for device with 2×10^{12} cm^{-2} drift dose, while it is nearly unchanged for device with 4×10^{12} cm^{-2} drift dose. As a result, thought they have similar temperature coefficient of power gain ($\Delta U/\Delta T$) at low frequencies (f<2 GHz), the $\Delta U/\Delta T$ of the low-drift-dose device is much lower than that of the high-drift-dose device at high frequencies. By analyzing the unilateral gain in terms of the admittance parameters of the two-port

$$U = \frac{\left|Y_{21} - Y_{12}\right|^2}{4\left[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{21})\mathrm{Re}(Y_{12})\right]}, \quad (3)$$

and considering the 4th-order frequency term, we derived the relation of U and small-signal model parameters as

$$U = \frac{f_T^2 / f^2}{4g_{ds}R_g + 8\pi f_T C_{gd}\left(R_g + \alpha R_d\right) + A\cdot(2\pi f)^2}, \quad (4)$$

where

$$A = 4R_g R_d C_{dd}^2 + 8\pi f_T C_{gd}\left(R_g + \alpha R_d\right)\left(R_d C_{dd}\right)^2. \quad (5)$$

When neglecting the third term in the denominator, we can obtain f_{max} formulation as (2) in the condition of U=1. Owing to the effect of 4th-order frequency term in (4), the slope of power gain versus frequency could be higher than -20 dB/decade at high frequencies. For device with a large R_d, U could be simplified as

$$U = \frac{f_T / f^2}{8\pi C_{gd}\left(R_g + \alpha R_d\right)\left[1 + (2\pi R_d C_{dd} f)^2\right]}. \quad (6)$$

Therefore, when the cutoff frequency decreases more rapidly than the increase of the drift resistance with increasing temperature, the curve slope of the power gain will decrease. In addition, $\Delta f_{max}/\Delta T$ might be between $0.5\times(\Delta f_T/\Delta T)$ and $0.25\times(\Delta f_T/\Delta T)$ for device with low temperature coefficient of R_d, as illustrated in Fig. 4(a).

IV. Conclusion

Effects of drift region resistance on the temperature behaviors of RF power LDMOS transistors were investigated. For low-drift-dose device, $\Delta g_m/\Delta T$ is reduced when device operation enters quasi-saturation region. Moreover, its $\Delta f_{max}/\Delta T$ is much lower than $\Delta f_T/\Delta T$ and $\Delta g_m/\Delta T$. For high-drift dose device, $\Delta f_{max}/\Delta T$ and $\Delta f_T/\Delta T$ are similar and close to $\Delta g_m/\Delta T$. The different temperature behaviors between low- and high-drift-dose devices can be explained by the effects of drift resistance through a power gain expression with 4th-order frequency term. The present analysis is helpful for designing less temperature-sensitive RF LDMOS and power integrated circuits.

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