A Fully Digital PWM-based 1 to 3 GHz Multistandard Transmitter in 40-nm CMOS

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***Abstract*—A fully digital 1 to 3 GHz multimode transmitter is presented which contains two RF modulators: One uses baseband (BB) PWM, while the other uses RF PWM. RF PWM produces less harmonics, while BB PWM has a higher dynamic range (DR) and consumes less power. The BB PWM system satisfies the WLAN EVM limit over the whole frequency range. The RF PWM system achieves sufficient EVM for standards such as EDGE and WCDMA. Both systems support the use of multiple PAs to extend the DR using multilevel PWM.**

***Index Terms*—CMOS integrated circuits, delay lines, digital integrated circuits, OFDM, PWM, RF signals**

I. Introduction

Fully digital transmitters based on switching power amplifiers (PAs) are gaining popularity thanks to the high efficiency of these PAs and the flexibility and beneficial scaling laws of digital hardware. However, in order to implement amplitude modulation (AM) using a switching PA, the amplitude needs to be encoded into a high-speed single-bit signal.

In [1], a fully digital transmitter was proposed which uses digital delay lines to implement phase modulation (PM) and pulse width modulation (PWM) with resolutions in the order of 10 ps. The PWM signal is created in baseband and then multiplied with the phase-modulated square-wave carrier. This is known as *baseband PWM* (BB PWM). This principle was shown to give good results in terms of error vector magnitude (EVM) and dynamic range (DR), but has the disadvantage of producing large harmonic distortion peaks close to the signal band. This imposes severe specifications on the output bandpass filter in order to meet spectral mask requirements.

An interesting alternative, known as *RF PWM* [2]–[4], consists of modulating the pulse width of the RF carrier pulses themselves instead of multiplying the carrier with a PWM signal. This technique only produces odd-order carrier harmonics, which are much easier to filter away. However, it is only suitable for signals with moderate peak-to-average power ratios (PAPR) [4].

Many modern CMOS transmitters [5], [6] employ multiple PAs with a power combiner in order to achieve sufficient output power. In this case, these PAs can be used to implement *multilevel PWM* by driving one PA with a PWM signal and additional PAs with a full-power signal that has only PM and no AM. This greatly extends the DR of the transmitter and allows using RF PWM for high-PAPR signals. Furthermore, the possibilities for power control are enhanced.

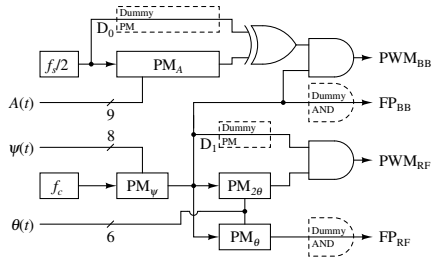

Fig. 1. System architecture

This paper presents a fully digital modulator that can produce both BB and RF PWM signals at carrier frequencies ranging from 1 to 3 GHz. This allows a good comparison between both principles. The presented system supports using both types of PWM with a multilevel PA. For this purpose, it has two outputs: a full-power (FP) output with only PM, and a PWM output with both PM and PWM.

In [3], the RF PWM signal is implemented using analog circuitry. Reference [4] proposes an outphasing implementation which combines two phase-modulated square waves, but does not go into detail about how these square waves are realized. In this work, the outphasing scheme from [4] is adopted but digital delay lines are used to generate all the required signals in a way similar to [1]. This way, a fully digital RF PWM modulator with ps accuracy is realized.

Section II gives an overview of the high-level system architecture. Section III discusses some circuit-level implementation aspects. Measurement results are given in Section IV, and Section V concludes the paper.

II. System Architecture

Fig. 1 shows an overview of the system architecture. It consists of four digital phase modulators (PMs), which are described in more detail in Section III, two dummy PMs D_0 and D_1, and some simple digital gates. Each PM has a square wave input and a multibit digital input which

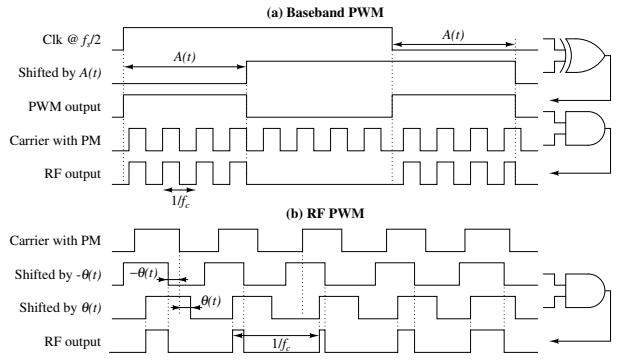

Fig. 2. PWM generation principle for BB and RF PWM

determines the amount by which the square wave input is delayed. The system produces a PWM and a FP output for either BB or RF PWM. Two multiplexers (not shown) select either the BB or the RF PWM outputs.

To simplify the figure, all signals are drawn as single wires. However, in reality, all RF signals (i.e. the path from the f_c input to all outputs) are implemented differentially.

A. Baseband PWM

The BB PWM system is based on the same principle as the system presented in [1] but achieves better resolution through its implementation in 40-nm CMOS. The PWM pulses occur at a frequency f_s which is an order of magnitude lower than the carrier frequency f_c. The BB PWM system uses only the phase modulators PM_A and PM_ψ; the others are switched off. PM_ψ is used to phase-modulate the carrier at f_c. The digital input $\psi(t)$ is equal to the desired carrier phase $\varphi(t)$. PM_A is used to delay a reference square wave with frequency $f_s/2$ by an amount determined by the desired amplitude $A(t)$. Combining the input and output of PM_A in an XOR gate produces a PWM signal at frequency f_s as shown in Fig. 2(a). This signal is then multiplied with the carrier using an AND gate.

Since the phase modulators have a constant delay in addition to the desired variable delay, the dummy phase modulator D_0 is added to match the delay of PM_A.

Linear cross point estimation (CPE) [7] is applied to $A(t)$ before applying it to PM_A to avoid in-band distortion which arises from using digital PWM implementations [1].

B. RF PWM

The RF PWM system uses all phase modulators except PM_A, which is turned off. It is based on the outphasing principle explained in [4]: If two square waves with frequency f_c are phase-modulated with phases $\varphi(t) + \theta(t)$ and $\varphi(t) - \theta(t)$, respectively, and then combined in an AND gate, the resulting signal is a square wave with phase $\varphi(t)$ and a duty cycle $d(t) = 1/2 - \theta(t)/\pi$, as shown in Fig. 2(b). The fundamental component of this signal is a modulated sinusoid with frequency f_c, phase $\varphi(t)$ and amplitude $A(t) = \cos\theta(t)$ [4]. Thus, $\theta(t)$ can be limited to the range $0 \leq \theta(t) \leq \pi/2$.

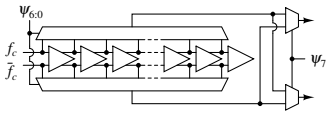

Fig. 3. Implementation of phase modulator PM_ψ

Since the phase modulators used in this work cannot apply a negative phase, PM_ψ is used to generate the phase $\psi(t) = \varphi(t) - \theta(t)$. The phase $\varphi(t) + \theta(t)$ is generated from this signal by adding a phase $2\theta(t)$ using the phase modulator $\text{PM}_{2\theta}$. The dummy phase modulator D_0 adds zero phase and serves only to match the delay of $\text{PM}_{2\theta}$. Finally, the phase modulator PM_θ is used to produce the FP output with phase $\varphi(t)$ and maximal amplitude.

The amplitude signal $A(t)$ needs to be converted to $\theta(t)$ using an arccosine function. Furthermore, due to unequal delays for rising and falling edges, pulse shrinking appears which causes the produced RF PWM pulses to be about 50 ps shorter than intended. Therefore, the arccosine transformation was combined with a linear mapping to compensate for this. This mapping is applied off-chip.

III. Implementation Details

A. Delay lines

Each PM is implemented using a differential delay line connected to one or two multiplexers as in [1]. Fig. 3 shows the implementation of PM_ψ. The total delay of the delay line is calibrated (see Section III-B) to match half a carrier period, which allows realizing phases from 0 to π depending on the least significant bits (LSBs) of the input $\psi_{6:0}$. Since the delay line is differential, phases from π to 2π can be achieved by interchanging both output signals. This is done by two small multiplexers at the outputs, which are controlled by the most significant bit (MSB) ψ_7. PM_θ and $\text{PM}_{2\theta}$ are identical but do not have the output multiplexers, since $2\theta(t) \leq \pi$.

The delay elements in PM_ψ, PM_θ, and $\text{PM}_{2\theta}$ are implemented as in [1] but achieve a unit delay around 8 ps thanks to technology scaling. This resolution is enhanced to 4 ps using resistive interpolation [1], [8]. PM_A is implemented in a way similar to PM_ψ, but since the output signal does not need to be differential, the multiplexer on one side is replaced by a dummy load. The delay elements are slower and smaller in area and achieve a unit delay around 16 ps. Nevertheless, since $f_s \ll f_c$, more quantization steps are available for $A(t)$ than for $\psi(t)$ so that the multiplexer now has 9 input bits. This explains why BB PWM offers a better DR: in this case, 9 amplitude bits are available compared to only 6 for RF PWM. Since the reference input has frequency $f_s/2$, the total delay line also needs to span half a period of the input signal.

B. Delay matching and locking

Since the paths from the f_c and $f_s/2$ inputs to the outputs are completely unclocked (as this would require clocking

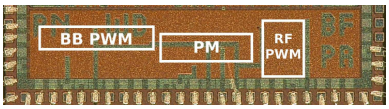

Fig. 4. Chip photograph (2.7 mm × 0.7 mm)

at $1/(4\text{ ps}) = 250$ GHz), delay matching between different paths is very important. For this reason, many dummy components are included on the chip, and the layout was made with much attention to symmetry. Furthermore, all components on these paths were made larger than minimal in order to reduce delay mismatch. In particular the delay elements are sized up, since their mismatch accumulates along the delay lines.

In order to overcome process variations and to adapt the delays to match different carrier frequencies, the delay lines are locked to a reference square wave input by changing their supply voltage. In the BB PWM mode, when $A(t)$ is set to 1, the PWM output should have a 100% duty cycle, i.e. it should be constant and equal to 1. If the delays are either too short or too long, this will result in shorter duty cycles and thus a lower DC value. Thus, this delay line can be locked by measuring the DC value or the duty cycle of the PWM output (this is done off-chip) and changing the supply voltage until this value is maximal.

The other delay lines are locked based on the same principle: An XOR gate was added to each delay line in order to produce a PWM signal suitable for locking. Locking is performed during an initial calibration phase, after which the voltages are fixed and the chip goes into normal operation.

C. Multistandard support

In order to implement a multistandard transmitter, f_c and f_s need to be variable. Since changing the supply voltage does not provide a very large tuning range for the unit delays, the number of delay elements that is used varies with f_c and f_s: The higher the frequency, the shorter the period that should be covered by a delay line, and thus the lower the number of delay lines that are used. This results in quantization noise that increases with f_c and f_s, so that the EVM is best at low frequencies [1], [9].

IV. Measurement Results

The system was implemented in 40-nm general-purpose CMOS. The chip is shown in Fig. 4. It has a total area of 2.7 mm × 0.7 mm with a core area of about 0.35 mm^2.

A. Baseband PWM

The BB PWM system was measured using 64-QAM OFDM signals generated according to the WLAN standard with 5 and 20 MHz channel spacing and a PAPR of 10.8 dB, centered at different carrier frequencies f_c ranging from 1 to 3 GHz. The ratio f_c/f_s was taken to be at least 10 in order to maintain good PA efficiency [1], but never exactly 10 in order to prevent intermodulation products

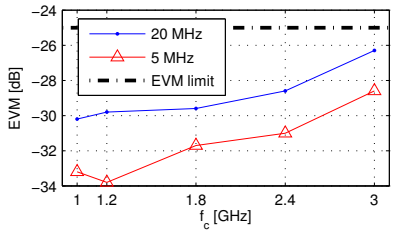

Fig. 5. EVM for WLAN signals with different channel spacing in BB PWM mode

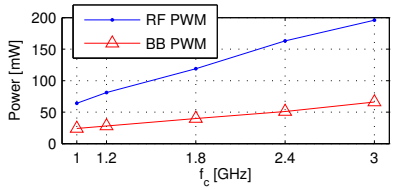

Fig. 6. Power consumption in BB and RF PWM mode. The BB PWM power was measured with 20-MHz WLAN signals, while the RF PWM power was measured with 20-MHz 16-QAM signals. However, the power consumption is dominated by the RF carrier and the dependence on signal type and bandwidth is negligible.

from the PWM harmonics and the carrier harmonics from falling into the signal band [1], [9].

Fig. 5 shows the resulting error vector magnitude (EVM) values, which increase with f_c as predicted in Section III-C. Clearly, the system meets the EVM specification of –25 dB imposed by the WLAN standard over the full f_c range.

Fig. 6 shows the power consumption of the chip. Since the power is dominated by the RF carrier going through PM_ψ and subsequent blocks, it increases linearly with f_c.

B. RF PWM

Since the RF PWM system is intended to process signals with lower PAPR, it was first measured using single carrier QPSK, 16-QAM, and 64-QAM signals which have a PAPR of 5.0, 6.9, and 6.8 dB, respectively. They are centered at the same carrier frequencies f_c as for the BB PWM system. Since the carrier and PWM harmonics are now the same, there is no intermodulation and f_c/f_s can be an integer. In the measurements presented here, $f_c/f_s = 4$.

Fig. 7 shows the resulting EVM for signals with symbol rates of 5 and 20 MHz. As in the BB PWM case, the EVM increases with f_c due to increasing quantization noise. However, the quantization noise is now higher since the number of quantization levels for $\theta(t)$ is much lower than for $A(t)$ as explained in Section III-A, and is further reduced by the pulse shrinking. Furthermore, since the pulses are much shorter than for BB PWM, they are much more sensitive to circuit-level effects such as mismatch, jitter and supply and ground noise. Nevertheless, the achieved EVM values are sufficient for many communication standards such as WCDMA and GSM/EDGE, which have EVM limits of –15.1 and –20.9 dB, respectively [10]. Furthermore,

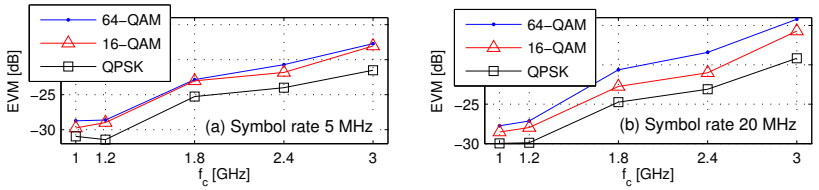

Fig. 7. EVM for single-carrier signals with (a) 5-MHz and (b) 20-MHz symbol rate in RF PWM mode

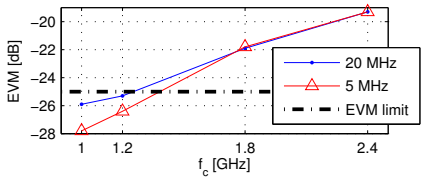

Fig. 8. EVM for WLAN signals with different channel spacing in RF PWM mode

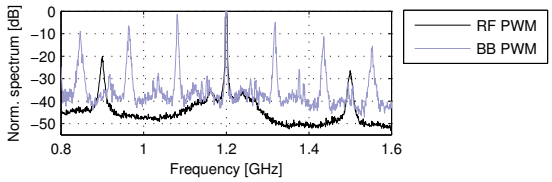

Fig. 9. Output spectra for a 5-MHz 64-QAM WLAN signal centered at 1.2 GHz for baseband and RF PWM. The resolution bandwidth is 20 kHz.

if the RF PWM system is combined with multiple PAs to implement multilevel PWM, the EVM can be significantly improved by extending the DR.

The RF PWM system was also tested with the WLAN signals used in Section IV-A, which have a PAPR of 10.8 dB. The resulting EVM is shown in Fig. 8. The plot shows that the RF PWM system even satisfies the WLAN specification for f_c up to 1.2 GHz. At higher f_c, the EVM is 3 to 6 dB too high, which suggests that a multilevel implementation with 2 or 3 PAs should be able to meet the specification also at higher f_c.

Fig. 6 shows the power consumption of the RF PWM system. It also increases linearly with f_c but it is significantly higher than for BB PWM as the RF carrier now goes through three phase modulators PM_ψ, PM_θ, and $\text{PM}_{2\theta}$.

Fig. 9 shows the output spectra of the RF and BB PWM modulators for a 5-MHz WLAN signal centered at 1.2 GHz. The BB PWM spectrum clearly shows the PWM harmonics at $f_c + nf_s$, where n is any nonzero integer and $f_s = f_c/10.2 = 118$ MHz. The smaller peaks in between are intermodulation products at $-f_c + nf_s$ and $3f_c + nf_s$ [1], [9]. The RF PWM spectrum shows harmonics caused by sampling the signal at $f_s = f_c/4 = 300$ MHz. These are much lower and further away than the PWM harmonics and therefore easier to filter away. They can be completely removed by setting $f_s = f_c$ at the expense of increased power consumption.

V. Conclusion

A fully digital multistandard transmitter was presented, which includes a BB PWM and an RF PWM modulator, which allows trading off spectral shape versus DR and power consumption. Both transmitters support carrier frequencies from 1 to 3 GHz and achieve good results for different bandwidths and modulation schemes. The BB PWM transmitter satisfies the WLAN EVM limit over the full frequency range; the RF PWM transmitter achieves sufficient EVM for standards with lower PAPR, such as GSM/EDGE and WCDMA. Both modulators were designed to implement multilevel PWM in combination with a power combining PA. This will further extend the DR and allow producing signals with higher PAPR. Comparison of the resolution and EVM results with [1] proves the beneficial scaling of the proposed type of digital transmitters.

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