A Current-Mode mm-Wave Direct-Conversion Receiver with 7.5GHz Bandwidth, 3.8dB Minimum Noise-Figure and +1dBm $P_{1dB,out}$ Linearity for High Data Rate Communications

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***Abstract* — A current-mode mm-wave direct-conversion receiver breaking trade-offs among bandwidth, NF and linearity is designed and realized in 65nm CMOS. The 60GHz receiver employs novel Frequency-staggered Series Resonance Common Source (FSRCS) stage to extend RF bandwidth with superior noise performance. The receiver's current-mode operation offers excellent out-of-band blocker tolerance and linearity. With on-chip quadrature LO generations, the fabricated receiver simultaneously achieves minimal noise figure of 3.8dB, RF bandwidth of 7.5GHz, output P1dB of 1dBm, maximum conversion gain of 32dB, and IRR of -35dB. The receiver is capable of tolerating out-of-channel blocker up to -9dBm at 3.5GHz away. It occupies silicon area of 1.3mm^2 and draws 25.5mA from 1V supply.**

***Index Terms* — mm-Wave, 60GHz, CMOS integrated receiver, Frequency-staggered Series Resonance Common Source, current-mode, blocker tolerant.**

I. Introduction

Multi-Gb/s wireless communications via vastly available mm-wave spectra (60GHz and above) have drawn increasing attention in recent time, yet the receiver (Rx) performance has suffered from limited CMOS device performance, especially when wide bandwidth and high sensitivity/linearity are simultaneously needed for high-order modulated Gb/s digital communications. Recently reported works on 60GHz Rx achieved low noise figure (NF) but lacked in bandwidth coverage (<5% fractional bandwidth) [3], or covered wide bandwidth (>10% fractional bandwidth) but achieved only moderate NF (>5.5dB) [1,2]. Most reported works relied heavily on accumulative voltage gains from multiple LNA stages, which greatly limited Rx's linearity and bandwidth. In addition, out-of-channel but in-band blocker may cause issues for broadband receiving, because it can desensitize the front-end and corrupt the overall Rx performance.

In this work, we present a non-traditional current-mode mm-wave Rx architecture to overcome aforementioned issues. Its prototype is realized in 65nm CMOS for 60GHz ISM band applications. The same architecture however is generally applicable to broadband Rx designs at any other mm-wave frequencies. The prototype Rx is a direct-conversion receiver featuring a Gm Front-end with *Frequency-staggered Series Resonance Common Source* (*FSRCS*) stage to break conventional Rx design trade-offs among the bandwidth, noise and linearity. The prototype Rx is also integrated with an on-chip 60GHz quadrature VCO for ease-of-testing. The resulting prototype achieves optimized NF = 3.8dB, bandwidth = 7.5GHz, $P1dB_{out}$ = +1dBm, and concurrently demonstrates effective out-of-channel blocker tolerance level (marked at 1dB Rx gain compression point) up to -9dBm at 3.5GHz away. In this paper, Section II will present the proposed receiver architecture and details of its each sub-block. Section III will present the tested receiver performance. Section IV will summarize the overall work.

II. Receiver Architecture

The Rx, as shown in Fig. 1, comprises a low noise Gm Front-end tuned to 60GHz, the I/Q passive mixers and the baseband trans-impedance amplifiers (TIAs).

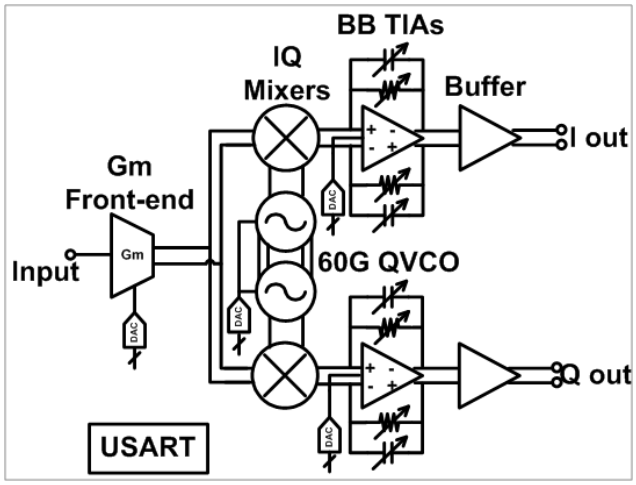


Fig. 1. Block diagram of proposed current-mode broadband mm-wave receiver with integrated QVCO.

A. FSRCS Gm Front-end

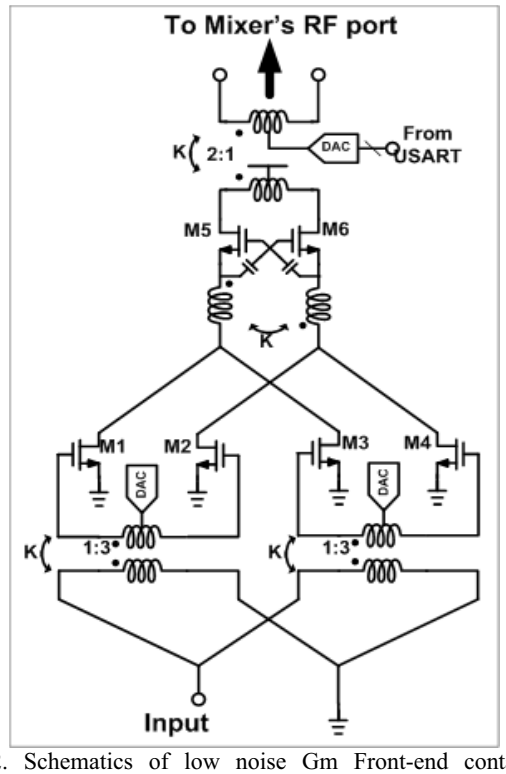


Fig. 2. Schematics of low noise Gm Front-end containing FSRCS stage

The Gm Front-end provides input impedance matching, ESD protection, balun and voltage-to-current conversion. The 1:3 transformers at the input offer passive voltage gain. Afterwards, transformer's secondary coil forms a series resonator with subsequent common source stage to further boost the gain by a factor of resonance Q, which is inversely equal to its fractional bandwidth Δf/f. Since the specific on-chip transformer has Q of 15, it approximately limits Rx bandwidth to 4GHz. In order to broaden this bandwidth to the desired 7GHz, an *FSRCS* stage is implemented as shown in Fig. 2, where two parallel input transformers would resonate with the following common source stages (configured by M1/M2 and M3/M4, respectively) at two staggered frequencies (58GHz and 61.5GHz) with similar passive gains. The additional resonance in *FSRCS* contributes insignificant noise (~0.1dB) based on simulations, primarily due to each of resonators' off-peak filtering effect. The output mm-wave signals are then combined at differential drain nodes in the current domain with expanded 7GHz bandwidth. To reduce the noise, minimize the LO-RF feed-through and improve the front-end stability, M5/M6 cascode devices with differential inductors (between M1/M3 and M5 or between M2/M4 and M6) and push/pull capacitors (between M5-source to M6-gate or M6 -source to M5-gate) are inserted. The Rx current mode front-end can therefore be built by using a single *FSRCS* stage in contrast to conventional multi-stage LNAs.

B. Passive Mixer and TIA

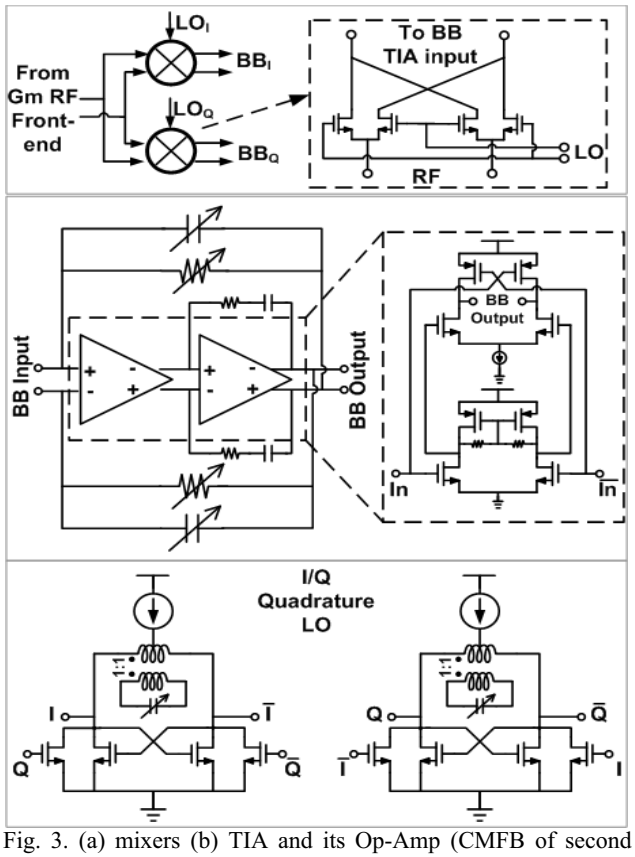


Fig. 3. (a) mixers (b) TIA and its Op-Amp (CMFB of second stage not shown) (c) QVCO schematic (LO buffer not shown).

The front-end output current is then fed into passive I/Q mixers through a 2:1 transformer which offers passive current gain. Current driven passive mixer is used to achieve high linearity in frequency down-conversion, lower 1/f noise and reciprocal impedance up-conversion. Afterwards, I/Q TIAs transfer the down-converted signal current back to voltage. Each of these TIAs employs wideband two-stage differential Op-Amps with resistive feedback. The TIA has low input impedance (≈50Ω at the highest gain setting). Such low impedance is consequently up-converted back to the front-end via the passive mixer to draw the signal current from the Gm stage. The low impedance seen into the mixer has two extra advantages: (1) it further extends Rx's bandwidth by de-Q-ing the transformer tank located between the Gm Front-end and the passive mixer; (2) it does not amplify signal swing but only passes the current until the blocker is filtered out at TIA's output [6]. Strong blocker current can be filtered out by the feedback capacitor in TIA.

Shown in Fig. 3(b), TIA's first stage is biased close to transistor's sub-threshold to maximize its g_m/Id. Its second stage is configured with feed-forward and Miller compensation to ensure stability. This TIA has a simulated input referred noise less than 1.6nV/√Hz, gain of 35dB, and GBW product of 3.2GHz. Note that Rx's baseband bandwidth is determined by the closed loop TIA rather than Op-Amp. It is set as the channel bandwidth. The Rx gain can be varied by adjusting TIA's feedback resistance.

C. 60GHz Quadrature VCO and Control ASIC

The passive mixer is driven by an on-chip 60GHz LC-QVCO with cross-coupled NMOS differential pair shown in Fig. 3(c). The LO frequency is tuned by MOS varactors. The I/Q LO distribution is routed as symmetrical as possible to minimize I/Q mismatch. LO buffers are inserted between QVCO and mixer. Both receiver and QVCO are digitally controlled by on-chip DACs. They set the bias for Rx stages and QVCO for frequency tuning and current control. Each control DAC has an 8-bit R2R architecture with small area. They are driven from an external PC through on-chip serial-to-parallel interface (USART).

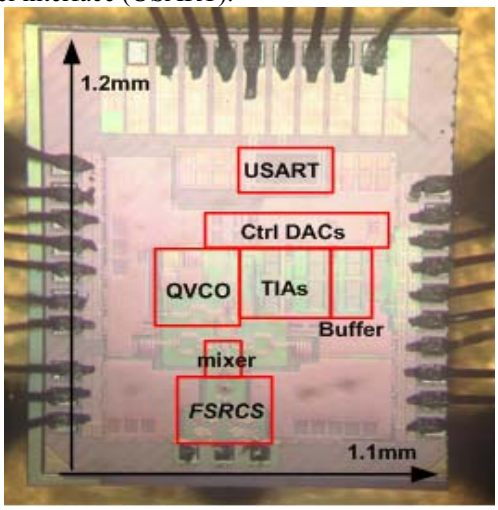


Fig. 4. Receiver die-photo

III. Measurement Results

Figure 4 shows the 65nm CMOS Rx prototype. Fig. 5 plots conversion gain, NF, and input matching versus mm-Wave frequencies. The peak gain is 36dB with 3dB bandwidth >7.5GHz (>12.5% fractional bandwidth). The on-chip QVCO provides LO for Rx and has a 15.06% frequency tuning range from 54.8GHz to 63.8GHz. NF is measured using a V-band noise source with the Y-factor method. The minimum NF is 3.8dB after de-embedding out the input cable and probe losses. The return loss shows a good input matching (<-10dB from 57GHz to 63GHz).

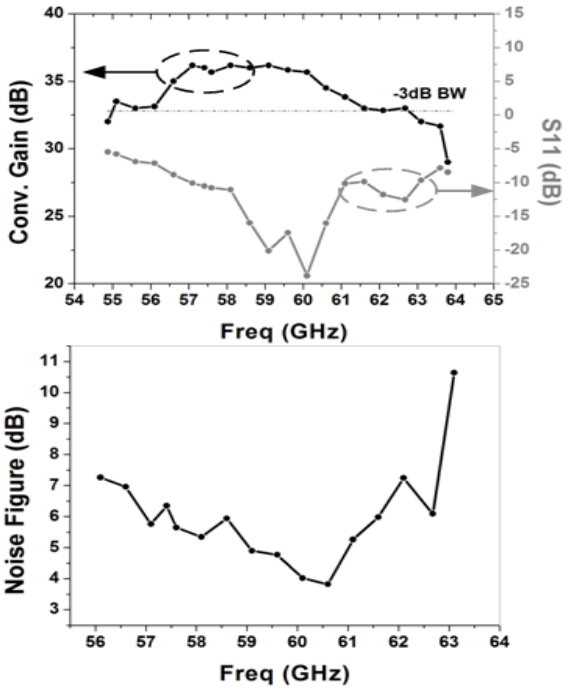


Fig. 5. Measured conversion gain, return loss and noise figure of the receiver versus RF frequency

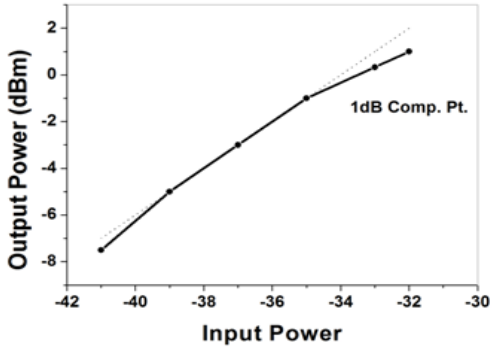
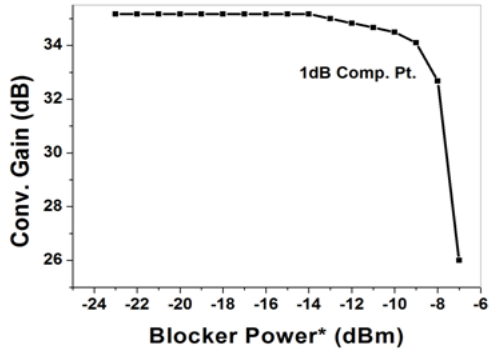


Fig. 6. Measured gain compression (output P1dB) of the receiver

Gain compression is tested to characterize Rx's linearity. The input P_{1dB} is –35dBm at high gain setting (36dB) and –18dBm at low gain setting (17dB). The output non-linearity must also meet the EVM requirement for required modulation schemes while not substantially backing off from ADC's full input scale. The tested output P_{1dB} is +1dBm. As shown in Fig. 7, gain compression with out-of-channel blocker is also measured with Rx signal gain compressed by 1dB in the presence of a -9dBm blocker located 3.5GHz away (-54dBm input signal at 57GHz, blocker at 60.5GHz). Fig. 8(a) shows that the I/Q amplitude and phase mismatches are 0.15dB and 1.62 degrees, respectively, indicating an IRR of -35dB. The measured feed-through from the LO to the RF input is -59dBm. A stand-alone QVCO is also fabricated for characterization. Its free-running phase noise is -91dBc/Hz

at 1MHz offset from 61GHz, Fig. 8(b). The Rx core consumes total power of 25.5mW: the Gm front-end draws 7.5mW, each TIA draws 9mW. QVCO and LO buffer draw 72mW. The die occupies 1.3mm^2 silicon area including pads.



*** Desired signal at 57GHz with input power of -54dBm, blocker at 60.5GHz**

Fig. 7. Measured blocker gain compression of the receiver

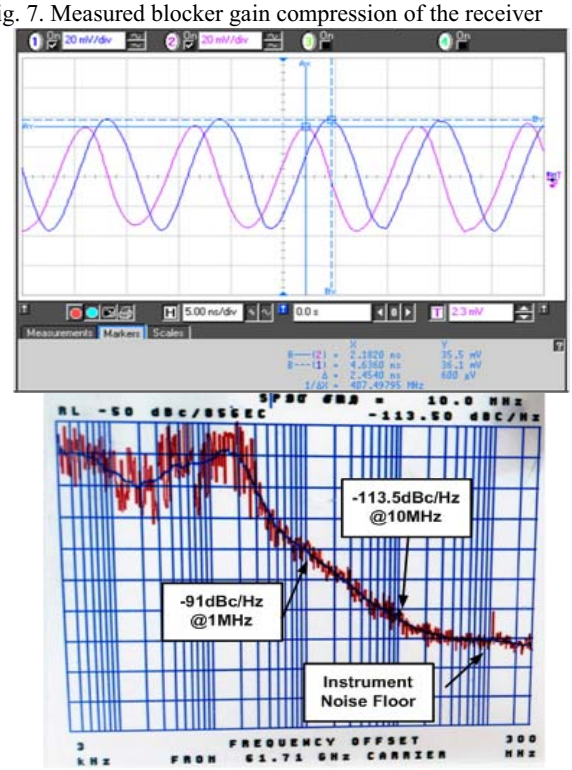


Fig. 8. (a) Measured output I/Q waveform of the receiver; (b) measured phase noise of the 60GHz QVCO

IV. Conclusion

This work realizes a highly integrated broadband low noise high linearity V-band receiver. Compared with other recently published wideband receivers with >7GHz bandwidth [1,2], our prototype simultaneously achieves the best NF=3.8dB, $P_{1dB,in}$=-18dBm and $P_{1dB,out}$=1dBm among state-of-the-arts. It also tolerates out-of-channel blocker up to -9dBm at 3.5GHz away. It consumes less power and silicon area than prior arts. The proposed current-mode architecture is also generally applicable to mm-wave wideband receivers.

TABLE I
COMPARISON OF STATE-OF-THE-ART

	This Work	ISSCC 2012 [1]	ISSCC 2010 [2]	RFIC 2011 [3]	ISSCC 2011 [4]	ISSCC 2011 [5]
Gain [dB]	36	30	35.5	60	17.3	41
Minimum NF [dB]	3.8	5.5	5.6	4	6.8	7.6
$P_{1dB,in}$ [dBm]	-18	-31	-21	-33	N./A.	-29
$P_{1dB,out}$ [dBm]	+1	-1	-3.5	-5	N./A.	-1
RF BW [GHz]	7.5	10	13	1.5	<4	<5
$P_{1dB,blocker}$ [dBm]*	-9	N./A.	N./A.	N./A.	N./A.	N./A.
I/Q Mismatch/IRR [dB/deg/dB]	0.15/1.6/ -35	N.A./N.A./ -30	N.A./3/ N.A.	N./A.	N./A.	N./A.
VCO Phase Noise [dBc/Hz]**	-91	-79	-90	N./A.	-85	N./A.
Technology	65nm CMOS	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Rx Power [mW]	25***/ 53.5	35	40	20***/34	81.5	74
Area [mm^2]	1.3	N./A.	2.4	1.1****	8	N./A.

***Defined as "input power of an out-of-band blocker located at 3.5GHz offset that causes the desired signal gain to compress by 1dB"**
**** VCO Free-running, at 1MHz off set**
***** Excluding output buffer**
****** No on-chip LO generation**

Acknowledgement

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