A Linear-in-dB Analog Baseband Circuit for Low Power 60GHz Receiver in Standard 65nm CMOS

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***Abstract* - This paper presents an analog baseband (ABB) circuit for low power 60 GHz wireless receiver in standard 65 nm CMOS. The proposed analog baseband system combines variable gain amplifiers (VGA) with a 3rd-order type II Chebyshev filter and provides linear steps as well as filter tuning range to achieve sufficient out-of-band rejection. The ABB demonstrates 2 dB gain step tuning range from 3 – 31 dB, 3-dB bandwidth of 980 MHz, OP1dB of 0dBm, and noise figure of 6 dB to 21 dB. The ABB consumes 48 mW at max gain setting and 32 mW at minimum gain setting from a 1.1 V supply. The entire ABB occupies an area of 1.1 mm^2 with active area of 0.2 mm^2.**

***Index Terms* - Analog, baseband, Chebyshev filter, variable gain amplifier**

I. INTRODUCTION

Use of the ISM band at 60 GHz has been widely discussed in the literature [1-5]. Phased array systems have been proposed for increased range however, this comes with increased die size, system cost, and power consumption. Systems using a single antenna have been demonstrated [5]. Such systems, while limited in range, offer the opportunity for low power consumption and extremely high energy efficiency (low energy per bit).

Fig.1 shows the block diagram of a direct conversion receiver system, which offers the opportunity for reduced complexity and die size. An ABB with a large gain-control range, dc offset correction, channel selection filtering and low power consumption is highly desired. We present an ABB with programmable gain tuning for wide dynamic range, and current-mode Chebyshev type II filtering for adjacent and alternate channel selectivity. The proposed architecture and design topology provides robust noise performance and relax the design to achieve precise gain steps with wide range. The use of current-mode design allows for wide bandwidth and is less sensitive to device mismatch. The servo-feedback loop is also implemented in the system to reduce output dc offset to < 10mV at all gain settings with worst-case process mismatch.

The paper is organized as follows, the ABB system architecture and specification is illustrated in Section II and detail circuit design for the essential blocks of the proposed ABB is demonstrated in Section III. Section IV shows the measurement results of the design with a performance comparison. Finally, the paper is concluded with a brief summary in Section V.

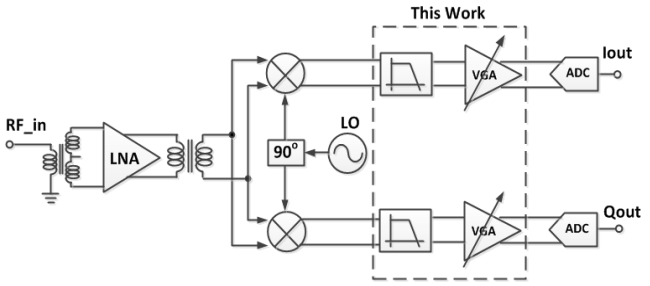


Fig. 1. Block diagram of the low power 60GHz receiver.

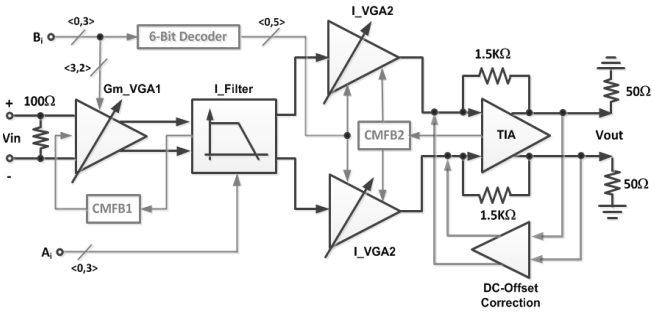


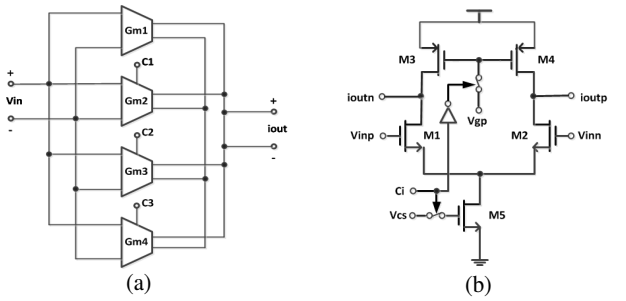
Fig. 2. Block diagram of the proposed baseband section.

II. THE ABB ARCHITECTURE AND SPECIFICATION

The architecture of the proposed analog baseband system is shown in Fig.2. It is composed of four stages which are input stage G_m-cell based coarse-gain-step tuning amplifier (Gm_VGA1), current-mode type II Chebyshev filter, internal stage current-mode fine-gain-step tuning amplifier (I_VGA2), and output stage trans-impedance amplifier (TIA).

A total of 28 dB baseband gain tuning range is needed for the dynamic range of the system. To minimize the mismatch issues, a 2 dB gain tuning step is also required. A coarse VGA with three steps of 6dB each is implemented at the first stage in the system, while the precise gain tuning stage is placed in a following stage. This topology provides for wide and precise gain tuning and low noise figure.

To keep the output DC level small (<10 mV), a DC-offset correction feedback loop is added from the output of the TIA to the input. This method is used instead of AC coupling capacitance to save area and to eliminate the impact of bottom-plate parasitics on the signal-path response. The output common-mode level of the previous stage directly determines the input common-mode level of the next stage. To



(a) (b)

Fig. 3. Gm-VGA1 (a) block diagram, and (b) Gm cell schematic.

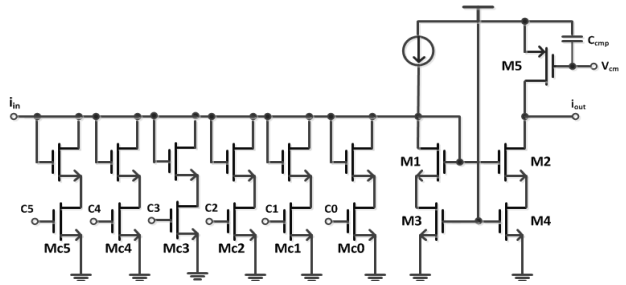


Fig. 4. Current-mode VGA2 schematic.

maintain correct DC operating level, two common-mode feedback circuits are implemented in the system between the I_filter and Gm_VGA1, as well as TIA and I_VGA2 respectively.

For testing purposes, a 100 Ω resistor was placed across the input differentially to achieve matching. Similarly, the output impedance of the TIA is matched to 100 Ω differential.

III. ANALOG BASEBAND DESIGN APPROACH

A. Programmable Variable Gain Amplifiers

Fig.3(a) shows the block diagram of the input stage coarse variable gain transconductance (g_m) amplifier (G_m_VGA1). The amplifier consists of four fixed Gm cells (G_{m1} to G_{m4}) with the size ratio of 1:1:2:4. The G_{m1} cell is always on, with a transconductance value of g_{m1}, and $G_{m2,3,4}$ is turned on based on the digital control bit. The detailed schematic of the Gm cell is shown in Fig.3 (b), which is a simple differential pair with PMOS active load. The digital control bit (C_1, C_2, C_3) turn on/off the PMOS load (M_3/M_4) and source tail transistor (M_5) to determine the gm value. The total G_{mtotal} = 1, 2, 4, 8 x g_{m1} which provides precise 6 dB variable gain step.

Fig.4 shows the schematic of the current-mode variable fine-gain-step tuning amplifier (I_VGA2). The current amplification is done by current-mirror amplifier $M_{1,2,3,4}$. The output current flowing through M_2 /M_4 traces the total current on M_1/M_3 and transistor ratio between M_2/M_1 and M_4/M_3 determines current amplification level. In parallel with M_1/M_3 there are 6 current branches M_{c0} to M_{c5} which

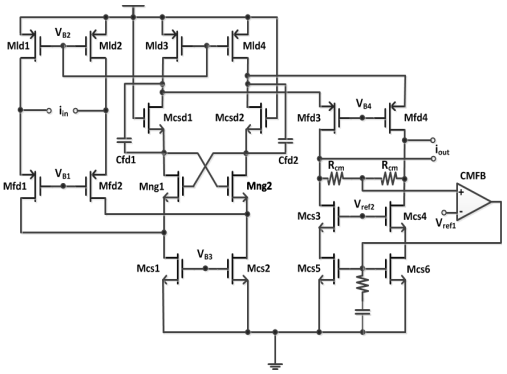


Fig. 5. Current-mode Chebyshev II Filter schematic.

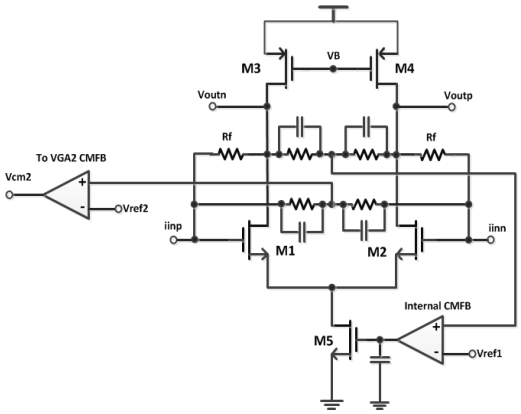


Fig. 6. TIA schematic.

are controlled by digital control bit $C_{0\text{-}5}$. If any of the current branches are turned on, the total current flowing through M_1/M_3 will be reduced by the current flowing to ground in that branch and results in less output current. The amount of the reduced current can be determined by the size of the transistors of M_{c0} to M_{c5}. In general, smaller size of the transistor provides lower gain step, but it causes mismatch and reduces the precision of the gain step. Therefore, the trade-off between gain step resolution and accuracy must be taken into account during the design.

B. Current-mode Chebyshev II Filter

The schematic of the current-mode Chebyshev type II filter is shown in Fig.5. It consists of three parts: first, the folded cascode input stage, internal 3-pole/2-zero filter stage, and folded output stage.

The input stage is a PMOS common-gate current-buffer, which produces low voltage swing at the input and high output impedance. The latter is needed for the filter stage to perform properly. The filter stage is designed with cross-coupled feedback and cascading as previously proposed in a lower-speed application [6]. The use of NMOS cascode is required in order to maintain good g_m matching between cascode devices ($M_{CSd1/2}$) and lower devices ($M_{ng1/2}$). This is necessary to keep the positive feedback loop gain < 1 for sta-

bility. The positive feedback enhances the quality factor of the poles. Feed-forward capacitors $C_{fd1,2}$ add complex zeros in the transfer function for improved selectivity. MOSFET parasitic capacitances form the 3 poles of the transfer function. The output stage also uses a folded common-gate stage to maintain low impedance on the drain of $M_{CSD1,2}$ and high output impedance to drive VGA2.

The common-mode feedback circuitry uses a pair of 20 KΩ resistors to stabilize the output stage common-mode level of the filter which also determines the DC operating point of the following I_VGA2. Moreover, there are two bias gate voltages $V_{B2}/_4$ which can be digitally tuned by an extra DAC circuitry. By doing so, the current flowing through the filter is adjusted and results in digitally programmable 3-dB bandwidth (BW) as well as the level of notching.

C. Transimpedance Amplifier

Fig.6 shows the schematic of the output stage transimpedance amplifier (TIA). The TIA converts the internal current signal to output voltage, while driving a 100 Ω differential output load. In the actual ABB system implementation, the output load of the TIA is determined by the input impedance of the ADC which could be higher than the standard 100 Ω differential load used for stand-alone testing.

The TIA is formed by a differential pair with a feedback resistor (1.5 KΩ) and a pair of PMOS transistors as active load. A large resistor of 10 KΩ in parallel of 100 fF MOM cap is utilized to keep good track of the common-mode voltage value at both input and output nodes. To maintain the correct common-mode value, two common-mode feedback loops (CMFB) for both input and output are implemented in TIA.

The first CMFB1 is formed by a desired reference voltage 0.85 V (V_{ref1}) from PTAT and CM voltage from TIA output as the inputs of an opamp. The output of the opamp is connected the gate of the transistor M_5 to provide correct DC current flowing through the differential pair of the TIA. The second CMFB2 takes reference voltage 0.51 V (V_{ref2}) and the input DC bias of the TIA as the input, provides the output voltage at the gate of PMOS M_5 in I_ VGA2 as shown in Fig.4. Therefore, the output DC level of the VGA2 is stabilized together with the input DC operation level of the TIA.

IV. MEASUREMENT RESULTS

The proposed receiver analog baseband section was implemented in a standard 65 nm CMOS process and measured by on-wafer probing. The chip micrograph of the circuits is shown in Fig.7 with the total area of 1 mm^2 and the core area of 420 µm by 470 µm. The ABB (I + Q) area without bandgap bias circuitry is 330 µm by 470 µm.

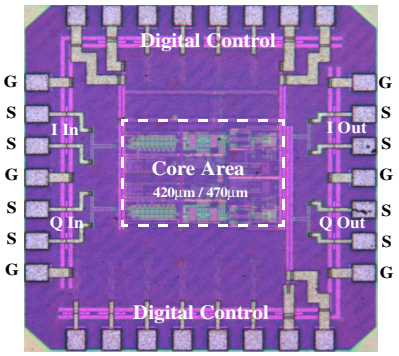


Fig. 7. Chip microphotograph of the design.

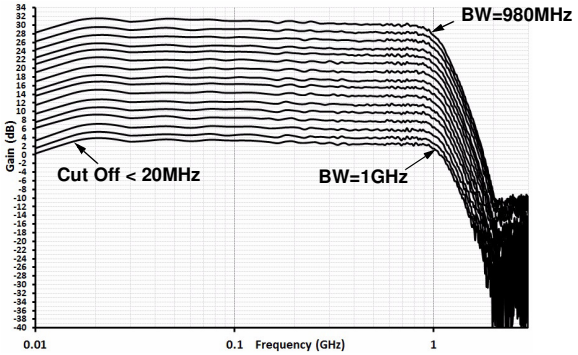


Fig. 8. Measured frequency response vs. gain settings.

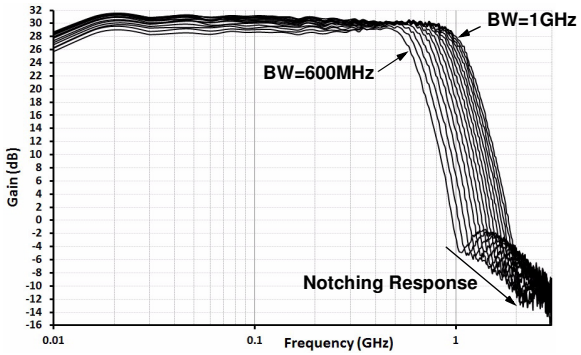


Fig. 9. Measured BW response with various notching settings.

The ABB is first characterized by its small-signal performance. The variable gain capability and the low-pass filtering response are illustrated in Fig.8. The DC gain is programmed between 3 dB up to 31 dB, and with higher 3-dB BW of 980 MHz to 1 GHz respectively. The lower cut-off frequency can be set below 20 MHz to ensure sufficient in-band flatness. The out-of-band injection function provided by the current-mode filter is also verified as there is more than 25 dB attenuation at 1.6 GHz. Fig.9 shows the bandwidth tuning response at max gain setting. The 3-dB BW can be tuned from 600 MHz to 1 GHz, and the notching response tracks the 3-dB BW nicely to ensure sufficient out-of-band rejection.

The DC gain is controlled in the Gm-cell VGA1 with 6 dB coarse gain step and in current-mode VGA2 with 2 dB fine gain. The gain at 100 MHz is utilized to characterize the gain

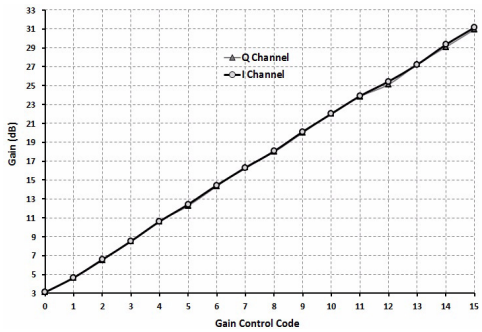


Fig. 10. Measured DC gain vs. digital gain control code.

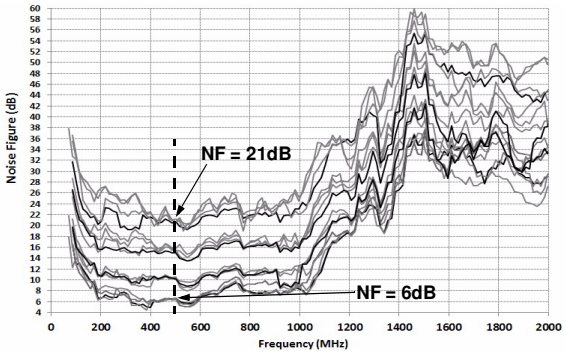


Fig. 11. Measured NF with different gain settings.

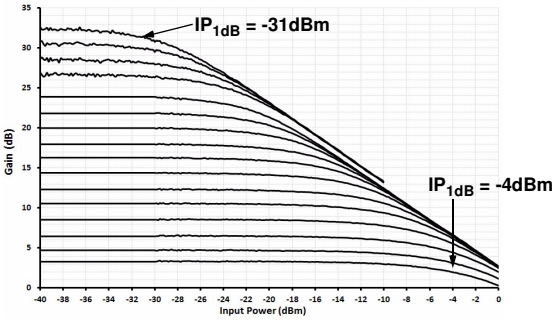


Fig. 12. Measured AM-AM response vs. gain settings.

tuning performance of the VGAs against 4-bit digital control code. Fig.10 shows that the gain of the ABB can be programmed linearly in dB from 3 dB to 31 dB with 2 dB steps. At the max gain setting, a good matching is obtained between I channel and Q channel with the measured mismatch less than 0.25 dB.

To characterize the noise performance of the baseband section, a group of noise figure (NF) versus all gain settings is plotted in Fig.11. A minimum NF of 6 dB with max gain and max NF of 21 dB with minimum gain are obtained at 500 MHz which is at the middle of the bandwidth. It is also learnt from the plots that the NF mainly depends on the coarse gain tuning of the VGA1, which is placed the first stage of the baseband section. The impact on NF from following current-mode VGA2 is less sensitive, which provides robust NF performance over fine gain tuning.

The linearity performance of the ABB is measured as shown in Fig.12. A 100 MHz signal is utilized to measure the IP1dB of the design. The IP_{1dB} of -4 dBm and -31 dBm at minimum and max gain setting respectively with constant OP_{1dB} of 0 dBm are obtained. This gives enough margin for ABB when the signal is strong.

Table I summarizes the performance of the proposed ABB circuit and the recently published designs. The proposed design achieves 28 dB gain tuning with linear-in-dB performance and good NF performance with other competitive performance.

TABLE I COMPARISONS OF RECENT REPORTED FRONT-ENDs

References	[1]	[2]	[3]	[4]	This Work
Frequency (MHz)	1000	970 - 1100	900	915	**980 - 1000**
DC Gain (dB)	0 - 40	10.6 - 30	2 -32	0.1 - 19.6	**3 - 31**
Noise Figure (dB)	N/A	N/A	N/A	20 -35	**6 - 21**
IP1dB (dBm)	N/A	N/A	-18 - -34	-4.4*	**-4 - -31**
Power (mW) (I + Q)	18	30 - 42	24.8	9.5 -10.8	**32 - 48**
Core Area (mm^2)	0.16	0.54	0.24	0.15	**0.2**
Technology	40nm CMOS	40nm CMOS	65nm CMOS	90nm CMOS	**65nm CMOS**

* IP1dB is theoretically calculated from IIP3;

V. CONCLUSION

An ABB section for low power 60 GHz wireless receiver is proposed and implemented in a standard 65 nm CMOS. The ABB achieves 3-dB BW of 980 MHz with gain tuning range from 3 – 31 dB, OP1dB of 0 dBm, and noise figure of 6 dB to 21 dB. The ABB achieves VGA and filtering functionalities simultaneously, which is ideal for integrating with full transceiver system in CMOS.

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REFERENCES

[1] M. Miyahara, et al., “An 84 mW 0.36 mm2 Analog Baseband Circuits for 60GHz Wireless Transceiver in 40 nm CMOS”, IEEE RFIC 2012, pp. 495-498, June 2012.
[2] V. Szortyka, et al., “A 42 mW Wideband Baseband Receiver Section with Beamforming Functionality for 60 GHz Applications in 40nm Low-Power CMOS”, IEEE RFIC 2012, pp. 261-264, June 2012.
[3] M. Hosoya, et al., “A 900-MHz Bandwidth Analog Baseband Circuit with 1-dB Step and 30-dB Gain Dynamic Range”, IEEE EuSSC 2011, pp. 466-469, 2010.
[4] S. D’Amico, et al., “A 9.5 mW Analog Baseband RX Section for 60GHz Communications in 90nm CMOS”, IEEE RFIC 2011, pp. 1-4, June 2011.
[5] A. Matsuzawa, et al., “60GHz Direct Conversion CMOS Transceiver Design”, EDSSC, pp. 1-2, 2011.
[6] A. Liscidini, et al., “A 1.25mW 75dB-SFDR CT Filter with In-Band Noise Reduction”, ISSCC, pp. 336-337, 2009.