# Ultra-Low Phase Noise 7.2-8.7 GHz Clip-and-Restore Oscillator with 191 dBc/Hz FoM

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***Abstract* — In this paper we investigate benefits of a recently introduced clip-and-restore (C&R) oscillator for ultra-low phase noise RF applications and reconsider the original choices in light of further insight into the oscillator behavior. We also tackle undesired resonance frequencies and exploit them to facilitate clipping with proper choices of tuning capacitances. Based on the new theory, the proposed oscillator was implemented in 65-nm CMOS and verified to achieve 4 dB better phase noise and 1.8 dB better FoM than the original C&R oscillator, thus making it the lowest phase noise CMOS oscillator ever published. The measured phase noise is -145 dBc/Hz at a 3 MHz offset from a 4.2 GHz carrier. The resulting average FoM is 191 dBc/Hz and varies less than 2 dB across the tuning range. It covers the 7.2-8.7 GHz frequency band for a 19% tuning range, drawing 32 mA from a 1.3 V power supply.**

## I. Introduction

Phase noise (PN) requirements of a local oscillator (LO) for base-station (BTS) receivers are extremely challenging when attempted in the bulk CMOS technology. These requirements derive from the stringent in-band blocking characteristics and carrier-to-noise specifications of the 3GPP cellular standard. The PN requirements of GSM-900 and DCS-1800 "normal" BTS at 800 kHz offset are -147 dBc/Hz and -138 dBc/Hz, respectively [1]. They are considered the toughest RF specifications of the cellular standards.

The oscillator phase noise (PN) is typically addressed by improving a quality factor (Q) of its LC tank and increasing its power consumption. The Q-factor is usually limited by the inductor due to physical constraints on the width and thickness of the metal and the substrate loss in bulk CMOS. In addition, increasing power consumption stops improving PN when the gm devices enter the triode region. Thus, the traditional CMOS oscillators could not even approach the GSM BTS strict PN requirements. On the other hand, the class-C oscillator [2] achieves high figure-of-merit (FoM) as a result of a better conversion efficiency of the bias-to-fundamental-harmonic current as well as preventing the gm transistors from entering the triode region. However, its output swing constraint limits the lowest achievable PN. The clip-and-restore (C&R) digitally controlled oscillator (DCO) [1] considers impulse sensitivity function (ISF) [3] of the oscillator as opposed to merely its Q-factor and power consumption in order to achieve an outstanding PN performance. It exploits clipping of the resonating waveform to eliminate the effect of active devices on the PN. Recently-introduced class-F oscillator [4] enforces a pseudo-square voltage waveform around the tank to decrease PN sensitivity to circuit noise. It satisfies the mobile station (MS) PN requirements of 3GPP cellular standards with the highest reported FoM without any additional inductor for tail-current noise filtering. However, its measured PN is 2 dB short of meeting the DCS BTS specifications. In this paper, we investigate benefits of the C&R structure that make it suitable for ultra-low PN applications. The original circuit is modified in light of the analysis on the position of $1/f^3$ PN corner, the effects of Q-factor degradation and frequency response of the tank. A significant improvement in performance is further achieved.

## II. Circuit Design and Performance Outline

The modified C&R oscillator schematic is shown in Fig. 1. To have a better understanding of the C&R advantages for ultra-low phase-noise (PN) applications, let us first review the linear time-variant phase noise model [3]. The oscillator phase noise is predicted by:

$$L(\Delta\omega) = 10\log_{10}\left[\frac{R_p^2(\sum_i \frac{1}{T_0}\int_0^{T_0}\Gamma_i^2(t)\overline{i_{n,i}^2(t)}dt)}{2Q_{tank}^2V_p^2}\frac{\omega_0^2}{\Delta\omega^2}\right] \quad (1)$$

where, $\omega_0$ is the resonant frequency, $T_0$ is the oscillation period, $Q_{tank}$ is the tank quality factor, $V_p$ is the oscillator voltage swing, $R_p$ is an equivalent parallel resistor modeling the loss of the tank, $\overline{i_{n,i}^2(t)}$ is the white current noise power spectral density produced by $i$th device and $\Gamma_i$ is the corresponding ISF function. In view of the above, the C&R structure brings us the following benefits:

1) A conventional LC oscillator is usually biased at the boundary of the current-limited and voltage-limited regions, where the voltage swing $V_p$ reaches an upper limit set by twice the supply voltage $V_{DD}$. $V_{DD}$ scales down in the advanced CMOS technology. Hence, $V_p$ decreases and degrades the PN. The C&R utilizes two 1:2 step-up transformers ($T_1$ & $T_2$), which bring enough voltage gain between the drain and the gate terminals of $M_{1/2}$ NMOS transistors. The circuit works at the nominal supply voltage and the drain oscillation voltage is limited by $2V_{DD}$. However, the gate oscillation swing can be as large as $4V_{DD}$, which can compensate for the phase noise penalty of the scaled-down supply voltage, but at the cost of larger die area and using thick-oxide gm devices in order to withstand large gate-drain swing.

2) Eq. (1) demonstrates a trade-off between power consumption and PN. It appears desired to scale down

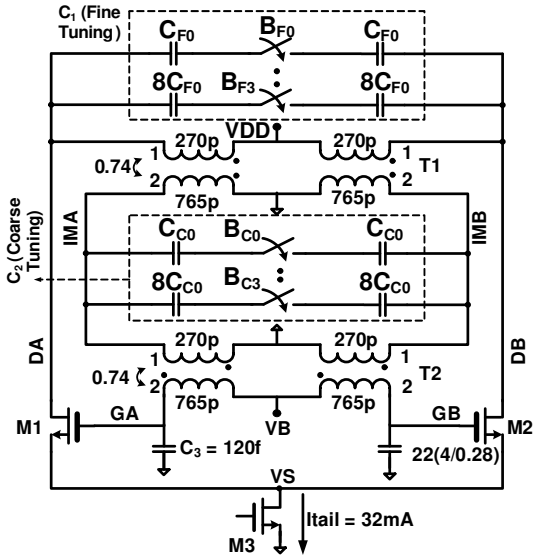


Fig. 1. The proposed clip-and-restore oscillator schematic.

tank equivalent resistance $R_P$ (thus, lower inductance) while keeping the tank Q-factor constant. For example, by reducing inductance by half, $R_p$ could theoretically decrease by half, which improves phase noise by 3 dB with twice the power consumption at the same FoM. However, the inductor substrate loss is likely become larger than its conductive loss and, consequently, the inductor Q would decrease by further reducing the inductance value. Hence, this improvement stops due to the inductor Q-factor degradation. At the same time, the tank capacitance must increase to keep the oscillation frequency constant. This would increase the layout size of the tuning capacitors and their interconnection routing, thus introducing undesired low-Q parasitic inductance that could degrade the PN.

Figure 2 shows the simplified model of the C&R tank. The equivalent inductance of the tank seen at the drain is $L_p/(1+n^2)$, where $n$ is a secondary-to-primary turns ratio, $L_p$ is the primary inductance of the $T_1$ and $T_2$ transformers. Consequently, the C&R realizes a factor of $(1+n^2)$ smaller inductance compared to the traditional oscillator for the same Q-factor and resonance frequency. Hence, the equivalent $R_p$ is smaller and the oscillator power consumption can be increased to reach lower PN at the same FoM. On the other hand, $C_2$ and $C_3$ capacitances appear at the drain through a scaling factor of $n^2$ and $n^4$. This impedance transformation can decrease the total required capacitance for an oscillation frequency, which reduces the routing capacitance parasitics and effectively increases the tuning range. Consequently, by using two step-up transformers, we are able to push the PN improvement suggested by (1) much further than practically possible with the traditional LC oscillators.

3) The rms value of ISF function of the C&R oscillator is much smaller than in the traditional structures (compare the blue and dotted red plots in Fig. 3, bottom). Hence, it can achieve lower PN and better FoM. According to the

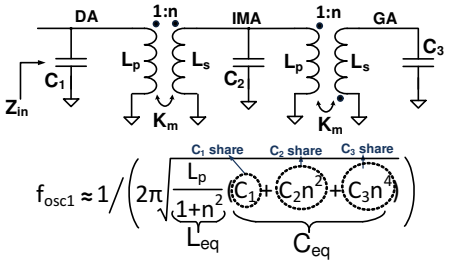


Fig. 2. The C&R tank and its main resonance frequency

linear time-variant phase noise model [3], ISF is dependent on the derivative of the oscillation voltage. Consequently, its value is zero throughout the clipping region (see Fig. 3, bottom). Thus, noise injected through the transformer's primary, power supply and active devices does not contribute to the oscillator phase noise during the clipping. It can be shown that the shape and position of the clipping is a function of gate voltage swing of gm-devices, relative phase and amplitude of $2^{nd}$ harmonic component of the drain current, amplitude ratio and phase difference of the tank input impedance at the main resonance frequency and its $2^{nd}$ harmonic.

### A. NMOS versus PMOS as gm-device

The original C&R oscillator used PMOS transistors as the gm devices for their lower $1/f$ noise corner. However, the oscillation waveform shape also affects the $1/f^3$ PN corner frequency, by the following expression [3]:

$$f_{1/f^3} = f_{1/f} \cdot \frac{C_0^2}{\Gamma_{rms}^2} \tag{2}$$

where, $C_0$ and $\Gamma_{rms}$ are average and rms values of ISF function, respectively. The C&R drain oscillation waveform (see Fig. 3, top) has asymmetric rise and fall times caused by the output clipping. Hence, this asymmetric waveform increases $C_0$ and is a more dominant factor on the position of the $1/f^3$ PN corner than is the $1/f$ device noise corner. NMOS devices reach the same gm with smaller size and offer higher cut-off frequency, $f_t$, which is beneficial to have sharper transitions and a more symmetric waveform. Although NMOS devices have a higher $1/f$ noise corner, their conversion factor is lower than with the PMOS transistors in the C&R oscillator. As an effect, there is a negligible difference between NMOS and PMOS choice on the $1/f^3$ phase noise corner. In addition, PMOS devices suffer from negative bias temperature instability (NBTI). This phenomenon causes an increase in the absolute threshold voltage, a degradation of the mobility, drain current and transconductance of MOS transistors when a negative gate-source voltage $V_{gs}$ is applied to the transistors. Although NMOS devices can be damaged in an NBTI stress, the damage occurs at negative $V_{gs}$ where NMOS devices are not active.

### B. Quality Factor Degradation

The gm devices load the tank and degrade its Q-factor during the triode region operation. However, the ISF is zero

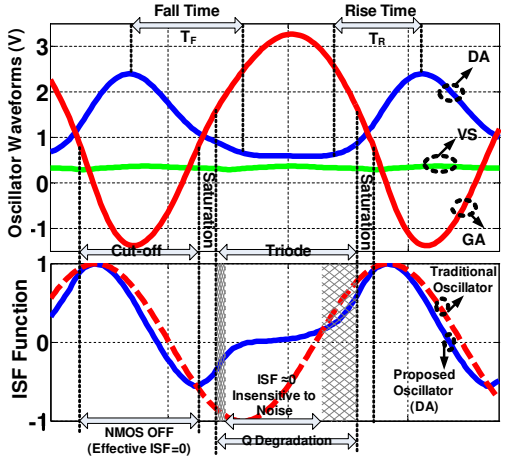


Fig. 3. Simulated NMOS gate, drain and source voltage waveforms (top), ISF function at DA node (bottom).

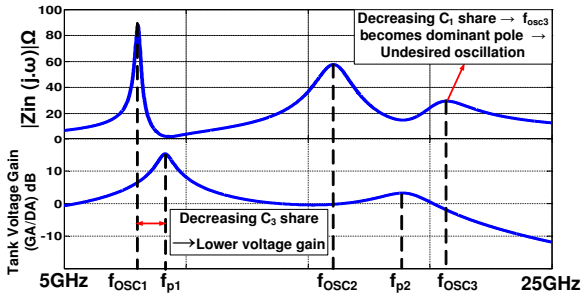


Fig. 4. Tank differential-mode input impedance and its voltage gain versus frequency.

in the hard clipping region. Consequently, the degraded Q-factor does not affect the PN. However, near the clipping area (shaded region in Fig. 3), the gm device loads the tank and the ISF function is not zero. Thus, the degraded tank Q can dramatically affect the PN. Sharper gate voltage results in smaller rise and fall times ($T_R$ & $T_F$) and alleviates this issue. The bias-voltage $V_B$ of the gm devices has a direct effect on the shaded region span. The optimum $V_B$ is the lowest possible value that satisfies the tuning range requirements, the operation at the boundary of the voltage-limited region and results in practical tail current and gm device lay-out sizes. Larger $V_B$ causes wider shaded triode region and more overlap between the active region of the gm devices, which has an adverse effect on PN degradation. Introducing the tail current, which was missing in [1], offers a degree of freedom to adjust the oscillator to the optimum PN performance. It also brings more control on the oscillation voltage swing versus the tuning range and process variations, which is vital for low time-dependent dielectric breakdown failure rate during long-term base-station operation.

### C. Tank Optimization

The tank plays a vital role in the C&R oscillator. First, it determines the fundamental oscillation frequency $f_{osc1}$ and controls impedance transformation at gm-device terminals. Second, it has a filtering function, which amplifies the drain oscillation voltage at the fundamental frequency and attenuates its harmonic components on the path to GA/GB nodes. Third, it brings positive feedback between the drain and gate terminals of the gm devices. Forth, it provides enough common-mode rejection to prevent unwanted oscillations. Fifth, its impedance at $2^{nd}$ harmonic of $f_{osc1}$ flattens the clipping area. The clipping largely desensitizes the PN due to the Q-factor of the primary winding. Thus, one should optimize the transformer based on Q of the secondary winding. The tuning capacitances are divided between the following terminals: DA, IMA and GA (see Fig. 1). Actually, non-ideal coupling causes undesired resonance frequencies, which should be dealt with by properly tuning these capacitances. Figure 4 shows the differential-mode input impedance and voltage gain of the tank versus frequency. It can be shown that for a fixed $f_{osc1}$, decreasing $C_1$ could make the third resonance frequency $f_{osc3}$ to be the dominant pole, thus seeing an undesired oscillation. On the other hand, it is necessary to use fixed capacitors $C_3$ at the gate terminal due to high sensitivity of the PN to parasitic inductance and low-Q capacitance at this node. It can be shown that, at the fixed $f_{osc1}$, increasing $C_3$ results in larger tank voltage gain, higher gate swing, shorter rise/fall time and better PN performance. However, $C_3$ is a fixed capacitor and larger $C_3$ limits the tuning range. Based on the mentioned trade-offs, $C_3$ and $C_1$ need to have at least 20% share of the total tank capacitance. On the other hand, the ratio of differential to single-ended capacitance of $C_1$ adjusts the peak position of the tank common-mode input impedance, which is desired to be near the second harmonic of $f_{osc1}$. Consequently, it enhances the $2^{nd}$ harmonic component of the drain voltage, which flattens the clipping area and improves the PN.

## III. Measurement Results

The oscillator is prototyped in TSMC 1P7M 65 nm CMOS (see chip micrograph in Fig. 5). A stack of two 3.4 $\mu$m thick copper top-metal and 1.4 $\mu$m Al-cap layers are used to construct the transformers. The Q-factors of the primary and secondary windings are 15 and 22 at 8 GHz, respectively. Eight switched MoM-capacitors $(B_{C0}-B_{C3})$ & $(B_{F0}-B_{F3})$ [1] are across the secondary and primary windings of $T_1$ to change the resonance frequency with coarse and fine steps, respectively. A resistive shunt buffer

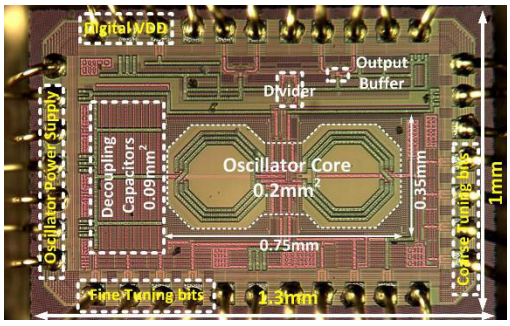


Fig. 5. Chip microphotograph.

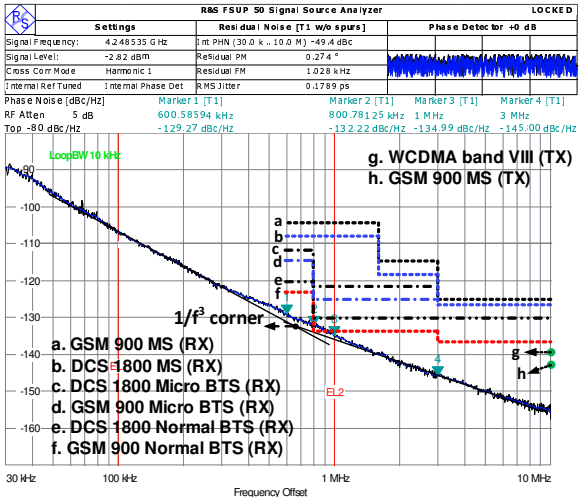


Fig. 6. Measured phase noise at 4.2 GHz. Specifications are normalized to the carrier frequency.

interfaces the oscillator output to the dynamic divider. A differential output buffer drives a 50 Ω load.

The PN measured at 4.2 GHz (after the on-chip ÷2 divider) at 1.3 V and 32 mA current consumption is shown Fig. 6. The phase noise of -145 dBc/Hz at 3 MHz offset lies on the 20 dB/dec region, which extrapolates to -174.7 dBc/Hz at 20 MHz offset (normalized to 915 MHz) and meets the GSM TX mobile station spec with a very wide 13 dB margin. The GSM/DCS "micro" BTS and DCS "normal" BTS specs are met with a few dB of margin. The DCO is the best purity performing RF oscillator ever published. However, due to large $1/f^3$ corner frequency, its measured PN would be off by 1.5 dB only for the toughest GSM base-station BTS "normal" specifications at 800 kHz offset. The $1/f^3$ corner frequency is at 650 kHz, which is the same as the original design with PMOS transistors. The PN noise beyond the 10 MHz offset is dominated by thermal noise from the divider and buffers. The oscillator has a 19% tuning range from 7.2 to 8.7 GHz. Figure 6 shows the PN and FoM around the tuning range (after the ÷2 divider) at 800 kHz and 3 MHz offset frequencies. The average FoM is as high as 191 dBc/Hz and varies less than 2 dB across the tuning range.

Table I summarizes the DCO performance and compares

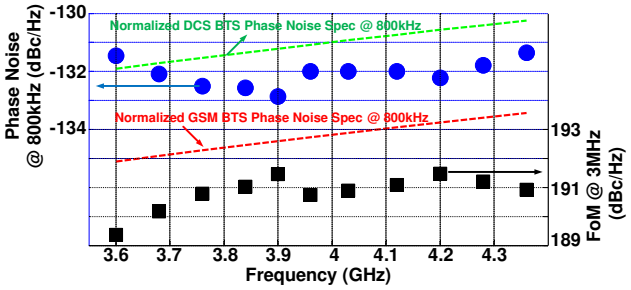


Fig. 7. Measured phase noise at 800kHz (top), FoM at 3MHz (bottom) versus tuning range.

TABLE I
COMPARISON OF STATE-OF-ART OSCILLATORS

| | This Work | [1] | [2] | [5] | [4] | [6] |
|---|---|---|---|---|---|---|
| CMOS(nm) | 65 | 65 | 130 | 55 | 65 | 130 |
| $V_{DD}$(V) | 1.3 | 1.2 | 1 | 1.5 | 1.25 | 3.3 |
| $F_0$ (GHz) | 4.2 | 3.92 | 5.2 | 3.35 | 3.7 | 1.56 |
| TR (%) | 18.8 | 10.2 | 14 | 31.4 | 25 | 9.6 |
| PN[1](dBc/Hz) | -145 | -142 | -131 | -142 | -142 | -150 |
| Normalized PN[2] (dBc/Hz) | -158 | -154 | -146 | -153 | -154 | -155 |
| $I_{DC}$ (mA) | 32 | 21.5 | 1.4 | 18 | 12 | 88 |
| $P_{DC}$ (mW) | 41.6 | 25.8 | 1.4 | 27 | 15 | 290 |
| FoM (dB/Hz) | 192 | 190 | 195 | 189 | 192 | 180 |
| $FoM_T^3$(dB/Hz) | 197 | 190 | 197 | 199 | 200 | 180 |
| Core ($mm^2$) | 0.24 | 0.19 | 0.11 | 0.196 | 0.12 | N/A |
| Oscillator description | New C&R | C&R | Class C | Class B/C | Class F | Colp-itts |

[1] PN at 3MHz, [2] PN at 3MHz offset Normalized to 915MHz carrier, [3] $FOM_T = |PN|+20\ log_{10}(\ f_0/\Delta \cdot f\ \text{TR}/10\ )\ -\ 10\ log_{10}(P_{DC}/1\text{mW})$

it with relevant state-of-the-art oscillators. Phase noise is also normalized to a 915 MHz carrier for comparison. The presented oscillator has the lowest phase noise. Improvement of 4 dB phase noise and 1.8 dB FoM are demonstrated over the original C&R design.

## IV. Conclusion

The benefits, constraints, trade-offs and optimization procedure of the clip-and-restore (C&R) oscillator have been reconsidered from the viewpoint of minimizing the phase noise. As a result, an 8 GHz prototype was designed and fabricated in 65-nm CMOS technology. The oscillator demonstrates the lowest phase noise ever achieved in bulk CMOS technology. It complies with the LO phase noise requirements of the DCS base-station receivers. A 4 dB phase noise and 1.8 dB FoM improvements are demonstrated over the original C&R oscillator.

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