A 105GHz VCO with 9.5% Tuning Range and 2.8mW Peak Output Power Using Coupled Colpitts Oscillators in 65nm Bulk CMOS

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***Abstract*—In this work, a loop of unidirectionally coupled oscillators to demonstrate high tuning range and output power is proposed. To achieve large tuning range, two different tuning mechanisms are simultaneously exploited. First each core oscillator is tuned using a variable capacitor. Next, by controlling the phase/delay between the coupled oscillators, the entire loop dynamics and hence its frequency is tuned. In this paper, we analyze a loop of "n" coupled oscillators using Adler's equation and derive the expression for the maximum tuning range. The proposed system is designed and implemented using four coupled Colpitts VCOs in a 65nm bulk CMOS process. The VCO achieves continuous tuning range of 9.5% at the center frequency of 105GHz with the peak output power of 2.8mW. The circuit consumes 54mW from a 1.2V supply. To the best of our knowledge, this VCO has the highest output power and tuning range among all the CMOS oscillators at or above 100GHz.**

***Index Terms*—Voltage controlled oscillator, Injection locking, Coupled oscillator, Millimeter wave circuits, Varactor**

I. INTRODUCTION

High frequencies (100GHz to 1THz) have many interesting applications in different areas including imaging, spectroscopy, and short range communication. Signal generation at these frequencies is usually accomplished by harmonic generation. Either higher order harmonics are collected from a fundamental oscillator or separate frequency multipliers are employed. For an integrated solution of wideband signal generation, both approaches require high power and tunable fundamental oscillators at mm-wave frequencies.

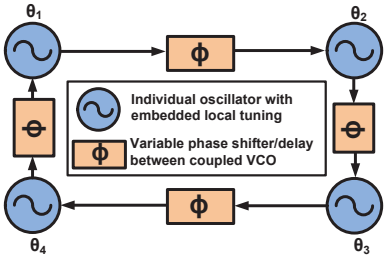

Fig. 1. A loop of coupled oscillators having local & global tuning

At mm-wave frequencies, achieving high power and large tunability at the same time is challenging. Varactors employed in LC tanks have low quality factor and mostly happen to be in parallel with device parasitics. The low quality factor degrades the phase noise performance as well as achievable power and parallel combination with device parasitics reduces tuning range along with oscillation frequency. In this work, we target this problem using a system of coupled oscillators as shown in Fig. 1. Two kinds of tuning phenomenon occur in such a system: local tuning and global tuning. Local tuning is implemented at the level of individual oscillators using varactors inside each core. On the other hand, global tuning is achieved at the system level where frequency variation is performed by changing the coupling between core oscillators [1]. In this work, we design the system in such a way that the overall tuning range is the addition of both approaches. At the same time, coupling multiple oscillators increases the output power and enhances phase noise. Using a 65nm CMOS process, this methodology demonstrates a VCO with 9.5% tuning range at 105GHz and output power of 4.5dBm. These results outperform any previously reported CMOS VCO at or above 100GHz in terms of tuning range, output power and DC-RF efficiency.

II. TUNING MECHANISMS

Adler presented dynamics of a system of coupled electrical oscillators in the context of injection locking [2]. When a free running oscillator at ω_o is injected with a signal from another oscillator at ω, under certain conditions the first oscillator locks to second oscillator at ω. This locking results in a phase difference ($\Delta\phi$) between two oscillators which is proportional to the frequency difference ($\Delta\omega = \omega - \omega_o$) given by

$$\Delta\phi \quad = \quad sin^{-1}\left(2Q\frac{I_{core}}{I_{inj}}\frac{\Delta\omega}{\omega_o}\right) \tag{1}$$

where Q is the quality factor of the resonator and I_{core} and I_{inj} are the currents inside core and injected from the outside, respectively. Conversely, the oscillation frequency of two mutually coupled oscillators can be controlled by enforcing a certain phase shift between them [1]. In Fig. 1, the oscillation frequency can be varied by changing the delay between oscillators. For further explanation we look at the phase dynamics of any system of "n" coupled oscillators similar to Fig. 1. If ϕ is the rotating phase of i^{th}

oscillator in the loop and ω_o is its free running frequency then from the theory of injection locking the instantaneous frequency is given by

$$\omega \quad = \quad \omega_o + Ksin(\phi - (\theta_i - \theta_{i-1})) \qquad (2)$$

where $K = \frac{I_{inj}}{I_{core}} \frac{\omega_o}{2Q}$ is the coupling factor and ϕ is the phase shift resulting from the phase shifter in Fig. 1.

Now we assume each oscillator consists of an LC tank and has a varactor that results in local tuning. If ΔC is the change in capacitance then eq. (2) can be transformed in to

$$\omega \quad = \quad \omega_o \left(1 + \frac{\Delta C}{2C_o}\right) + K_s sin(\phi - (\theta_i - \theta_{i-1})) \quad (3)$$

where

$$K_s \quad = \quad \left(1 + \frac{\Delta C}{C_o}\right) \frac{I_{inj}}{I_{core}} \frac{\omega_o}{2Q}$$

is the coupling factor of the system. The maximum tuning range of the overall system is

$$\left.\frac{\Delta\omega_{max}}{\omega_o}\right|_{total} \quad = \quad \frac{\Delta C_{max}}{C_o} + \frac{I_{inj}}{I_{core}} \frac{1}{Q} \qquad (4)$$

This first term on the right hand side comes from the purely capacitive/local tuning. The second term arises from the global tuning caused by controlling the delay between the oscillators. It is noteworthy that eq. (3) shows the relationship between the frequency of the coupled oscillators and the phase shift between them. In particular, as the phase shift, ϕ, increases (or the delay between oscillators decreases) the frequency of the system, ω, increases.

III. CIRCUIT DESIGN

The implementation of both global and local tuning in one system is challenging. We choose common drain Colpitts topology for the implementation of each oscillator of Fig. 1 because, as explained later, it allows us to implement global tuning without any explicit phase shifters hence resulting in a simpler implementation. Moreover, in the case of Colpitts, varactor comes in series with the parastic capacitance hence the presence of varactor does not decrease the oscillation frequency. The common drain Colpitts is shown in Fig. 2 with a varactor at the source of transistor. The parasitic capacitance between gate and source (C_{gs}) acts as a feedback capacitor so we can eliminate C_1. The small signal analysis yields to

$$Z_{in} = \left(\frac{1}{C_s} + \frac{1}{C_{gs}}\right) \frac{1}{j\omega} - \frac{g_m}{\omega^2 C_{gs} C_s}$$

at the gate of transistor. The above equation contains negative real impedance along with the variable imaginary part. The negative real impedance compensates for the loss of the tank. We couple "n" Colpitts oscillator as shown in Fig. 3. We do not employ any explicit phase shifters. The energy from each stage is injected from the gate of transistor in to the next stage via the drain current. The varactor inside each core also varies the phase of injected current along with changing the oscillation frequency of the system. To explain this further, we look that the imaginary part of Y_{21} of the transistor with the varactor at its source (Fig. 4),

$$|Imag\,(Y_{21})\,| \quad = \quad \frac{g_m^2 C_s}{g_m^2 - s^2\,(C_s + C_{gs})^2}.$$

The graph in Fig. 4 shows that global tuning and local tuning works in the same direction. In the proposed coupled system, any decrease in varactor capacitance (C_s) increases the oscillation frequency of LC oscillator (local tuning) as well as decreases the delay of injected signal from each stage (imaginary of Y_{21}) which further increases the oscillation frequency (global tuning) and vice versa. Further more, couping enhances the power as well as phase noise hence the adverse effect of lossy varactor is compensated.

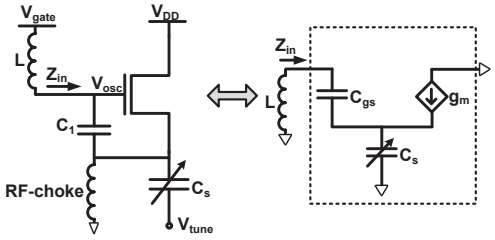

Fig. 2. Common drain Colpitts topology

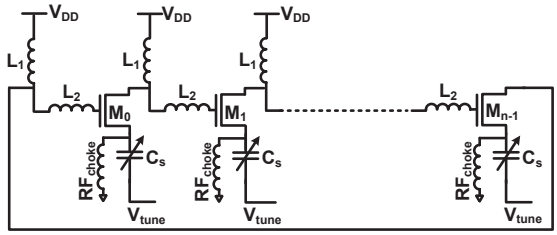

Fig. 3. Loop of Colpitts oscillators

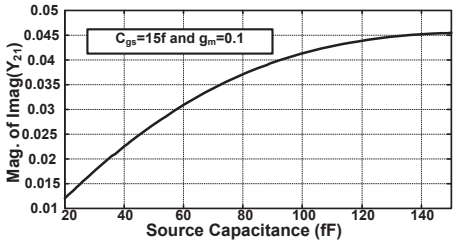

Fig. 4. Principle behind global tuning

IV. Implementation

Fig. 5 shows the schematic of four coupled Colpitts VCOs. If the RF-choke is used for biasing the source of

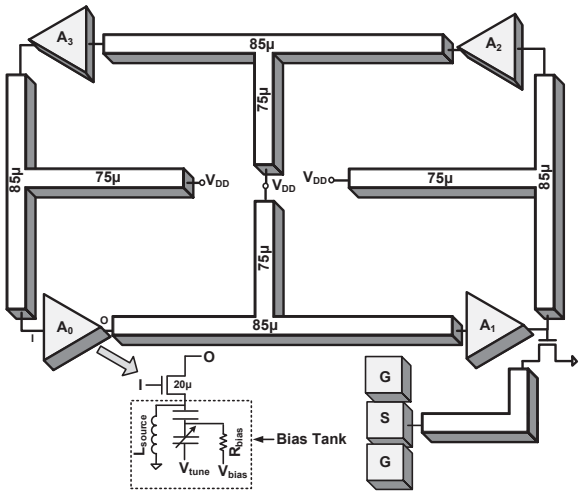

Fig. 5. Schematic of four coupled Colpitts VCOs

each transistor (as in Fig 4.), the size of varactor comes out to be comparable with the size of C_{gs}. The implementation of the big RF-choke inductor can potentially increase the area and make layout difficult. We resolve this problem by implementing an LC tank (referred as bias tank in Fig. 5) at the source of each transistor. To attain capacitive behavior at the source, resonance frequency of the "bias tank" is kept lower than the oscillation frequency of the VCO and inductance of the bias tank is selected accordingly. This biasing approach gives us an extra degree of freedom in terms of varactor design. Furthermore, the varactor can be designed for the highest tunability because its capacitance does not need to be close to C_{gs}.

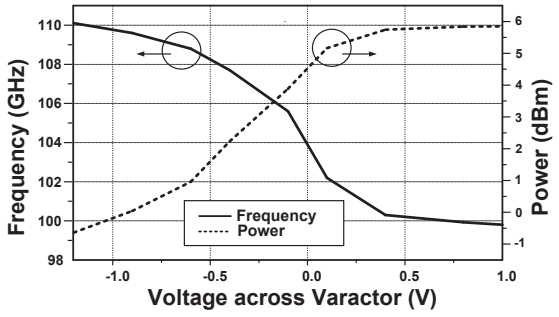

Fig. 6. Simulated output power and frequency.

The proposed structure is designed at 105GHz and fabricated in a 65nm CMOS process. Each transistor is 20μm wide. The inductors are implemented as coplanar transmission lines with ground shielding.The design dimensions are shown in Fig. 5. All the lines and interconnects are carefully simulated in Sonnet. The varactor is carefully chosen for the highest C_{max}/C_{min} ratio. The capacitance varies from 40fF to 200fF ($C_{max}/C_{min} > 3$).

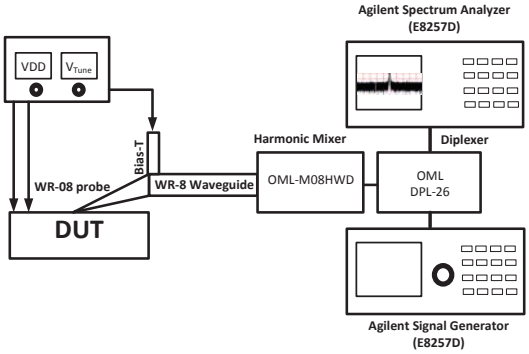

Fig. 7. Measurement Setup

A coupling capacitor to bias the varactor was designed using the top two metal plates. We use an 18μm wide transistor as common source buffer and absorb its loading effect by adjusting the sizes of adjacent transistors. The buffer is connected to a low capacitive pad via a 50 ohms transmission line. A small 50μm x 50μm output pad is designed using the top two metal layers with no ground plane. The capacitance of the pad is only 10.8fF with Q of 24 at 105GHz. The inductances of V_{DD} traces and bypass capacitors are also carefully modeled and included in the simulation. Fig. 6. shows the simulation results of our design. The frequency can be continuously tuned from 99GHz to 110GHz. The maximum simulated output power is 5.9dBm at 99GHz.

For testing, the chip was mounted on a PCB and all the DC voltages were wire bonded. Fig. 7. shows the measurement setup to determine the output power and frequency. The output is measured using a WR-08 probe by GGB with a built-in bias-T. The loss of probe is measured using a 110GHz network analyzer to be around 2.5dB at frequencies from 100GHz to 110GHz. The output buffer of oscillator is power up using the probe bias-T. The probe is directly attached to an OML harmonic mixer via a WR-08 waveguide. An external diplexer is employed to connect to a spectrum analyzer and signal generator. The conversion loss of harmonic mixer is measured at various LO powers for 8_{th}, 10_{th} and 12_{th} harmonic using a PM4 calorimeter. The loss of mixer is 37-44dB from 100-110GHz at 8_{th} harmonic of LO. The output frequency was determined by sweeping the LO at various harmonics. The oscillator core draws 45mA of current from a 1.2V supply. Fig. 8 shows the measured output frequency and calibrated output power. The output frequency can be continously tuned from

TABLE I
COMPARISON WITH PRIOR ART

Ref	Tech.	Freq (GHz)	Tuning Range	Core P_{DC}(mW)	P_{out} (dBm)	DC-RF %	Phase Noise (dBc/Hz)	FOM_T
[3]	90nm CMOS	104	NA	5.8	-8.2	2.6	Not reported	NA
[4]	65nm CMOS	100.6	4.3%	7.2	-25	0.04	-84.1 at 1MHz	-168.25
[5]	32nm SOI	102.2	4.12%	7.6	-30.65	0.013	-100.8 at 10MHz	-164.48
[7]	130nm CMOS	104	NA	21	-2.7	1.97	-93.3 at 1MHz	NA
[7]	130nm CMOS	121	NA	28	-3.5	2.23	-88 at 1MHz	NA
[6]	65nm CMOS	118.3	7.8%	5.6	-14	0.71	-83.9 at 1MHz	-175.72
This work	65nm CMOS	105	9.5%	54	4.5	5.3	-92.83 at 1MHz	-175.48

100GHz to 110GHz. Measured power and tuning range is very close to the simulated results. The maximum measured power is 4.5dBm at 100GHz which is 1.4dB less than our simulations. The output power remains above 0dBm from 100GHz to 109GHz. Fig. 9 presents the typical spectrum of output at 105GHz and chip photograph. Fig. 10 shows

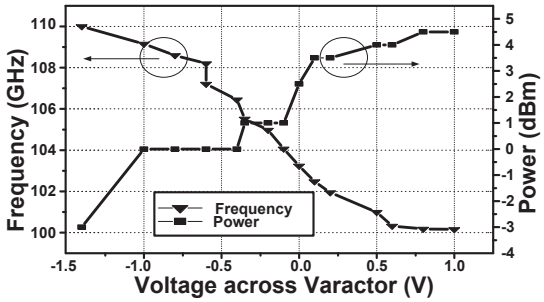

Fig. 8. Measured output power and frequency VS. voltages.

measured phase noise at 105GHz. The measured phase noise is -92.83dBc/Hz at 1 MHz offset. Table I shows the comparison with prior art. This work demonstrates the highest tuning range and output power among the VCOs in the same frequency range implemented in a standard CMOS process.

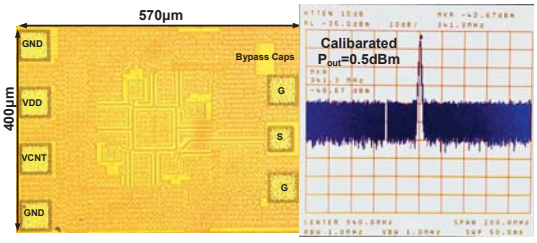

Fig. 9. Die photograph and typical output spectrum.

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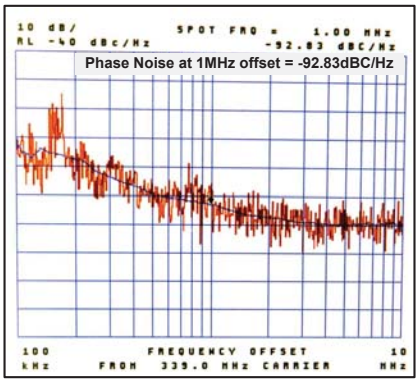

Fig. 10. Measured phase noise

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