A T-DMB Mobile TV SoC Tuner with Compact Size, Low Power and BoM in 65nm CMOS

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***Abstract* — This paper presents a direct conversion Korean standard T-DMB SoC tuner using a 65nm low power CMOS technology with the best feature of size, power and BoM ever reported. A digital F/E enhanced function is implemented to reduce analog signal processing empowered by oversampled A/D converter, digital channel selection filter and lots of digital calibration blocks. And the designed LNA excludes all required inductors. Thus high voltage gain and low current consumption are achieved due to their high Q factor. A single-to-differential signaling down-conversion mixer is also announced which has well balanced output characteristic. A DC/DC converter is adopted as well for the further low power consuming. The tunable clock frequency scheme of DC/DC buck converter can prevent a degradation of sensitivity performances which is planed value to escape the channel center frequency. This reported SoC tuner consumes only 28mA at maximum gain mode. And -103.5dBm of sensitivity and 48dBc of N±1 adjacent-channel selectivity are achieved also with only 5 external LC components. This SoC occupies 2.5×2.5mm^2 die and WLCSP chip size.**

***Index Terms* — T-DMB, Mobile TV, Tuner, Sensitivity, ACS, IM3 canceling LNA, Single-to-differential conversion mixer, Digital F/E, DC/DC buck converter, LDO.**

I. Introduction

Nowadays the speed of mobile TV tuner development is quite fast to meet a new mobile device model launching which has to be smaller, thinner and lower power than before. And also this market condition presses us to make a low cost TV tuner with better figure of merit. Therefore we have concluded from these posed severe conditions to have advanced features as follows. At first one standard specific solution can meet these needs. Multi-standard solution is hard to achieve the mentioned requirements at the same time compared with single one. Secondly single supply solution is preferred to customers than multi supplies. Therefore tuner has to integrate regulators into the SoC. Third, low number of external component must be considered to reduce BoM and mounted PCB area at mobile devices.

This paper reports mobile TV SoC tuner for Korean standard T-DMB with challenging features as described at above. Our SoC tuner can receive -103.5dBm input signal power as sensitivity and also 48dBc adjacent channel selectivity at closest allocated frequency with flowing 28mA current in 2.5×2.5mm^2 die size.

II. Architecture and Circuit Design

The receiver block diagram is shown at Fig. 1 as below. To meet low power consumption DC/DC buck converter and lots of LDOs are integrated in this chip. Each LDOs drives assigned building block respectively. All integrated LDOs do not hire external capacitors to achieve a low BoM. In this SoC SAR type 10-bit I/Q ADCs are adopted.

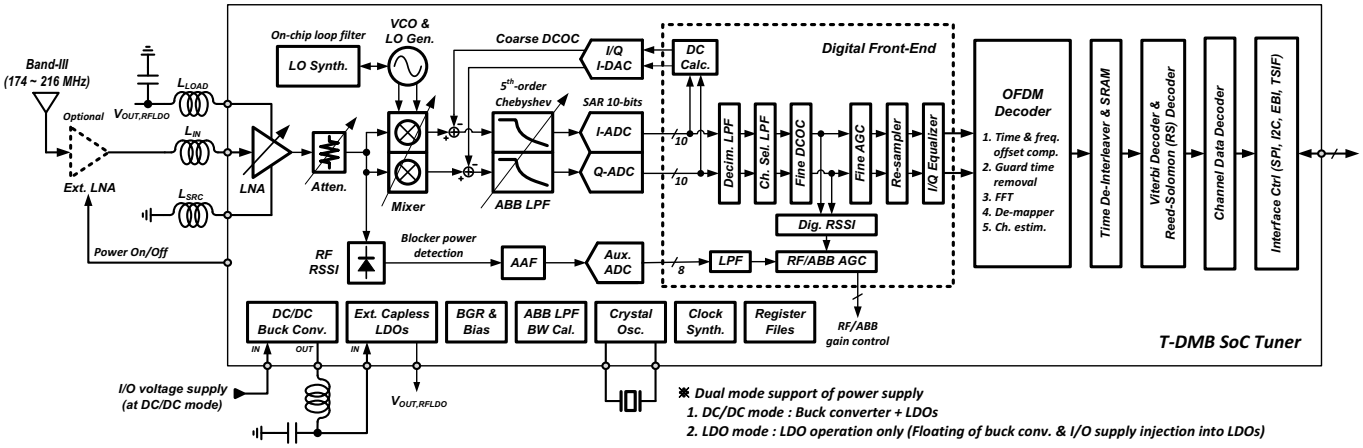

Fig. 1. Receiver Architecture

The implemented SAR A/D converters have lower power consumption by its natural characteristic than other types of Nyquist ADC. A 24.576MHz is chosen which is 16-times of T-DMB bandwidth for A/D converter sampling clock. A 10-bit resolution with 16-times of OSR produces higher in-band ADC SNR that can alleviate analog filter and gain block burden that makes optimal size and power consumption. Therefore digital F/E can be organized to take a blocker filtering function as a companion of analog baseband filter. Furthermore, digital signal processing helps DC offset cancelling, analog filter cut-off bandwidth calibration, I/Q mismatch equalization and automatic gain control that is much simpler and easier than analog fashioned solution.

In general switching regulator output ripple is not easily rejected even though there is a post LC filter. Therefore normally LDO follows to improve power supply rejection. However residual ripple harms RF in-band SNR by its harmonic terms. Due to this overall performance will be degraded by this spurious response. We designed DC/DC buck converter that can operate under tunable clock condition. A specially designated clock frequency is fed into DC/DC buck converter according to the input channel center frequency. Hence, each channel does not affected by its clock harmonics. Well tuning plan can reserves enough deviation from signal in-band edge. According to our frequency planning minimum frequency deviation is more than 2.5MHz at least case. This clock is generated by LO synthesizer via variable frequency divider. Therefore DC/DC buck converter input switching clock jitter is quite clean because LC VCO based PLL can reserve the best phase noise performances than others.

A. LNA Design

T-DMB RF input frequency is from 174 to 216MHz. Therefore, LNA input and output are consist of tunable capacitor banks as shown in Fig. 2. The designed LNA follows a traditional inductive source degenerated type. Because power consumption has been our main concern, we decided to exclude all inductors. Due to their high Q factors a major part of voltage gain is accomplished by matching networks. And tracking filtering characteristic can be also acquired by excluded inductors. Thus the *gm* of M1 contribution will be lower down to achieve targeted gain considerably. On the other hand MGTR has been well known solution to improve linearity. [1] But this MGTR is not convenient to compromise a low noise and a high IP3 at the same in this amplifier. To overcome this issue [2] was introduced. But [2] requires on-chip 3-terminal source inductor that requires self EM modeling. And also lower noise figure and higher gain are difficult than inductor excluded LNA. Instead of [1] and [2] we utilized another way to boosting IP3 [3]. M2 and M3 make negative feedforward path as depicted in Fig.2. If M2 is in triode region, fundamental gain is affected at least. But IM3 distortion will be cancelled out well [3]. The designed LNA has high, mid and low gain paths and each path has inner gain control steps as fine level.

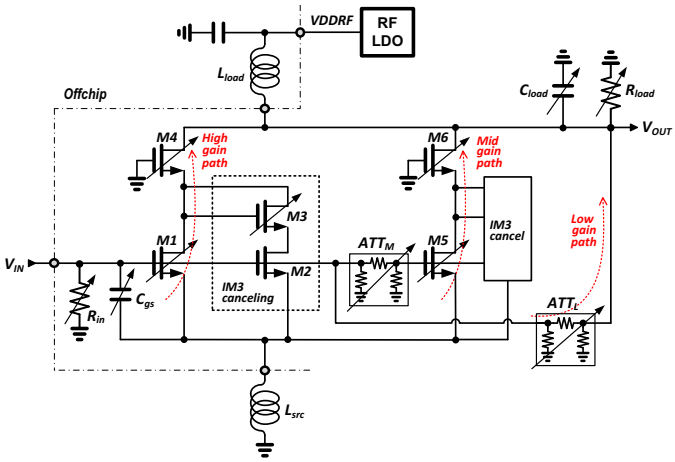

Fig. 2. Designed LNA Schematic (AC Only)

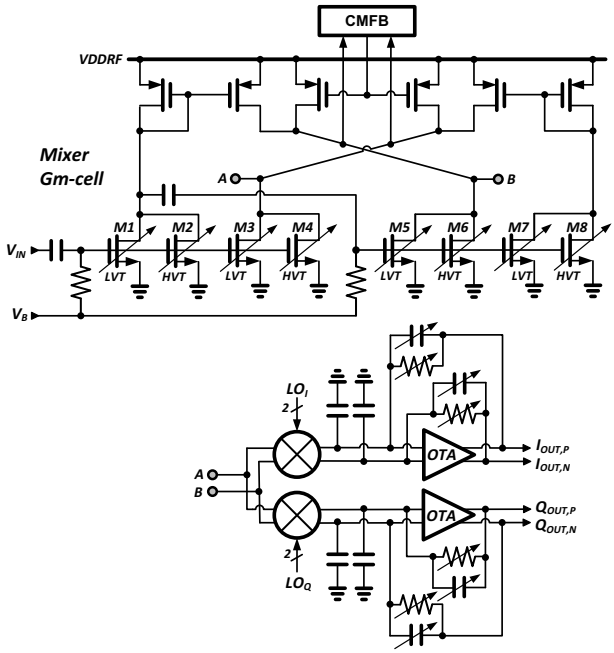

Fig. 3. Designed Mixer Schematic

B. Mixer Design

Single-ended signal interface is maintained before mixer. We let mixer Gm-cell take the first step of differential signaling. Therefore system IP2 characteristic is mainly determined by this Gm-cell performance. The presented mixer Gm-cell schematic is depicted in Fig. 3. Differential

signal comes from two pairs of common-source amplifier output. To improve IP3 performance *gm* is compensated by composition of LVT and HVT to be MGTR. Secondly, fully-differential is accomplished by cross connection between the first and second stage common-source amplifier. Phase and gain mismatch are shuffled though this cross connection. This circuit topology can generate a high IP2 performance without calibration.

C. Analog baseband

The implemented analog filter is Chebyshev 5th order LC-ladder type. Gain tuning can be easily embedded in this type filter with no changing of skirt characteristic. And also LC-ladder filter has better filter sensitivity than biquad version. According to the link budget analysis the 4th order filter is suitable for this due to the OSR and SNDR of A/D converter. A additional order is a marginal purpose.

Coarse DC offset measurement is calculated at digital F/E as shown in Fig. 1. I/Q current DACs compensate DC offset in coarse way. The residue is finely cancelled out at digital F/E.

D. Digital Front-End

Digital F/E takes major role for overall performances. At first A/D converter has to have considerable SNDR to enable digital processing. The designed A/D converter its own performance can reach up to 72dB at T-DMB in-band with 16-times of OSR. The post FIR decimation and channel filter follows to get rid of residual blocker terms. Coarse and fine DC offset remover, AGC loop related blocks and re-sampler are located respectively. Finally, I/Q equalizer is followed to calibrate magnitude and phase mismatches between I and Q signal path.

III. Measured Results

A 65nm LP CMOS process is used for presented chip fabrication with RF option. Overall die and chip size is 2.5×2.5mm^2. Fig. 4 is die and WLCSP photograph. Fig. 5(a) shows measured sensitivity and N±1 adjacent channel selectivity (ACS) performances. The Measured sensitivity is around -103.5dBm and 48dBc of N±1 ACS over all input channels. Due to a 24.576MHz system main clock frequency 10C channel (196.736MHz) is affected by its 8th harmonic. System clock frequency shifting scheme can improve 10C channel sensitivity by allocating the 8th clock harmonic at out of wanted band.

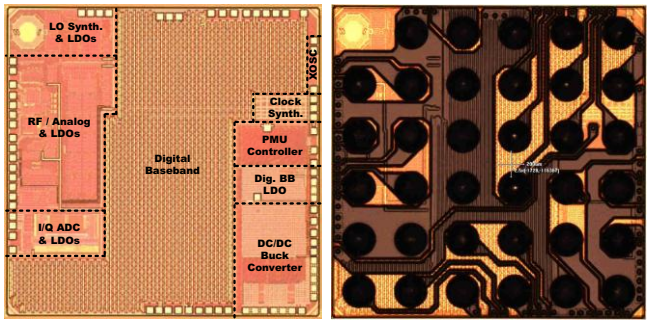

Fig. 4. Die and WLCSP Chip Microphotograph

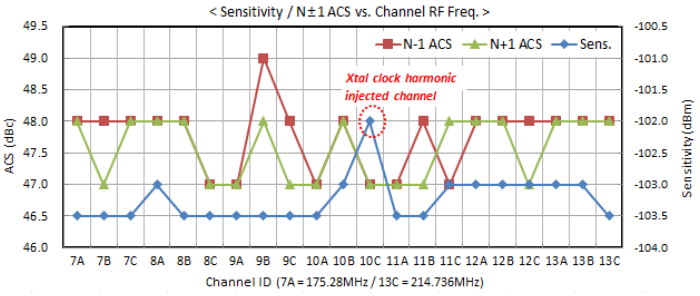

Fig.5. Sensitivity and N±1 ACS vs. Input channels

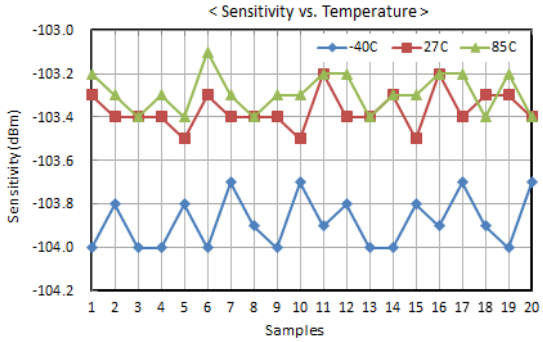

Fig.6. Sensitivity vs. Temperature and Samples

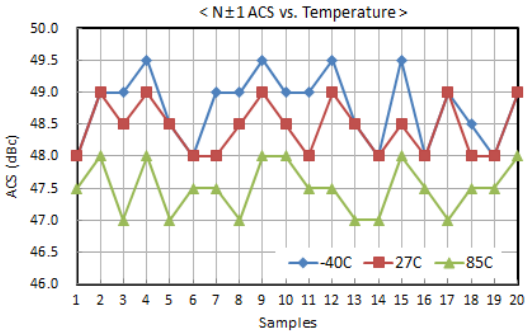

Fig. 7. N±1 ACS vs. Temperature and Samples

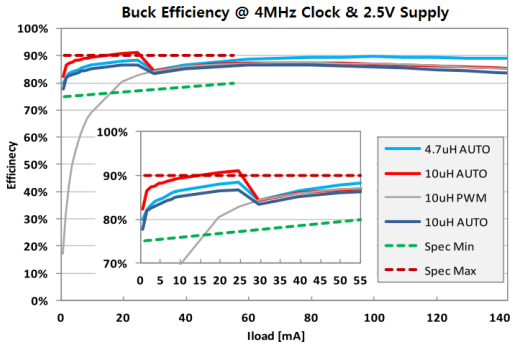

Fig. 8. Buck Converter Power Conversion Efficiency

Temperature and sample varying performances are shown at Fig. 5 to 7 based on LDO mode. The DC/DC mode ACS performance is quite similar to LDO mode by assigning buck clock frequency. Sensitivity is a little higher than LDO mode by 0.3dB to 0.5dB. If there is no specific buck clock planning, 5dB of sensitivity will be worse than before approximately.

Maximum buck converter power conversion efficiency is up to 90% with 24mA current loading as depicted in Fig. 8. Normally buck converter power conversion efficiency is higher at large current loading condition than at small. The buck converter was designed for low current loading specific condition to achieve high power efficiency. The clock which is from 3.2 to 4.5MHz enables to escape buck converter clock harmonic injection at in-band.

TABLE I
MEASURED PERFORMANCE SUMMARY

Process		65nm LP CMOS	
Package		35-balls WLCSP	
Die & Package Size		2.5×2.5 mm^2	
RF Input Frequency		MHz	174 ~ 216 (T-DMB)
Channel Bandwidth		MHz	1.536
Voltage Supply	DC/DC mode	V	2.2 ~ 4.3
	LDO mode	V	1.5 ~ 3.6
	Core voltage	V	1.2 (After LDO)
Current Consumption		mA	28[a]
Bill of Material (BoM)	DC/DC mode	7[b] (L = 4, C = 3)	
	LDO mode	5[b] (L = 3, C = 2)	
System Noise Figure		dB	2.0 @ max gain
Sensitivity[c]	DC/DC mode	dBm	-103.2
	LDO mode		-103.5
N±1 Adjacent-Ch. Selectivity[c,d]		dBc	48
Far-Off Selectivity[c]	Tone blocker	dBc	59
	Mod. blocker		55
FM-radio Blocking[c] (FM=1/2 LO)		dBc	Over 50
LO synth. Phase Noise		dBc/Hz	-135 @ 1MHz offset
Buck Conv. Power Efficiency		%	86[e]
Measurement Conditions	a = System max gain at LDO mode b = Only crystal excluded BoM c = 2.0X10^{-4} BER (Post-RS dec. criterion) d = -65dBm of P_{WANTED} e = With 28mA current loading		

VII. CONCLUSION

This paper presents a SoC for T-DMB mobile TV tuner chip in 65nm LP CMOS process. It integrates all power management blocks such as DC/DC buck converter and LDOs. This T-DMB SoC tuner achieves the smallest size, lowest power and BoM features until now. The measured -103.5dBm of sensitivity, 48dBc of N±1 ACS results are announced with flowing 28mA overall system current at maximum gain state on 2.5×2.5mm^2 die and WLCSP size.

TABLE II
PERFORMANCE COMPARISON SUMMARY

Item	Unit	[4]	[5]	This Work
Process	-	65nm CMOS		
Chip Size	mm^2	2.64×2.64[a]	2.9×2.9[b]	2.5×2.5
Current	mA	85[c]	29.2[d]	28
BoM	-	N/A	N/A	5[e]
Noise Figure	dB	2.5	2.8	2.0
Sensitivity	dBm	-98[f,g]	-102.5[g]	-103.5
N±1 ACS	dBc	N/A	48[g]	48
Comparison Conditions	a = DVB-T/H, T-DMB, ISDB-T (RF only) b = FM, T-DMB, DAB, ISDB-T 1-seg SoC (Buck converter included) c = 102mW reported only (1.2V ref. calculation) d = 35mW reported only (1.2V ref. calculation) e = At LDO mode f = DVB-T/H QPSK (CR=1/2) (Not T-DMB) g = No reference of BER			

ACKNOWLEDGEMENT

The authors wish to acknowledge the layout assistance and support by Kihyeok Hong.

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