A 120GHz quadrature frequency generator with 16.2GHz tuning range in 45nm CMOS

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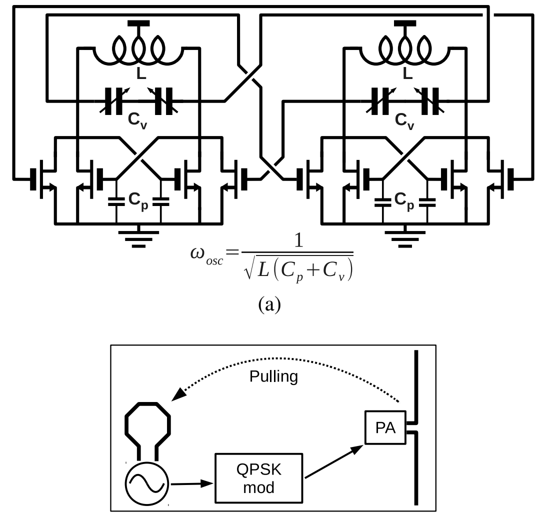
***Abstract*—This paper presents a new architecture for a 120GHz quadrature frequency generator with large tuning range and immunity against PA-VCO coupling. Combining the output signals of two independent oscillators, the pulling effect is removed and the oscillator can be integrated with a PA and an antenna on the same chip. This architecture also makes quadrature generation with large tuning range feasible at 120GHz. The chip is fabricated in a 45nm CMOS technology and shows a tuning range of 16.2GHz (13.5%), a phase noise of -112dBc/Hz @ 10MHz offset and a phase error of 5°.**

***Index Terms*—quadrature VCO, millimeter wave, tuning range, frequency pulling.**

I. Introduction

Highly integrated mm-wave CMOS circuits for high data rate wireless communication systems have emerged in recent years. These systems certainly benefit from the high bandwidth that is available at mm-wave frequencies and thus can achieve high data rates even with simple modulation schemes. But nevertheless, also these systems are now evolving towards more complex quadrature modulation schemes like QPSK and QAM [1] and thus require a quadrature mm-wave LO. When designing a fundamental mm-wave quadrature VCO, three fundamental problems need to be solved. First of all, a large tuning range is necessary to overcome process variations and the uncertainty of the transistor models at these high frequencies. In a fundamental mm-wave VCO, a large tuning range is difficult to achieve due to the large portion of parasitic capacitance and inductance in the resonant LC tank. Furthermore, conventional quadrature VCOs utilize coupling transistors to force 90 degrees phase difference between two oscillators (Fig. 1a). These coupling transistors are indeed an extra load on the LC-tank which makes it more difficult to sustain an oscillation with the limited device gain at mm-wave frequencies, and to combine this with a large tuning range. Finally, the integration of antennas on a silicon chip (Fig. 1b) becomes feasible at these high frequencies. However, integrating both an oscillator, a transmitter and an antenna on the same chip increases the coupling between the power amplifier and the antenna, back to the oscillator, potentially leading to injection locking or spurious mixing products to appear in the output spectrum. Therefore, a fundamental mm-wave VCO becomes problematic for LO generation if the antenna is placed on chip or integrated in the package.



(b)

Fig. 1. (a) Conventional fundamental quadrature VCO, and (b) QPSK transmitter with on-chip antenna causing VCO pulling.

This paper presents a solution by first generating the quadrature signals at a lower frequency and then up-converting them to generate 120GHz quadrature signals. By using two oscillators, that are operating at independent frequencies which are not harmonically related to the output frequency, the unwanted PA-VCO coupling is eliminated. This approach therefore enables to integrate the antennas either on-chip or in the package. It is also demonstrated that, by utilizing two VCOs at lower frequencies, a large tuning range is achieved at mm-wave frequencies.

The proposed architecture is presented in Section II. Section III gives the circuit implementation and the results are summarized in Section IV.

II. Architecture

The proposed architecture of the 120GHz quadrature signal generator is shown in fig. 2a. Two coupled 48GHz oscillators generate the four quadrature phases. The out-

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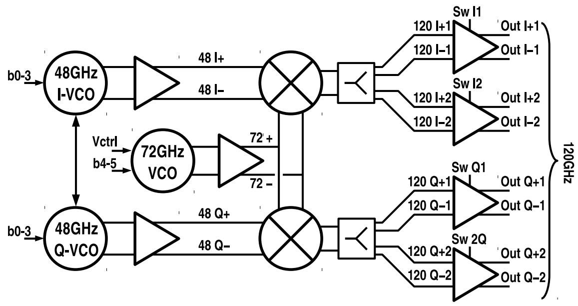
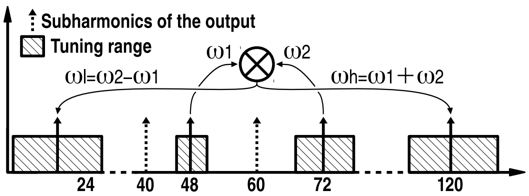


(a)



(b)

Fig. 2. (a) The proposed architecture of the 120GHz VCO containing two coupled 48GHz VCOs, a 72GHz VCO, two mixers, two output splitters and buffers, and (b) overview of the frequency locations in the system.

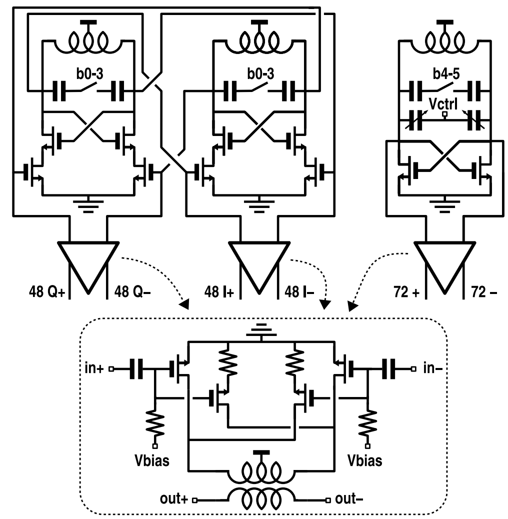


Fig. 3. The implementation of the 48GHz quadrature VCO (4 bit digital tuning), the 72GHz differential VCO (analog and 2 bit digital tuning) and their output buffer.

puts of the quadrature oscillators and a 72GHz oscillator are multiplied to produce the 120GHz quadrature signals. Differential buffers are placed between the oscillators and the mixers to avoid extra loading on the LC-tank of the oscillators. A large tuning range is achieved by controlling the frequency of both the 48GHz and the 72GHz oscillators and by making a combination of digital tuning (b_{0-3} and b_{4-5}) and analog tuning (V_{ctrl}). Due to the lower oscillation frequencies of both oscillators, a larger variable capacitance can be tolerated, which results in a larger tuning range. At the outputs of the two mixers, signal splitters and switchable buffers provide the ability to drive two isolated outputs with differential I/Q signals, e.g. for both a transmitter and a receiver. For measuring purposes one output is connected to a GSG probepad while the other quadrature outputs are downconverted by an on-chip mixer and baseband amplifier to measure the quadrature accuracy. The key advantage of this architecture is the signal generation at lower frequencies, which enables quadrature generation and large tuning range. Also with this set of frequencies, fundamental and harmonic coupling between an on-chip antenna and the VCO is avoided (see fig. 2b).

III. Circuit implementation

The circuit implementation of the 48GHz and 72GHz oscillators and their output buffer is shown in fig. 3. The 48GHz generation is based on a differential cross-coupled pair oscillator. The oscillation frequency can be tuned using 4 digital switched capacitors, of which the switch is a 41μm wide transistor with source and drain connected with a large resistor to ground. The result is 4 frequency steps of approximately 1.4GHz, giving a 5.5GHz tuning range for this VCO alone. Series coupled transistors guarantee the 90 degrees phase shift between both 48GHz oscillators. In comparison with the conventional parallel coupled quadrature oscillators, series coupling results in better phase noise and lower power consumption, but larger parasitic capacitance in the LC-tank [2]. The 72GHz VCO consists of a cross-coupled pair, an inductor, a varactor for analog tuning and two switched capacitors for digital tuning (42.5μm wide switches). The tuning range of this oscillator alone is 10.7GHz, resulting in a total tuning range of 16.2GHz. For the output buffers a neutralized differential pair is used. The neutralization guarantees stable operation and reverse isolation between the input and the output. At the input, series capacitors are placed to decouple the supply voltage of the oscillator and the bias voltage of the buffer. A transformer performs a conjugate match between the output of the buffer to input of the next stage. The power gain of the 48GHz and 72GHz buffers is 8.8dB and 5dB respectively.

The generation of the 120GHz quadrature signals from the 48GHz and 72GHz signals is realized with two gilbert cell mixers. Fig. 4 shows the implementation of the mixers. The output of the mixer is matched to the load using a transformer. This tuning also suppresses the 24GHz mixing product. The output of the mixer is split by a 3-coil transformer to provide a dual differential output e.g. to send

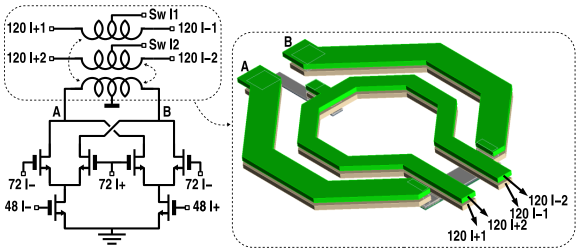


Fig. 4. The implementation of the gilbert cell mixers and the 3-coil output transformer.

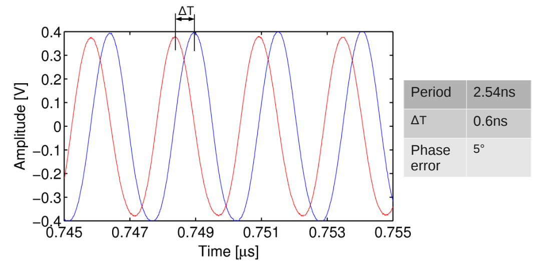


Fig. 7. Measured phase error of the downconverted I/Q signals.

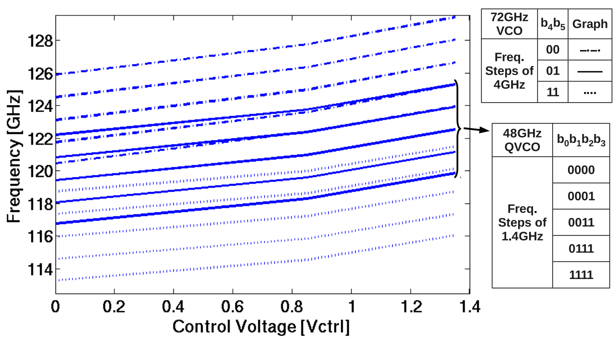


Fig. 5. Measured digital and analog tuning range.

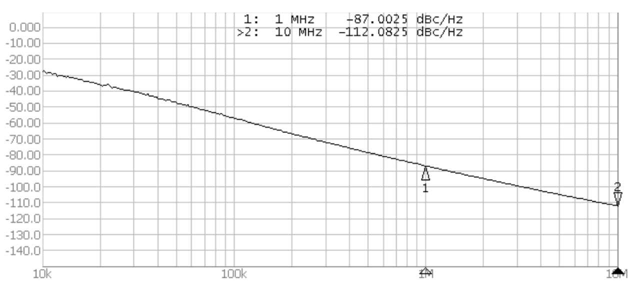


Fig. 6. Measured phase noise at 120GHz.

the quadrature LO to both a transmitter and a receiver. In the design of this transformer, advantage is taken of the fact that both top metal layers have the same thickness resulting in a more symmetric layout as shown in fig. 4. The 120GHz output of the mixers is buffered with neutralized differential pairs. For switching the buffers on or off, the bias voltages of the gates are connected to the center taps of the 3-coil transformer.

IV. Measurement Results

The circuit is fabricated in a TSMC 45nm LP CMOS technology with 7 metal layers. To measure the tuning range and output power, one of the output signals is connected to a GSG probe pad. The 120GHz output signal is measured with an external downconversion mixer and a spectrum analyzer. The results are shown in fig. 5. The analog tuning range around the center frequency of 120GHz is 3.3GHz and the output power varies from -25dBm to -27dBm. Since the output of the 72GHz oscillator is always larger than 0.35V, no excessive voltages are applied across the varactor when the control voltage goes up to 1.35V. Utilizing the digitally controlled capacitors in both the 48GHz and 72GHz VCOs, the frequency range goes from 113.2GHz to 129.4GHz. This means a tuning range of more than 16.2GHz or 13.5%. The output power varies from -23dBm to -30dBm over the entire frequency range. Note that even if the control voltage is limited to 1V, the analog tuning is sufficient to overlap the discrete tuning curves. The phase noise is measured using the delay-line method. The phase noise at the center frequency is -87dBc/Hz and -112dBc/Hz at 1MHz and 10MHz offset, respectively (see fig. 6). The 120GHz signals are also applied to an on-chip down conversion mixer. Using an external LO near 120GHz brings down the quadrature signals to a much lower frequency of a few hundreds of MHz. The output of the down conversion mixer is amplified and applied to an oscilloscope. Fig. 7 shows the down converted differential quadrature signals. The measured phase error and I/Q amplitude imbalance are 5 degrees and 0.67dB respectively. These numbers include the errors from the on-chip down conversion mixer and the measurement setup.

Intensive sweep measurements by injecting a very close adjacent carrier have been performed, and no pulling or spurious generation has been observed for signals around the 120 GHz generated signal. The measurement setup is shown in fig. 8. As example in fig. 9 a measurement of a -21 dBm injected interferer at an offset of 2MHz (marker 1) is shown, with no lock-in of the generated signal as a result. Note that the signal is measured with an external mixer, using an LO of 119.192GHz. The interferer is injected by radiating the chip with a 120GHz carrier and -21dBm incident power. Both the wanted signal and injected interferer are present at the output of the chip, but no locking or spurious generation occurs. This demonstrates the robustness of the proposed architecture against antenna-VCO coupling.

The DC power consumption, including the two VCOs

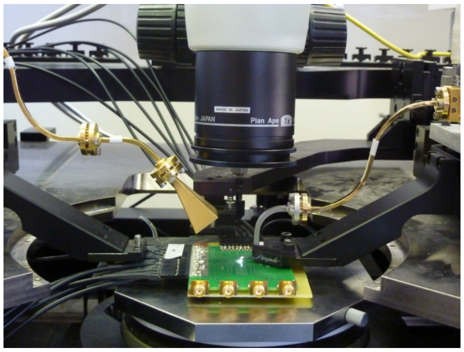


Fig. 8. Measurement setup to test the pulling behaviour of the QVCO.

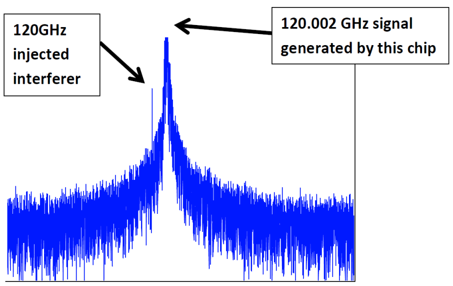


Fig. 9. Spectrum of the output signal of the QVCO. The injected interferer couples into the probe and is also visible in the spectrum. No change in frequency of the oscillator is observed.

(19%), buffers (35%), mixers (22%) and dual differential output buffers (24%), is 64mW. The results are compared against previous published D-band and mm-wave differential and quadrature VCOs in table I. The presented frequency generator has both the best tuning range and FOM of the mm-wave quadrature VCOs reported to date. A chip photograph is given in fig. 10. The chip size is 1mm^2 and the core area is 0.2mm^2.

TABLE I

Comparison with previous reported D-band VCOs and mm-wave QVCOs.

Ref	Freq [GHz]	P_{DC} [mW]	L(Δf) [dBc/Hz]	FTR* [%]	Type	FOM**
2009 [3]	115	6.2	-85@1MHz	4.4	Diff	-171.2
2010 [4]	118.3	5.6	-83.9@1MHz	7.8	Diff	-175.7
	122.5	2	-83@1MHz	4.4	Diff	-174.6
2008 [5]	90	75.7	-95@1MHz	3.3	Quad	-165.7
2011 [6]	58.2	22	-96@1MHz	4.35	Quad	-170.6
This work	120	64	-87@1MHz	13.5	Quad	-173.1
	120	64	-112@10MHz	13.5	Quad	-178.1

*Frequency Tuning Range

**$L(\Delta f) - 20log(f0/\Delta f \cdot FTR/10) + 10log(P_{DC})$

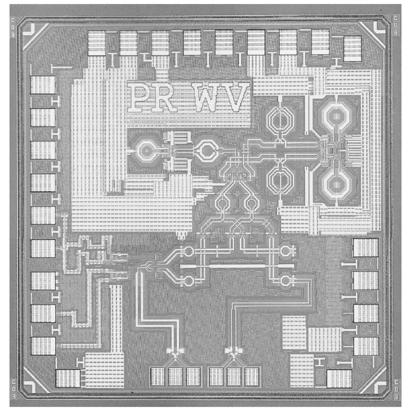


Fig. 10. Die photograph of the chip (1x1mm).

V. Conclusion

A 120GHz quadrature oscillator is presented. By muliplying the output signals of two independent oscillators, quadrature generation and large tuning range becomes feasible at 120GHz. Another major advantage of the architecture is that the output signal is not harmonically related to both oscillators, which enables integration with on-chip antennas. A record tuning range of 16.2GHz (13.3%) and a phase noise of -112dBc/Hz at 10MHz offset is measured.

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