A 6 GHz Input Bandwidth 2 $V_{pp\text{-}diff}$ Input Range 6.4 GS/s Track-and-Hold Circuit in 0.25 µm BiCMOS

Matthias Buck, Markus Grözing, Manfred Berroth, Michael Epp*, Sébastien Chartier*

Institute of Electrical and Optical Communications Engineering, University of Stuttgart, Germany
* Cassidian - EADS, Ulm, Germany

***Abstract* — A 0.25 µm SiGe-BiCMOS 6.4 GS/s track-and-hold circuit with an input bandwidth exceeding 6 GHz and up to 2 $V_{pp\text{-}diff}$ input voltage range applies a hold-mode muted preamplifier that reduces signal feedthrough and improves linearity. The track-and-hold circuit provides more than 59 dBc hold-mode SFDR3 for 1.0 to 6.0 GHz 1$V_{pp\text{-}diff}$ input signals at 6.4 GS/s, outperforming the best commercial THs operated at only 4 GS/s.**

***Index Terms* — Analog-digital conversion, analog integrated circuits, BiCMOS integrated circuits, dynamic range, linearity, signal sampling, silicon germanium.**

I. Introduction

Modern cellular, ultra wideband and cognitive radio receivers as well as agile broadband radar sensors are characterized by increasing instantaneous RF bandwidth to be processed. Due to the large bandwidth, the probability of strong interferers in the receive band increases and the reception of small signals gets more difficult. To avoid blocking and interference, the linearity requirements for the analog and mixed signal circuits in front of the analog-to-digital converter (ADC) quantizer increase. Third order nonlinear products are especially harmful.

To ease the application of advanced digital filtering, digital correction algorithms and to allow for fast reconfiguration of the receiver characteristics, ADCs with large input bandwidth, high conversion rate, high resolution and excellent linearity are required in front of the DSP section of the receiver. Moreover, direct sampling of the signal in the RF domain or at a high intermediate frequency avoids some problems of direct conversion receivers like DC offset, 1/f noise and quadrature phase matching for the IQ downconverters. The most challenging individual circuit block of an ADC that is suited for such broadband DSP-centric RF receivers is the front-end track-and-hold circuit (TH).

A highly linear TH demonstrator for sampling rates up to 6.4 GS/s with an input bandwidth exceeding 6 GHz is presented. The circuit performance is optimized for input frequencies in the 2nd Nyquist zone between 3.2 and 6.4 GHz. The circuit is implemented in a 0.25 µm SiGe-BiCMOS technology with a transit frequency of 180 GHz.

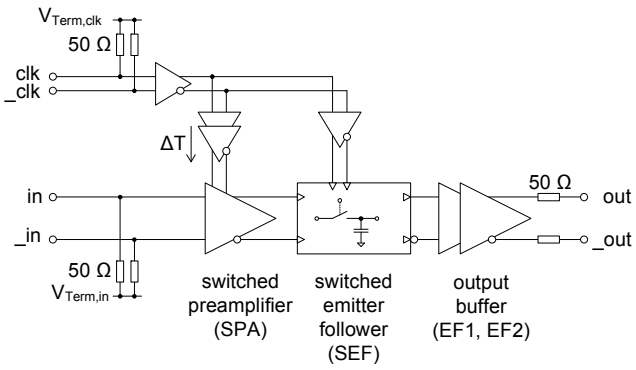

Fig. 1. Block diagram of the track-and-hold circuit.

The paper is organized as follows. The circuit topology is explained in section II. The measurement setup and the results are shown in section III. Section V concludes.

II. Circuit Design

Fig. 1 shows the block diagram of the TH. It is composed of a switched preamplifier (SPA, Fig. 2), a switched emitter follower (SEF, Fig. 3), a two-stage output buffer (EF1 and EF2, Fig. 3) and a clock driver. All circuits are fully differential.

The major sources of nonlinearity in a bipolar TH are the nonlinear preamplifier (PA) gain characteristic, the limited track time available to charge the hold capacitor (C_H) via the SEF and hold-mode signal feedthrough via the nonlinear base-emitter junction capacitance C_{BE} in the SEF. The error introduced by feedthrough increases with 20 dB/decade and is especially severe for RF frequencies.

The static linearity of the SPA is improved by resistive shunt feedback (R_E). An SPA voltage gain of one is achieved by setting 2 R_C approximately equal to $R_E/2$. The resistor values R_C and R_E are relatively large to get good linearity for large voltage swings, but the resistance values and corresponding voltage drops are limited by the 3dB-bandwidth requirement of about 6 GHz and also by the CE-breakdown voltages of the BJTs. The dynamic linearity requirement of the C_H charging process at the

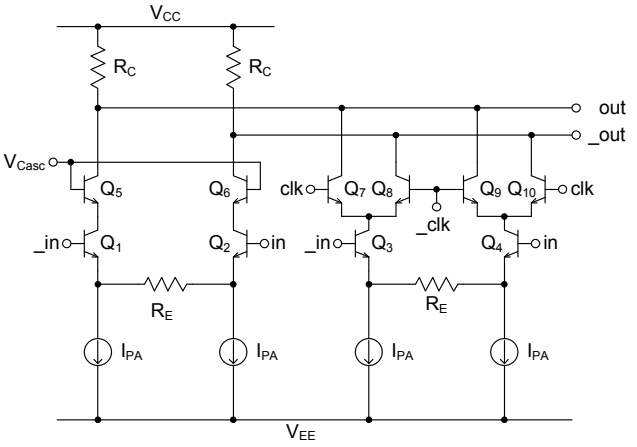

Fig. 2. Schematic of the switched preamplifier (SPA) with a first cascode transconductor on the left and a second transconductor with current-mode-switches for muting on the right.

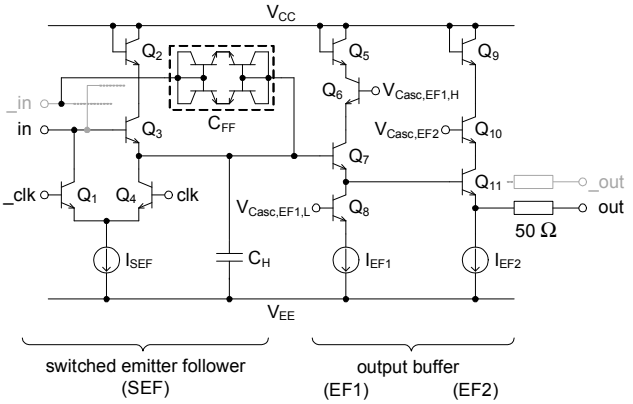

Fig. 3. Schematic showing one half of the differential switched emitter follower (SEF) and the cascaded two emitter followers (EF1 and EF2) of the output buffer.

maximum input signal frequency of 6 GHz is ensured by increasing the SEF tail current I_{SEF} and decreasing C_H.

A common method to cancel the feedthrough via C_{BE} is to use cross-connected C_{BE}-replica circuits C_{FF} [1]. But the cancelation of the feedthrough signal by C_{FF} is not accurate enough to achieve sufficient 3rd order harmonic rejection in the 2nd Nyquist zone.

In [2], a TH with additional feedthrough attenuation by muting the PA in hold mode is described. The muting is done by cancelation of the PA transconductor output current by an additional transconductor current in hold mode. Current-mode switches placed above the additional transconductor perform the clocked cancelation, resulting in a switched preamplifier (SPA) topology. Additional pedestal compensation is implemented in [2] by active feedback of the hold voltage across C_H to the SPA output in hold mode. Similar circuit topologies, but without pedestal compensation, are presented in [3] and [4].

Compared to the SPAs presented in [2], [3] and [4] the new SPA topology shown in Fig. 2 offers the following advantages. The SPA tail current utilization is doubled by using the differential output current of the switched transconductance stage in hold mode for cancelation and in track mode for amplification, instead of draining the current to V_{CC} in track mode. Moreover, perfect phase matching of the output currents of the two transconductance stages is achieved by using a cascode topology in the non-switched transconductance that is a replica of the switched transconductance stage topology in track mode. Pedestal compensation by active feedback is omitted in this work as it increases the SPA load capacitance and decreases the achievable voltage swing at the SPA output for a given BV_{CE} of the transconductance cascode transistors. The SEF is switched off some picoseconds earlier than the SPA to avoid attenuation of the hold voltage. Therefore an additional clock buffer is inserted into the SPA clock path.

The output buffer is set up by two cascaded emitter followers, the first one providing high input impedance to C_H and the second one providing the ability to drive the external 50 Ω measurement equipment with sufficient linearity margin. The output buffer implements 50 Ω source termination by additional series resistors to avoid reflections in the measurement setup. Due to the resulting output voltage division, due to the output resistance of EF2 and due to parasitic wiring resistance, the overall TH voltage gain is slightly smaller than ½. When the circuit is integrated with a quantizer on a single chip, the termination resistors are omitted and the voltage gain will be nearly one.

III. Measurement Setup and Results

The TH output signal is characterized on-wafer with the help of a 70 GHz input bandwidth two-channel subsampling oscilloscope, 40 GHz on-wafer probe heads and short phase matched cables. The input signal is made differential by a broadband 180° hybrid. The clock and

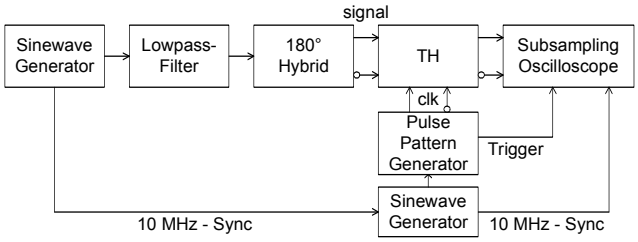

Fig. 4: TH measurement setup.

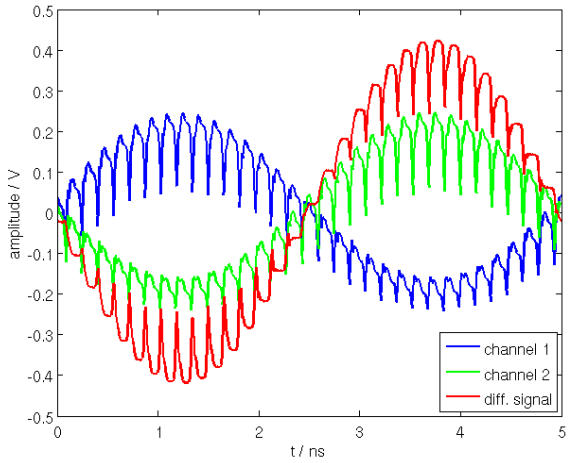

Fig. 5. Measured TH single-ended and differential output voltage @ f_{in} = 200 MHz, f_s = 6.4 GHz.

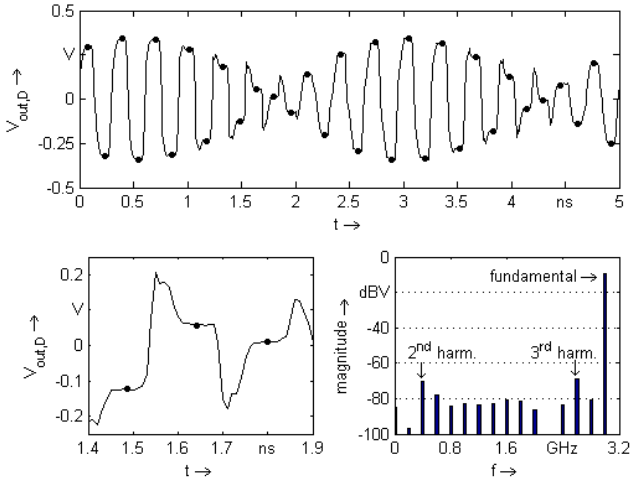

Fig. 6. Measured differential output signal $V_{out,D}$ for f_{in} = 3.4 GHz and f_s = 6.4 GS/s in time domain (32-DFT sampling points indicated, detail point placement shown in zoom) and in DFT frequency domain with fundamental and harmonic products indicated.

input signal generators are synchronized via the generators' 10 MHz reference (see Fig. 4). The subsampling scope is triggered by $f_{clk}/32$ pulses provided by a pulse pattern generator. The characterisation of the TH is done for input frequencies between 1 and 6 GHz, the frequency range being limited by the input signal generator's harmonic performance and filter availability.

Fig. 5 shows the TH single-ended and differential output voltages. The SPA transition from mute to gain mode that takes place some picoseconds after the SEF transition from hold to track mode causes f_S-periodic voltage drops that are intended by design.

At 6.4 GS/s, a 32-point DFT is calculated on a 5 ns long differential output waveform that is 64-times averaged by the scope to attenuate the scope's sampling head noise

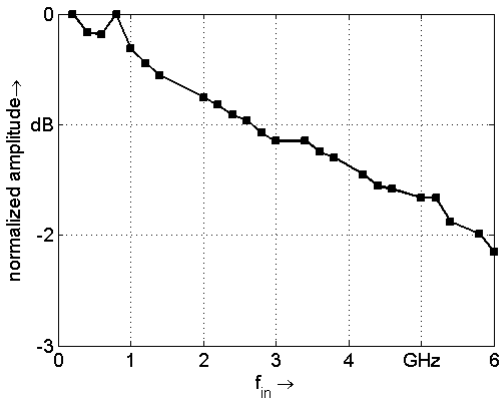

Fig. 7. TH frequency response. Normalized amplitude of sampled signal fundamental component versus input frequency.

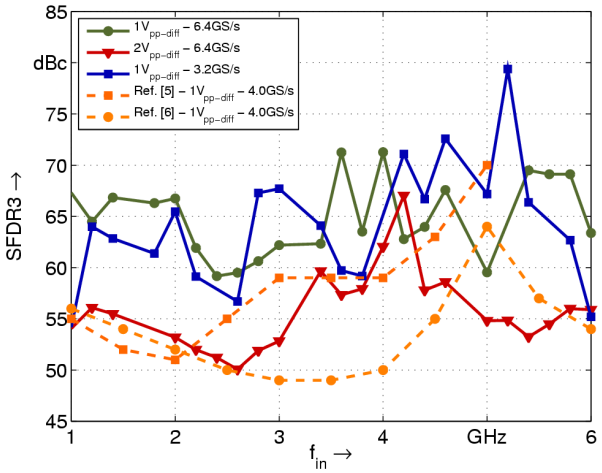

Fig. 8. Comparison of track-and-hold circuit hold-mode SFDR3 performance versus input signal frequency f_{in} with leading-edge commercial circuits [5, 6].

(Fig. 6). The DFT sampling points are placed in the centre of the hold time intervals to evaluate the hold-mode linearity performance of the circuit. Multiples of 200 MHz are allowed as input frequencies for the 32-DFT in the 5 ns window. The output fundamental and all nonlinear and noise components are then placed on 16 discrete frequency points between DC and 3.2 GHz.

Fig. 7 shows the frequency response of the fundamental component of the sampled signal versus input signal frequency. The fundamental output signal component at 6 GHz input signal frequency is 2.2 dB smaller than with a 200 MHz input signal, with the differential voltage swing at the input probe head held constant at 2 $V_{pp-diff}$. Thus the large-signal 3-dB bandwidth of the TH is considerably larger than 6 GHz.

Fig. 8 shows the hold-mode 3rd order spurious-free dynamic range (SFDR3) of the circuit and a comparison to two leading edge commercial circuits [5, 6]. The measure

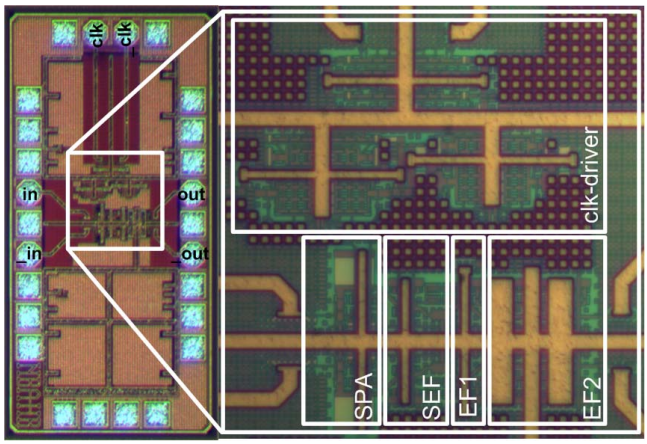

Fig. 9: Die photo of the demonstrator chip on the left with zoom to core circuit layout on the right.

hold-mode SFDR3 denotes the ratio of the fundamental tone magnitude to the spurious tone magnitude that is caused by 3rd order distortion [5]. This measure is taken in the discrete frequency domain calculated from time-domain samples in hold mode. The discrete frequencies range from DC to $f_S/2$ and thus cover one Nyquist band (refer to the discrete spectrum shown in Fig. 6).

At an input swing of 1 $V_{pp\text{-}diff}$, the TH operated at 6.4 GS/s outperforms the commercial circuits (operated at only 4 GS/s) at all input frequency points except 5 GHz, providing more than 59 dBc SFDR3 between 1.0 and 6.0 GHz. Even at an input swing of 2 $V_{pp\text{-}diff}$, i.e. two times the full scale input swing of the commercial circuits, the SFDR3 is better than 50 dBc between 1.0 and 6.0 GHz and better than 57 dBc between 3.4 and 4.6 GHz.

Fig. 9 shows the die photograph with the layout location of the SPA, the SEF, the output buffers and the clock driver indicated. The circuit is implemented in a 0.25 µm SiGe-BiCMOS technology with a transit frequency of f_T = 180 GHz. The die area is 1.1 mm^2 and the circuit core layout area is 260 µm x 300 µm. The power consumption of the chip is 470 mW from a 5.1 V supply.

VII. Conclusion

Table I summarizes the track-and-hold circuit parameters and performance and compares it with the reference circuits that provide measured data for hold-mode linearity. The TH provides improved SFDR3 performance at input frequencies of several GHz compared to leading-edge commercial products simultaneously with increased sampling rate. The high linearity of the circuit is achieved by preamplifier muting in hold mode and careful dimensioning of all sub components. This highly linear track-and-hold circuit will ease the implementation of frequency agile ultra wideband and cognitive radio receivers as well as radar sensors that use a large instantaneous RF bandwidth. Due to the implementation in a 180 GHz-f_T SiGe-BiCMOS technology, the track-and-hold circuit can be integrated with a high-performance quantizer and subsequent receiver DSP functions in CMOS, as well as with a RF front end on a single system-on-chip.

TABLE I.
TH Circuit Performance Summary and Comparison

Reference	**This work**	**[5]**	**[6]**
Process	0.25 µm SiGe BiCMOS f_T = 180 GHz	SiGe	SiGe
Full scale input voltage range	2 $V_{pp\text{-}diff}$	1 $V_{pp\text{-}diff}$	1 $V_{pp\text{-}diff}$
Max. sampling rate f_S	6.4 GS/s	4 GS/s	4 GS/s
3-dB input bandwidth	> 6 GHz	5 GHz	18 GHz
SFDR3 @ 1$V_{pp\text{-}diff}$, f_{in} = 1.0…6.0 GHz	> 59 dBc f_S= 6.4 GS/s	> 51 dBc f_S= 4 GS/s	> 49 dBc f_S= 4 GS/s
SFDR3 @ 2 $V_{pp\text{-}diff}$, f_{in} = 1.0…6.0 GHz	> 50 dBc f_S= 6.4 GS/s	-	-
SFDR3 @ 2 $V_{pp\text{-}diff}$, f_{in} = 3.4…4.6 GHz	> 57 dBc f_S = 6.4 GS/s	-	-
Die area	1.1 mm^2	-	-
Circuit core layout area	260 x 300 μm^2	-	-
Supply voltage	5.1 V	6.75 V	6.75 V
Power consumption	470 mW	1422 mW	1591 mW

References

[1] P. Vorenkamp, J.P.M. Verdaasdonk, "Fully bipolar, 120-Msample/s 10-b track-and-hold circuit," *IEEE J. Solid-State Circuits*, vol. 27, no. 7, pp. 988- 992, July 1992.

[2] T. Baumheinrich, B. Pregardier, U. Langmann, "A 1-GSample/s 10-b full Nyquist silicon bipolar Track & Hold IC", *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1951-1960, December 1997.

[3] X. Li; W.-M. L. Kuo; J. D. Cressler, "A 40 GS/s SiGe track-and-hold amplifier", *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) 2008*, October 2008.

[4] Y. Borokhovych, J.C. Scheytt, "10 GS/s 8-bit bipolar THA in SiGe technology," *NORCHIP Conference 2011*, November 2011.

[5] Hittite HMC760LC4B Wideband 4 GS/s Track-and-Hold Amplifier (DC – 5 GHz) data sheet, http://www.hittite.com/products/view.html/view/HMC760LC4B.

[6] Hittite HMC661LC4B Ultra Wideband 4 GS/s Track-and-Hold Amplifier (DC - 18 GHz), http://www.hittite.com/products/view.html/view/HMC661LC4B.