A 5–9-mW, 0.2–2.5-GHz CMOS Low-IF Receiver for Spectrum-Sensing Cognitive Radio Sensor Networks

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***Abstract* — A low-power, wideband CMOS receiver for spectrum-sensing cognitive radio sensor networks is presented. The low-IF receiver equipped with an inverter-based LNA-balun and I/Q sub-threshold rectifier enables low-power and high-speed spectrum sensing. For further extension to support higher data-rate radio systems, our local oscillator provides a frequency-dividing function when a low-phase-noise signal source is optionally used. A prototype chip fabricated in a 65-nm CMOS process can support a wide frequency range of 0.2–2.5 GHz with 43-dB maximum gain, 6-dB NF, and −9-dBm IIP3 and only occupies 0.6 mm^2 while consuming as low as 5–9 mW at a 0.6-V supply.**

***Index Terms* — Cognitive radio, spectrum sensing, wideband receiver, wireless sensor network.**

I. Introduction

Demand for energy- and spectrum-efficient, low-cost wireless sensor networks has been increasing for connecting a wide variety of sensors/machines to the cloud network. Cognitive radio capabilities enable the nodes/gateways to sense the radio environment for the sake of avoiding data collisions in a crowded situation (e.g., the 2.4-GHz ISM band), and to transmit data streams using a frequency band with a better propagation property (e.g., the UHF digital-TV band), which resulting in saving transmission power as well as efficiently using unoccupied spectrum resources [1]. In such a spectrum-sensing cognitive radio sensor network (CRSN) shown in Fig. 1, supporting multi-data-rate, multi-band systems with scalable power consumption makes it possible to improve wireless connectivity, expand field of application, and enable low-cost, large-scale production. In addition, when sending or receiving large data such as image files, the system can reduce power dissipation because extremely low duty-cycle operation is achievable [2]. A typical lifetime of an AA battery-powered sensor node exceeds a few years when it operates in 1% duty-cycle with its intermittently-activated radio that consumes 10 mW.

In this paper, we propose a low-power (5–9 mW), wideband (0.2–2.5 GHz) CMOS receiver that is capable of both spectrum sensing and radio-signal receiving. The key features of our chip are: A) low-intermediate-frequency (low-IF) architecture for low-power, high-speed spectrum sensing, B) an inductor-less wideband low-noise amplifier (LNA) with an embedded balun function for implementing a small-sized, low-power radio, and C) a local oscillator (LO) with a frequency-dividing capability for additionally supporting higher-data-rate radio systems.

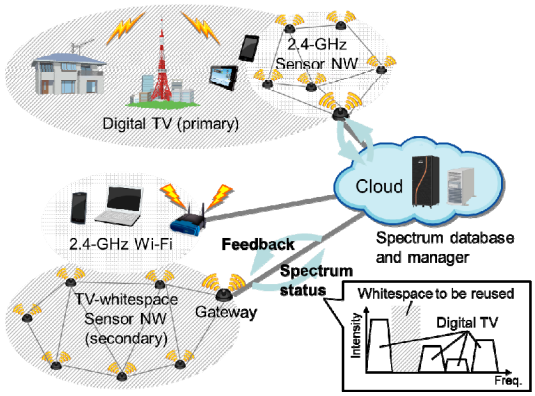

Fig. 1. Spectrum-sensing cognitive radio sensor network.

II. Architecture and Circuit Design

A. Low-IF Receiver Architecture

Figure 2 is a block diagram of the developed receiver, which is composed of a wideband LNA-balun, followed by a harmonic-rejection mixer (HRM), a complex band-pass filter (BPF), an energy detector, and a ring oscillator (RO) that can also function as a frequency divider when optionally utilizing a low-phase-noise LC oscillator. Although it is possible to integrate a phase-locked-loop (PLL) frequency synthesizer using the RO and LC oscillator, as also shown in Fig. 2, the PLL was not fully integrated in this prototype design.

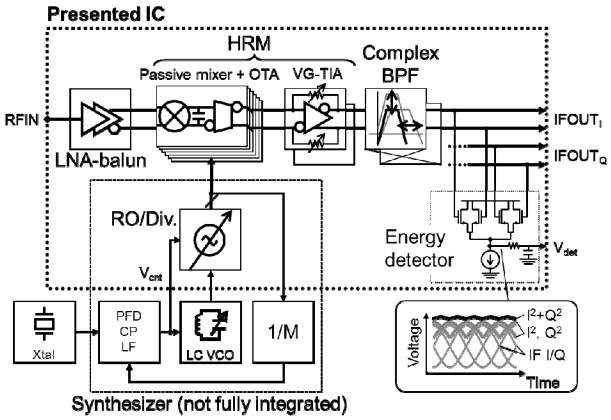

Fig. 2. Low-power, wideband low-IF receiver.

For the purpose of lowering operation duty-cycle and reducing power consumption of wireless sensor nodes, spectrum sensing should be executed in the shortest possible time. Low-IF receiver architecture can not only avoid large flicker noise, even with narrow detection bandwidth (BW), but also shorten settling time for energy detection compared with direct-conversion one. This is because the settling time for the low-IF detection is characterized by 1/IF, whereas that for the baseband is characterized by 1/BW, which is generally longer than 1/IF. The detection BW of our chip is defined by a source-follower-based, second-order complex BPF that employs only two-stacked transistors for low-voltage operation [3], and the BW can be tuned from 1 to 5 MHz by switching capacitor arrays. The IF is chosen to be 1.2 times the frequency of the BW; too large ratio of IF to BW increases the influence of thermal noise, whereas too small ratio makes it difficult to avoid flicker noise and image interference. The BPF also has a switchable gain stage in parallel with the input source-follower so as to reduce noise contribution from the following circuits.

For further settling-time reduction, our energy detector rectifies both in-phase and quadrature-phase (I/Q) IF signals and outputs the sum of I/Q rectified waveforms. Since the I/Q summation suppresses even-order harmonic components, the following passive filter can attenuate residual harmonics sufficiently by using only a small resister and capacitor, which makes spectrum sensing faster. This rectifier uses four strongly-nonlinear NMOS transistors biased in the sub-threshold region for low-power operation. Our simulation indicates the settling time within 5 μsec is possible for 1-MHz I/Q IF signals. A dynamic-range is about 20 dB with a single rectifier, and further expansion is easily achieved by cascading limiting amplifiers and rectifiers as is the case with a conventional received signal strength indicator circuit.

B. RF Front-end

In order to reduce size and cost of wireless sensor nodes, we propose an inductor-less wideband LNA with an embedded balun function, which also improves the receiver noise figure since an insertion loss of the off-chip balun can be removed. The proposed LNA, shown in Fig. 3, is composed of three CMOS inverters with resistive feedbacks. The first feedback (R_1) provides wideband impedance matching and the second one (R_2) generates an inverting signal. The feedback of R_3 from the negative-output port to the input cancels input capacitances due to its inductive behavior. The CMOS configuration enables low-power operation because the sum of NMOS and PMOS transconductances are obtained with reused bias current while canceling second-order distortion. In order to achieve low-voltage operation with a supply of 0.6 V or less, the NMOS and PMOS transistors are capacitively coupled and each transistor is biased in the near-threshold region, where the third-order nonlinear coefficient is small and transconductance per drain current (g_m/I_D) is large. The replica biasing circuit, shared among three inverters, also maintains the common mode level at a half of the supply voltage.

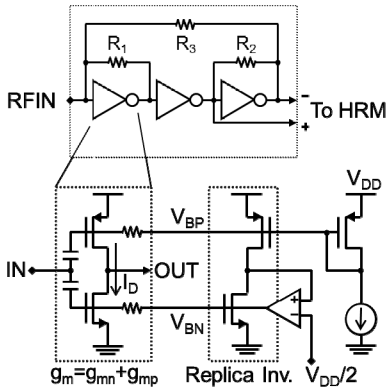

Fig. 3. LNA schematic.

The following HRM, which consists of three-phase I/Q passive mixers with capacitive loads, operational transconductance amplifiers (OTAs), and variable-gain trans-impedance amplifiers (VG-TIAs), down-converts the RF signal to the IF while simultaneously avoiding a harmonic mixing problem caused by LO harmonic components in order to relax the requirements for the off-chip filters. This mixer also works as a narrow-band, high-impedance load for the LNA around the LO frequency due to frequency translation effect of the capacitive impedance from the baseband to the LO frequency [4]. Thus, although the above-mentioned LNA alone amplifies the input signals including interferers over a wide frequency range, the narrow-band impedance matching and amplification are possible by means of this mixer, which improves linearity performance of the RF front-end.

C. LO Generator

LO frequency sweep time, as well as the settling time for energy detection, is also a major limiting factor in spectrum sensing. Considering only the use for energy-detection-based spectrum sensing and low-data-rate communication, a ring oscillator (RO) is suitable because its wide frequency tuning range allows the PLL to sweep the frequency while maintaining a locked condition, resulting in fast sweep time. It also provides scalable power consumption in terms of the operating frequency with small area occupancy.

To further extend our receiver for use with higher-data-rate radio systems based on a multi-level modulation scheme, we propose a CMOS-inverter-based RO with a frequency-dividing capability when low-phase-noise clocks are optionally provided. Figure 4 shows a schematic of the RO, which consists of four delay cells (D_{0-3}) that can also operate as D-latches (Fig. 5). The oscillation frequency is widely tunable by controlling the tail current when differential clocks (CK and CKB) are

not given (Fig. 6(a)). If CK and CKB are provided to the D-latches, this circuit is no longer an oscillator but a frequency divider. When $D_{0,2}$ are driven by the same clock (CK), and $D_{1,3}$ are driven by the opposite clock (CKB), it functions as a divide-by-four circuit, which is used for eight-phase LO generation (Fig. 6(b)). In contrast, when $D_{0,1}$ are driven by CK and $D_{2,3}$ are driven by CKB, this circuit works as a divide-by-two circuit since D_1 (D_3) only passes the D_0's (D_2's) output directly to the following D_2 (D_0) with a short delay, as shown in Fig. 6(c). This mode is for four-phase LO generation used when the carrier frequency is above 0.8 GHz, where the third-order harmonic frequency is out-of-band [3]. Since there is no need to change the LO signal paths to the HRM among these three operation modes, direct connection from this LO generator to the HRM is possible without any path selector. This means that the number of power-hungry LO buffers can be reduced thanks to the simple and compact chip layout with small parasitic capacitances. The poly-phase configuration of the LO buffers, a schematic of which is also shown in Fig.4, achieves sharp rising/falling edges even with a low-voltage supply.

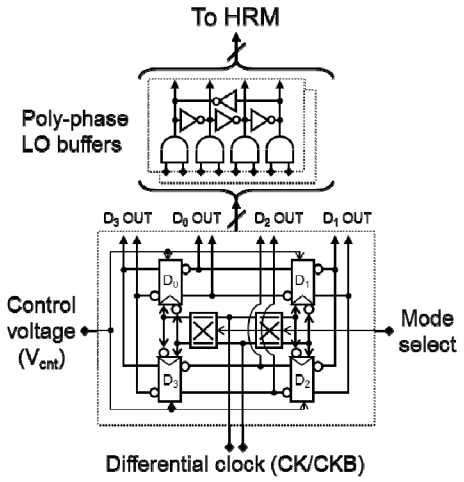

Fig. 4. LO generator schematic.

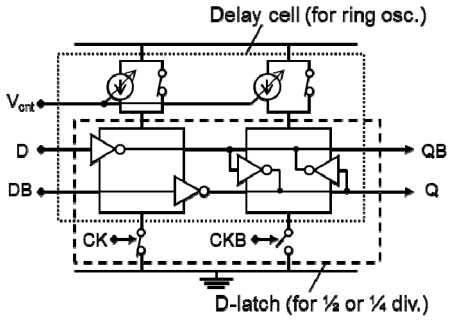

Fig. 5. Delay cell schematic.

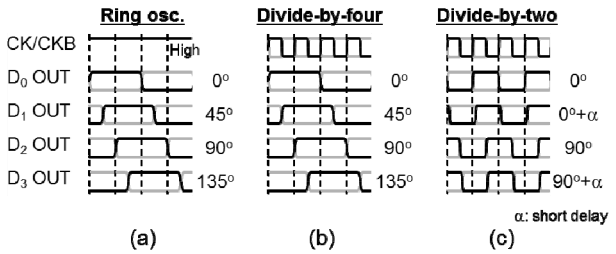

Fig. 6. Waveforms of LO signals.

III. Measurement Results

A prototype chip was fabricated in a 65-nm CMOS process. Figure 7 shows the measurement results of the receiver. A maximum gain of 43 dB and a noise figure (NF) of 6–9 dB were obtained over a wide frequency range from 0.2 to 2.5 GHz, which was limited by the LO generator. In-band second- and third-order input intercept points (IIP2 and IIP3) were also measured to be 20 dBm and −9 dBm, respectively, at 1 GHz, and out-of-band IIP3 was −7 dBm at 100-MHz frequency offset. Adopting passive mixers with lower on-resistance and larger capacitive loads will improve out-of-band linearity performance because it can provide further attenuation of out-of-band interference. The rejection ratios of third- and fifth-order harmonics and an image signal were more than 33 dB, 31 dB, and 27 dB, respectively, for available three samples. Figure 8 depicts the measured frequency characteristics of the tunable complex BPF with variable capacitance values. Further image suppression is possible with additional filters.

Table I compares measured performance with that of other recently published papers. Our receiver achieved comparable wideband operation with frequency-scalable, extremely low power consumption of 5–9 mW, including clock circuitry, at a 0.6-V supply (Fig. 9). In addition, it can support 0.4-V operation at up to 0.8 GHz and 0.5-V operation at up to 1.5 GHz as shown in Fig. 10. Figure 11 shows the die photograph of the developed chip, which occupies only 0.6-mm^2 active area.

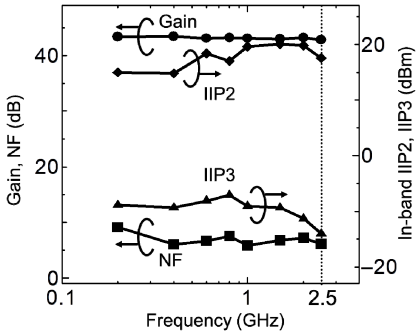

Fig. 7. Measured receiver performance.

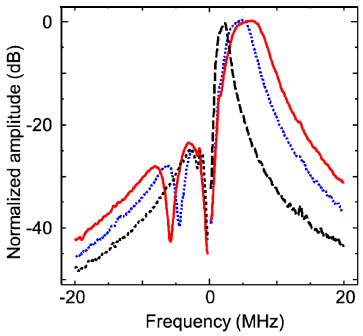

Fig. 8. Measured frequency characteristics of complex BPF.

TABLE I
PERFORMANCE SUMMARY

	This work	[3]	[4]	[5]	[6]	[7]
CMOS tech. (nm)	65	90	40	65	65	40
Active area (mm^2)	0.6	2.3	2	2	< 0.06	1.2
Freq. range (GHz)	0.2–2.5	0.03–2.4	0.4–6	0.1–2.4	1–2.4	0.08–2.7
BW (MHz)	1–5	0.2–30	0.4–30	20	5	N/A
Max. gain (dB)	43	67	70	70	30	70
NF (dB)	6–9	5–8	3	3–5	7–9	1.9
In-band IIP3 (dBm)	−9	−11	+6	−67	−20	N/A
3rd/5th HRR (dB)	33/31	42/42	N/A	35/43	N/A	42/45
Supply voltage (V)	0.6	1.2	1.1/2.5	1.2/2.5	1.2	1.3
Power cons. (mW)	**5–9**	**30–44**	**30–55**	**37–70**	**62***	**27–60**

* Exclude clock circuitry

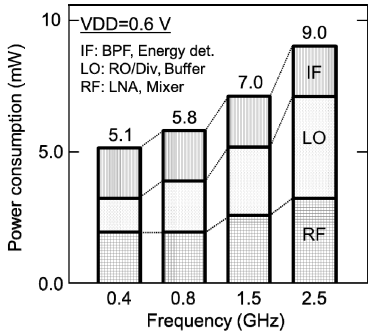

Fig. 9. Measured power consumption with 0.6-V supply.

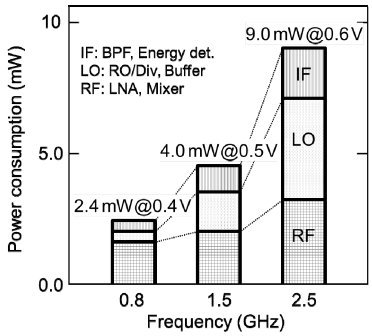

Fig. 10. Measured power consumption and maximum operating frequency with 0.4–0.6-V supply.

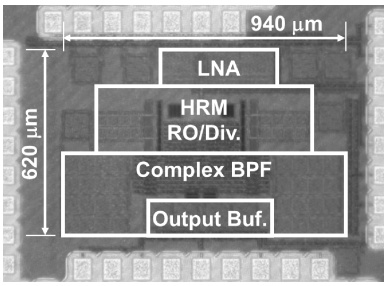

Fig. 11. Die photograph of prototype chip.

IV. CONCLUSION

A low-power, wideband CMOS low-IF receiver for CRSNs is presented. A prototype chip fabricated in a 65-nm CMOS process can support a wide frequency range of 0.2–2.5 GHz while consuming as low as 5–9 mW at a 0.6-V supply. This receiver equipped with an inductor-less LNA-balun and frequency-division-capable ring oscillator is a strong candidate for utilization as a building block for multi-data-rate, multi-band, spectrum-sensing CRSN systems in many application areas.

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