A Single Chip HBT Power Amplifier with Integrated Power Control

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***Abstract* — The GSM power amplifier market continues to drive towards low cost and small size, but remains reluctant to compromise on performance. Current generation PA products utilize InGaP HBT to deliver RF performance and integrate bias and control on a supporting silicon die. This approach is common amongst many PA manufacturers with the exception of CMOS PA [1] solutions. This paper describes a solution using an HBT BiFET [2] technology to integrate both the precision control function and power amplifier onto a common die. The resulting solution opens opportunity for industry leading size and performance at no additional cost or RF performance penalty.**

***Index Terms* — power control, power amplifiers.**

I. Introduction

Modern front-end modules (FEM) typically consist of a three die solution (see Fig. 1) including the quad band GaAs HBT power amplifier die, a silicon control die in a CMOS or BiCMOS technology, and a pHEMT antenna switch die. This solution is packaged within a 6 mm x 7 mm multichip module (MCM) using a laminate substrate with embedded inductance and discrete capacitor passives forming the match and filter functions. Next generation product must support a package size of 6 mm x 6 mm or smaller at a reduced cost. Although this smaller package could be achieved using smaller footprint passives, this introduces increased cost. The approach presented here eliminates one of the die from the existing solution and takes advantage of the area gained to reduce package size, while maintaining the lower component cost.

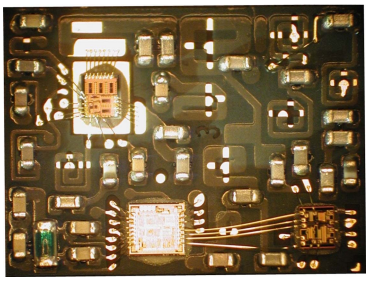

Figure 1. Previous Generation 6 mm x 7 mm, Three-die Solution

II. Current Sense Feedback

The current sense feedback architecture shown in Fig. 2 utilizes a discrete resistor placed in the collector of the HBT amplifier to sense amplifier current and control the output power through feedback in the amplifier bias. The voltage generated across the sense resistor ranges from 1 mV to 100 mV over the complete power control dynamic range, and requires a precision error amplifier for sensing.

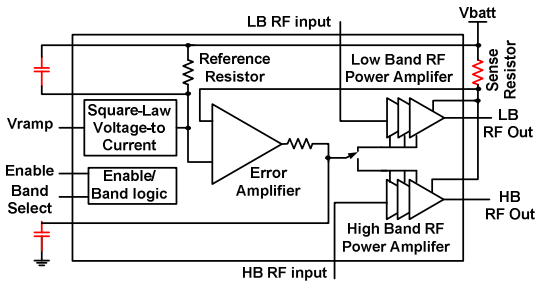

Figure 2. Block Diagram Detailing Current Sense Architecture

Key parameters of this error amplifier include low input offset to minimize part-to-part variation, low input offset temperature drift to minimize power control variation, and very low noise to ensure low noise power in the RX band of the transmit output spectrum. These three requirements can typically only be met in a simple analog design using bipolar devices. A second key aspect of the current sense architecture is the shaping of the power control transfer function to ensure low dB/V control slope for easy application with standard data converter resolutions. This shaping has been achieved through the use of an analog squaring function which provides a significant improvement over a single linear response as shown in Fig. 3. Again, a simple analog circuit solution for this squaring function can only be achieved using bipolar devices.

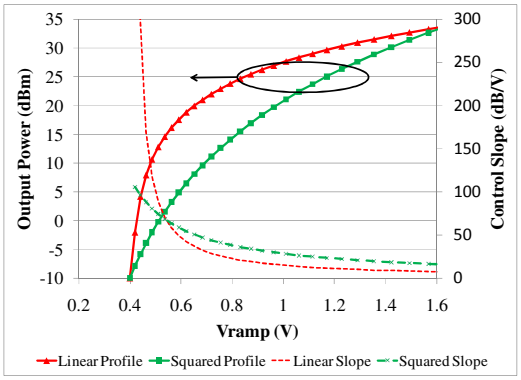

Figure 3. Control Transfer Function

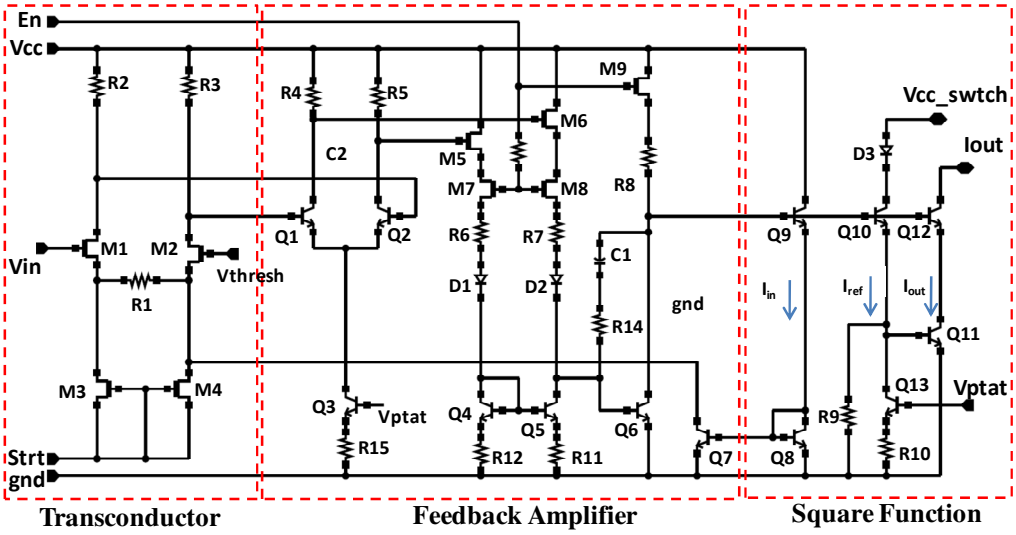

Figure 4. V-I Squaring Circuit

III. Voltage to Current Squaring Function

The V-I squaring schematic is shown in Fig. 4. This design performs the task of translating the input Vramp signal into a current and shaping it to reduce the power control slope. It is desired that the input be high impedance, CMOS compatible input. A BiFET input device was used in a differential configuration providing low input common mode as well as cancelling the extreme threshold variation of the FET. An architecture was selected which incorporates the V-I within a feedback loop along with the squaring function[3]. An op-amp is used to sense the differential output of the basic transconductor and introduce an error current in the feedback which maintains a balanced current density of both BiFET devices within the differential input pair. This error current ultimately becomes the input to the squaring circuit. The V-I with feedback exhibits multiple steady-state operating points and requires a start-up current, provided by M3 and M4. Miller compensation (C1) is used for the V-I feedback loop to minimize the amount of circuit area. The squaring function is obtained through logarithmic arithmetic using the exponential characteristic of the bipolar devices Q8 – Q12 and results in the transfer function of equation 1, 2.

$$I_{out} = I_{in}^{2}/I_{ref} \quad (1)$$

$$I_{in} = (V_{in}-V_{thresh})/R_1 \quad (2)$$

Iref is a bandgap-based current formed by summing a PTAT current with the Vbe_{Q11}/R9 current at the emitter of Q10. The squared output current is later sourced across a resistance (R16 of fig. 6) to create the control loop reference voltage. The result is an output voltage which has a square law relationship relative to Vramp and is completely process, temperature and supply independent. Measured characteristics of this V-I circuit over supply and temperature are shown in Fig. 5. PA output is related to the Log of output current which requires precision at low Vramp levels and tolerates variation at higher Vramp levels.

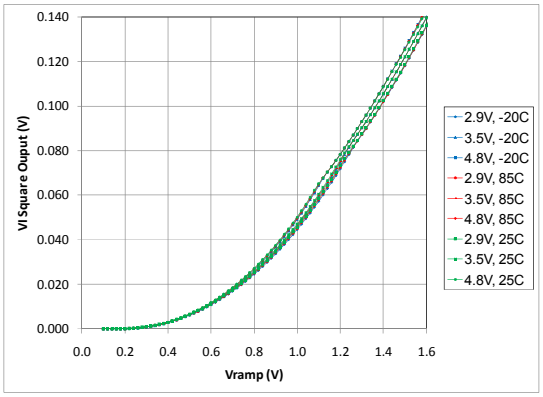

Figure 5. Measured V-I Squaring Response

IV. Error Amplifier Design

The schematic for the error amplifier is shown in Fig. 6. The error amplifier consists of a three-stage design providing 60 dB DC gain. The first stage incorporates a differential bipolar input pair (Q1,2) which meets the offset and noise requirements and supports a common mode interface with the battery voltage for sensing of the feedback signal. An intentional 1 mV offset is introduced

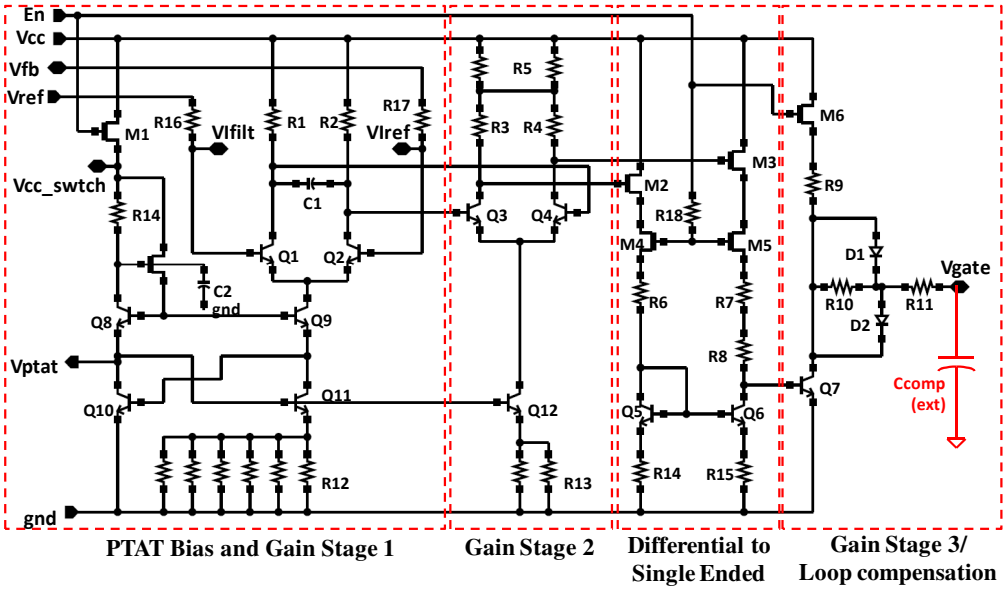

Figure 6. Error Amplifier Schematic

through an un-balanced resistive load (R1,2) to compensate for random input offsets. This first stage is followed by a second differential gain stage before conversion to single-ended and driving the output common emitter gain stage. The output stage must support a full rail-to-rail signal swing to cover the entire dynamic range of the PA bias profile and is implemented with a switched resistive load to supply. Given that the design must support a supply variation of 2.9 V to 4.8 V, a significant challenge exists in the translation of the supply-referenced differential signals to the ground-based single-ended signal. The differential to single-ended conversion stage utilizes BiFET source followers (M2,3) and resistive level-shifting to drive an NPN mirror for high supply rejection resulting in minimal input offset drift over supply. BiFET switches (M4,5) are used to disable the currents in the level-shift for sleep-mode performance. Stages 1 and 2 are biased with a conventional PTAT bias which maintains a constant transconductance in the error amp, and minimizes the temperature drift of input offsets. This PTAT bias is also used as a common reference for the other control functions within the die design.

V. RF Amplifier and Bias Interface

The power amplifier bias interface is shown in Fig. 7. The output of the error amplifier is filtered with a single pole R-C filter which suppresses noise, limits slew rate, and ultimately forms the dominant pole for compensation of the power control feedback loop. The output of this filter then drives the gate of the BiFET source follower M1. Band selection for the high and low band control is accomplished through BiFET switch devices (M2,3) in the source of the primary BiFET bias device. High impedance control of the gates to these BiFET switch devices limits the gate current and allows the switch bias to float as the parasitic Schottky junction becomes forward biased over the dynamic range of the PA bias. Moderate pull-down currents are used to bias the BiFET follower and ensure sufficiently low output bias voltage.

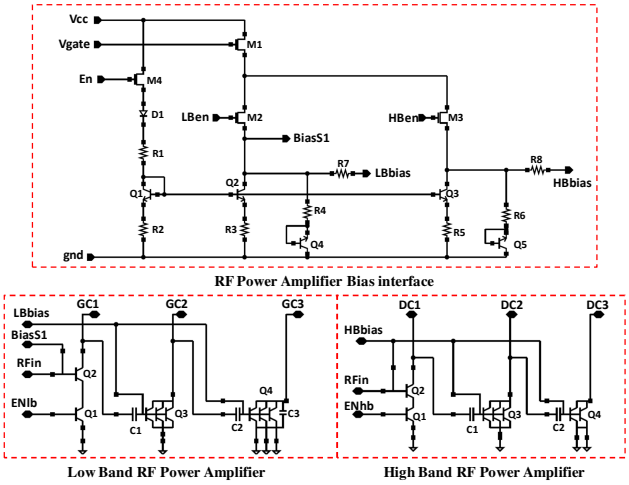

Figure 7. PA Bias Driver Interface

VI. Final Module Solution

The total HBT die size is 785 um x 1345 um and is shown in Fig. 8. The complete design is assembled into a 6 mm x 6 mm MCM package along with the SOI RF switch die as shown in Fig. 9. Top level module performance confirms the individual block level performance. The

measured results of Fig. 10 demonstrate that the power control accuracy over temperature and supply meets 3GPP specifications with margin. The transient performance of the control loop formed with the error amplifier closed around the PA is shown in the Fig. 11 – demonstrating compliant GSM transmit burst operation with spectrally compliant envelope shaping over all supply and temperature conditions.

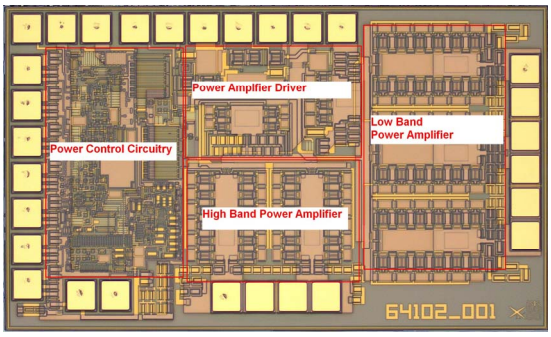

Figure 8. Amplifier Die with Integrated Power Control

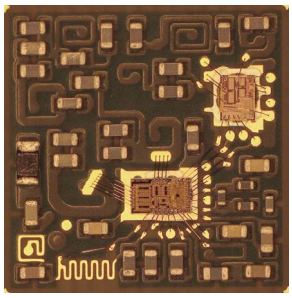

Figure 9. Complete 2-die, 6 mm x 6 mm Module Solution

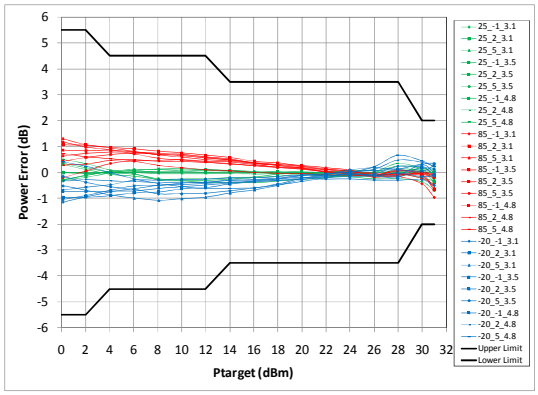

Figure 10. Power Control Accuracy

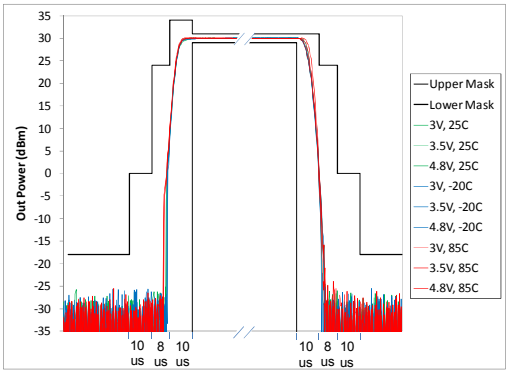

Figure 11. GSM Transmit Burst Performance

VII. Conclusion

A solution has been described which integrates the complete bias and power control function onto a single BiFET GaAs HBT power amplifier die for the GSM market. This solution is capable of meeting all system specifications and offers silicon-level integration with HBT RF performances.

Acknowledgement

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