PREPARED BY: David Hsu and James Pau		DOCUMENT NUMBER: NPB PS-0947
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R50 RELIABILITY REPORT FOR FAB 3 SBC18H2 PROCESS

REVISION	REVISION DESCRIPTIONS	DATE
01	Initial Release	02/10/2009
02	Add EM and MIM test results	03/23/2009
03	Add HTOL and SBC18HX PLR test results	07/31/2009
04	Allow external distribution and identify raw qual data location	09/30/2009
05	Add all package level reliability test results	10/19/2009
06	Corrected FAB Location from FAB 1 to FAB 3	05/02/2011

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Summary

This report summarizes the results obtained from reliability tests of the FAB 3 SBC18H2 Process. The purpose of this report is to measure reliability at wafer level and package level, highlight potential quality problems, and implement and verify corrective actions.

FAB 3 SBC18H2 process has successfully completed all wafer level reliability tests and package level reliability tests according to TowerJazz process qualification. The process meets all reliability requirements for Production Release.

Process Description

Manufacturer: TowerJazz
Facility: Newport Beach, CA
Basic Process: Built on the 1.8V and 3.3V FETs of CA18 CMOS process backbone

SBC18H2 process overview

- 6 layers of aluminum metals
- 1.8V and 3.3V FETs and also includes a 1.8V MOS Varactor
- High speed NPNs with Ft = 200 GHz
- Low voltage (high speed) and medium voltage (standard speed) NPNs with deep trench
- The 1.8V / 3.3V devices are built on gate oxides with as-grown (optical) thicknesses of 26 and 57 angstroms respectively
- Metal, low value unsilicided, unsalicided poly, high value unsalicided poly, silicided poly, and nwell resistors
- 2fF/um^2 MIM capacitor on Metal 4.
- Metal resistor between Metal 3 and Metal 4
- The MIM capacitor is between Metal 4 and Metal 5.
- The Via 4 is 2um in height and Metal 5 is 1.6um thick aluminum
- High performance junction Varactor
- Deep Nwell (triple well) isolation layer, and
- Inductors using 2.8um thick aluminum top metal layer (Metal 6) and 2um thick top via layer (Via 5)

Applicable documents

- NPB PS-0179: SBC18 Design Rules
- NPB PS-0267: SBC18 Electrical Specifications
- NPB PS-0140: SBC18 Mask Requirement Specifications
- NPB-PS-0542: Design Application Note for SBC18H2
- NPB-PS-0500: MiniPic Manual - MP050 Narrow Scribe PCM for SBC18HA, SBC18HX, SBC18HXL, SBC18HKL and SBC18HK Processes
- NPB-PS-0570: MiniPic Manual - MP088 for SBC18H2 Process

Test Vehicle Description

PCM Structure Description

The MP088 Process Control Monitor (PCM) monitors SBC18H2 process, and it is the same as MP050, the Process Control Monitor (PCM) for monitoring SBC18HA, SBC18HX, SBC18HXL, SBC18HKL and SBC18HK processes. For details, refer to “NPB PS-0570” and “NPB PS-0500”.

MOSFET’s

					Pads				
Dev.	Standard FETs	Type	Width	Length	Source	Drain	Gate	Body	Module
1	FET_10xP18N	N 1.8v	10	0.18	10	9	7	16	NL
2	FET_10xP36N	N 3.3v	10	0.36	10	9	7	16	NH
3	FET_10xP18P	P 1.8v	10	0.18	10	9	7	16	PL
4	FET_10xP30P	P 3.3v	10	0.30	10	9	7	16	PH

EM

Dev.	Electro-Migration	Width (um)	Space (um)	Length (um)	Pads					Module
					IH	VH	VL	IL	Bridge	
1	EM_M1_CT	0.23	0.23	375	10	11	13	14	15	EM
2	EM_M2_V1	0.28	0.28	375	16	17	19	20	15	EM
3	EM_M6_V5	2.5	N/A	375	19	20	21	22	N/A	EM

BJT’s

Dev.	NPN Transistors	Emitter Size (um)	Pads				Module
			Collector(s)	Base	Emitter	Sub	
1	NPN_LV_P76	0.15[A] x 0.76	1	2	4	16	T1
2	NPN_HV_P76	0.15[A] x 0.76	3	7	4	16	T1
3	NPN_HS	0.15[A] x 0.76	8	9	15	14	T3

Note A – NPNs for other SBC18HX are 0.2 x 0.76 (um)

TDDB

					Pads			
Dev.	Capacitor/TDDB Structure	Type	Area (um^2)	Perimeter (um)	POLY	N+	Body	Module
1	TDDB_EXT_1.8v_N	N-CH Area/Edge	53231	32700	26	25	24	NL
2	TDDB_EXT_3.3v_N	N-CH Area/Edge	53231	32700	26	25	24	NH
3	TDDB_EXT_1.8v_P	P-CH Area/Edge	53231	32700	26	25	24	PL
4	TDDB_EXT_3.3v_P	P-CH Area/Edge	53231	32700	26	25	24	PH

MIM CAP

					Pads			
Dev.	MIM Capacitor	Type	Area (um^2)	Perimeter (um)	TM	M4	Body	Module
1	MIM_CAP	MIM	60000	24000	26	25		RC

Package Description

Die information:

1) Die Number: “RFQ” A0132_RH_002 gds from A0974 MPW
2) Die Size: 2.554mm x 2.554mm;
3) Operating Voltage: 3.3V IO, 1.8V & 3.3V Core

Assembly and Package Information:

1) Package Family: 64 LQFP
2) Package Supplier: Quik-Pak
3) Package Dimensions: 10mm x 10mm x 1.4mm
4) Backgrind to 11 mils
5) Die Attach: QMI529HT
6) Wirebond = 1.2mil
7) Mold Compound = FP4323
8) Branding method = Ink

Wafer Level Reliability Tests Summary

Tests	Reference	Sampling Plan	General Test Conditions	Acceptance Criteria	Results	Conclusion
Hot Carrier Injection (HCI)	JESD28	3 lots, 1 wafer per lot, 3 or 4 stress conditions per wafer, 1 device per stress condition	At 25°C, bias drain and gate to develop peak substrate current and accelerate degradation	At 25°C, lifetime > 0.2 years at 1.1* *Vcc*	See Test Results	Pass
Threshold Voltage Stability (TVS)	N/A	3 lots, 1 wafer per lot, 1 device per wafer	At 150°C, bias gate at 1.1* V_{CC} for 24 hours to accelerate threshold shift	At 25°C, V_T shift < 15%	See Test Results	Pass
Reverse Beta Degradation	N/A	3 lots, 1 wafer per lot, 4 stress conditions per wafer, 1 device per stress condition	At 25°C, reverse-bias base-emitter junction from -3.1V to -2.6V to accelerate degradation	At 25°C, lifetime > 10 years at *Vbe* = -1V	See Test Results	Pass
Gate Oxide Integrity (GOI)	JESD35	Divide the total PCM capacitors failures by total PCM area to calculate defect density (total area > $1cm^2$)	At 25°C, use current source to screen for short failures and use V-Ramp to screen for weak failures	D_o < 6 defects/cm^2	See Test Results	Pass
Electro-migration (EM)	JESD63	M1, M2 and top layers, 16 metal lines per layer	Stress metal lines at 240°C and accelerated current density to accelerate the resistance change	At 85°C and max allowed current density, T_0.1% > 10 years	Inferred	Pass
MIM Capacitor Integrity	JESD35	Divide the total PCM capacitors failures by total PCM area to calculate defect density (total area > $1cm^2$)	At 25°C, use current source to screen for short failures and use V-Ramp to screen for weak failures	D_o < 3 defects/cm^2	Inferred	Pass
Passivation Integrity	MIL-STD-883E method 2021.3	1 lot	Thermal shock & overcoat pinhole etch	D_0 < 1 in^{-2}	0	Pass

Test Results

Hot Carrier Injection

	Lot	Wafer	Lifetime (years)	Criteria	Pass/Fail
1.8V_NFET_HCI	K71632	19	3.27	>0.2 year	Pass
	K75693	2	6.10	>0.2 year	Pass
	K67324	16	3.33	>0.2 year	Pass
3.3V_NFET_HCI	K71632	19	2.05	>0.2 year	Pass
	K75693	2	1.08	>0.2 year	Pass
	K67324	16	0.55	>0.2 year	Pass

Threshold Voltage Stability

	Lot	Wafer	Vt shift	Criteria	Pass/Fail
1.8V_PFET_TVS	K71632	19	2.36%	<15%	Pass
	K75693	2	4.65%	<15%	Pass
	K67324	16	4.54%	<15%	Pass
3.3V_PFET_TVS	K71632	19	8.24%	<15%	Pass
	K75693	2	7.17%	<15%	Pass
	K67324	16	7.83%	<15%	Pass
1.8V_NFET_TVS	K71632	19	0.22%	<15%	Pass
	K75693	2	0.43%	<15%	Pass
	K67324	16	1.05%	<15%	Pass
3.3V_NFET_TVS	K71632	19	0.34%	<15%	Pass
	K75693	2	0.51%	<15%	Pass
	K67324	16	1.03%	<15%	Pass

Beta Degradation

	Lot	Wafer	Lifetime (years)	Criteria	Pass/Fail
Beta Degradation (Reversed)	K71632	1	30354	>10 years	Pass
	K75693	1	457	>10 years	Pass
	K67324	19	107	>10 years	Pass

Thin Gate Ox V-Ramp Data Summary

This table summarizes the thin gate V-Ramp test results from the thin gate structures:

#Lots	Type	#Samples Tested	Area (cm^2)	# Weak Fails	Weak Defects/cm^2
27	n-channel	1282	0.78	0	0
27	p-channel	1282	0.78	0	0

Combining the n-ch and p-ch data, no weak failures were seen in a tested area of 2.96 cm^2.

Thick Gate Ox V-Ramp Data Summary

This table summarizes the thick gate V-Ramp test results from the thick gate structures:

#Lots	Type	#Samples Tested	Area (cm^2)	# Weak Fails	Weak Defects/cm^2
17	n-channel	841	0.511	1	1.95
17	p-channel	809	0.49	0	0

Combining the n-ch and p-ch data, one weak failure was seen in a 1cm^2 tested area.

Electromigration

Since metal schemes are the same for SBC18H2 and all other SBC18 processes which are already in full production, we don't need to run separate qualification tests for Electromigration. Therefore, the EM test results can be inferred from our Quarterly On-going Reliability Monitoring Report. Also, M1 and M2 reflect the tightest design rules of any process, and MT with unique metal thickness. Therefore, running EM on M1, M2, and MT is justified and there is no need to run EM on other metal layers.

Metal Layer	Reference	Sample Size	Test Conditions	Acceptance Criteria	Test Results
M1	Q3, 2008 ORM	16	Stress metal lines at 240°C and accelerated current density	At 85°C and max allowed current density, T_0.1% > 10 years	1.01E+03 yrs
M2					3.58E+02 yrs
MT					8.06E+02 yrs

MIM

Since MIM schemes are the same for SBC18H2 and all other SBC18 processes, we can also infer MIM test results from our Q3, 2008 Quarterly ORM Report:

MIM Type	#Samples Tested	Area Tested (cm^2)	# of Failures	# of Shorts	# of Weaks	Total Do/cm^2	Shorts D0/cm^2	Weaks Do/cm^2
M3M2	24031	14.42	13	3	10	0.90	0.21	0.69
M4M3	11900	7.14	2	2	0	0.28	0.28	0

Wafer Level Reliability Testing Methodologies

Hot Carrier Injection (HCI) of I_{SUB} Model

Reference	JESD28: A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation Under DC Stress
Model	For devices with separate drain and substrate, use I_{SUB} Model: T = C (I_{sub}/W)^(-B)
Sampling Plan	3 lots, 1 wafer per lot, 3 or 4 stress conditions per wafer, 1 device per stress condition
General Test Conditions	At 25°C, bias drain and gate to develop peak substrate current and accelerate degradation
Acceptance Criteria	At 25°C, lifetime > 0.2 years at 1.1* *Vcc*
Method	HCI test is performed at 25°C on the minimum channel length NMOS device in the PCM structure. Four stress conditions are derived by sweeping gate voltages under different drain voltages to achieve peak substrate currents (I_{sub}), under the condition that the I_{sub}/Device Width ≅ 20μA/μm to ensure HCI effect. The derived stress conditions ensure truly maximum substrate current and therefore are more accurate than the condition of V_{gate} = ½ $V_{dtrain.}$ For each stress condition, one virgin device is stressed on the drain and gate, with substrate and source grounded, and drain current (I_D) at 1.1* *Vcc* is recorded periodically. Log(% ΔI_D) versus log(Time) is generated for the each stressed device. The time to achieve a 10% reduction in forward saturation drain current (I_{Dsat}) is derived from measurement, given that data follow a linear trend line. For each stress condition, I_{sub} is also recorded. These "10% reduction times" verses the I_{sub} are plotted on a log-log scale with a power-fitting trend line from MS Excel. The HCI lifetime is then derived by extrapolating the trend line to the 1.1* *Vcc* operation point. TowerJazz requires this HCI lifetime be greater than 0.2 years at 1.1* *Vcc*.

Threshold Voltage Stability (TVS)

Reference Procedure	N/A
Model	N/A
Sampling Plan	3 lots, 1 wafer per lot, 1 device per wafer
General Test Conditions	At 150°C, bias gate at 1.1* V_{CC} for 24 hours to accelerate threshold shift
Acceptance Criteria	At 25°C, V_T shift < 15%
Method	TVS test is performed on the minimum channel length PMOS/NMOS devices in the PCM structure. The procedure for one device is as follows: 1. Measure the threshold voltage (V_{T0}) at 25°C with peak-beta method; 2. Heat up the device to 150°C while 1.1* *Vcc* is applied at gate, with substrate, drain and source grounded; 3. Keep the device at 150°C for 24 hours; 4. Cool down the device to 25°C while 1.1* *Vcc* is applied at gate, with substrate, drain and source grounded; 5. Measure threshold voltage (V_{T+}) with peak-beta method; 6. ΔV_T = (V_{T0} - V_{T+})/ $V_{T0;}$ 7. TowerJazz requires $\lvert\Delta V_T\rvert$ < 15%.

Reverse Beta Degradation

Reference	N/A
Model	T = C*EXP(-B* V_{be})
Sampling Plan	3 lots, 1 wafer per lot, 4 stress conditions per wafer, 1 device per stress condition
General Test Conditions	At 25°C, reverse-bias base-emitter junction from -3.1V to -2.6V to accelerate degradation
Acceptance Criteria	At 25°C, lifetime > 10 years at *Vbe* = -1V
Method	Reverse Beta Degradation test is performed at 25°C on the minimum-sized standard NPN device in the PCM structure. At one of the four stress voltage levels ranging from -3.1V to -2.6V, two virgin devices are stressed at the base-emitter junction. For each device, beta ($\beta = I_{CE} / I_{BE}$) is recorded periodically at the point where I_{CE} = 100μA in the Gummel Plot. Then (beta degradation $\Delta\beta$% on linear Y axis) vs. (stress time on log X axis) is plotted. For each NPN device, the time to achieve a 10% reduction in beta degradation ($\Delta\beta$%) is derived from the data, given that the data follows a linear distribution. Then (the "10% reduction times" on log Y axis) vs. (V_{EB} on linear X axis) is plotted. The lifetime to reach 10% beta degradation (I_{CE} = 100μA) at V_{BE} = -1V is derived from an exponential-fitting trend line. TowerJazz requires that this lifetime be greater than 10 years.

Gate Oxide Integrity (GOI)

References	JESD35: Procedure for Wafer-Level Testing of Thin Dielectrics; Chenming Hu "Projecting Gate Oxide Reliability and Optimizing Reliability Screens"
Model	V-Ramp
Sampling Plan	Divide the total PCM capacitors failures by total PCM area to calculate defect density (total area > 1cm^2)
General Test Conditions	At 25°C, use current source to screen for short failures and use V-Ramp to screen for weak failures
Acceptance Criteria	D_o < 6 defects/cm^2
Method	Voltage-ramp test is performed at 25°C to evaluate the extrinsic behavior of the gate oxide. Type "A" failures or shorts are tested by applying 1.0μA force on the gate. A device with a gate voltage exceeding V_{CC} is considered to have a Type "A" or "short" failure and will not continue testing for type "B" failures. If the device passes the "shorts" test, then a staircase voltage ramp (50mV per step) is applied on the gate at a rate of 2V/second from V_{CC}. A device is considered to have a Type "B" or "weak" failure if : 1) a gate current exceeds 10mA, or 2) the current is 5 times greater than the current measured at the previous step. If the site passes GOI test, theory projects that the device's GOI lifetime is greater than 10 years for a 1.8V device to sustain above 4V, a 3.3V device to sustain 8V, and 5V device to sustain 14V. To calculate Poisson defect densities with a high degree of confidence, a total capacity area of at least 1 cm^2 is used. TowerJazz requires that the total number of failures (short and weak combined) D_o < 6 defects/cm^2.

Electro-Migration (EM)

Reference	JESD63: Standard Method for Calculating the Electro-Migration Model Parameters for Current Density and Temperature
Model	Black's equation: $t_{50\%}$= A*J^(-n)*EXP(Ea/kT); $t_{0.1\%}=t_{50\%}$*EXP(-3.09*σ)
Sampling Plan	M1, M2 and top layers, 16 metal lines per layer
General Test Conditions	Stress metal lines at 240°C and accelerated current density to accelerate the resistance change
Acceptance Criteria	At 85°C and max allowed current density, T_0.1% > 10 years
Method	EM test is performed on M1, M2 and top metal lines with minimum design rules, on via-line-via structures with Kelvin connection. A metal line is isothermally stressed at 240°C with a constant current density that is chosen to minimize joule heating. Based on experiments, the activation energy (Ea) is 0.9 for M1 and M2, and 1.04 for top metal. The current density exponent (n) is assumed to have a value of 2, according to Industry standard. The failure time is recorded when a metal line's relative resistance change is greater than 20%. If a metal line does not fail after 168 hours, then 168 hours is used as the worst-case number. After all samples are tested, the median time to failure ($t_{50\%}$) is calculated. $t_{0.1\%}$ is calculated based on the equation $t_{0.1\%}=t_{50\%}$*EXP(-3.09σ), where σ is calculated from the sample data. EM $t_{0.1\%}$ lifetime under worst case operating condition (85°C and maximum design rule current density: 3mA for M1 and M2, and 15mA for top metal) is back-extrapolated based on Black's equation. TowerJazz and industry requirement is a lifetime exceeding 10 years.

MIM Capacitor Integrity

Reference	JESD35: Procedure for Wafer-Level Testing of Thin Dielectrics
Model	V-Ramp
Sampling Plan	Divide the total PCM capacitors failures by total PCM area to calculate defect density (total area > 1cm^2)
General Test Conditions	At 25°C, use current source to screen for short failures and use V-Ramp to screen for weak failures
Acceptance Criteria	D_o < 3 defects/cm^2
Method	Voltage-ramp test is performed at 25°C to evaluate the extrinsic behavior of the capacitor dielectric. A "short" test is performed, by applying 1.0μA force on the capacitor dielectric. A device with a gate voltage exceeding V_{CC} is considered to have a "short" failure and will not be tested for a weak failure. If the device passes the "shorts" test, a staircase voltage ramp (50mV per step) is applied on the capacitor dielectric at a rate of 2V/second from V_{CC}. A device is considered to have a "weak" failure and the test is completed if: 1) the MIM capacitor current exceeds 10mA, or, the current is 5 times greater than the current measured at the previous step. If there are no failures, theory projects that the device's MIM Capacitor Lifetime is greater than 10 years for a 1.8V device to sustain above 4V, a 3.3V device to sustain 8V, and 5V device to sustain 14V. To calculate Poisson defect densities with a high degree of confidence, a total capacity area of at least 1 cm^2 is used. TowerJazz requires that the total number of failures (short and weak combined) D_o < 3 defects/cm^2.

Passivation Integrity

Reference	MIL-STD-883E method 2021.3: Glassivation Layer Integrity		
Model	N/A		
Sampling Plan	1 lot		
General Test Conditions	Thermal shock & overcoat pinhole etch		
Acceptance Criteria	$D_0 < 1$ in^{-2}		
Methods			
	Test vehicle	Temperature	Test time
	Hot plate	450^0 C	30 seconds
	Cold plate	25^0 C	30 seconds
	Passivation Pinhole Etch		
	Chemical	Temperature	Etch time
	Phosphoric/Nitric/water	90^0 C	15 minutes
	DI H2O Rinse	Room T.	15 minutes
	Blue M Oven	70^0 C	15 minutes

Package Level Reliability Tests Summary

Tests	Reference	Sampling Plan	General Test Conditions	Accept Criteria	Results	Conclusion
High Temperature Operating Life (HTOL)	JESD22-A108-B	3 lots, 77 devices per lot	Stress devices with V_{bias} =1.1* V_{CC} and ambient temperature of 125°C for 1000 hours to accelerate operating condition	0 failures in full-functional and parametric tests	See Test Results	Pass
Highly Accelerated Stress Test (HAST)	JESD22-A110-B	3 lots, 77 devices per lot	Stress devices with V_{bias} =1.1* V_{CC}, ambient temperature of 130°C, and 85%RH for 96 hours to accelerate penetration of moisture	0 failures in full-functional and parametric tests	See Test Results	Pass
High Temperate Storage Life (HTS)	JESD22-A103-B	1 lot, 77 devices per lot	Store devices in ambient temperature of 150° for 1000 hours	0 failures in full-functional and parametric tests	See Test Results	Pass
Temperature Cycling	JESD22-A104-B	3 lots, 77 devices per lot	Alternate ambient temperature from –65°C to 150°C for 500 cycles, according to Cond C.	0 failures in full-functional and parametric tests	See Test Results	Pass
ESD (HBM)	JESD22-A114-B	1 lot, 3 devices per voltage level	Test all I/O and power pin combinations per HBM standard	0 failures in full-functional and parametric tests	Inferred	Pass (SBC18HX)
Latch-Up	JESD78	1 lot, 3 devices for current test and 3 devices for over-voltage test	Test device susceptibility to damage by exposure to I-trigger and over-voltage latch-up	0 failures in full-functional and parametric tests	Inferred	Pass (SBC18HX)

Other than HTOL, the other PLR tests are inferred from SBC18HX process. Please refer to document NPB PS-0901, R50 Reliability Report for FAB 3 SBC18HX, HXL, HK, HKL, and HA Processes. This inference is justified because the only difference between SBC18H2 and SBC18HX is the addition of HS NPN transistors on the SBC18H2 process, and its reliability is demonstrated by HTOL test results. The other PLR tests are not affected by this HS NPN device. The ESD and Latchup tests for SBC18H2 can also be inferred from the tests done for SBC18HX as they share the same I/O and use the same ESD protection scheme.

Subsequently, 85/85 TH, T/C, and HTS were run on SBC18H2 RFQ devices and the results are included in the following tables

Test Results

High Temperature Operating Life

Device No.	Lot No.	Wafer No.	Quantity	# of Failures
A0974	K79742.1	01	80	0[A]
A0974	K79877.1	04	80	0
A0974	K79742.5	12	80	0

Note A – There are some failures, such as junction varactor capacitance failures, but these failures are believed to be due to package assembly (glob-top manual packages) and very high frequency testing (8 – 9 GHz). They are not stress-related failures.

85C / 85% RH Temp / Humidity (1,000 hours)

Device No.	Lot No.	Wafer No.	Quantity	# of Failures
A0974	K79742.1	01	74	0
A0974	K79877.1	04	53	0
A0974	K79742.5	12	72	0

Temp Cycling (-65C to +150C, 500 Cycles)

Device No.	Lot No.	Wafer No.	Quantity	# of Failures
A0974	K79742.1	01	75	0
A0974	K79877.1	04	53	0
A0974	K79742.5	12	71	1[B]

Note B – There is one Open failure, and found broken leads, not stress-related.

High Temp Storage

Device No.	Lot No.	Wafer No.	Quantity	# of Failures
A0974	K79877.1	04	52	0

Package Level Reliability Testing Methodologies

High Temperature Operating Life

Reference	JESD22-A108-B: Temperature, Bias, and Operating Life
Model	Arrhenius thermal equation: TTF = A * exp[Ea/kT], activation energy = 0.7eV
Sampling Plan	3 lots, 77 devices per lot
General Test Conditions	Stress devices with V_{bias} =1.1* V_{CC} and ambient temperature of 125°C for 1000 hours to accelerate operating condition
Acceptance Criteria	0 failures in full-functional and parametric tests
Method	High temperature operating life is an accelerated dynamic life test performed typically at an ambient temperature that targets a maximum junction temperature of 150°C. Infant mortality (PPM) and long-term reliability (FIT) of a given process technology is determined by JESD22-A108. FIT rates at different burn-in temperatures are as follows: 17@55C, 71@75C, and 339@100C. HTOL covers Early Life Test (ELT) by taking readout after 6 hours of under HTOL condition.

Highly Accelerated Stress Test

Reference	JESD22-A110-B: Highly-Accelerated Temperature and Humidity Stress Test (HAST)
Model	Peck's corrosion equation: TTF = A * RH^-N * f(V) * exp[Ea/kT]
Sampling Plan	3 lots, 77 devices per lot
General Test Conditions	Stress devices with V_{bias} =1.1* V_{CC}, ambient temperature of 130°C, 85%RH, 18.6 psig, for 96 hours.
Acceptance Criteria	0 failures in full-functional and parametric tests
Method	HAST is an accelerated temperature humidity bias test that monitors corrosion, ionic migration, dendritic growth, and other moisture and temperature related defect mechanisms according to JESD22-A110-B.

High Temperature Storage

Reference	JESD22-A103-B: High Temperature Storage Life
Model	TTF = A * S^-n * exp[Ea/kT]
Sampling Plan	1 lot, 77 devices per lot
General Test Conditions	Store devices in ambient temperature of 150° for 1000 hours
Acceptance Criteria	0 failures in full-functional and parametric tests
Method	HTS is performed to evaluate stress migration on metal according to JESD22-A103-B.

Temperature Cycle

Reference	JESD22-A104-B: Temperature Cycling
Model	Modified Coffin-Manson equation: Nf = C * (ΔT - ΔT0)^-q, where ΔT0 is elastic strain range.
Sampling Plan	3 lots, 77 devices per lot
General Test Conditions	Alternate ambient temperature from –65°C to 150°C for 500 cycles, according to Condition C.
Acceptance Criteria	0 failures in full-functional and parametric tests
Method	Temperature cycle is performed to evaluate die level and package mechanical stress failure mechanisms that result from CTE mismatch, according to JESD22-A104-B.

Electrostatic Discharge, Human Body Model

Reference	JESD22-A114-B: Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
Model	N/A
Sampling Plan	1 lot, 3 devices per voltage level
General Test Conditions	Test all I/O and power pin combinations per HBM standard >/= 1500 V
Acceptance Criteria	0 failures in full-functional and parametric tests
Method	HBM ESD is performed according to JESD22-A114-B. Machine Model is not performed.

Latch-Up

Reference	JESD78: IC Latch-Up Test
Model	N/A
Sampling Plan	1 lot, 3 devices for current test and 3 devices for over-voltage test
General Test Conditions	Trigger current > 150 mA, 85ºC and 1.5XVdd over voltage.
Acceptance Criteria	0 failures in full-functional and parametric tests
Method	Latch-up test is performed to test device susceptibility to damage by exposure to I-test and over-voltage latch-up, according to JESD78.

Reference Documents

Test Name	Reference Documents	Document Title
Hot Carrier Injection (HCI)	JESD28	A Procedure for Measuring N-Channel MOSFET Hot-Carrier-Induced Degradation at maximum Substrate Current Under DC Stress
Threshold Voltage Stability (TVS)	N/A	N/A
Thermal Bias Stress	N/A	N/A
Reverse Beta Degradation	N/A	N/A
Gate Oxide Integrity (GOI)	JESD35	Procedure for Wafer-Level Testing of Thin Dielectrics
	Reza Moazzami and Chenming Hu "Projecting Gate Oxide Reliability and Optimizing Reliability Screens" *IEEE Trans. on Electron Devices,* Vol. 37, No. 7, July 1990, pp. 1643-1650.	
Electro-Migration (EM)	JESD63	Standard Method for Calculating the Electro-Migration Model Parameters for Current Density and Temperature
MIM Capacitor Integrity	JESD35	Procedure for Wafer-Level Testing of Thin Dielectrics
Passivation Integrity	MIL-STD-883E method 2021.3	Glassivation Layer Integrity
Bond-Ability	MIL-STD_883E method 2011.7	Bond Strength (Destructive Bond Pull Test)
	JESD22-B116	Die Shear Strength
	GN-0829 (CONEXANT)	Bond Pad Cratering Testing
HTOL	JESD22-A108-B	Temperature, Bias, and Operating Life
HAST	JESD22-A110-B	Highly-Accelerated Temperature and Humidity Stress Test (HAST)
HTS	JESD22-A103-B	High Temperature Storage Life
TC	JESD22-A104-B	Temperature Cycling
ESD	JESD22-A114B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)
	JESD22-C101A	Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components
Latch-Up	JESD78	IC Latch-Up Test