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		TYPE OF DOCUMENT: PCM Manual

TITLE:

MP088-SBC18H2 PCM Manual
(6 Metal Layers, SiGe BiCMOS process)

REV	REVISION DESCRIPTION	DATE
01	Initial release	06/10/08
02	Reduced upper split limits of via1,2,3 resistance tests from 20 to 10 ohms/via. Small adjustments made to the metal serpentine resistance tests. Added ICN 0.15x10 std device array leakage test. Updated bias current for BVebo and BVcbo 0p15x10 HS NPN test Small adjustments to limits for Vt 10X0p18NH and Vt 10Xp36NH.	08/10/09

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1 Purpose and Scope

This document describes the methods used to monitor the electrical parameters of JAZZ Semiconductor SBC18H2 process. The SBC18H2 process is a 6 layer metal, 0.18µm SiGe BiCMOS process. Parametric PCM MP088 is used as the process monitor vehicle.

The MP088 mini-PIC monitors the SBC18H2 (6 metal layers) process. It is a small test chip used in the scribe line area. The MP088 consists of thirteen separate modules.

Module Name	Layout Name	Width (mm)	Height (mm)	Area(mm^2)
N-ch-LV	MP088NL	4.556	0.080	0.364
N-ch-HV	MP088NH	4.556	0.080	0.364
P-ch-LV	MP088PL	4.553	0.080	0.364
P-ch-HV	MP088PH	4.555	0.080	0.364
Mixed-signal	MP088M	4.696	0.080	0.376
Back-end	MP088BE	4.388	0.080	0.351
Elect. Migration	MP088EM	3.523	0.080	0.282
Resistor/Cap.	MP088RC	4.922	0.080	0.394
Bipolar 1	MP088T1	4.018	0.080	0.321
Bipolar 2	MP088T2	3.986	0.080	0.319
Bipolar 3	MP088T3	3.776	0.080	0.302
RF1	MP088R1	5.000	0.080	0.400
RF2	MP088R2	3.216	0.080	0.257

2 Applicable Documents

NPB PS-0267: SBC18 Electrical Specifications

NPB PS-0543: SBC18H2 Design Application Note

NPB PS-0570: SBC18H2 MiniPic Manual

3 Test Methodology and Test Conditions

3.1 Test name: IDSAT Device name: 10xP36N_HV

This test is to measure the saturation current of 10x0.36um high-voltage NMOS device. During measurement, both the drain pad and the gate pad are biased at 3.3V, p-body pad and the source pad are biased at 0V. Drain current is measured.

3.2 Test name: IDSAT Device name: 10xP30P_HV

This test is to measure the saturation current of 10x0.30um high-voltage PMOS device. During the measurement, both the drain pad and the gate pad are biased at -3.3V, Nwell pad and the source pad are biased at 0V. Drain current is measured.

3.3 Test name: IDSAT Device name: 10xP18P

This test is to measure the saturation current of low-voltage10x0.18um PMOS device. During the measurement, both the drain pad and the gate pad are biased at –1.8V, Nwell pad and the source pad are biased at 0V. Drain current is measured.

3.4 Test name: IDSAT Device name: 10xP18N

This test is to measure the saturation current of low-voltage10x0.18um NMOS device. During the measurement, both the drain pad and the gate pad are biased at 1.8 V, p-body pad and the source pad are biased at 0V. Drain current is measured.

3.5 Test name: VT Device name: 10xp36N_HV

This test is to measure the threshold voltage of 10x0.36um high-voltage NMOS device in linear region. Drain current Id is measured while gate voltage Vg ramps from 0V to 1.5V. During the test, drain pad is biased at 100mV and body pad is biased at 0V. The reported VT is the Vgs intercept of maximum slope tangent line of the Ids-Vgs curve subtracted by ½ Vds.

3.6 Test name: VT Device name: 10xp30P_HV

This test is to measure the threshold voltage of 10x0.30um high-voltage PMOS device in linear region. Drain current Id is measured while gate voltage Vg ramps from 0V to -1.5V. During the test, drain pad is biased at -100mV and body pad is biased at 0V. The reported VT is the Vgs intercept of maximum slope tangent line of the Ids-Vgs curve subtracted by ½ Vds.

3.7 Test name: VT Device name: 10xp18N

This test is to measure the threshold voltage of low-voltage10x0.18um NMOS device in linear region. Drain current Id is measured while gate voltage Vg ramps from 0V to 1V. During the test, drain pad is biased at 50mV and body pad is biased at 0V. The reported VT is the Vgs intercept of maximum slope tangent line of the Ids-Vgs curve subtracted by ½ Vds.

3.8 Test name: VT Device name: 10xp18P

This test is to measure the threshold voltage of low-voltage10x0.18um PMOS device in linear region. Drain current Id is measured while gate voltage Vg ramps from 0V to -1V. During the test, drain pad is biased at -50mV and body pad is biased at 0V. The reported VT is the Vgs intercept of maximum slope tangent line of the Ids-Vgs curve subtracted by ½ Vds.

3.9 Test name: BVDSS Device name: 10xp36N

This test is to measure the punch through breakdown voltage between the drain and source of high-voltage 10x0.36um NMOS. During the measurement, the source pad, the gate pad and the body pad are all biased at 0V, while drain voltage ramps from 0V until the drain current reaches 1uA. The final drain voltage is at BVDSS.

3.10 Test name: BVDSS Device name: 10xp30P

This test is to measure the punch through breakdown voltage between the drain and source of high-voltage PMOS. During the measurement, the source pad, the gate pad and the body pad are all biased at 0V, while drain voltage ramps from 0V until the drain current reaches 1uA. The final drain voltage is reported as BVDSS.

3.11 Test name: BVDSS Device name: 10xp18N

This test is to measure the punch through breakdown voltage between the drain and source of low-voltage 10x0.18um NMOS. During the measurement, the source pad, the gate pad and the body pad are all biased at 0V, while drain voltage ramps from 0V until the drain current reaches 1uA. The final drain voltage is at BVDSS.

3.12 Test name: BVDSS Device name: 10xp18P

This test is to measure the punch through breakdown voltage between the drain and source of low-voltage 10x0.18um PMOS. During the measurement, the source pad, the gate pad and the body pad are all biased at 0V, while drain voltage ramps from 0V until the drain current reaches 1uA. The final drain voltage is reported as BVDSS.

3.13 Test name: TDDB Device name: Gateox_ HV

The voltage-ramp test is performed to evaluate the behavior of the gate oxide of high-voltage MOS device. The test structure is a large gate poly-oxide-Psubstrate MOS cap plates with long active and poly edge. The voltage ramp of 2Mv/cm*sec is applied at the top gate plate, and the leakage current at the gate plate is monitored. The TDDB breakdown voltage is defined where the leakage current increases very rapidly and reaches 10uA.

3.14 Test name: TDDB Device name: Gateox_LV

The voltage-ramp test is performed to evaluate the behavior of the gate oxide of low-voltage MOS device. The test structure is a large gate poly-oxide-Psubstrate MOS cap plates with long active and poly edge. The voltage ramp of 2Mv/cm*sec is applied at the top gate plate, and the leakage current at the gate plate is monitored. The TDDB breakdown voltage is defined where the leakage current increases very rapidly and reaches 10uA.

3.15 Test name: VFI Device name: PolyN

This test is to characterize the leakage between two adjacent NMOS devices using a poly- field inversion transistor structure. During the test, poly-gate pad and the drain pad of the field inversion transistor are tied together, and voltage ramp is applied on these two pads to force the transistor into inversion mode. Current flowing through the drain pad is measured. The voltage ramp stops when the current reaches 1uA and the final supply voltage is the reported VFI. Both the Source pad and the Body pad of the field inversion transistor are biased at 0V during test.

3.16 Test name: VFI Device name: PolyP

This test is to characterize the leakage between two adjacent PMOS devices using a poly field inversion transistor structure. During the test, poly gate pad and the drain pad of the field inversion transistor are tied together, and voltage ramp is applied on these two pads to force the transistor into inversion mode. Current flowing through the drain pad is measured. The voltage ramping stops when the current reaches 1uA and the final supply voltage is the reported VFI. Both the Source pad and the Body pad of the field inversion transistor are biased at 0V during test.

3.17 Test name: RHO Device name: NPOLY

This test is to measure the NMOS gate poly sheet resistance using a gate ploy serpentine test structure. This is a simple 2 terminal test. During the test, current is forced into the High pad and voltage on the High pad is measured. The total resistance is calculated by dividing the measured voltage by the supply current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the serpentine. Both Low pad and Body pad are biased at 0V during the test.

3.18 Test name: RHO Device name: NDIFFUSION

This test is to measure the N+ diffusion sheet resistance using a N+ diffusion serpentine test structure. This is a simple 2 terminal test. During the test, current is forced into the High pad and the voltage on the High pad is measured. The total resistance is calculated by dividing the measured voltage by the supply current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the serpentine. Both Low pad and Body pad are biased at 0V during the test.

3.19 Test name: RHO Device name: PDIFFUSION

This test is to measure the P+ diffusion sheet resistance using a P+ diffusion serpentine test structure. This is a simple 2 terminal test. During the test, current is forced into the High pad and the voltage on the High pad is measured. The total resistance is calculated by dividing the measured voltage by the supply current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the serpentine. Both Low pad and Nwell pad are biased at 0V during the test.

3.20 Test name: RHO Device name: NWELL

This test is to measure sheet resistance of N well resistor. This is a simple 2 terminal test. During test, current is forced into the High pad and the voltage on the High pad is measured. The total resistance is calculated by dividing the measured voltage by the supply current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both low pad and body pad are biased at 0V during the test.

3.21 Test name: RHO Device name: RESISTORLV

This test is to measure sheet resistance of high value unsilicided poly resistor using a 0.75umX10um resistor structure. This is a four terminal test where separate pads are used for forcing current (100uA) and sensing voltage. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.22 Test name: RHO Device name: RESISTORHV

This test is to measure sheet resistance of high value unsilicided poly resistor. Resistances from three different high value resistor sizes (0.75x10um, 0.75x100um, 10x100um) are measured using simple two-terminal measurements. Then the sheet resistance, end resistance, and delta_W are extracted by solving the equation below using data from the three resistors.

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Re\,nd}{W + \Delta W}$$

3.23 Test name: RHO Device name: M1

This test is to measure sheet resistance of Metal 1 layer using a Metal 1 serpentine test structure. This is a simple 2 terminal resistor test. During test, current of 100uA is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.24 Test name: RHO Device name: M2

This test is to measure sheet resistance of Metal 2 layer using a Metal 2 serpentine test structure. This is a simple 2 terminal resistor test. During test, current is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.25 Test name: RHO Device name: M3

This test is to measure sheet resistance of Metal 3 layer using a Metal 3 serpentine test structure. During test, current is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.26 Test name: RHO Device name: M4

This test is to measure sheet resistance of Metal 4 layer using a Metal 4 serpentine test structure. During test, current is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.27 Test name: RHO Device name: M5

This test is to measure sheet resistance of Metal 5 layer using a Metal 5 serpentine test structure. During test, current is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.28 Test name: RHO Device name: M6

This test is to measure sheet resistance of Metal 6 layer using a Metal 6 serpentine test structure. During test, current is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.29 Test name: CR Device name: PDIFFUSION

This test is to measure the P+ diffusion contact resistance using a contact chain test structure. During test, current is forced into the High pad and voltage on High pad is measured. The total contact resistance is calculated by dividing the measured voltage by the supply current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of the contacts of the contact chain. Both Low pad and Body pad are biased at 0V during the test.

3.30 Test name: CR Device name: NDIFFUSION

This test is to measure the N+ diffusion contact resistance using a contact chain test structure. During test, current is forced into the High pad and voltage on High pad is measured. The total contact resistance is calculated by dividing the measured voltage by the supply current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of the contacts of the contact chain. Both Low pad and Body pad are biased at 0V during the test.

3.31 Test name: CR Device name: NPOLY

This test is to measure the NMOS gate poly contact resistance using the gate poly contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supplied current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of contacts on the contact chain. The Low pad is biased at 0V during the test.

3.32 Test name: CR Device name: PPOLY

This test is to measure the PMOS gate poly contact resistance using the gate poly contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supplied current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of contacts on the contact chain. The Low pad is biased at 0V during the test.

3.33 Test name: CR Device name: SINKER

This test is to measure the NPN collector sinker contact resistance using the sinker contact chain test structure. During test, current is forced into the High pad and voltage on High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supplied current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by number of contacts on the contact chain. Both Low pad and Body pad are biased at 0V during the test.

3.34 Test name: CR Device name: EP

This test is to measure the NPN emitter poly contact resistance using the emitter poly contact chain test structure. During test, current is forced into the High pad and voltage on High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supplied current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by number of contacts on the contact chain. Both Low pad and Body pad are biased at 0V during the test.

3.35 Test name: CR Device name: BP

This test is to measure the NPN base poly contact resistance using the base poly contact chain test structure. During test, current is forced into the High pad and voltage on High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supplied current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by number of contacts on the contact chain. Both Low pad and Body pad are biased at 0V during the test.

3.36 Test name: CR Device name: VIA1

This test is to measure the Via1 contact resistance using the Via1 contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supplied current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of the contacts of the contact chain. The Low pad is biased at 0V during the test.

3.37 Test name: CR Device name: VIA2

This test is to measure the Via2 contact resistance using the Via2 contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supply current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of contacts on the contact chain. The Low pad is biased at 0V during the test.

3.38 Test name: CR Device name: VIA3

This test is to measure the Via3 contact resistance using the Via3 contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supply current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of contacts on the contact chain. The Low pad is biased at 0V during the test.

3.39 Test name: CR Device name: VIA4

This test is to measure the Via4 contact resistance using the Via4 contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supply current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of contacts on the contact chain. The Low pad is biased at 0V during the test.

3.40 Test name: CR Device name: VIA5

This test is to measure the Via5 contact resistance using the Via5 contact chain test structure. During test, current is forced into the High pad and the voltage on the High pad is measured. Total contact resistance is calculated by dividing the measured voltage by the supply current. The reported contact resistance per contact is then calculated by dividing the total contact resistance by the number of contacts on the contact chain. The Low pad is biased at 0V during the test.

3.41 Test name: BVCBO Device name: P15x10HS

This test is to characterize the collector-to-base junction avalanching breakdown voltage of high-speed 0.15x10.16um NPN device. During test, a reverse leakage current of 100uA is forced from collector pad into base pad. The measured collector-base voltage is reported as BVCBO. The emitter is open during the test.

3.42 Test name: BVCBO Device name: P15x10STD

This test is to characterize the collector-to-base junction avalanching breakdown voltage of standard 0.15x10.16um NPN device. During test, a reverse leakage current of 1uA is forced from collector pad into base pad. The measured collector-base voltage is reported as BVCBO. The emitter is open during the test.

3.43 Test name: BVCEO Device name: P15x10HS

This test is to measure the C-E breakdown voltage of high-speed 0.15x10.16um NPN device. During test, base-emitter junction is biased at 0.7V. The voltage applied on the collector pad Vc ramps from 0V until the current at the base node approaches 0.The final force collector voltage is reported as BVCEO.

3.44 Test name: BVCEO Device name: P15x10STD

This test is test is to measure the C-E breakdown voltage of standard 0.15x10.16um NPN device. During the test, base-emitter junction is biased at 0.7V. The voltage applied on the collector pad Vc ramps from 0V until the current at the base node approaches 0.The final force collector voltage is reported as BVCEO.

3.45 Test name: BVEBO Device name: P15x10HS

This test is to characterize the emitter-to-base junction reverse breakdown voltage of high-speed 0.15x10.16um NPN device. During the test, a reverse leakage current of 15.24uA is forced from emitter pad into base pad. The measured emitter-base voltage is reported as BVEBO. The collector is open during the test.

3.46 Test name: BETA Device name: P15x10HS_M

This test is to measure the current gain Beta of high-speed 0.15x10.16um device. A current of 20uA is supplied at emitter node. The collector-to-base voltage is 1V. Base current and collector current are measured, and the current gain BETA is then calculated as Ic /Ib.

3.47 Test name: IC Device name: P15x10HS

This test is to measure the high-speed 0.15x10.16um NPN collector current when base-emitter junction is forward biased. Both collector pad and base pad are biased at 700mV. Emitter pad is biased at 0V. Collector current is measured and reported.

3.48 Test name: CA Device name: MIM 2FF@0V

This test is to measure the capacitance of a MIM Cap. The DC bias is 0V, and the frequency at which the measurement is conducted is 100KHz.

3.49 Test name: BVGO Device name: MIM 2FF

This test is to measure the breakdown voltage of MIM capacitor. During the test, the voltage applied across the capacitor ramps from 0V until the leakage current reaches 1uA. The final force voltage across the capacitor is reported as BVGO_MIM.

3.50 Test name: RHO Device name: TR

This test is to measure sheet resistance of Metal (TiN) resistor using a serpentine test structure. During test, current is forced into High pad and voltage at high pad is measured. Total resistance is calculated by dividing the measured voltage by the forcing current. The reported sheet resistance is then calculated by dividing the total resistance by the number of squares on the test structure. Both Low pad and body pad are biased at 0V during the test.

3.50 Test name: LK Device name: ICN P15X10STD

This test is to measure the leakage of a 200 0.15x10 standard device NPN array. The collector is biased to 1V and 0.2V is applied to the base with the emitter grounded. The collector current is reported.

4 Wafer Acceptance Criteria

The following table summarizes the limits used for the SBC18H2 process, as they pertain to moving, holding, and scrapping wafers/lots.

PCM data is extracted from all of the wafers in a production lot. Seven sites are measured on each wafer. A wafer is considered acceptable if there are less than or equal to 3 sites/wafer out of the PCM electrical specification (shown below) for every parameter listed below. The wafer will be rejected if there are more than 3 sites/wafer out of the specifications for any single parameter.

TestName	*DeviceName*	*LrL*	*UrL*	*Unit*
VT	10XP18N	0.41	0.57	Volt
IDSAT	10XP18N	0.0051	0.0069	Amp
BVDSS	10XP18N	3.2	8	Volt
CR	NDIFFUSION	4	40	Ohm
RHO	NDIFFUSION	2	12	Ohm/sq
RHO	NPOLY	2	12	Ohm/sq
TDDB	GATEOX_LV	-8	-4	Volt
VT	10XP36N_HV	0.50	0.70	Volt
IDSAT	10XP36N_HV	0.005	0.007	Amp
BVDSS	10XP36N	6	12	Volt
VFI	POLYN	4	15	Volt
CR	NPOLY	2	20	Ohm
CR	PPOLY	0.1	20	Ohm
TDDB	GATEOX_HV	-12	-8	Volt
VT	10XP18P	-0.52	-0.36	Volt
IDSAT	10XP18P	-0.003	-0.0021	Amp
BVDSS	10XP18P	3.2	8	Volt
CR	PDIFFUSION	4	40	Ohm
RHO	PDIFFUSION	2	12	Ohm
VT	10XP30P_HV	-0.84	-0.64	Volt
IDSAT	10XP30P_HV	-0.0034	-0.0024	Amp
BVDSS	10XP30P	5	10	Volt
VFI	POLYP	4	15	Volt
RHO	NWELL	710	1070	Ohm/sq
RHO	RESISTORLV	205	269	Ohm/sq
CA	MIM 2FF@0V	102	138	pFarad
BVGO	MIM 2FF	14	45	Volt
RHO	M1	0.065	0.099	Ohm/sq
RHO	M2	0.065	0.099	Ohm/sq
RHO	M3	0.065	0.099	Ohm/sq
RHO	M4	0.045	0.087	Ohm/sq
RHO	M5	0.013	0.023	Ohm/sq
RHO	M6	0.008	0.013	Ohm/sq
CR	VIA1	0.1	10	Ohm
CR	VIA2	0.1	10	Ohm
CR	VIA3	0.1	10	Ohm

CR	VIA4	0.1	8	Ohm
CR	VIA5	0.1	8	Ohm
BVCEO	P15X10STD	2.8	4.2	Volt
BVCBO	P15X10STD	8	12	Volt
CR	EP	2	18	Ohm
CR	BPOLY	4	100	Ohm
CR	SINKER	1	20	Ohm
BETA	P15X10HS_M	100	600	NONE
IC	P15X10HS	4.00E-06	2.00E-05	Amp
BVCEO	P15X10HS	1.6	2.4	Volt
BVEBO	P15X10HS	1.8	3.2	Volt
BVCBO	P15X10HS	4	7.6	Volt
RHO	TR	21	28	Ohm/sq
LK	ICN P15X10STD	-2.00E-08	2.00E-08	Amp