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TITLE:

SBC18 DESIGN RULES:
SBC18HX/ SBC18HXL / SBC18HA / SBC18PT / SBC18QTD / SBC18QTR/ SBC18QTL/ SBC18QW / SBC18MW/ SBC18MWD/ SBC18MV

REV	REVISION DESCRIPTION (FROM 2005 ONWARDS)	DATE
10	Added Section 5.13 on Miscellaneous Rules; Updated rules 16.A and 16.B in Section 4.12 to 0.6 from 0.44; Updated section 3.5.2 to include dummy active and poly field exclusions by adding notes 6, 7 and 8; Updated note 4 in this section. Completely updated Section 12 and renamed it Artifact Region from General device Requirements.	01/03/05
11	Added Section 8.3 on custom bump pads; Updated rules 14.A, 14.B, 16.A, 16.B in Sections 4.11 and 4.12 Added rules 9.A and 9.B in Section 4.25; Added rule B41 in section 5.1 for NPNs; Added rule 23.D in section 5.1.1; Changed custom bond pad rule B.6 from unchecked to checked in Section 8.2; Updated rules MVAR.1 and MVAR.2 to rules MVAR.1.A/MVAR.1.B and MVAR.2.A/MVAR.2.B, respectively, in Section 5.5.3 to match limits in released MOSVAR models; Added rule 5.6 in Section 5.8; Added show* rules in Section 5.13 for Miscellaneous Rules; Added Section 4.26 on Polyimide Protective Overcoat (Layer 99); Added layer 99 description in Section 3; Updated minimum vertical scribe width in table in Section 13.2 for SBC18MV/MW/MWD/PT processes	06/15/05
12	In section 7.2, clarify applicability of stress relief rules MC13-MC16; In section 1.1, add Schottky diode to process description of SBC18QTR; In section 4.13, change contact rule 7.D from 0.21 to 0.20um; Change 48.F (max metal 5 density) from 70% to 60%; Add SBC18HA process; Removed “aligns to” column in tables in section 3.1; Removed MC6/MCB6/MCC6/SMC6, MC7/MCB7/MCC7/SMC7; Updated DNW.11 device list and added rule DNW.17 in Section 5.9;	03/10/2006
13	Update scribe line information table in section 13.2	04/13/2009
14	Added section 5.14 for Large Die Rules; Added layer 118/36 for standard cell marking layer;	06/27/2011

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1 Purpose and Scope

This document contains the design rules for SBC18 silicon germanium (SiGe) BiCMOS process family. This includes design rules for a 0.18 um CMOS process based upon Jazz Semiconductor's CA18 (digital/mixed-signal) process family. The CA18 process is a CMOS bulk silicon process with 26Å gate oxide and 0.18µm minimum drawn gate length.

These rules are general for digital designs with nominal Vdd supplies of 1.8V and up to 3.3V for the thick gate oxide transistors (63Å gate oxide, and 0.3µm minimum drawn gate length). All dimensions are in microns (µm) or square microns (μm^2). This process has silicided diffusions and poly. All rules apply to 1.8V nominal operation except where specified.

Design rules of RF and mixed/signal components, such as three types of SiGe NPN transistors (High speed NPN, Standard NPN, and High Voltage NPN, in decreasing order of cut-off frequencies), five types of resistors (metal, high value unsilicided poly, low value unsilicided poly, silicided poly, and n-well), MIM capacitors, varactors, MOS capacitors, etc. are also included.

The drawn resolution of layout grid is 0.005µm.

1.1 Description of Processes

The SBC18HX process has six layers of aluminum metal. It supports (a) both 1.8V and 3.3V FETs (b) high speed, standard and high voltage NPNs with deep trench (c) metal, low value unsilicided poly, silicided poly, and nwell resistors (d) 1fF/um^2 MIM capacitor on metal 4 (e) high performance junction varactor and (f) inductors using 2.8um thick aluminum top metal layer (metal 6) and 2um thick top via layer (Via 5). The metal resistor is between metal 3 and metal 4. The MIM capacitor is between metal 4 and metal 5. The via4 is 2um in height and metal 5 is 1.6um thick aluminum.

The SBC18HXL process is identical to the SBC18HX process with the addition of a deep nwell mask to support triple well process for NFETs and a schottky diode.

SBC18HA is a variant of HXL with (a) addition of high value poly resistorand (b) different MIM cap specifications of 2.8fF/um^2 single and 5.6fF/um^2 stacked MIM capacitors.

The SBC18PT process has five layers of aluminum metal. It supports (a) both 1.8V and 3.3V FETs (b) standard and high voltage NPNs without deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 and 4fF/um^2 stacked MIM capacitor on Metal 2 and Metal 3 (e) high performance junction varactor and (f) inductors using 5.2um thick aluminum top metal layer (metal 5) and 2um thick top via layer (Via 4). The 2fF/um^2 MIM capacitor is located between metal 2 and metal 3 and the stacked 4fF/um^2 MIM capacitor is located between metals 2, 3 and metals 3, 4. The via3 is 2um in height and metal 4 is 1.6um thick aluminum.

The SBC18QTD process has four layers of aluminum metal. It supports (a) 3.3V FETs only (b) standard and high voltage NPNs with deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 (e) high performance junction varactor and (f) inductors using 5.2um thick Aluminum top metal layer (metal 4), 3um thick top via layer (Via 3). The MIM capacitor is between metal 2 and metal 3.

The SBC18QTR process is identical to the SBC18QTD process with the additions of (a) metal resistor between metal-1 and metal-2 and (b) a Schottky diode.

The SBC18QTL process is identical to SBC18QTD process with the addition of a deep nwell mask to support triple well process for NFETs.

The SBC18QW process has four layers of aluminum metal. It supports (a) 3.3V FETs only (b) standard and high voltage NPNs without deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor on Metal 2 and 4fF/um^2 stacked MIM capacitor on Metal 2 and Metal 3 (e) p+/nwell junction varactor and (f) inductors using 2.8um thick Aluminum top metal layer (metal 4), 2um thick top via layer (Via 3). The 2fF/um^2 MIM capacitor is located between metal 2 and metal 3 and the stacked 4fF/um^2 MIM capacitor is located between metals 2, 3 and metals 3, 4.

The SBC18MW process has three layers of aluminum metal. It supports (a) 3.3V FETs only (b) standard and high voltage NPNs without deep trench (c) high value unsilicided poly, low value unsilicided poly, silicided poly, and nwell resistors (d) 2fF/um^2 MIM capacitor (e) p+/nwell junction varactor and (f) inductors using 2.8um thick Aluminum top metal layer (metal 3), 2um thick top via layer (Via 2). The MIM capacitor is between metal 2 and metal 3.

SBC18MWD process is the SBC18MW process with (a) the standard and high voltage NPNs having the deep trench and (b) the p+/nwell junction varactor replaced with the high performance junction varactor.

SBC18MV process is the SBC18MW process with the p+/nwell junction varactor replaced with the high performance junction varactor

The look-up tables below distinguish the various processes described above. Only typical values are provided in this summary

Table 1.1 : Front end process differentiators

	1.8V FET	3.3V FET	Nat-ive FET	Deep N Well for triple well isolation	Deep Trench Process	HS NPN*	Varactor type (bl, ni, or MOS)	High value poly resistor **	Schottky Diode
SBC18HX	Yes	Yes	No	No	Yes	Yes	BI, MOS	No	No
SBC18HXL	Yes	Yes	No	Yes	Yes	Yes	BI, MOS	No	Yes
SBC18HA	Yes	Yes	No	Yes	Yes	Yes	BI, MOS	Yes	Yes
SBC18PT	Yes	Yes	No	No	No	No	BI, MOS	Yes	No
SBC18QTD	No	Yes	No	No	Yes	No	BI	Yes	No
SBC18QTR	No	Yes	No	No	Yes	No	BI	Yes	Yes
SBC18QTL	No	Yes	No	Yes	Yes	No	BI	Yes	No
SBC18QW	No	Yes	No	No	No	No	Ni	Yes	No
SBC18MW	No	Yes	No	No	No	No	Ni	Yes	No
SBC18MWD	No	Yes	No	No	Yes	No	BI	Yes	No
SBC18MV	No	Yes	No	No	No	No	BI	Yes	No

* Standard and high voltage NPNs are available for all processes
** Silicided poly resistors, low value unsilicided poly resistors and nwell resistors are available for all processes

Table 1.2 : Back end process differentiators

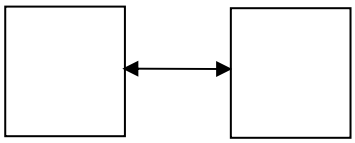
	No. of metal layers	MIM cap	Stacked MIM cap	Metal resistor	MT thickness/ VT height*	MT-1 thickness / VT-1 height
SBC18HX	6	1fF between M4/M5	No	Yes	2.8um/ 2.0um	1.6um/ 2.0um
SBC18HXL	6	1fF between M4/M5	No	Yes	2.8um/ 2.0um	1.6um/ 2.0um
SBC18HA	6	2.8fF between M4/M5	Yes***	Yes	2.8um/ 2.0um	1.6um/ 2.0um
SBC18PT	5	2fF between M2/M3	Yes**	No	5.2um/ 2.0um	1.6um/ 2.0um
SBC18QTD	4	2fF between M2/M3	No	No	5.2um/ 3.0um	0.635um/0.95um
SBC18QTR	4	2fF between M2/M3	No	Yes	5.2um/ 3.0um	0.635um/0.95um
SBC18QTL	4	2fF between M2/M3	No	No	5.2um/ 3.0um	0.635um/0.95um
SBC18QW	4	2fF between M2/M3	Yes**	No	2.8um/ 2.0um	0.635um/0.95um
SBC18MW	3	2fF between M2/M3	No	No	2.8um/ 2.0um	0.635um/0.95um
SBC18MWD	3	2fF between M2/M3	No	No	2.8um/ 2.0um	0.635um/0.95um
SBC18MV	3	2fF between M2/M3	No	No	2.8um/ 2.0um	0.635um/0.95um

MT = topmost metal; VT = topmost via
** Stacked capacitor density is 2 + 2 = 4fF/um^2 between M2/M3/M4
*** Stacked capacitor density for SBC18HA is 5.6fF/um^2 between M3/M4/M5.
Note: Process names which end with letter “Z” have polyimide overcoats

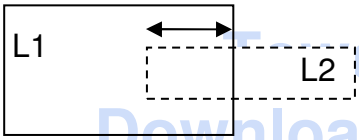
1.2 Terminology of Rules

A description of typical terminology used in the design rules is shown below.

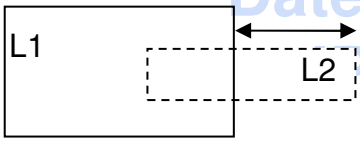
WIDTH OR LENGTH



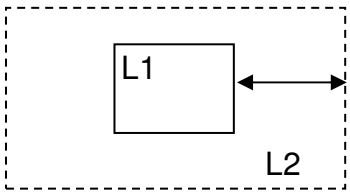
SPACE OR DISTANCE



L2 OVERLAP INTO L1



L2 OVERLAP OUT OF L1



L2 OVERPLOT OF L1
(Note: L1 is covered by L2)

2 Applicable Documents

SBC18 Electrical Specification	NPB-PS-0267
SBC18 Analog Characterization Report	NPB- PS 0392
SBC18 Design Manual	NPB-PS-0288
Digital Design Manual	NPB PS-0402
Spice Data Bank	NPB-PS-0268
SBC18 ESD Design Manual	NPB-PS-0411

3 Mask Set

3.1 Reticle Layers per Process Sequence:

Layer No.	Layer Name	Mask Name	Field	Process			
				SBC18 HX	SBC18 HXL	SBC18 HA	SBC18 PT
4	N+ Buried Layer	BL	Negative	Y	Y	Y	Y
36	Deep N Well	DNW	Negative		Y	Y	
0	Zero layer*	ZL	Positive	Y	Y	Y	Y
2	Active	A	Positive	Y	Y	Y	Y
15	Reverse active	RA	Negative	Y	Y	Y	Y
41	Deep Trench	DT	Negative	Y	Y	Y	
10	Collector Sinker	CS	Negative	Y	Y	Y	Y
3	Field Implant	F	Positive	Y	Y	Y	Y
1	Well	W	Negative	Y	Y	Y	Y
12	Dual Gate	DG	Positive	Y	Y	Y	Y
5	First Poly	FP	Positive	Y	Y	Y	Y
14	DN implant	DN	Negative	Y	Y	Y	Y
61	NK implant	NK	Negative	Y	Y	Y	Y
59	PK implant	PK	Negative	Y	Y	Y	Y
16	DP implant	DP	Negative	Y	Y	Y	Y
44	Local Collector Implant	LC	Negative	Y	Y	Y	Y
34	High Speed NPN implant	HS	Negative	Y	Y	Y	
21	Spacer Clear	SC	Negative	Y	Y	Y	Y
31	Emitter	EM	Positive	Y	Y	Y	Y
33	Emitter Window	EW	Negative	Y	Y	Y	Y
29	Emitter Poly	EP	Positive	Y	Y	Y	Y
23	Base Poly	BP	Positive	Y	Y	Y	Y

Layer No.	Layer Name	Mask Name	Field	Process			
				SBC18 HX	SBC18 HXL	SBC18 HA	SBC18 PT
6	N+ Implant	NI	Negative	Y	Y	Y	Y
11	P+ Implant	PI	Negative	Y	Y	Y	Y
13	Varactor	VR	Negative	Y	Y	Y	Y
54	High Value Resistor Implant	HR	Negative			Y	Y
40	Silicide Block	SB	Positive	Y	Y	Y	Y
7	Contact	C	Negative	Y	Y	Y	Y
8	First Metal (Metal 1)	M1	Positive	Y	Y	Y	Y
17	First Via (Via1)	VA	Negative	Y	Y	Y	Y
22	Top MIM capacitor plate	TM	Positive				Y
18	Second Metal (Metal 2)	M2	Positive	Y	Y	Y	Y
27	Second Via (Via2)	V2	Negative	Y	Y	Y	Y
30	Stacked Top MIM cap. Plate	TM2	Positive			Y	Y
28	Third Metal (Metal 3)	M3	Positive	Y	Y	Y	Y
26	Metal Resistor	TR	Positive	Y	Y	Y	
37	Third Via (Via 3)	V3	Negative	Y	Y	Y	Y
22	Top MIM capacitor plate	TM	Positive	Y	Y	Y	
38	Fourth Metal (Metal 4)	M4	Positive	Y	Y	Y	Y
47	Via 4	V4	Negative	Y	Y	Y	Y
48	Fifth Metal (Metal 5)	M5	Positive	Y	Y	Y	Y
57	Via 5	V4	Negative	Y	Y	Y	
58	Sixth Metal (Metal 6)	M6	Positive	Y	Y	Y	
9**	Protective Overcoat	S	Negative	Y	Y	Y	Y
	Total No. of masks			39	40	42	36

* Not included in total number of mask count

** Mask layer 9 becomes mask layer 99 for polyimide overcoat process variants with letter “Z” appended to parent process name

Layer No.	Layer Name	Mask Name	Field	Process						
				SBC 18 MW	SBC 18 MWD	SBC 18 MV	SBC 18 QW	SBC 18 QTD	SBC 18 QTR	SBC 18 QTL
4	N+ Buried Layer	BL	Neg.	Y	Y	Y	Y	Y	Y	Y
36	Deep N Well	DNW	Neg.							Y
0	Zero layer*	ZL	Pos.	Y	Y	Y	Y	Y	Y	Y
2	Active	A	Pos.	Y	Y	Y	Y	Y	Y	Y
15	Reverse active	RA	Neg.	Y	Y	Y	Y	Y	Y	Y
41	Deep Trench	DT	Neg.		Y			Y	Y	Y
10	Collector Sinker	CS	Neg.	Y	Y	Y	Y	Y	Y	Y
3	Field Implant	F	Pos.	Y	Y	Y	Y	Y	Y	Y
1	Well	W	Neg.	Y	Y	Y	Y	Y	Y	Y
12	Dual Gate	DG	Pos.							
5	First Poly	FP	Pos.	Y	Y	Y	Y	Y	Y	Y
14	DN implant	DN	Neg.	Y	Y	Y	Y	Y	Y	Y
61	NK Implant	NK	Neg.							
59	PK implant	PK	Neg.	Y	Y	Y	Y	Y	Y	Y
16	DP Implant	DP	Neg.							
44	Local Collector Implant	LC	Neg.	Y	Y	Y	Y	Y	Y	Y
34	High Speed NPN Implant	HS	Neg.							
21	Spacer Clear	SC	Neg.	Y	Y	Y	Y	Y	Y	Y
31	Emitter	EM	Pos.	Y	Y	Y	Y	Y	Y	Y
33	Emitter Window	EW	Neg.	Y	Y	Y	Y	Y	Y	Y

Layer No.	Layer Name	Mask Name	Field	Process						
				SBC 18 MW	SBC 18 MWD	SBC 18 MV	SBC 18 QW	SBC 18 QTD	SBC 18 QTR	SBC 18 QTL
29	Emitter Poly	EP	Pos.	Y	Y	Y	Y	Y	Y	Y
23	Base Poly	BP	Pos.	Y	Y	Y	Y	Y	Y	Y
6	N+ Implant	NI	Neg.	Y	Y	Y	Y	Y	Y	Y
11	P+ Implant	PI	Neg.	Y	Y	Y	Y	Y	Y	Y
13	Varactor	VR	Neg.		Y	Y		Y	Y	Y
54	High Val. Resistor Implant	HR	Neg.	Y	Y	Y	Y	Y	Y	Y
40	Silicide Block	SB	Pos.	Y	Y	Y	Y	Y	Y	Y
7	Contact	C	Neg.	Y	Y	Y	Y	Y	Y	Y
8	First Metal (Metal 1)	M1	Pos.	Y	Y	Y	Y	Y	Y	Y
26	Metal Resistor	TR	Pos.						Y	
17	First Via (Via1)	VA	Neg.	Y	Y	Y	Y	Y	Y	Y
22	Top MIM capacitor plate	TM	Pos.	Y	Y	Y	Y	Y	Y	Y
18	Second Metal (Metal 2)	M2	Pos.	Y	Y	Y	Y	Y	Y	Y
27	Second Via (Via2)	V2	Neg.	Y	Y	Y	Y	Y	Y	Y
30	Stacked Top MIM cap. Plate	TM2	Pos.				Y			
28	Third Metal (Metal 3)	M3	Pos.	Y	Y	Y	Y	Y	Y	Y
37	Third Via (Via3)	V3	Neg.				Y	Y	Y	Y
38	Fourth Metal (Metal 4)	M4	Pos.				Y	Y	Y	Y
9**	Protective Overcoat	S	Neg.	Y	Y	Y	Y	Y	Y	Y
	Total No. of masks			27	29	28	30	31	32	32

* Not included in total number of mask count

** Mask layer 9 becomes mask layer 99 for polyimide overcoat process variants with letter “Z” appended to parent process name

3.2 Assigned Layer Numbers

Note: In the Type column, D = DRAWN layer, G = GENERATED layer, M = MARKING layer, P = pin layer, R = Resistor, B = Block, F = Fill

Layer No/ datatype	Layer Name	Cadence Layer Name	Abbr	Type
1/0	Nwell	nwell	W	D
2/0	Active	act	A	D
3/0	Field	field	F	G
4/0	N+ Buried Layer	nbur	B	D
5/0	First Poly	poly	FP	D
5/30	Dummy poly fill block	poly		B
6/0	N+ Implant	cni	NI	D
7/0	Contact	contact	C	D/G
8/0	Metal 1	metal1	M1	D
8/5	Dummy metal 1 resistor	metal1		R
8/30	Dummy metal 1 fill block	metal1		B
8/31	Dummy metal 1 fill	metal1		F
9/0	Silox	silox	S	D
10/0	Collector Sinker	csink	CS	D
11/0	P+ Implant	cpi	PI	D
12/0	Dual Gate	Dgate	DG	D
13/0	Varactor	Varac	VR	D
14/0	DN implant	Dni	DN	G
15/0	Reverse Active	revact	RA	G
16/0	DP Implant	Dpi	DP	G

Layer No/ Datatype	Layer Name	Cadence Layer Name	Abbr	Type
17/0	Via1	via1	VA	D/G
18/0	Metal 2	Metal2	M2	D
18/5	Dummy metal 2 resistor	Metal2		R
18/30	Dummy metal 2 fill block	Metal2		B
18/31	Dummy metal 2 fill	Metal2		F
21/0	Spacer Clear	spacec	SC	D
22/0	TiN Cap Metal	topmm	TM	D
23/0	Base Poly	Bpoly	BP	D
24/0	MIS capacitor marking	C_cell		M
26/0	Metal resistor	Tnr	TR	D
27/0	Via 2	via2	V2	D
28/0	Metal 3	metal3	M3	D
28/5	Dummy metal 3 resistor	metal3		R
28/30	Dummy metal 3 fill block	metal3		B
28/31	Dummy metal 3 fill	metal3		F
29/0	Emitter Poly	epoly	EP	D
30/0	Stacked TiN Cap Metal	topmm2	TM2	D
31/0	Emitter	emtr	EM	D

Layer No./ datatype	Layer Name	Cadence layer name	Abbr	Type
32/0	Slot Via1	slotvia	SV1	D
33/0	Emitter Window	ewin	EW	D
34/0	High Speed NPN Implant	hsimp	HS	D
36/0	Deep N Well	dnwell	DNW	D
37/0	Via 3	via3	V3	D
38/0	Metal 4	metal4	M4	D
38/5	Dummy metal 4 resistor	metal4		R
38/30	Dummy metal 4 fill block	metal4		B
38/31	Dummy metal 4 fill	metal4		F
39/0	Bipolar (CMOS vertical pnp) marking	bjtdev		M
40/0	Silicide Block	sblk	SB	D
41/0	Deep Trench	dtrench	DT	D
42/0	Reserved*			
44/0	Local Collector	lcoll	LC	D
45/0	Artifact Marking Layer	artifact	CART	M
46/0	Fuse Marking layer	dcty	DCTY	M
47/0	Via4	via4	V4	D
48/0	Metal 5	metal5	M5	D
48/5	Dummy metal 5 resistor	metal5		R
48/30	Dummy metal 5 fill block	metal5		B

*These layers are reserved for engineering development work or for potential future process enhancements, and may be added at a later time.

Layer No/ Datatype	Layer Name	Cadence Layer Name	Abbr	Type
48/31	Dummy metal 5 fill	metal5		F
49/0	Reserved*			D
51/0	Inductor marking layer	L_cell	LCELL	M
52/0	Native Implant	natvimp	NV	D
54/0	High value resistor	hrimp	HR	D
55/0	Slot contact	slotct	CC	D
57/0	Via 5	via5	V5	D
58/0	Metal 6	metal6	M6	D
58/5	Dummy metal 6 resistor	metal6		R
58/30	Dummy metal 6 fill block	metal6		B
58/31	Dummy metal 6 fill	metal6		F
59/0	PK Implant	pkmsk	PK	G
61/0	NK Implant	nkmsk	NK	G
62/0	Analog marking layer	analog		M
63/0	Cell Outline Marking Layer	Outline/ prboundary		M
64/0	Bipolar NPN Cell Marking	N_cell	N_Cell	M
66/0	Bipolar lateral PNP Cell marking	P_cell	P_Cell	M
68/0	Nwell 2	nwell2	Nwell_2	D
70/0	2fF MIM cap marking layer	cap2fF		M
74/0	Jazz Pad marking layer	jazzPad		M

*These layers are reserved for engineering development work or for potential future process enhancements, and may be added at a later time.

Layer No./ datatype	Layer Name	Cadence layer name	Abbr	Type
75/0	Diode marking layer	diodev	DIOD	M
78/0	RAM marking layer	Cram	CRAM	M
79/0	ROM marking layer	Crom	CROM	M
80/0	Nwell resistor marking	resdev	RWEL	M
88/0	Metal 1 Pin			P
89/0	Metal 2 Pin			P
90/0	Metal 3 Pin			P
91/0	Metal 4 Pin			P
92/0	Metal 5 Pin			P
93/0	Metal 6 Pin			P
95/0	Analog block border	ablb	ABLB	M
96/0	Bump Pad marking layer	bumpPad		M
97/0	Poly OPC block	Plybopc	POPCB	M
98/0	M1 OPC block	m1bopc	M1OPCB	M
99/0	Polyimide opening		PO	G
101/0	RF FET marking layer	fetRFmrk		M
102/0	Strip resistor marking layer	restrmrk		M
105/0	Analog (gated) LPNP marking	lpnp		M
106/0	Schottky diode marking layer	schotky		M
107/0	Varactor marking layer	varacm	Varacm	M
108/0	Silicided Resistor marking	rpsdev	SR_Cell	M
118/36	Standard cell marking layer	stdCMrk		M

These layers are reserved for engineering development work or for potential future process enhancements, and may be added at a later time.

3.3 Description of Mask Layers:

- **Buried-Layer (BL) – Layer 4**

This mask defines regions to be implanted with arsenic, forming low resistive paths for the NPN collectors and LPNP bases.

- **Deep N Well (DNW) – Layer 36**

This mask defines the regions to be implanted with additional deep triple well n-type implant for NFET isolation.

- **Active (A) – Layer 2**

This mask defines all active areas.

- **Reverse Active (RA) – Layer 15**

This mask defines all reverse active areas. This layer is generated from active per section 3.5.

- **Deep Trench (DT) – Layer 41**

This mask defines the deep trench used for NPN isolation.

- **Collector Sinker (CS) – Layer 10**

This mask defines regions to be implanted by phosphorus for low resistance connection to the underlying N+ buried layer.

- **N-well (W) – Layer 1**

This mask defines all CMOS regions to receive N-well, PMOS Vt, and PMOS punchthrough implants.

- **Field (F) – Layer 3**

This mask defines all regions to receive NMOS Vt, NMOS punchthrough, and boron field implants. The boron field implant is used for CMOS and NPN device isolation. This layer is generated from the N-well (layer 1) and N-well2 (layer 68) per section 3.5.

- **Dual Gate (DG) – Layer 12**

This mask defines the areas that are to have thick gate oxides for dual gate oxide process. Drawn DG and SC layers get thick oxide. This layer is generated per section 3.5.

- **First Poly (FP) – Layer 5**

This mask defines the gate of CMOS transistors. This mask also defines silicided and unsilicided poly resistors.

- **DN Implant (DN) – Layer 14**

This mask defines regions to receive the thick gate oxide NMOS LDD implants only. It is generated per section 3.5.

- **DP Implant (DP) – Layer 16**

This mask defines regions to receive the thin gate oxide PMOS pocket implants. It is generated per section 3.5.

- **NK Implant (NK) – Layer 61**

This mask defines regions to receive the thin gate oxide NMOS LDD implants and pocket implants. It is generated per section 3.5.

- **PK Implant (PK) – Layer 59**

This mask defines regions to receive the shared thin gate oxide and thick gate oxide PMOS LDD implants. It is generated per section 3.5.

- **Local Collector (LC) – Layer 44**

This mask opens the 3 V NPN for SIC implants for standard NPN version

- **High Speed NPN implant (HS) – Layer 34**

This mask opens the high speed NPN for SIC implants for high speed NPN version.

- **Spacer Clear (SC) – Layer 21**

This mask defines regions where the spacer dielectric is cleared to form the base of the NPN and the emitter of the L-PNP.

- **Emitter (EM) – Layer 31**

This mask define emitter area of NPNs

- **Emitter Window (EW) – Layer 33**

This mask defines an intermediate masking step during emitter formation for NPNs.

- **Emitter Poly (EP) – Layer 29**

This mask defines the NPN emitter poly.

- **Base Poly (BP) – Layer 23**

This mask defines the base poly layer.

- **N+ Implant (NI) – Layer 6**

This mask defines regions to receive the NMOS N+ source/drain implants.

- **P+ Implant (PI) – Layer 11**

This mask defines regions to receive the PMOS P+ source/drain implants. It is also used to implant the collector of the LPNP, P+ poly resistors, and substrate contacts.

- **Varactor (VR) – Layer 13**

This mask defines the areas getting varactor implants to obtain high Q.

- **High Value Resistor Implant (HR) – Layer 54**

This mask defines the implant regions for high value resistor.

- **Silicide Block (SB) – Layer 40**

This mask defines regions where silicide formation is blocked. This mask is used to form poly resistors.

- **Contact I – Layer 7**

This mask defines active and poly contacts to metal 1. This layer is used together with slot contact (layer 55) to generate the final contact layer (Layer 7) per section 3.4.

- **Slot Contact (CC) – Layer 55**

This mask defines emitter poly and collector sinker contacts to metal 1 in the NPN cell.

- **First Metal (M1) – Layer 8**

This mask defines the first metal layer.

- **Via1 (VA) – Layer 17**

This mask defines metal 2 to metal 1 contact areas. This layer is used together with slot via1 (layer 32) to generate the final via 1 layer (Layer 17) per section 3.4.

- **Slot Via1 (SV1) – Layer 32**

This mask defines metal 2 to metal 1 contact areas on emitter poly and collector sinker in the NPN cell

- **Second Metal (M2) – Layer 18**

This mask defines the second metal layer.

- **Top MIM Capacitor Plate – Layer 22**

This mask defines the top plate of the MIM capacitor. This mask also defines the top plate of the lower MIM capacitor of the stacked MIM capacitor.

- **Via2 (V2) – Layer 27**

This mask defines metal 3 to metal 2 contact areas.

- **Stacked Top MIM Capacitor Plate (TM2) – Layer 30**

This mask defines the top plate of the upper MIM capacitor of the stacked MIM capacitor.

- **Third Metal (M3) – Layer 28**

This mask defines the third metal layer.

- **Metal Resistor layer (TR) – Layer 26**

This mask defines the metal resistor layer.

- **Via3 (V3) – Layer 37**

This mask defines metal 4 to metal 3 contact areas.

- **Fourth Metal (M4) – Layer 38**

This mask defines the fourth metal layer.

- **Via4 (V4) – Layer 47**

This mask defines metal 5 to metal 4 contact areas.

- **Fifth Metal (M5) – Layer 48**

This mask defines the fifth metal layer.

- **Via5 (V5) – Layer 57**

This mask defines metal 6 to metal 5 contact areas.

- **Sixth Metal (M6) – Layer 58**

This mask defines the sixth metal layer.

- **Silox (S) – Layer 9**

This mask defines openings in the passivation layer over contact pads.

- **Polyimide Opening (PO) – Layer 99**

This mask defines openings in the passivation layer with additional polyimide overcoat over contact pads. Process variants with polyimide overcoat have layer 99 generated from drawn layer 9 as described in Section 3.5, and use PO (layer 99) mask instead of S (layer 9) mask.

3.4 Boundary, Pin, Device and LVS Marking Layers:

The following layers are used to identify device types for LVS and DRC checks and must be drawn to encompass the extent of each respective device type: NPN, L-PNP, Nwell resistor, silicided poly resistor, inductor, ESD, wirebond pads, varactor, fuse, SRAM cell, and diodes.

Layer No./ datatype	Layer Name	Device Type
45/0	Artifact	Part number and mask revision number / letter marking layer to prevent layer generation;
64/0	N_cell	Bipolar NPN marking layer*
66/0	P_cell	Bipolar Lateral PNP marking layer
39/0	bjtdev	Vertical PNP marking layer
68/0	Nwell2	This is a design layer that defines regions that do not receive either field implants or well implants. It is used in the NPN, lateral PNP and other devices. This layer is used together with the N-well (Layer 1) to generate the field layer (Layer 3) per section 3.4
75/0	DIOD	N and P Diode marking layer
106/0	schottky	Schottky Diode marking layer
80/0	RWEL	Nwell resistor marking layer
108/0	SR_cell	Silicided Poly Resistor marking layer
107/0	Varacm	Varactor marking layer
70/0	Cap2fF	2fF/um^2 density MIM capacitor marking layer
51/0	L_cell	Inductor marking layer
46/0	DCTY	Fuse marking layer
78/0	CRAM	Jazz SRAM cell marking layer
118/36	stdCMrk	Standard cell marking layer

Layer No./ datatype	Layer Name	Device Type
74/0	Jazzpad	Jazz pad marking layer
96/0	Bumppad	Bump pad marking layer
95/0	ABLB	Analog Block Border
62/0	Analog	LVS marking layer to isolate p-sub connections between circuit blocks
101/0	fetRFmrk	RF FET marking layer for LVS
102/0	restrmrk	Resistor Strip marking layer for LVS
88/0	Metal 1 Pin	Metal 1 Layout Node identification for LVS
89/0	Metal 2 Pin	Metal 2 Layout Node identification for LVS
90/0	Metal 3 Pin	Metal 3 Layout Node identification for LVS
91/0	Metal 4 Pin	Metal 4 Layout Node identification for LVS
92/0	Metal 5 Pin	Metal 5 Layout Node identification for LVS
93/0	Metal 6 Pin	Metal 6 Layout Node identification for LVS
8/5, 18/5, 28/5, 38/5, 48/5, 58/5		Datatype 5 for the metal layers is a marking layer used for dummy resistors which enables a net to be attached to multiple net names for lvs purpose
8/30, 18/30, 28/30, 38/30, 48/30, 58/30		Datatype 30 for the metal layers is a marking layer used for dummy metal fill block during dummy metal fill layer generation (as described in Section 3.5) for each individual metal layer
8/31, 18/31, 28/31, 38/31, 48/31, 58/31		Datatype 31 for the metal layers is used for customer drawn custom dummy metal fill. Datatype 31 is not allowed for poly layer as customer drawn custom poly fill interferes with dummy active layer generation. The soft erc check will ignore the floating metal violations for this datatype. Jazz dummy metal generation algorithm will still generate additional dummy metal in areas beyond datatypes 31 and 0, following dummy metal layer generation described in Section 3.

* Including High speed NPNs, Standard NPNs, and High Voltage NPNs.

3.5 Layer Generation Algorithms:

Note: This section is presented for reference only.

This section, along with sections 3.5.1 and 3.5.2, is reserved for documenting the MaskCAD operations used to generate specific process layers as well as generating dummy active and dummy metal fills. These MaskCAD operations are done after data tape-in at the foundry during data post processing and prior to data tape-out to the mask shop.

Please note that layer 45 (CART) is artifact marking layer.

```
Chip = EXTENT
resa = lay5 AND lay40        // finds poly resistors only
resb = SIZE resa BY 0.50     // poly resistor exclusion for generated implants
```

Active layer generation

```
//  Finds SRAM data and performs edge extensions on small geometries
    a1 = lay2 AND lay78
    b = int a1 < 0.01 abut ==90 intersecting only region
    c = int a1 < 0.6 opposite region
    d = size c by 0.02
    e = enc a1 d < 0.03 opposite region
    f = e interact b == 2          // f = special SRAM sizing

//  Finds active edges near deep trench and adds .05 bias
    act_a = lay2 NOT lay45
    edge1 = EXTERNAL act_a lay41 <= 0.50 REGION
    edge2 = TOUCH EDGE act_a edge1
    edge3 = EXPAND EDGE edge2 OUTSIDE BY 0.05 EXTEND BY 0.05
    act_b = edge3 OR lay2
    act_c = SIZE act_b BY –0.03
    act_d = SIZE act_c BY +0.03   // act_d = special NPN sizing
    act_e = act_d OR f
    final_active = act_e OR lay2
```


Reverse Active layer Generation

```
drn15 = lay15 AND lay45   // RA for drawn active
act1  = final_active NOT lay45
act2  = SIZE act1 BY –0.25
act3  = SIZE act2 BY +0.11
ra15  = drn15 OR act3
```

Field layer generation

drn3 = lay3 AND lay45 // Ignores drawn Field in ckt regions
ckt1 = lay1 NOT lay45
ckt64 = lay64 NOT lay45
ckt68 = (lay68 + 0.3) NOT lay45
f3 = (drn3 OR ckt1) OR (ckt64 OR ckt68)

Buried layer generation

drn4 = lay4 AND lay45
bl_1 = lay4 INTERACT lay64
bl_2 = lay4 NOT bl_1
bl_3 = SIZE bl_1 BY -0.50
bl4 = drn4 OR (bl_2 OR bl_3)

DG layer generation

npn_bl = (lay4 NOT lay45) INTERACT lay64
no_trch_npn = npn_bl NOT INTERACT lay41
dg1 = SIZE no_trch_npn BY +0.30
trch_npn = lay41 INTERACT npn_bl
holes_npn = HOLES trch_npn
dg2 = holes_npn OR (SIZE trch_npn BY +0.40)
dg3 = (dg1 OR dg2) OR lay12
dg12 = dg3 NOT lay10

DN layer generation

drn14 = lay14 AND lay45 // DN layer generation
dn1 = lay6 AND lay12
dn2 = dn1 NOT lay45
dn3 = dn2 NOT resb
dn4 = SIZE dn3 BY –0.17
dn5 = SIZE dn4 BY +0.17
dn14 = drn14 OR dn5

DP layer generation

drn16 = lay16 AND lay45 // DP layer generation
dp1 = lay11 AND lay1
dp2 = dp1 NOT lay45
dp3 = dp2 NOT resb
dp4 = dp3 NOT lay12
dp5 = SIZE dp4 BY –0.17
dp6 = SIZE dp5 BY +0.17
dp16 = drn16 OR dp6

PK layer generation

```
drn59 = lay59 AND lay45
pk1   = lay11 AND lay1
pk2   = pk1   NOT resb
pk3   = pk2   NOT lay45
pk4   = pk3   NOT lay64
pk5   = pk4   NOT lay68
pk6   = SIZE  pk5 BY +0.17  // notch fill
pk7   = SIZE  pk6 BY –0.34  // desliver
pk8   = SIZE  pk7 BY +0.17
pk59 = drn59 OR pk8
```

NK layer generation

```
drn61 = lay61 AND lay45
nk1   = lay6  NOT lay1
nk2   = nk1   NOT lay12
nk3   = nk2   NOT resb
nk4   = nk3   NOT lay64
nk5   = nk4   NOT lay68
nk6   = nk5   NOT lay45   // ni not well not dg not resistors not artifacts
nk7   = SIZE  nk6 BY –0.17  // desliver
nk8   = SIZE  nk7 BY +0.34  // notch fill
nk9   = SIZE  nk8 BY –0.17
nk61 = drn61 OR nk9
```


Contact layer generation

```
ckt55 = lay55 NOT lay45
cont1 = SIZE ckt55 BY –0.055
final_contact = lay7 OR cont1     // Contacts OR Slotted-Contacts
```

Via1 layer generation

```
ckt32 = lay32 NOT lay45
va1_1 = SIZE ckt32 BY –0.050
l17 = lay17 OR va1_1          // VIA OR Slotted-Via
```

Polyimide protective overcoat layer generation

```
po99 = lay9 NOT lay45
```

3.5.1 Dummy Metal Layer Generation

Dummy Metal 1 Layer Generation

Additional floating metal1 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 8.D. The following method of generation of dummy metal conforms to the process design rule.

1) The metal patterns consist of 3µmX3µm squares at a 4 µm pitch (1µm space). Filler patterns should be skewed from true horizontal and vertical by 1µm offset between squares (data file 1).

2) The circuit metal pattern is sized up by 17.5µm per edge (data file 2). Note: The 17.5µm exclusion may be changed to as low as 10µm if the metal density requirements are not met using the default dummy metal fill algorithm.

3) Subtracted data file 2 from dummy metal array (data file 1) – (data file 2) = (data file 3) to yield final dummy metal array with cut outs for the placement of circuit metal data.

4) Add data file 3 to the Layer 8 data to make metal 1 mask.

Dummy Metal 2 Layer Generation

Additional floating metal 2 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 18.D. The following method of generation of dummy metal conforms to the process design rule.

1) The metal patterns consist of 3µmX3µm squares at a 4µm pitch (1µm space). Filler patterns should be skewed from true horizontal and vertical by 1µm offset between squares (data file 1).

2) The circuit metal pattern is sized up by 17.5µm per edge (data file 2). Note: The 17.5µm exclusion may be changed to as low as 10µm if the metal density requirements are not met using the default dummy metal fill algorithm.

3) Subtracted data file 2 from dummy metal array (data file 1) – (data file 2) = (data file 3) to yield final dummy metal array with cut outs for the placement of circuit metal data.

4) Add data file 3 to the Layer 18 data to make metal 2 mask.

Dummy Metal 3 Layer Generation

Additional floating metal 3 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 28.D. The following method of generation of dummy metal conforms to the process design rule.

1. The metal patterns consist of 9µmX9µm squares at a 13µm pitch (4µm space) for SBC18MW/MV/MWD only. For all other processes with Metal 3, the metal patterns are consisted of 3µmX3µm squares at a 4 µm pitch (1µm space). Filler patterns should be skewed from true horizontal and vertical by 1µm offset between squares (data file 1).

2. The circuit metal pattern is sized up by 25µm per edge for all three metal layer SBC18 variants and 17.5µm per edge for all four, five and six metal layer SBC18 variants (data file 2). Note: The 25µm or 17.5µm exclusion may be changed to as low as 10µm if the metal density requirements are not met using the default dummy metal fill algorithm.

3. Subtracted data file 2 from dummy metal array (data file 1) – (data file 2) = (data file 3) to yield final dummy metal array with cut outs for the placement of circuit metal data.

4. Add data file 3 to the Layer 28 data to make metal 3 mask.

Dummy Metal 4 Layer Generation

Additional floating metal 4 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 38.D. The following method of generation of dummy metal conforms to the process design rule.

1. The metal patterns consist of 9µmX9µm squares at a 13µm pitch (4µm space) for SBC18QTD/QTR/QTL. For all other processes with Metal 4, the metal patterns are consisted of 3µmX3µm squares at a 4 µm pitch (1µm space). Filler patterns should be skewed from true horizontal and vertical by 1µm offset between squares (data file 1).

2. The circuit metal pattern is sized up by 25µm per edge for all four metal layer SBC18 variants and 17.5µm per edge for all five and six metal layer SBC18 variants (data file 2). Note: The 25µm or 17.5µm exclusion may be changed to as low as 10µm if the metal density requirements are not met using the default dummy metal fill algorithm.

3. Subtracted data file 2 from dummy metal array (data file 1) – (data file 2) = (data file 3) to yield final dummy metal array with cut outs for the placement of circuit metal data.

4. Add data file 3 to the Layer 38 data to make metal 4 mask.

Dummy Metal 5 Layer Generation

Additional floating metal 5 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 48.D. The following method of generation of dummy metal conforms to the process design rule.

1. The metal patterns consist of 9µmX9µm squares at a 13µm pitch (4µm space) for SBC18PT, only. For all other processes with Metal 5, the metal patterns are consisted of 3µmX3µm squares at a 4 µm pitch (1µm space). Filler patterns should be skewed from true horizontal and vertical by 1µm offset between squares (data file 1).

2. The circuit metal pattern is sized up by 25µm per edge for all five metal layer SBC18 variants and 17.5µm per edge for all six metal layer SBC18 variants (data file 2). Note: The 25µm or 17.5µm exclusion may be changed to as low as 10µm if the metal density requirements are not met using the default dummy metal fill algorithm.

3. Subtracted data file 2 from dummy metal array (data file 1) – (data file 2) = (data file 3) to yield final dummy metal array with cut outs for the placement of circuit metal data.

4. Add data file 3 to the Layer 48 data to make metal 5 mask.

Dummy Metal 6 Layer Generation

Additional floating metal 6 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 58.D. The following method of generation of dummy metal conforms to the process design rule

1. The metal patterns consist of 9µmX9µm squares at a 13µm pitch (4µm space) for SBC18HX/HXL only. For all other processes with Metal 6, the metal patterns are consisted of 3µmX3µm squares at a 4 µm pitch (1µm space). Filler patterns should be skewed from true horizontal and vertical by 1µm offset between squares (data file 1).

2. The circuit metal pattern is sized up by 25µm per edge. (data file 2). Note: The 25µm exclusion may be changed to as low as 10µm if the metal density requirements are not met using the default dummy metal fill algorithm.

3. Subtracted data file 2 from dummy metal array (data file 1) – (data file 2) = (data file 3) to yield final dummy metal array with cut outs for the placement of circuit metal data.

4. Add data file 3 to the Layer 58 data to make metal 6 mask.

3.5.2 Dummy Metal, Poly, Active Fill Exclusions

To prevent metal fill from causing mismatch on FETs, NPNs, capacitors, and resistors, and to eliminate additional parasitic capacitance on RF components, the following procedures will be followed.

1) All “white areas” of chip within ABLB (i.e. no features drawn in Nwell, active, poly, TM, TM2, TR or metal) will receive metal fills on all required metal layers as specified in Section 3.5.1.

2) Analog and RF blocks will be identified by drawing a marking border (ABLB Layer 95) 1um outside the analog/RF circuit regions. Normal metal fill rules as specified in Section 3.5.1 will be used to generate metal fill outside this border. All areas within ABLB layer must obey special RF metal overplot rules (See section 5.12)

3) For inductor areas of the circuit, an Inductor Marking Layer (layer 51) will be drawn. All mask areas containing layer 51 will not have any metal fill generated on any metal layer. This procedure will prevent metal fill from being placed in white space in the open region inside an inductor.

4) Dummy metal fill can be excluded in each individual metal layer by adding the dummy fill block marking layer, which is the metal layer number, datatype 30 (e.g., 8/30, 18/30, 28/30, 38/30, 48/30, and 58/30). However, metal density rules specified in the metal layer design rules in Section 4 must be met. Additionally, larger metal overplot rules of vias and larger minimum metal area rules, which are also applicable for regions within analog block border (ablb, layer 95) regions and described in Section 5.11, are triggered for ALL metal layers within dummy fill block marking layer for any metal.

5) Customer provided dummy metal fill can be added in each metal layer. All customer provided dummy metal fill must be drawn on regular metal (datatype 0), and enclosed and coincident with dummy metal fill marking layer which is the metal layer number, but datatype 31 (e.g., 8/31, 18/31, 28/31, 38/31, 48/31, and 58/31).

6) There is no provision to allow customers to define exclusion regions for dummy active fill. Guidelines for dummy active generation are described in Section 3.5.3 and 3.5.4. Note that these guidelines are applicable for dummy active fill below inductors, MIM capacitors, and pads.

7) Dummy poly fill can be excluded in certain regions by adding the dummy poly block marking layer, which is the poly layer number 5, datatype 30. However, poly density rules specified in the poly layer design rules in Section 4 must be met.

8) Customer provided dummy poly fill is disallowed as it affects dummy active layer generation. Soft_ERC check will flag any unconnected poly as floating_poly error (see Section 11).

The following rules are checked for dummy metal fill integrity

Rule No.	Rule Name
7.FILL	Layer 7 is not allowed within layer 8, datatype 31
8.FILL	Layer 8, datatype 31 is not coincident with layer 8, datatype 0
17.FILL	Layer 17 is not allowed within layer 8, datatype 31 or layer 18, datatype 31
18.FILL	Layer 18, datatype 31 is not coincident with layer 18, datatype 0
27.FILL	Layer 27 is not allowed within layer 18, datatype 31 or layer 28, datatype 31
28.FILL	Layer 28, datatype 31 is not coincident with layer 28, datatype 0
37.FILL	Layer 37 is not allowed within layer 28, datatype 31 or layer 38, datatype 31
38.FILL	Layer 38, datatype 31 is not coincident with layer 38, datatype 0
47.FILL	Layer 47 is not allowed within layer 38, datatype 31 or layer 48, datatype 31
48.FILL	Layer 48, datatype 31 is not coincident with layer 48, datatype 0
57.FILL	Layer 57 is not allowed within layer 48, datatype 31 or layer 58, datatype 31
58.FILL	Layer 58, datatype 31 is not coincident with layer 58, datatype 0

3.5.3 Dummy Active Generation

When the active features of the circuit design contains large open areas without active features, additional non-functional active features (dummy active) must be added to insure a uniform topography for CMP process.

The rules below are not checked but used while establishing layer generation algorithm

Rules 2.P through 2.Y are required to enable planarization process methods used for shallow trench isolation. A preferred generation method is described at the end of this section as a simple and effective way to meet the requirements of rules 2.P through 2.Y.

Rules 2.P through 2.Y are not checked since the dummy active pattern is algorithmically generated. It is assumed correct by generation.

Rule No.	Rule Name	
2.P	Maximum active to active space without dummy fill	10
2.U	Minimum dummy active separation from active -- distance that floating dummy active feature must be from circuit active feature	2.5
2.V	Minimum dummy active separation from N-well edge (including N-well resistors) (See Note 2)	2.0
2.W	Minimum dummy active separation from poly	2.0
2.Y	Dummy active is not allowed inside N-well resistors (See Note 2)	

Note 2: Rule 2.V and Rule 2.Y: A marking layer (Layer 80) is used to mark all the N-well resistors.

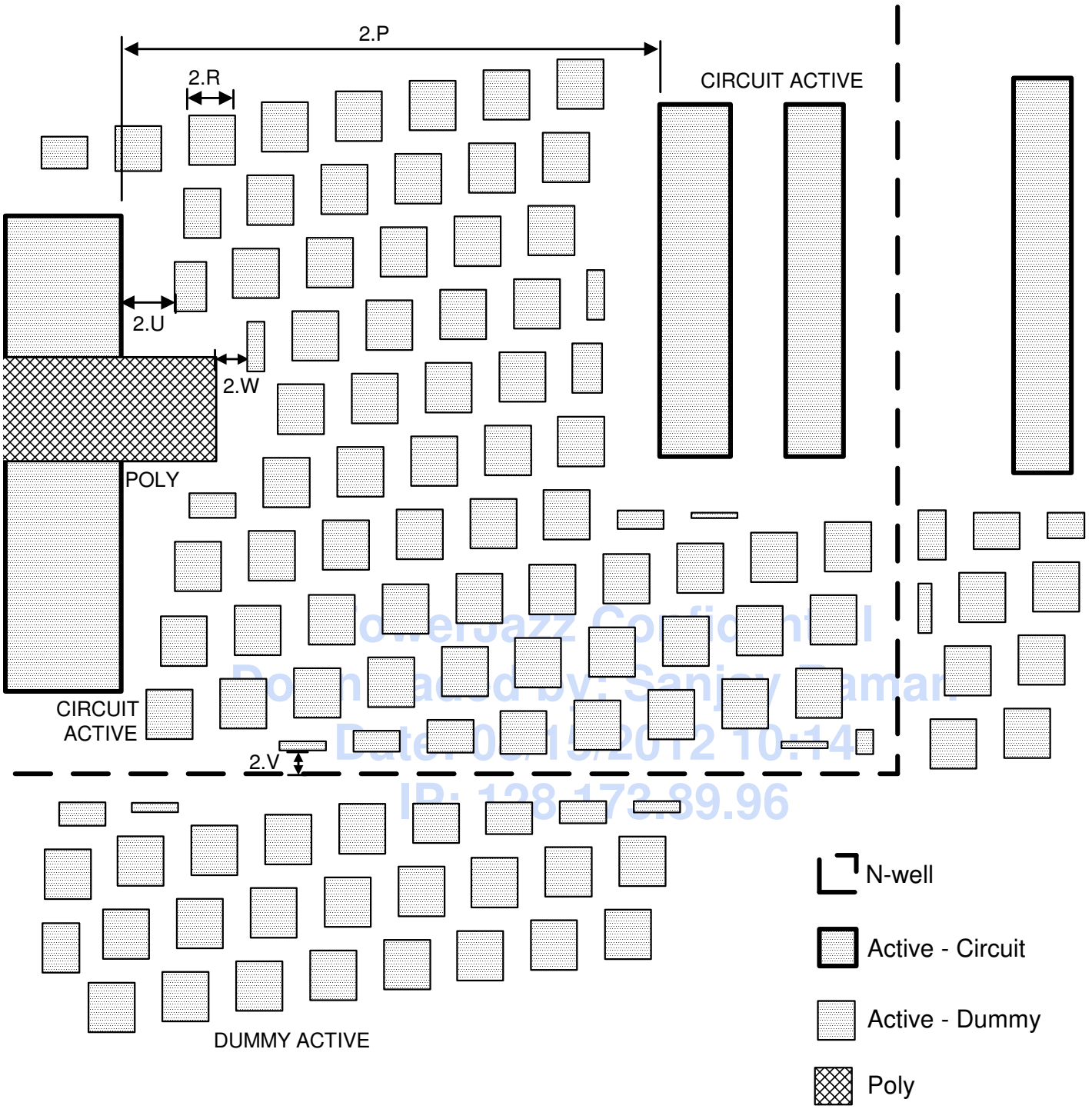


ILLUSTRATION 2.2

Dummy Active Generation and Rules

Dummy active generation algorithm: The following method for generation of dummy active conforms to the process design rules.

1) A staggered array of dummy active squares is created with the data center at chip center. 5µm X5 µm features with 3.0 µm separations. (data file 1) (See Illustration 2.2)

2) The circuit active pattern is sized up by 5 µm (half of Rule 2.P) per edge. Merge features and then size active pattern down by 2.5 µm ((half of Rule 2.P) – Rule 2.U) per edge. (data file 2).

3) Size poly layer up by 2 µm (Rule 2.W) per edge (data file 3)

4) Size up N-well resistor marking layer (layer 43) by 2 µm (data file 4)

5) Create a path 4.0 µm wide centered on All N-well boundaries. (data file 5) (Rule 2.V)

6) Add Data files (2+3+4+5 = data file 6)

7) Subtract data file 6 from dummy active array (data file 1) – (data file 6)= (data file 7) to yield dummy active array which has cut outs for the placement of circuit active data.

8) Size up circuit active pattern by 2.5 µm per edge (data file 8). Subtract data file 8 from data file 7 to yield final dummy active array (data file 9) = (data file 7) – (data file 8).

9) Size down final dummy active array (data file 9) by 0.20 µm per edge to eliminate slivers and then size up by 0.20 µm per edge to yield final dummy active array with no slivers. (data file 10)

10) Add data file 10 (no sliver final dummy active array) to the Layer 2 data for the original design. (data file 11)

11) Make active mask for circuit from data file 11. (Merged circuit active data and sized dummy active array)

See table in Section 3.5.4 for other exclusion regions in dummy active fill

3.5.4 Dummy Poly Fill Generation

The following method for generation of dummy poly conforms to the process design rules.

1) Exclusion regions in dummy active and dummy poly fill

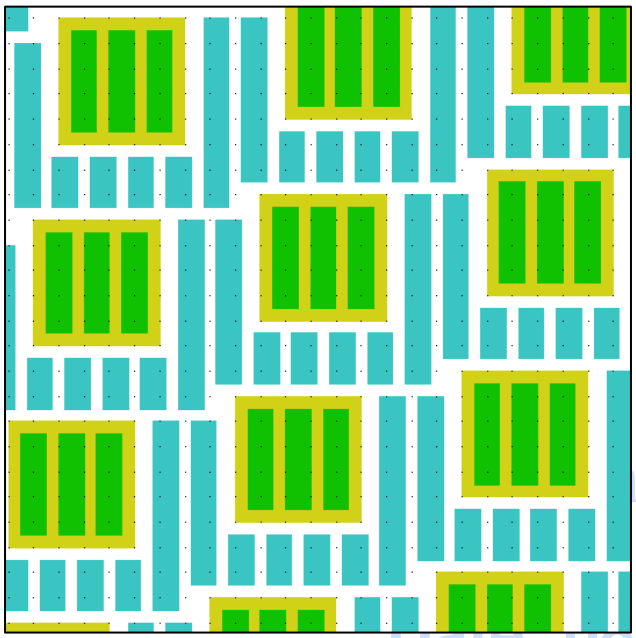
	For dummy active	For dummy poly
spacing to Active	2.5	2.5
spacing to Poly	2.0	2.0
spacing to nwell junction	2.0	2.0
spacing to nwell resistor marking (layer 80)	2.0	2.0
spacing to Artifact marking (layer 45)	0.3	0.3
spacing to N_cell marking (layer 64)	2.5	2.5
spacing to P_cell marking (layer 66)	2.5	2.5
spacing to NWell2	2.5	2.5
spacing to base poly	2.5	2.5
spacing to emitter poly	2.5	2.5
spacing to emitter window	2.5	2.5
spacing to TR (metal resistor)	5.0	5.0
spacing to deep trench	0.5	0.5
spacing to metal 1	N/A	2.0
spacing to TM (MIM capacitor)	N/A	5.0
spacing to fuse marking (layer 46)	N/A	10.0
spacing to inductor marking (layer 51)	N/A	25.0
spacing to bond pad	N/A	10.0
spacing to dummy poly block marking (layer 5, datatype 30)	N/A	5.0
Keep Partials	Yes	Yes
Keep Only Rectangles	No	Yes

2) Dummy Poly fill is not generated within partial dummy actives, i.e., dummy actives which are not 5um x 5um

3) Within the 5um x 5um dummy active, three 4x1 stripes of dummy poly are generated with 0.5um space to active edge and in between poly.

4) Within the field area, dummy poly is generated with feature width of 1um and space of 0.5um to active edge and in between poly. The minimum length of dummy poly is 2um and the maximum length is 7.5um

See Illustration 5.2 for examples of dummy poly fill.



Dummy active Dummy Poly

ILLUSTRATION 5.2

4 CMOS and Back End Design Rules

4.1 Active "A" (Layer 2)

Mask 2: This defines active areas (P-ch/N-ch FETs), diffused interconnect, and areas to be used for N-well and P-well (substrate) contacts. It is a positive mask and is aligned to the Zero layer. See Illustration 2.

Rule No.	Rule Name	SBC18HX SBC18HXL SBC18HA SBC18PT	SBC18HX SBC18HXL SBC18HA SBC18PT SBC18QTD SBC18QTR SBC18QTL SBC18QW SBC18MW SBC18MWD SBC18MV
		Thin gate	**Thick gate**
2.A	Minimum transistor width for thin gate oxide transistors	0.22	N/a
2.A.a	Minimum transistor width for thick gate oxide transistors, (DG mask)	n/a	0.40
2.B	Minimum conductor width	0.22	0.22
2.C	Minimum spacing.	0.28	0.28
2.D	Minimum spacing N+ outside the N-well to P+ inside the N-well	0.86	0.86
2.E	Minimum spacing P+ diffusion inside the N-well to N-well edge	0.43	0.43
2.F	Minimum spacing N+ diffusion outside the N-well to N-well edge.	0.43	0.43
2.G	Minimum spacing from N+ to P+ in the same type well and at the same potential (butting diffusion).	0.0	0.0
2.H	Minimum spacing N+ diffusion inside the N-well to N-well edge (except in the case of N-well resistors, see Rules 2.I, 2.I.a, in Section 5.3.5)	0.12	0.12
2.J	Minimum spacing P+ diffusion outside the N-well to N-well edge	0.12	0.12
2.K	Minimum active area	0.20 (μm^2)	0.20 (μm^2)

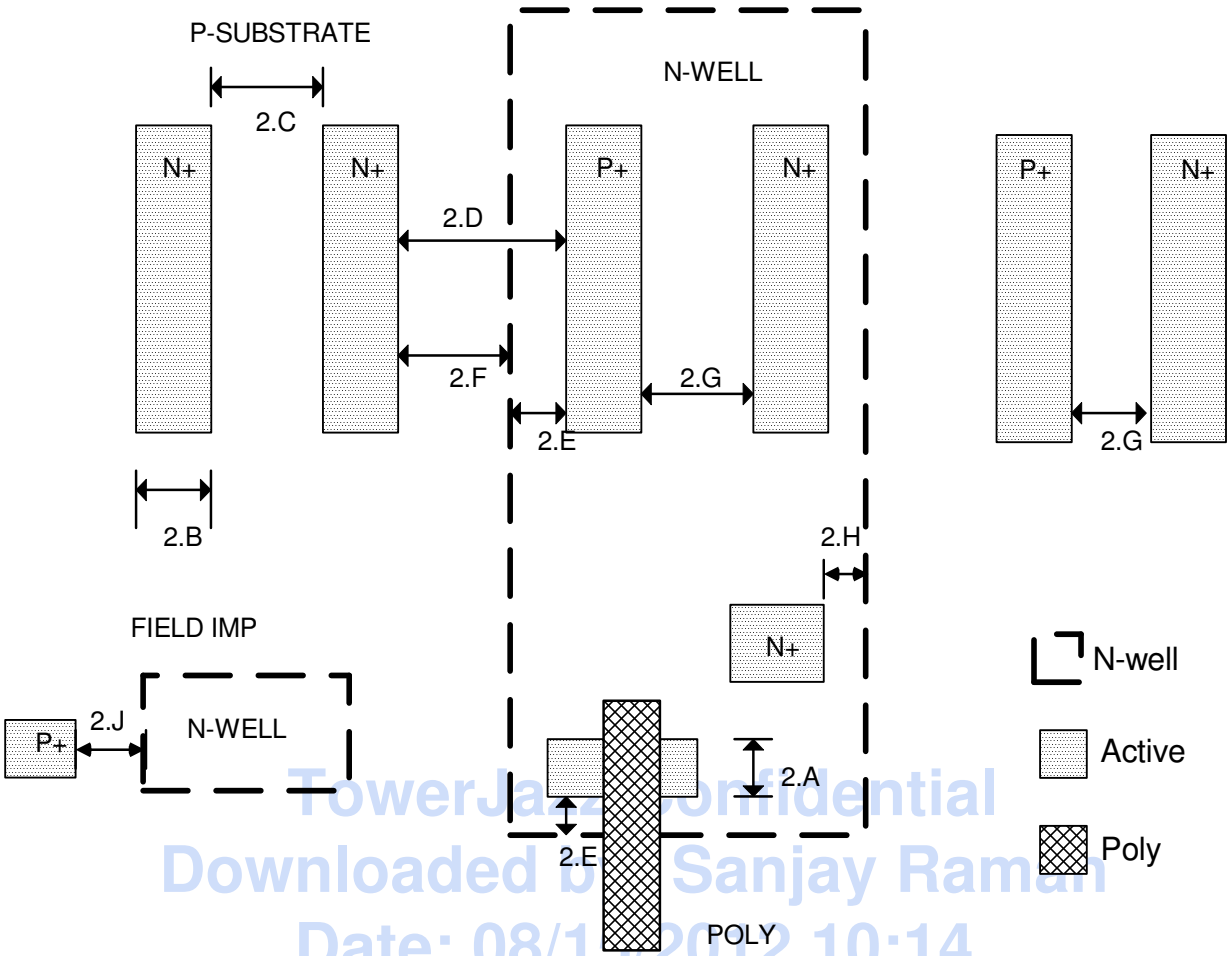


ILLUSTRATION 2

4.2 Reverse Active "RA" (Layer 15)

Mask 15: This mask is the reverse of the active mask. This layer is a derived layer. The reverse active mask is a negative mask and is aligned to the Zero layer. See Illustration 15.

The rules below are not checked and are used as guidelines for reverse active layer generation

Rule No.	Rule Name	
15.A	Reverse active feature required over all active which are larger than this minimum size	0.50X0.50
15.B	Minimum reverse active size	0.24
15.C	Active extension beyond reverse active feature (applied only when reverse active feature is present)	0.14
15.BAD	No drawn data is allowed for layer 15	

Note 1: Reverse active rules are not checked since the mask is algorithmically generated. It is assumed correct by generation.

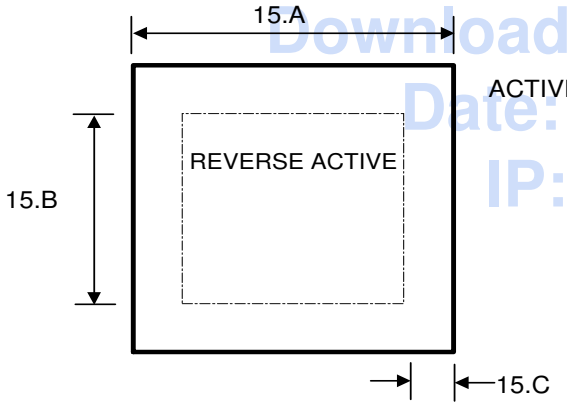


ILLUSTRATION 15

It is required that the reverse active layer be generated from the active mask data with the following algorithm:

1) Input file is mask active data. Mask active data = (original circuit active data and dummy active data). These elements may be processed separately, but reverse active must be created for both the circuit active data and dummy active filler pattern. (data file 1)
2) Size data file 1 down by 0.25um per edge to eliminate features of size 0.50um or smaller. Then size up the new result by 0.11um per edge, output the result on layer 15.The final result is active 0.14um per side overplot of reverse active.

4.3 N-well Implant "W" (Layer 1)

Mask 1: This mask defines the N-well regions in which phosphorus is implanted. All PFETs are located in the N-well region. The N-well is a negative (dark field) mask and is aligned to the Zero layer. The N-well edge is defined by the photoresist edge after developing. See Illustration 1.

Rule No.	Rule Name	
1.A	Minimum N-well width	0.86
1.B	Minimum N-well to N-well spacing for wells at the same potential (if smaller then merge)	0.60
1.C	Minimum N-well to N-well spacing for N-wells at different potentials	1.40

See Section 5.3.5 on Nwell resistors

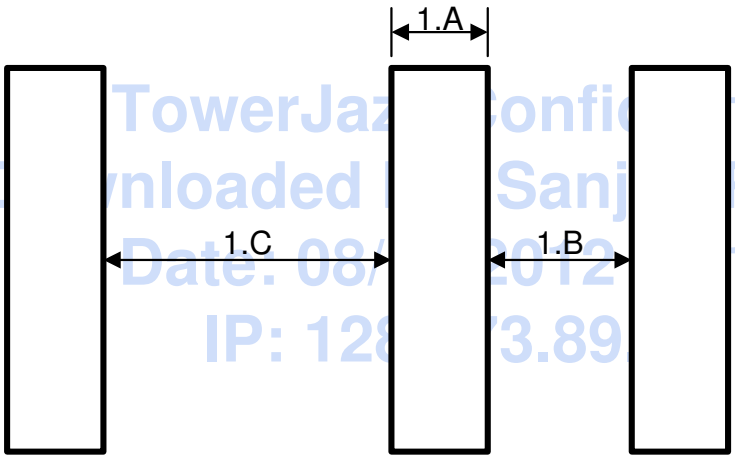


ILLUSTRATION 1

4.4 Field Implant "F" (Layer 3)

Mask 3: The field implant layer is a derived layer (see section 3.5). This mask is a positive mask and is aligned to the zero layer. The field implant edge is defined by the photoresist edge after developing.

Rule No.	Rule Name	
3.A	Minimum Field Implant width	0.60
3.B	Minimum spacing Field Implant to Field	0.60
3.BAD	No drawn data is allowed for layer 3 except within LDFETs	

4.5 DG: Dual Gate Oxide "DG" (Layer 12)

Mask 12: This mask defines the areas that are to have thick gate oxides for dual gate oxide process. This mask is a positive mask and is aligned to the zero layer. See Illustration 12.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA, SBC18PT, SBC18QTD**, SBC18QTR**, SBC18QTL**, SBC18QW**, SBC18MW**, SBC18MWD** SBC18MV**
12.A	Minimum Dual Gate mask overplot of thick oxide active	0.32
12.B	Minimum space Dual Gate mask to Dual Gate mask	0.70
12.C	Minimum space from Dual gate mask to active for thin oxide active	0.32
12.D	Minimum Dual Gate mask width	0.70
12.E	Dual Gate Mask layer must cover all poly on active in SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW, SBC18MW, SBC18MWD processes	

**Note: DG mask is not needed in these processes. However, this layer used in various parameterized cells and fixed cells in Jazz design kit including all 3.3V FETs, MUST be included in the GDS data submitted.

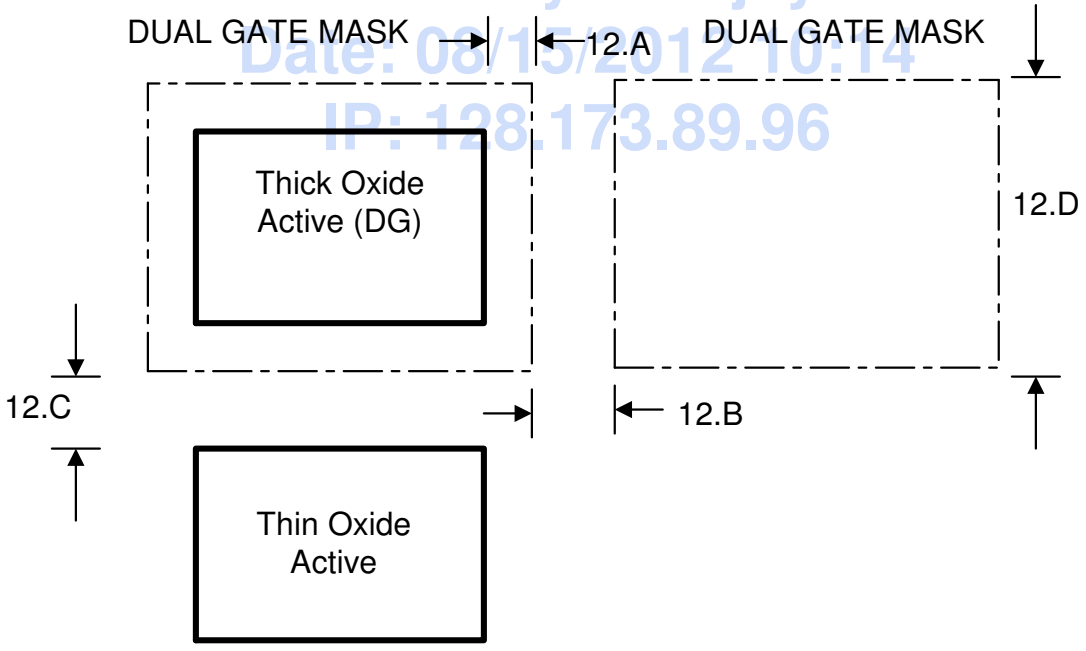


ILLUSTRATION 12

4.6 First Polysilicon Gate "FP" (Layer 5)

Mask 5: This mask defines the areas that are to become gates, MOS capacitors, and poly interconnects. This mask is a positive mask and is aligned to the zero layer. See Illustration 5.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA, SBC18PT	SBC18HX, SBC18HXL, SBC18HA, SBC18PT	SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW, SBC18MW, SBC18MWD, SBC18MV
		Thin gate	Thick gate	
5.A	Minimum gate length for thin gate oxide transistors	0.18	N/a	N/a
5.A.1	Minimum gate length for thin 45 degree bent gate oxide transistors (45 degree bent gate run must be less than 0.6µm)	0.21	N/a	N/a
5.A.a.1	Minimum gate length for thick gate oxide Nfet transistors	n/a	0.36	0.36
5.A.a.2	Minimum gate length for thick gate oxide Pfet transistors	n/a	0.30	0.30
5.B	Minimum width of conductors	0.18	0.18	0.30
5.C	Minimum poly overlap of gate on field for thin gate oxide transistors	0.22	N/a	
5.C.b	Minimum poly overlap of gate on field for thick gate oxide transistors (DG mask) only	n/a	0.30	0.30
5.D	Minimum poly to poly space on field	0.25	0.25	0.36
5.D.b	Minimum poly to poly space on active	0.25	0.25	0.36
5.D.b.1	Minimum poly to poly space on active area with contacts in the spacing	0.37	0.37	0.37
5.E	Minimum spacing of poly on diffusion to field edge	0.32	0.32	
5.E.a	Minimum spacing of poly on diffusion to field edge for run > 5um			0.42

5.E.b	Minimum spacing of poly on diffusion to field edge for run < = 5um			0.36
5.E.1	Maximum allowable gate related active run without contact	20	20	20
5.G	Minimum spacing of poly on field to adjacent diffusion	0.10	0.10	0.10
5.G.b	Minimum spacing of poly on field to adjacent diffusion for areas covered by the DG mask for poly that crosses active	n/a	0.10	0.10
5.G.b.1	Minimum spacing of poly on field to adjacent diffusion for areas covered by the DG mask for poly that does not cross active (poly jumper rule)	n/a	0.30	0.30
5.J	90 degree bent gates are not allowed for thin gate only		n/a	n/a
5.L.a	Minimum poly density (total poly area / chip area) (see Note 3) for die size < 10mm^2 Recommended minimum = 14%	12%	12%	
5.L.b	Minimum poly density (total poly area / chip area) (see Note 3) for die size >= 10mm^2	14%	14%	

Note 1: Rule 5.G: If poly on field to diffusion is less than 0.10um, designers must be aware of increased poly to diffusion capacitance.

Note 2: Active design rules require additional drawn active to be added near large poly areas. See Section 3.5.3 for details.

Note 3: Run density check in Calibre to find out if Jazz default dummy (floating) poly fill algorithm will meet metal density requirements. See section 3.5.4 for dummy poly fill. Customers cannot add dummy poly fill.

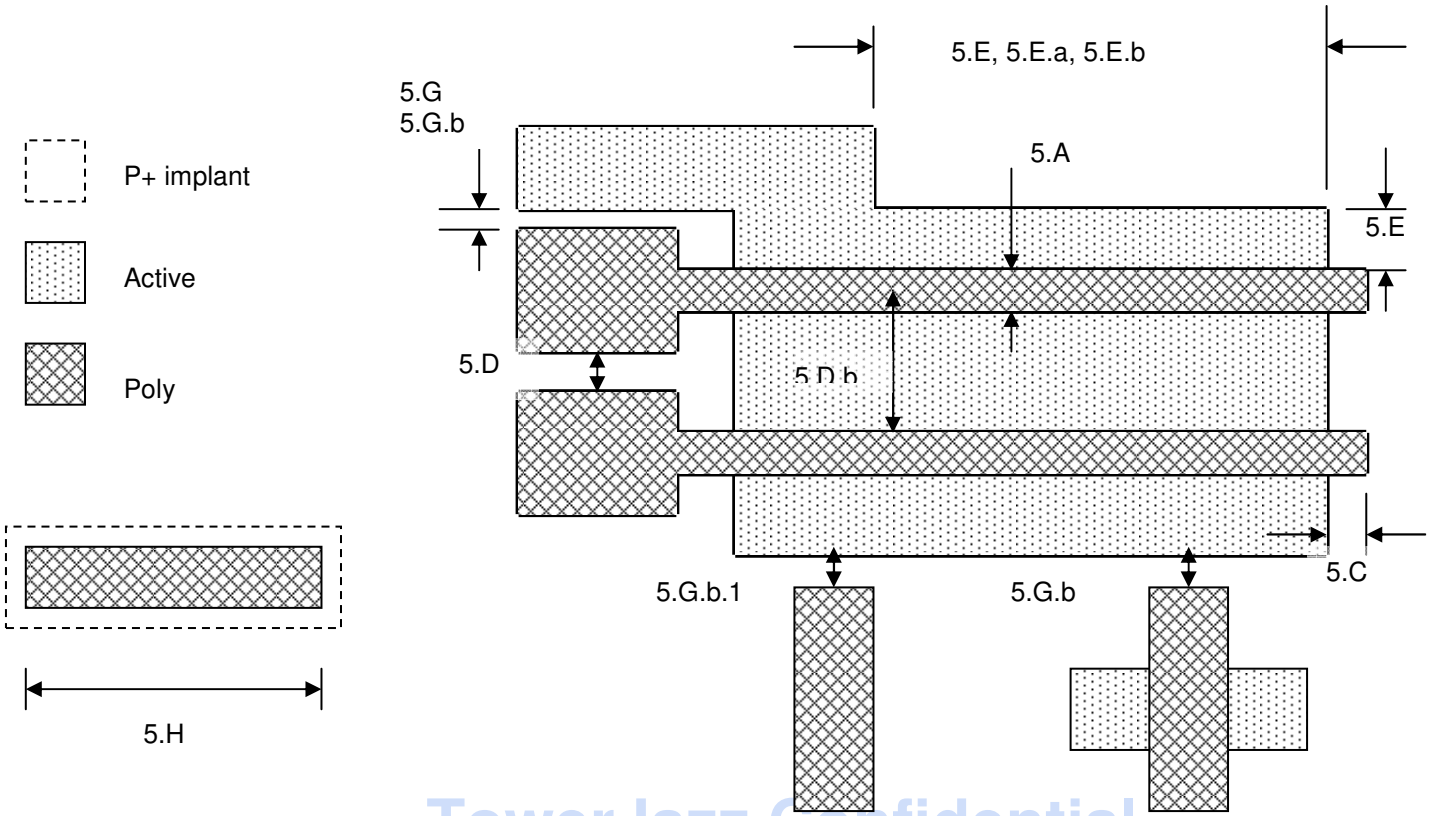
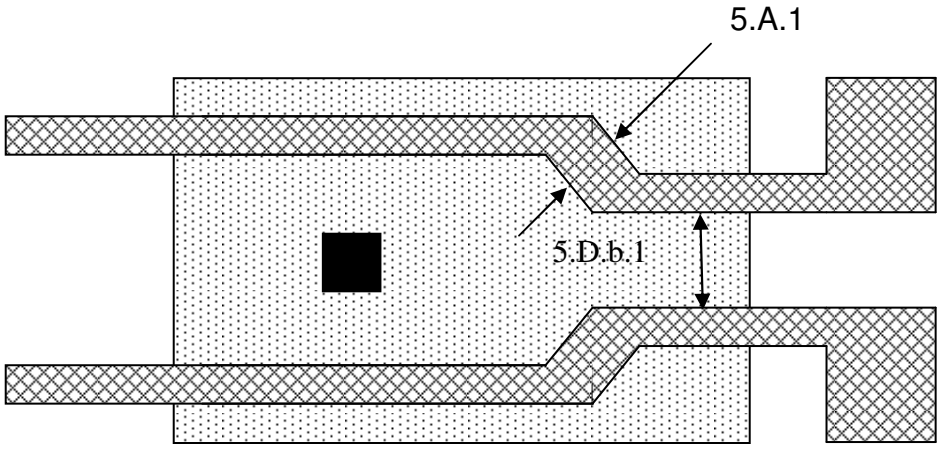


ILLUSTRATION 5



4.7 N+ Implant "NI" (Layer 6)

Mask 6: This mask defines all of the "N+ active" areas and is a negative mask. This mask allows Arsenic to be implanted in all "N+ active" areas (drains, sources, and gates of NFETs, topside N-well ties/guardbars and N+ interconnects). The N+ implant layer is allowed to cross N-well boundaries to meet the following rules. This mask is aligned to the zero layer. See Illustration 6.

Rule No.	Rule Name	
6.A.a	Minimum N+ implant (inside N-well) overplot of N-well tie/guardbar outside 0.43µm of N-well boundary (over field)	0.02
6.A.a.1	Minimum N+ implant (inside N-well or cross N-well boundary) overplot of N-well tie/guardbar (over field) within 0.43µm of N-well boundary (see Illustration 6)	0.18
6.A.b	Minimum N+ implant (outside N-well) overplot of N+ diffusion edge (over field) if the distance to related poly > 0.32µm	0.18
6.A.b.2	Minimum N+ implant (outside N-well) overplot of N+ diffusion edge (over field) if the distance to related poly ≤ 0.32µm (see Illustration 6)	0.35
6.A.c	Minimum N+ implant (outside N-well) overplot of N+ diffusion edge (over field) within "b" (X or Y) of a butted diffusion edge. "b"=0.30µm (see Illustration 6)	0.00
6.B.a	Minimum width of N+ implant	0.44
6.C.a	Minimum N+ implant (outside N-well) space to P-substrate tie/guardbar (over field)	0.10
6.C.a.1	Minimum N+ implant (inside N-well or cross N-well boundary) space to P-substrate tie/guardbar (over field) (see Illustration 6)	0.18
6.C.b	Minimum N+ implant (inside N-well) space to P+ diffusion edge (over field)	0.26
6.C.c	Minimum N+ implant (inside N-well) space to P+ diffusion edge (over field) within "b" (X or Y) of a butted diffusion edge. "b"=0.30µm (see Illustration 6)	0.00
6.D.a	Minimum butting N+ implant (N+ active/ P-substrate edge) overplot of gate (gate shoulder) over thin oxide.	0.32
6.D.b	Minimum butting N+ implant (P+ active/N-well tie edge) space to gate (gate shoulder) over thin oxide.	0.32
6.D.c	Minimum N+ implant overplot of nfet gate over thin oxide for an extension of a butted N+/P+ line closer than 0.35µm (see Illustration 6)	0.32
6.D.d	Minimum N+ implant space to pfet gate over thin oxide for an extension of a butted N+/P+ line closer than 0.35µm (see Illustration 6)	0.32
6.E.a	Minimum spacing of N+ implant to N+ implant	0.44
6.F.a	Minimum spacing of butted active edge in substrate to parallel P-substrate tie field edge	0.23
6.F.b	Minimum spacing of butted active edge in substrate to parallel N+ active field edge	0.23
6.J	Minimum N+ implant area	0.38µm^2

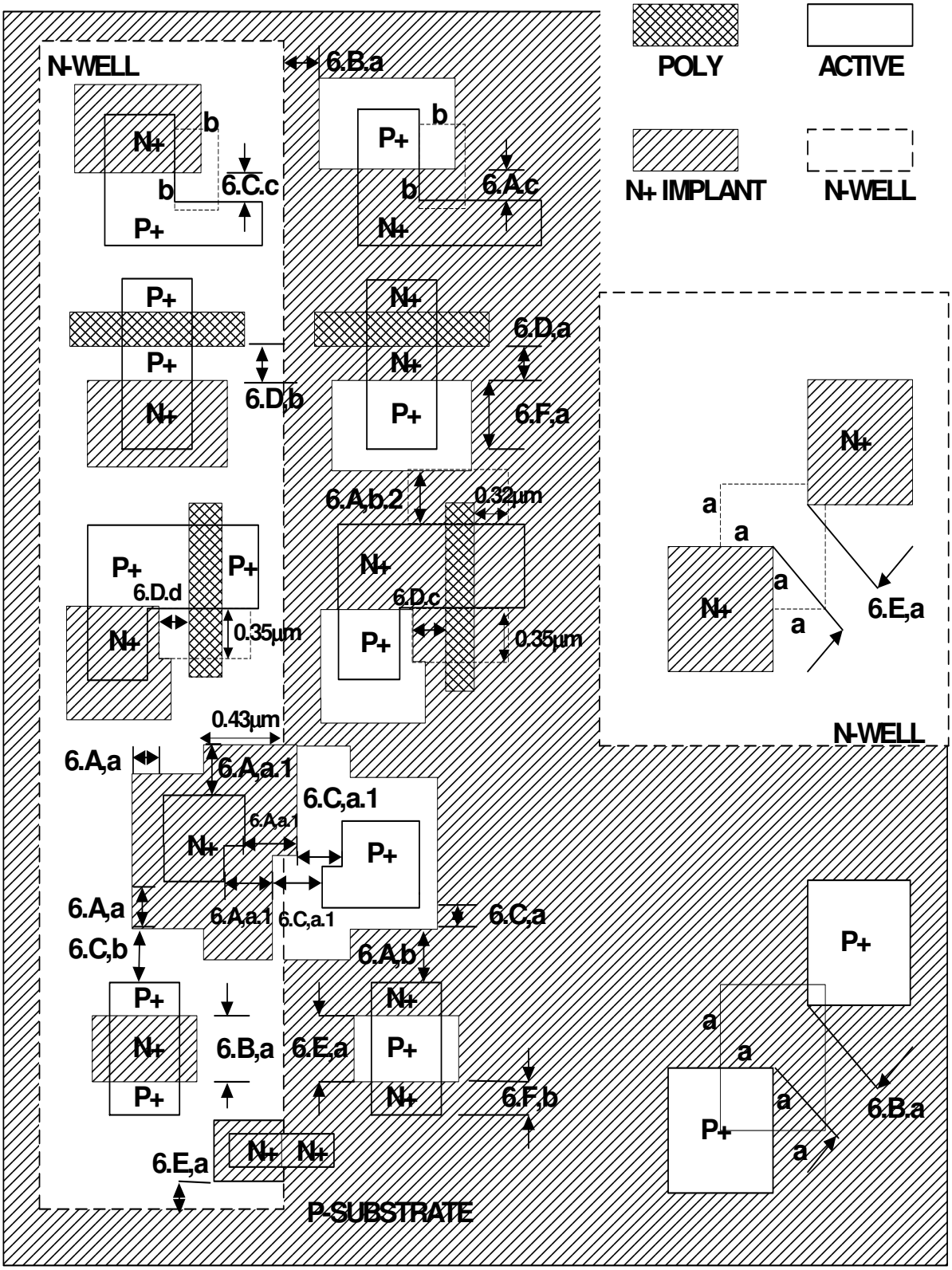


ILLUSTRATION 6

4.8 P+ Implant "PI" (Layer 11)

Mask 11: This mask defines all of the "P+ active" areas and is a negative mask. This mask allows Boron to be implanted in all "P+ active" areas (drains, sources, and gates of PFETs, topside P-substrate ties/guardbars and P+ interconnects). The P+ implant layer is allowed to cross N-well boundaries to meet the following rules. This mask is aligned to the zero layer. See Illustration 11.

Rule No.	Rule Name	
11.A.a	Minimum P+ implant (outside N-well) overplot of P-substrate tie/guardbar outside 0.43µm of N-well boundary (over field)	0.02
11.A.a.1	Minimum P+ implant (outside N-well or cross N-well boundary) overplot of P-substrate tie/guardbar (over field) within 0.43µm of N-well boundary (see Illustration 11)	0.18
11.A.b	Minimum P+ implant (inside N-well) overplot of P+ diffusion edge (over field) if the distance to related poly > 0.32µm	0.18
11.A.b.2	Minimum P+ implant (inside N-well) overplot of P+ diffusion edge (over field) if the distance to related poly ≤ 0.32µm	0.35
11.A.c	Minimum P+ implant (inside N-well) overplot of P+ diffusion edge (over field) within "b" (X or Y) of a butted diffusion edge. "b"=0.30µm (see Illustration 11)	0.00
11.B.a	Minimum width of P+ implant	0.44
11.C.a	Minimum P+ implant (inside N-well) spacing to N-well tie/guardbar (over field)	0.10
11.C.a.1	Minimum P+ implant (outside N-well or cross N-well boundary) spacing to N-well tie/guardbar (over field) (see Illustration 11)	0.18
11.C.b	Minimum P+ implant (outside N-well) spacing to N+ diffusion edge (over field)	0.26
11.C.c	Minimum P+ implant (outside N-well) spacing to N+ diffusion edge (over field) within "b" (X or Y) of a butted diffusion edge. "b"=0.30µm (see Illustration 11).	0.00
11.D.a	Minimum butting P+ implant (P+ active/N-well tie edge) overplot of gate (gate shoulder) over thin oxide.	0.32
11.D.b	Minimum butting P+ implant (N+ active/P-substrate edge) space to gate (gate shoulder) over thin oxide.	0.32
11.D.c	Minimum P+ implant overplot of pfet gate over thin oxide for an extension of a butted N+/P+ line closer than 0.35µm (see Illustration 11)	0.32
11.D.d	Minimum P+ implant space to nfet gate over thin oxide for an extension of a butted N+/P+ line closer than 0.35µm (see Illustration 11)	0.32
11.E.a	Minimum spacing of P+ implant to P+ implant (merge rule)	0.44
11.F.a	Minimum spacing of butted active edge in N-well to parallel N-well tie field edge	0.23
11.F.b	Minimum spacing of butted active edge in N-well to parallel P+ active field edge	0.23
11.J	Minimum P+ implant area	0.38µm^2
6_11.X	Active must be covered with N+ or P+ implant	

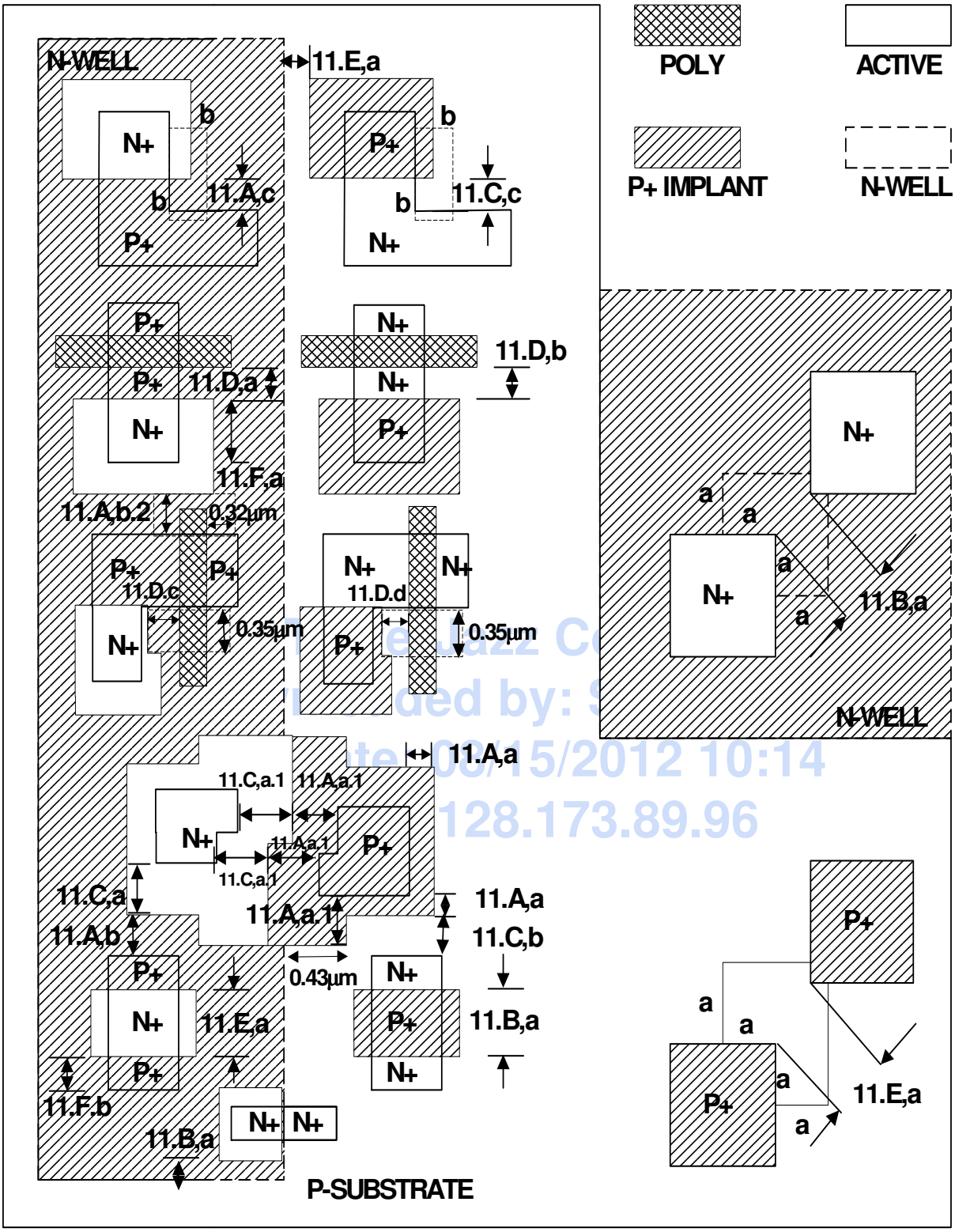


ILLUSTRATION 11

4.9 NK Implant "NK" (Layer 61)

Mask 61: This mask defines LDD (N-type) and pocket (P-type) implants into the thin gate oxide NFETs. This mask is aligned to the zero layer. See Illustration 61. This layer is a derived layer (See section 3.5) and is a negative mask.

This layer is applicable to SBC18HX, SBC18HXL, SBC18HA, SBC18PT processes only.

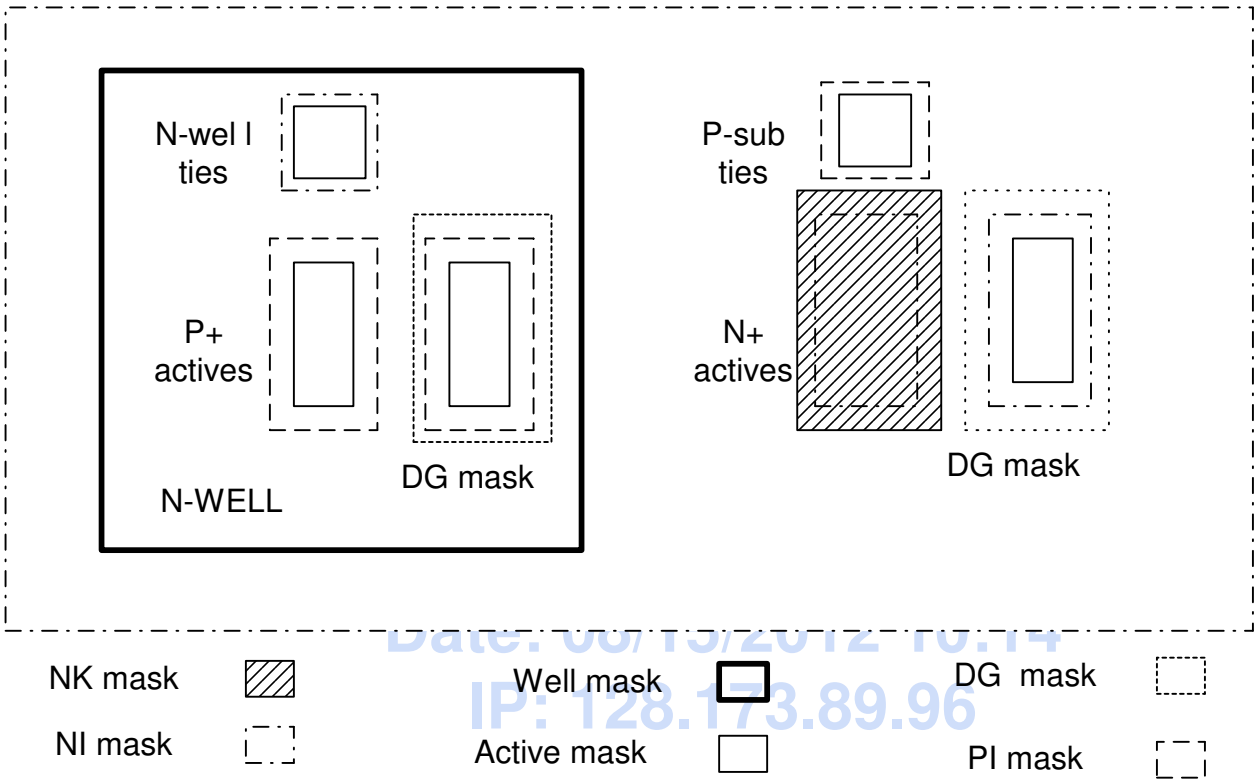


ILLUSTRATION 61

Rule No.	Rule Name	
61.A	Minimum width of NK implant	0.44
61.B	Minimum spacing of NK implant to NK implant	0.44
61.BAD	No drawn data is allowed for layer 61 outside artifact region	

4.10 PK Implant "PK" (Layer 59)

Mask 59: This mask defines LDD (P-type) implants in PFETs. This mask is aligned to the zero layer. See Illustration 59. This layer is a derived layer (see Section 3.5) and is a negative mask.

This layer is applicable to all SBC18 processes.

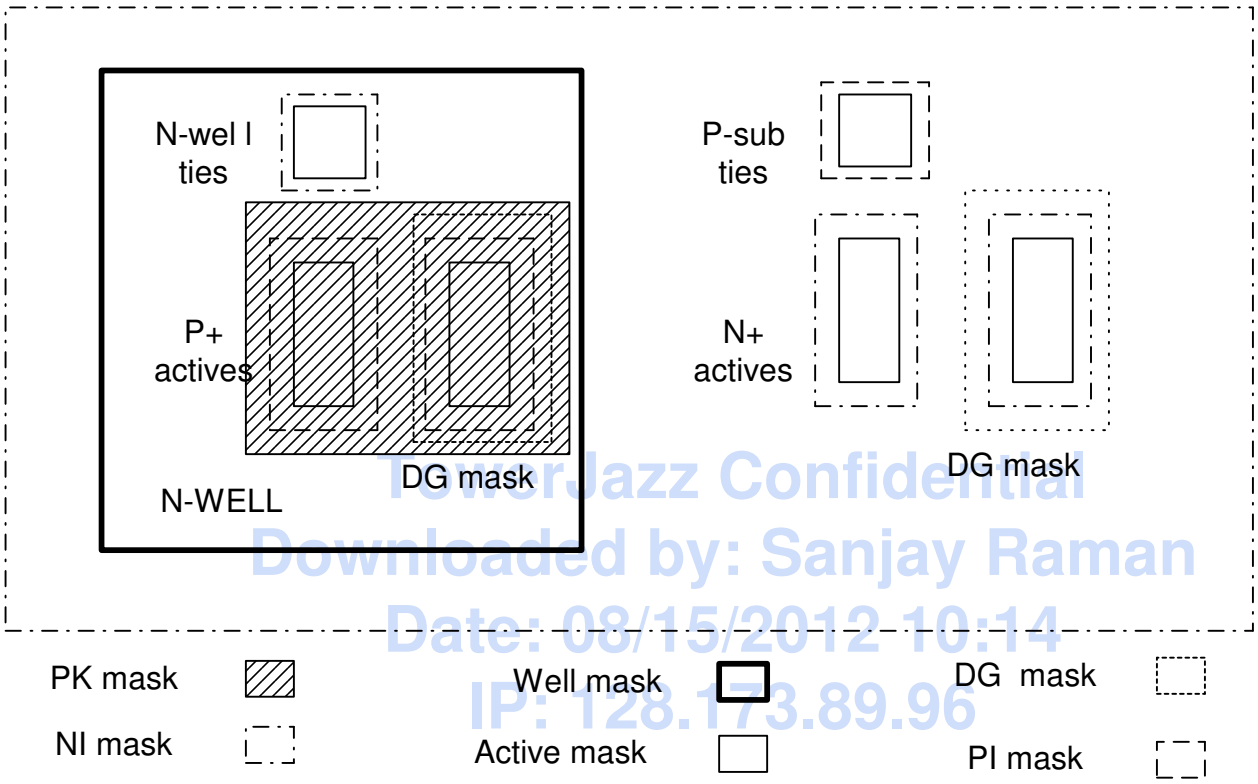


ILLUSTRATION 59

Rule No.	Rule Name	
59.A	Minimum width of PK implant	0.44
59.B	Minimum spacing of PK implant to PK implant	0.44
59.BAD	No drawn data is allowed for layer 59 outside artifact region	

4.11 DN Implant "DN" (Layer 14)

Mask 14: This mask defines LDD implant into the thick gate oxide NFETs only that are defined by the DG (Dual gate mask, layer 61). This mask is aligned to the zero layer. See Illustration 14. This layer is a derived layer (see Section 3.5) and is a negative mask.

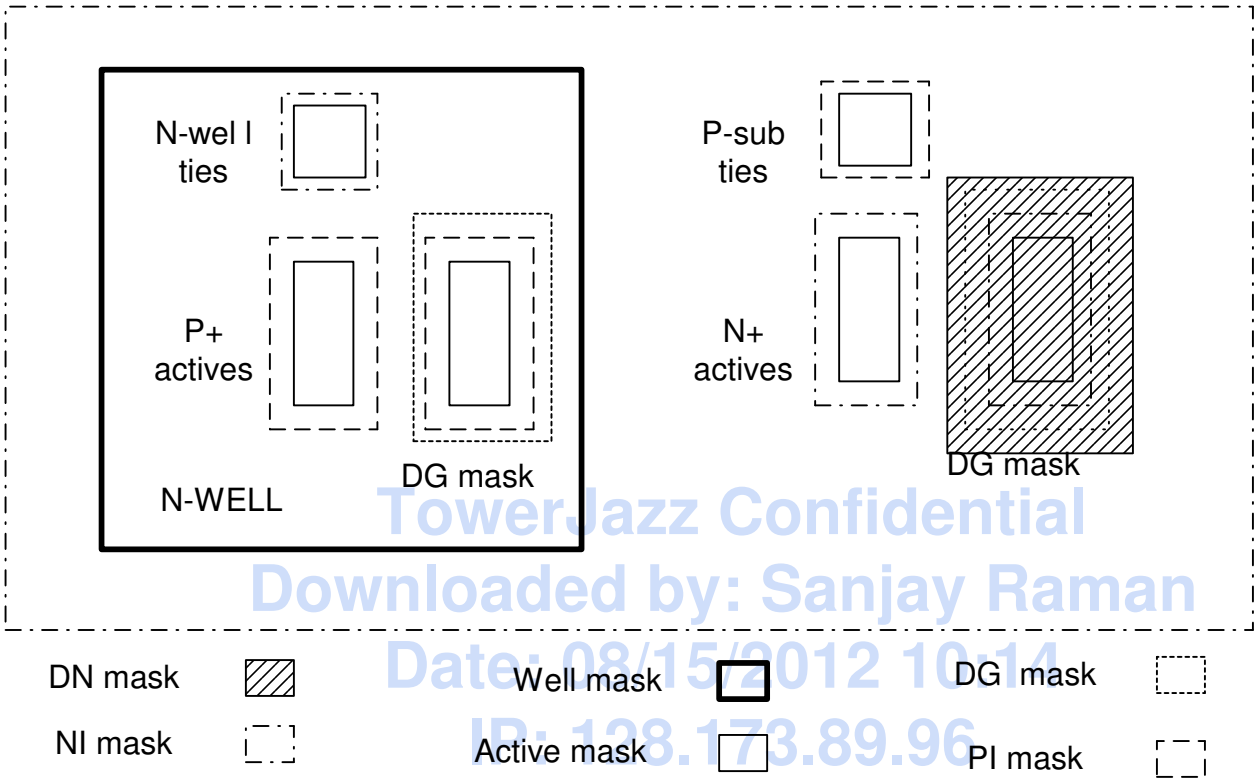


ILLUSTRATION 14

Rule No.	Rule Name	
14.A	Minimum width of DN implant	0.44
14.B	Minimum spacing of DN implant to DN implant	0.44
14.BAD	No drawn data is allowed for layer 14 outside artifact region, except in LDFETs	

4.12 DP Implant "DP" (Layer 16)

Mask 16: This mask defines the P-pocket implant for the thin gate oxide PFETs. This mask is aligned to the zero layer. See Illustration 16. This layer is a derived layer (see Section 3.5) and is a negative mask.

This layer is applicable to SBC18HX, SBC18HXL, SBC18HA, SBC18PT processes only.

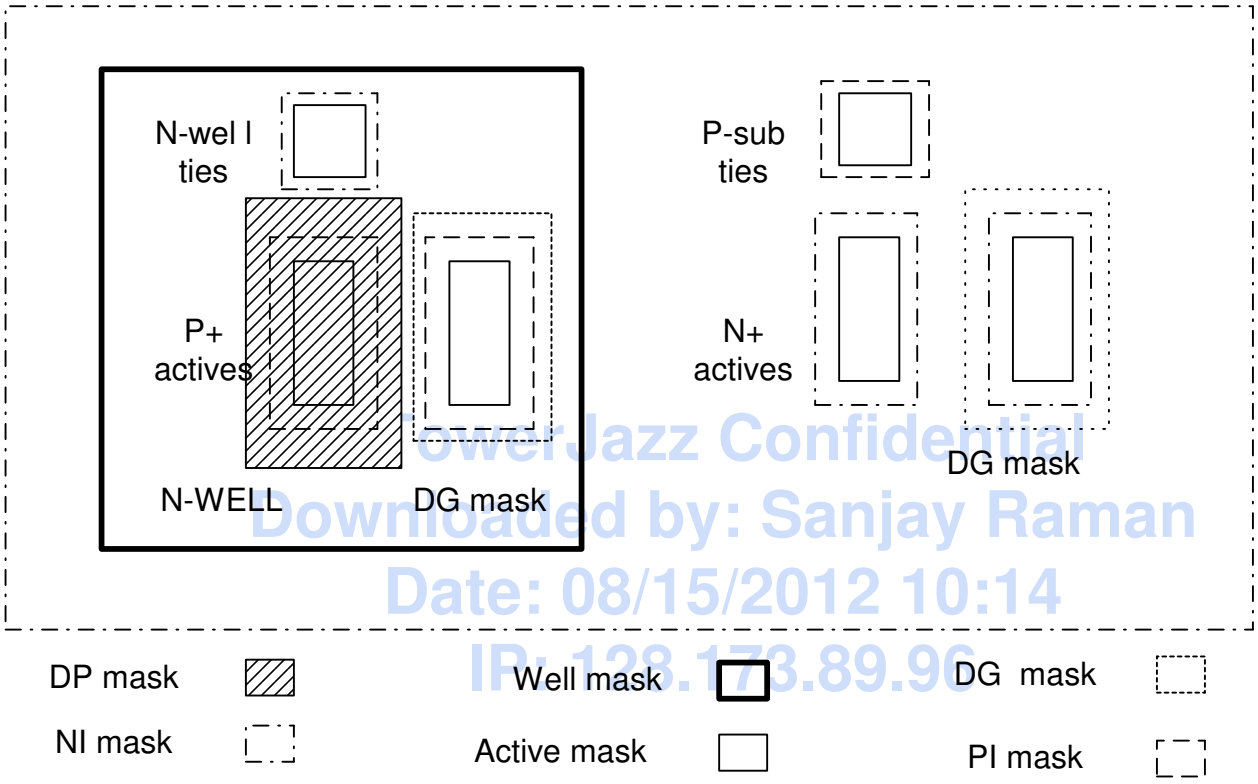


ILLUSTRATION 16

Rule No.	Rule Name	
16.A	Minimum width of DP implant	0.44
16.B	Minimum spacing of DP implant to DP implant	0.44
16.BAD	No drawn data is allowed for layer 16 outside artifact region	

4.13 Contact "C" (Layer 7)

Mask 7: This mask defines metal 1 to P+ diffusions, metal 1 to N+ diffusions, and metal 1 to poly contact areas. Poly contacts are not allowed over active areas. This mask is a negative mask and is aligned to the zero layer. See Illustration 7.
This layer is a generated layer. It is defined as the logical operation of the CONTACT layer (layer 7) OR the Slotted Contact layer (layer 55). The Slotted Contact layer rules are provided in SiGe NPN rules in Section 5.1.

Rule No.	Rule Name	
7.A	Minimum/maximum contact size	0.22X0.22
7.B	Minimum contact to contact space	0.25
7.B.a	Minimum contact to contact space in a contact array with both row and column number of contacts greater than 3. The maximum space between contacts to be considered part of an array is 0.3um.	0.28
7.C	Minimum spacing diffusion contact to unrelated poly	0.16
7.D	Minimum spacing poly contact on field to gate (channel region)	0.20
7.D.x	Poly contacts are not allowed over active	
7.E	Minimum poly extension beyond contact	0.10
7.F	Minimum active extension beyond contact	0.10
7.G	Minimum butting implant (N+ or P+) overplot of contact	0.13

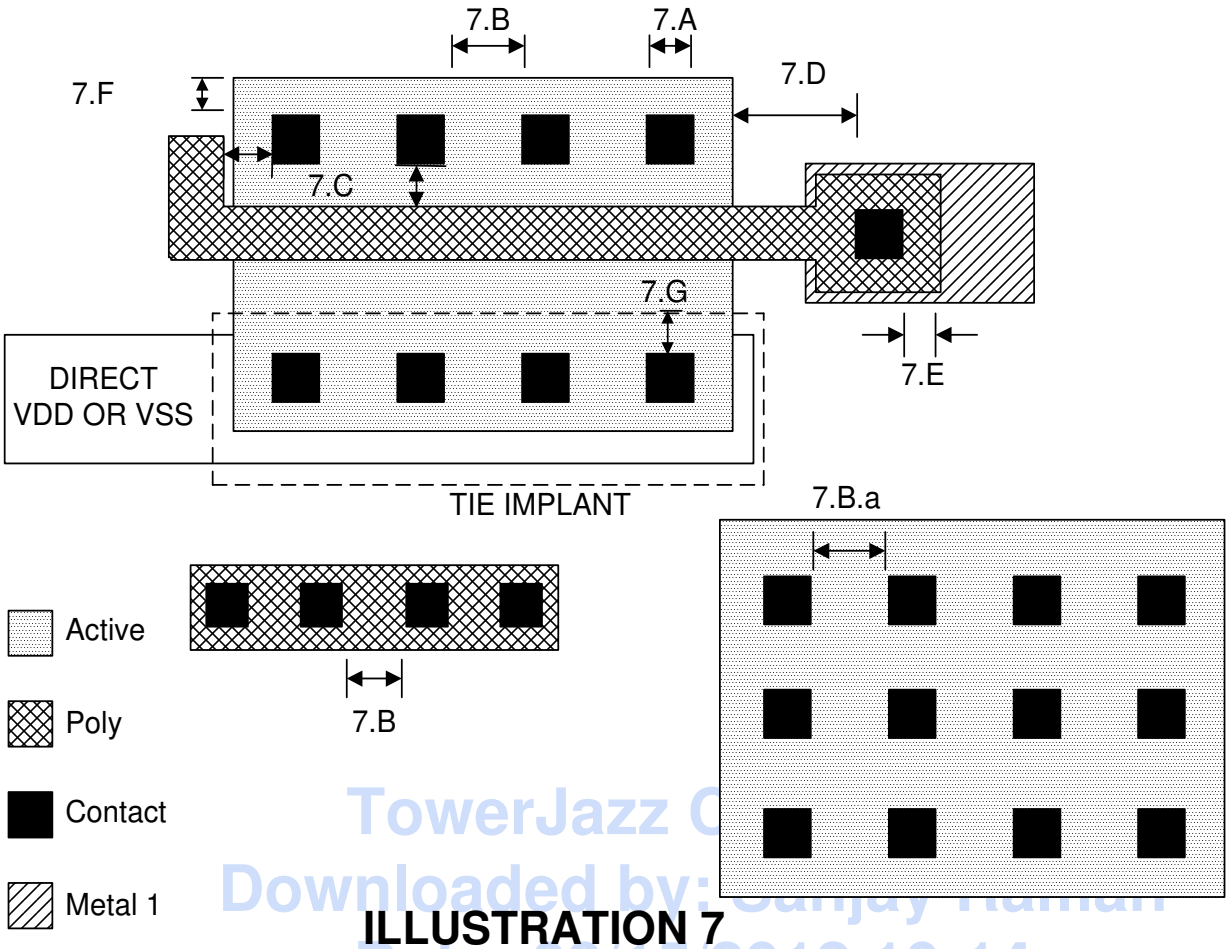


ILLUSTRATION 7

4.14 Metal 1 "M1" (Layer 8)

Mask 8: This mask defines the first layer metal interconnection for a circuit. The mask is a positive mask and is aligned to the zero layer. See Illustration 8.

Rule No.	Rule Name	
8.A	Minimum metal 1 line width	0.23
8.B	Minimum metal 1 to metal 1 space	0.23
8.B.b	Minimum metal 1 to metal 1 space when at least one metal 1 shape has width and length greater than 10µm (metal 1 polygon larger than 10µm x 10µm). This includes all attachments to a large metal 1 polygon and extending out with a run of 1.0µm or less.	0.60
8.C	Minimum metal 1 overplot of contacts	0.005
8.C.a	Minimum metal 1 overplot of contact at two opposite sides of contact (see Illustration 8). For contact located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and the other side can follow rule 8.c.	0.06
8.D	Minimum metal 1 density (total metal 1 area / chip area) (see Note 1)	30%
8.E	Minimum metal 1 area	0.20 (μm^2)
8.F	Maximum metal 1 density (total metal 1 area / chip area) (see Note 1)	60%

Note 1: **Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements.** See Section 3.5.1 and 3.5.2 for dummy metal fill generation.

Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 95). See section 5.11.

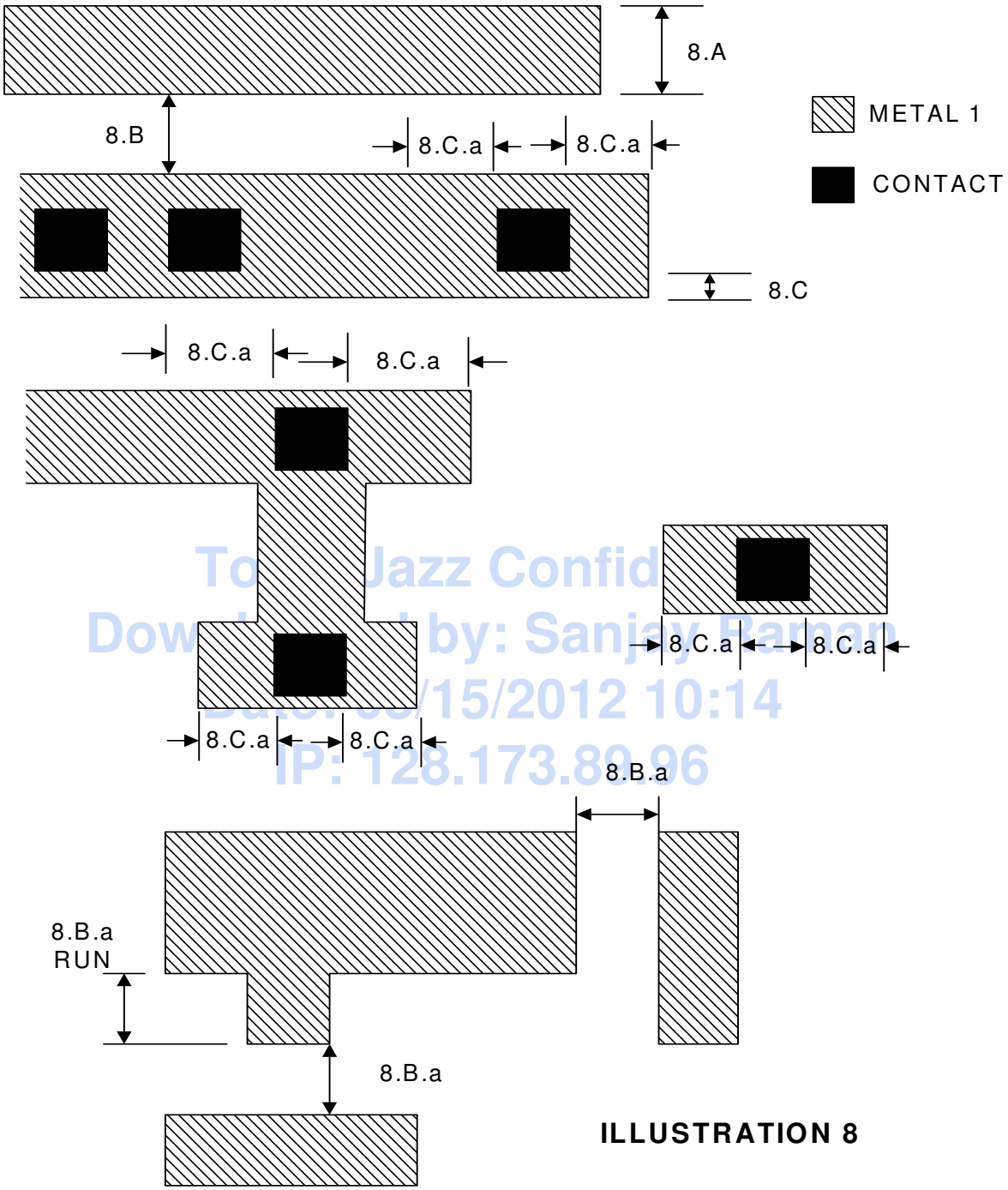


ILLUSTRATION 8

4.15 Via "V" (Layer 17)

Mask 17: This mask defines metal 1 to metal 2 contact areas. This mask is a negative mask and is aligned to the zero layer. Note: Vias may be placed over poly or diffusion contacts in the SBC18 process. See Illustration 17.
This layer is a generated layer. It is defined as the logical operation of the Via 1 layer (layer 17) OR the Slotted Via 1 layer (layer 32). The Slotted Via 1 layer rules are provided in SiGe NPN rules in section 5.1.

Rule No.	Rule Name	
17.A	Minimum/maximum via size	0.26X0.26
17.B	Minimum metal 1 overplot of via	0.01
17.B.a	Minimum metal 1 overplot of via at two opposite sides of via (see Illustration 17). For via located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and the other side can follow rule 17.B.	0.06
17.C	Minimum via to via space	0.26

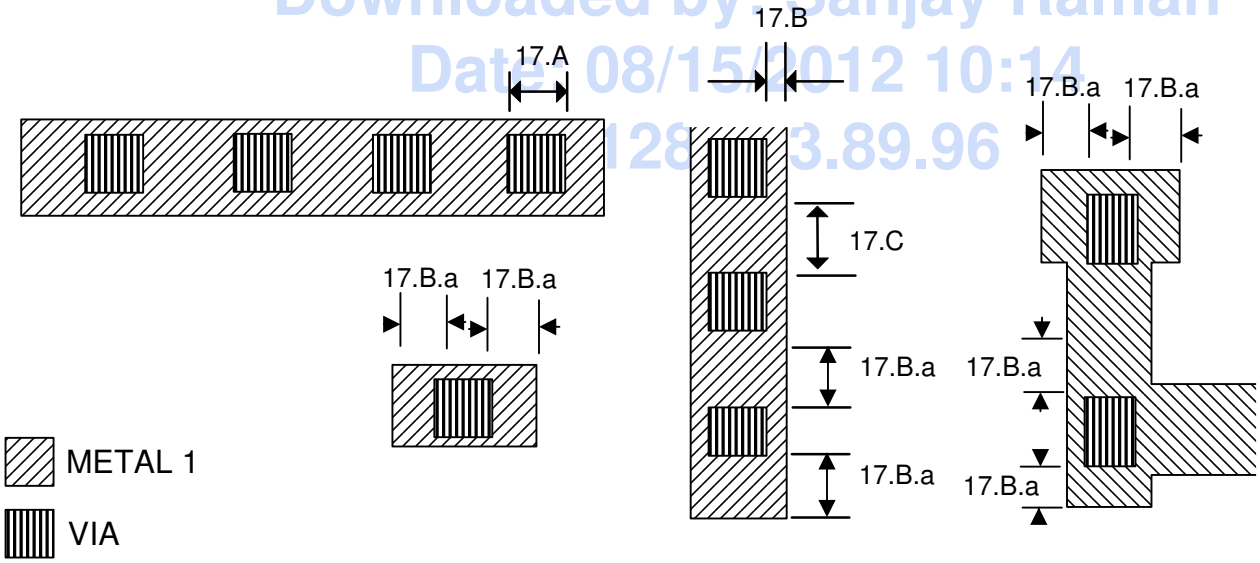


ILLUSTRATION 17

4.16 Metal 2 "M2" (Layer 18)

Mask 18: This mask defines the second metal interconnections. The mask is a positive mask and is aligned to the zero layer. See Illustration 18.

Rule No.	Rule Name	SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW, SBC18MW, SBC18MWD, SBC18MV	SBC18HX, SBC18HXL, SBC18HA, SBC18PT
18.A	Minimum metal 2 width	0.40	0.28
18.B	Minimum metal 2 to metal 2 space	0.40	0.28
18.B.a	Minimum metal 2 to metal 2 space when at least one metal 2 shape has width and length greater than 10µm (metal 2 polygon larger than 10µm x 10µm). This includes all attachments to a large metal 2 polygon and extending out with a run of 1.0µm or less.	0.60	0.60
18.C	Minimum metal 2 overplot of via	0.01	0.01
18.C.a	Minimum metal 2 overplot of via at two opposite sides of via (see Illustration 18). For via located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and the other side can follow rule 18.C.	0.06	0.06
18.D	Minimum metal 2 density (total metal 2 area / chip area) (see Note 1)	30%	30%
18.E	Minimum metal 2 area	0.32 (μm^2)	0.20 (μm^2)
18.F	Maximum metal 2 density (total metal 2 area / chip area) (see Note 1)	60%	60%

Note 1: **Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements.** See Section 3.5.1 and 3.5.2 for dummy metal fill generation.

Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 95). See section 5.11.

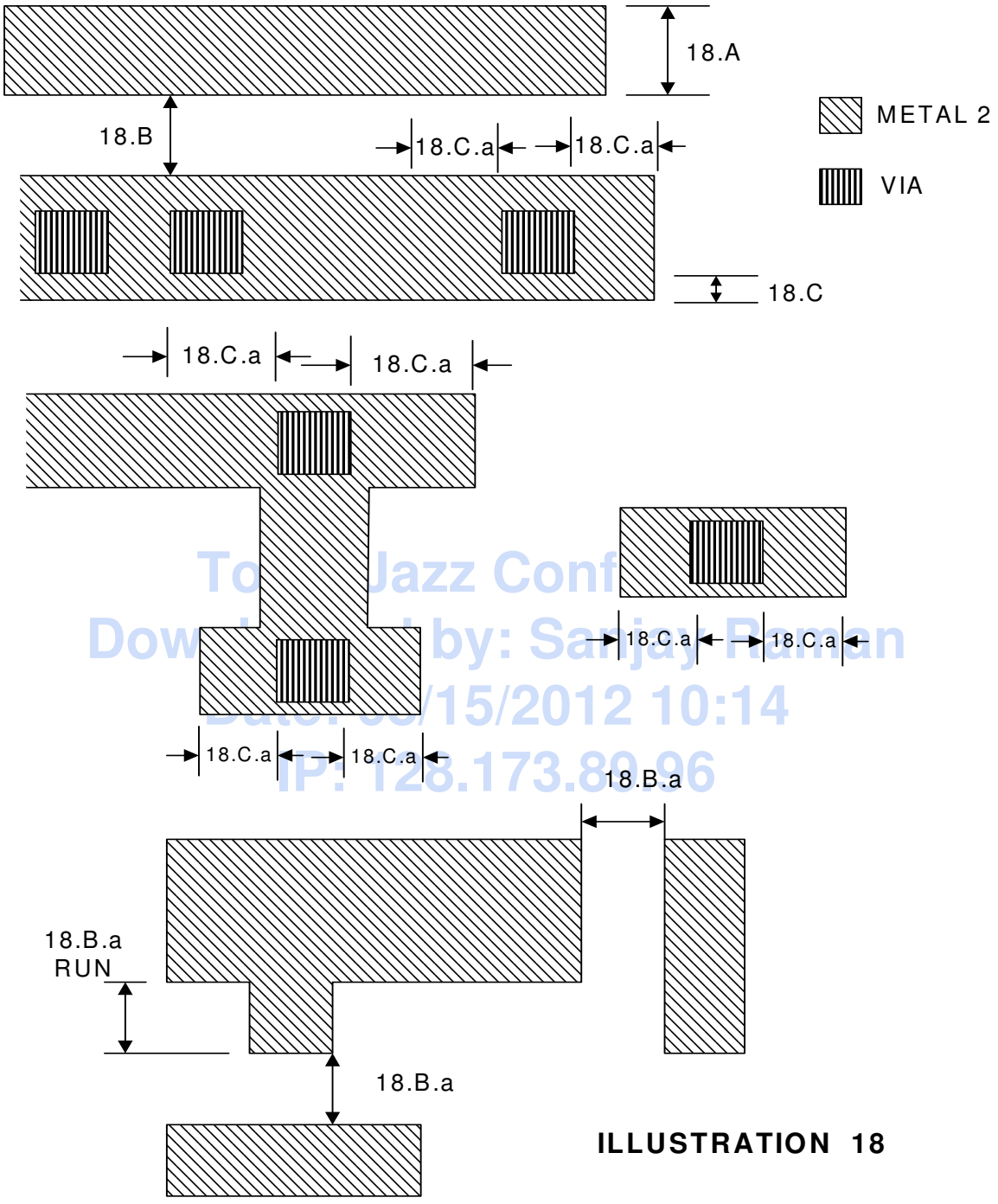


ILLUSTRATION 18

4.17 Via2 "V2" (Layer 27)

Mask 17: This mask defines metal 2 to metal 3 contact areas. This mask is a negative mask and is aligned to the zero layer. Note: Via2s may be placed over poly, diffusion contacts or vias in the SBC18 processes. See Illustration 27.

Rule No.	Rule Name	SBC18MW, SBC18MWD, SBC18MV	SBC18QW, SBC18QTD, SBC18QTR, SBC18QTL	SBC18HX, SBC18HXL, SBC18HA, SBC18PT
27.A	Minimum/maximum via2 size	0.50X0.50	0.38x0.38	0.26X0.26
27.B	Minimum metal 2 overplot of via2	0.35	0.01	0.01
27.B.a	Minimum metal 2 overplot of via2 at two opposite sides of via2 (see Illustration 27). **	0.35	0.06	0.06
27.C	Minimum via2 to via2 space	0.50	0.36	0.26

** For via2 located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and the other side can follow rule 27.B.

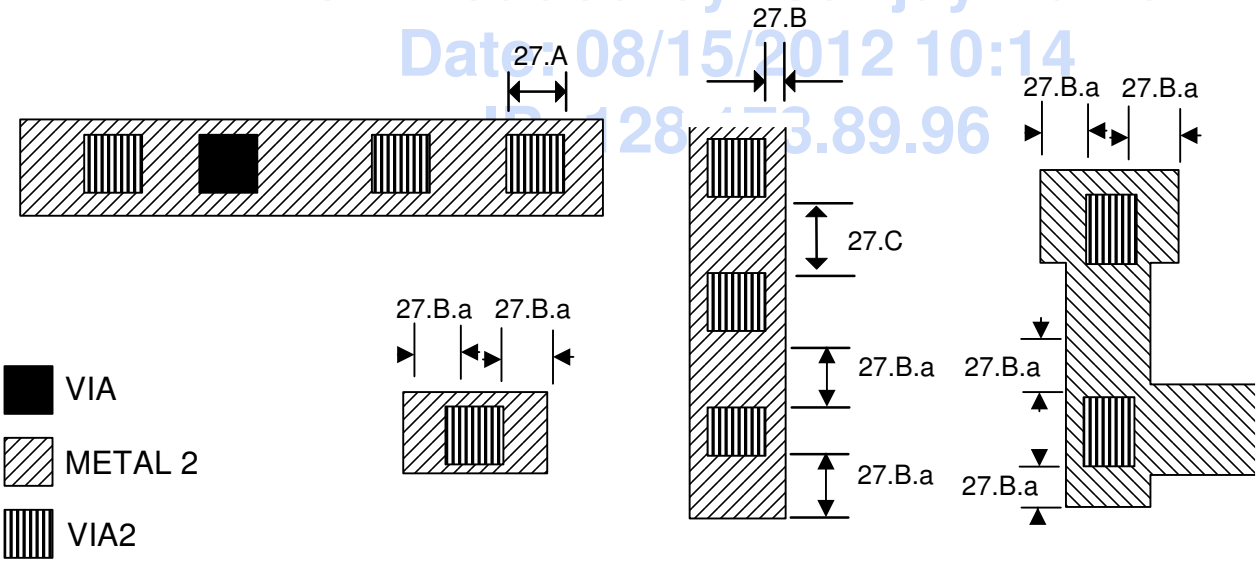


ILLUSTRATION 27

4.18 Metal 3 "M3" (Layer 28)

Mask 28: This mask defines the third metal interconnects. The mask is a positive mask and is aligned to the zero layer. See Illustration 28.

Rule No.	Rule Name	SBC18MW, SBC18MWD, SBC18MV	SBC18QW, SBC18QTD, SBC18QTR, SBC18QTL	SBC18HX, SBC18HXL, SBC18HA, SBC18PT
28.A	Minimum metal 3 width	2.5	0.40	0.28
28.B	Minimum spacing metal 3 to metal 3 space	2.0	0.40	0.28
28.B.a	Minimum metal 3 to metal 3 space when at least one metal 3 shape has width and length greater than 10µm (metal 3 polygon larger than 10µm x 10µm). This includes all attachments to a large metal 3 polygon and extending out with a run of 1.0µm or less.	NA	0.60	0.60
28.C	Minimum metal 3 overplot of via2	0.35	0.01	0.01
28.C.a	Minimum metal 3 overplot of via2 at two opposite sides of via2 (see Illustration 28). For via2 located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and the other side can follow rule 28.C.	NA	0.06	0.06
28.D	Minimum metal 3 density (total metal 3 area / chip area) (see Note 1)	25%	30%	30%
28.E	Minimum metal 3 area	6.25 (μm^2)	0.32 (μm^2)	0.20 (μm^2)
28.F	Maximum metal 3 density (total metal 3 area / chip area) (see Note 1)	60%	60%	60%

Note 1: **Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements.** See Section 3.5.1 and 3.5.2 for dummy metal fill generation.

Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 95). See section 5.11.

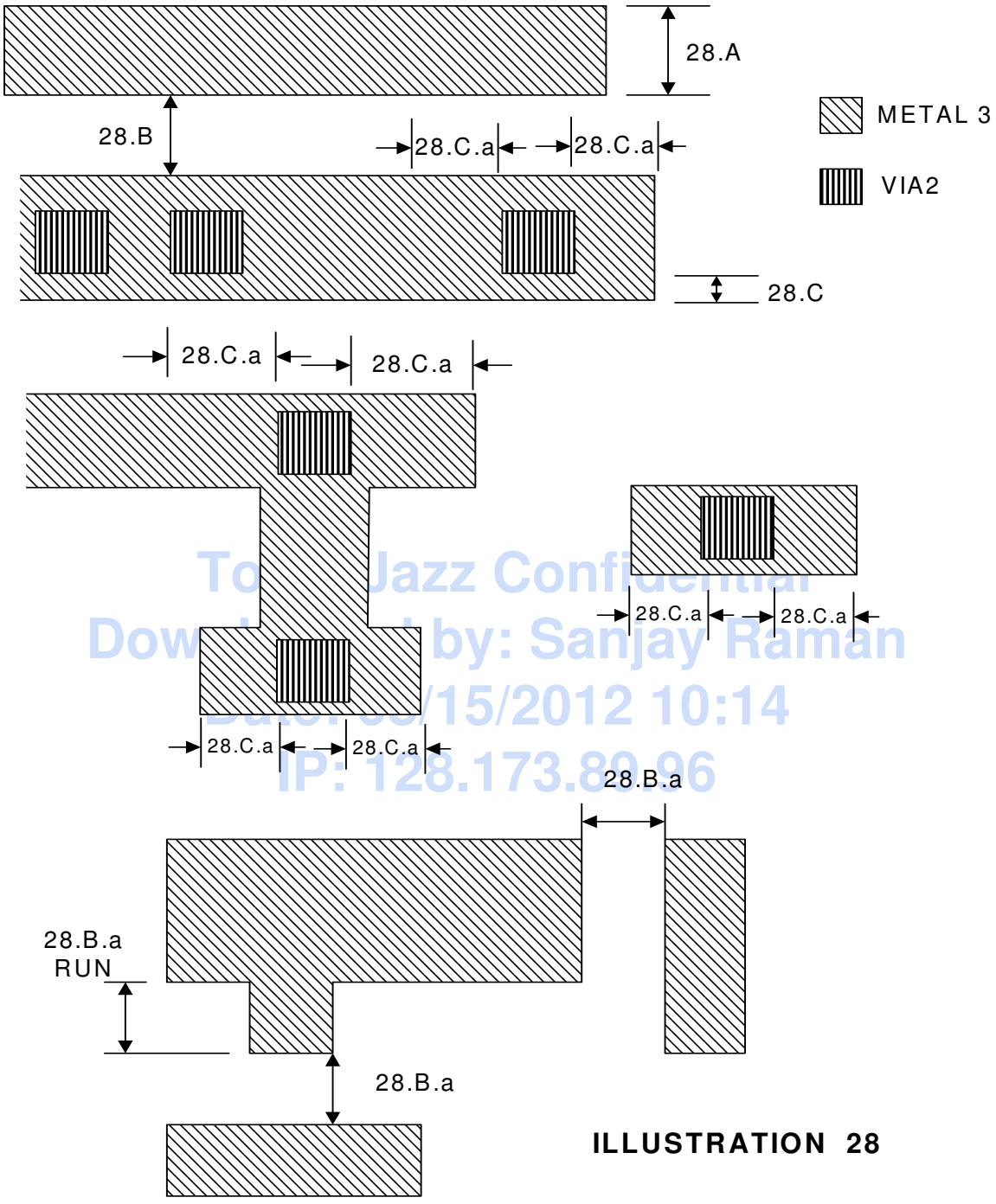


ILLUSTRATION 28

4.19 Via3 "V3" (Layer 37)

Mask 37: This mask defines metal 3 to metal 4 contact areas. This mask is a negative mask and is aligned to the zero layer. Note: Via3s may be placed over contacts, vias or via2s in this process. See Illustration 37.

Rule No.	Rule Name	SBC18PT, SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW	SBC18HX, SBC18HXL, SBC18HA
37.A	Minimum/maximum via3 size	0.50X0.50	0.26X0.26
37.B	Minimum metal 3 overplot of via3	0.35	0.01
37.B.a	Minimum metal 3 overplot of via3 at two opposite sides of via3 (see Illustration 37). **	N/A	0.06
37.C	Minimum via3 to via3 space	0.50	0.26

** For Via3 located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and the other side can follow rule 37.B.

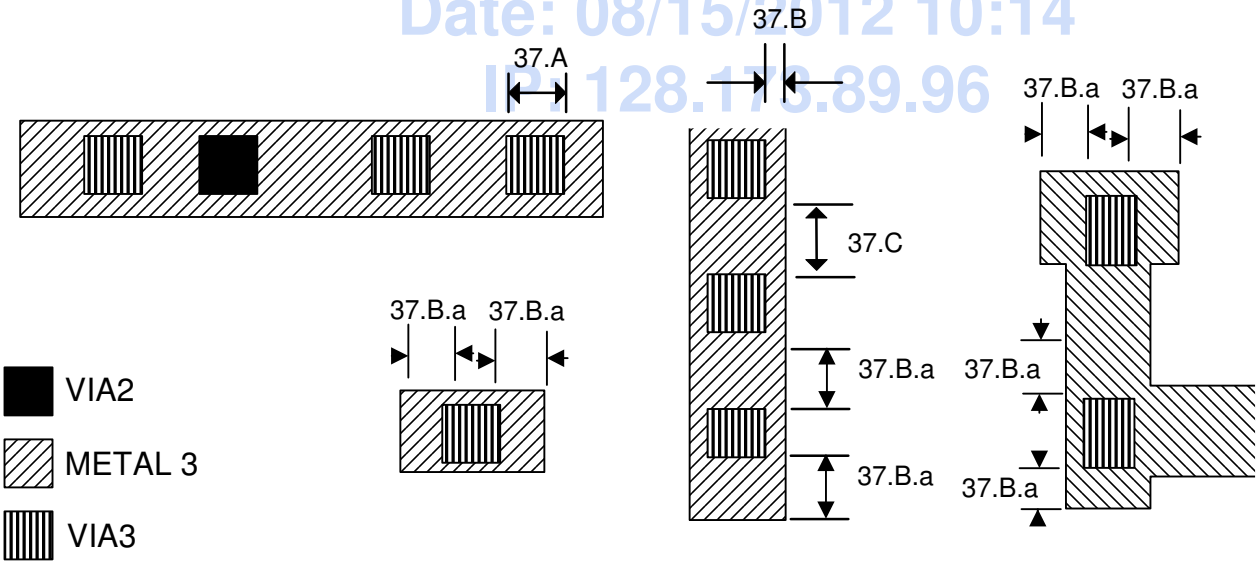


ILLUSTRATION 37

4.20 Metal 4 "M4"(Layer 38)

Mask 38: This mask defines the fourth metal interconnects. The mask is a positive mask and is aligned to the zero layer. See Illustration 38.

Rule No.	Rule Name	SBC18QW, SBC18QTD, SBC18QTR, SBC18QTL	SBC18PT	SBC18HX, SBC18HA, SBC18HXL
38.A	Minimum metal 4 width	2.5	1.0	0.44
38.B	Minimum metal 4 to metal 4 space	2.0	1.25	0.46
38.B.a	Minimum metal 4 to metal 4 space when at least one metal 4 shape has width and length greater than 10µm (metal 4 polygon larger than 10µm x 10µm). This includes all attachments to a large metal 4 polygon and extending out with a run of 1.0µm or less.	N/A	N/A	0.60
38.C	Minimum metal 4 overplot of via3	0.35	0.35	0.09
38.D	Minimum metal 4 density (total metal 4 area / chip area). See Note 1	25%	25%	30%
38.E	Minimum metal 4 area	6.25 (μm^2)	1.44 (μm^2)	0.56 (μm^2)
38.F	Maximum metal 4 density (total metal 4 area / chip area). See Note 1	60%	60%	60%

Note 1: **Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements.** See Section 3.5.1 and 3.5.2 for dummy metal fill generation.

Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 95). See section 5.12.

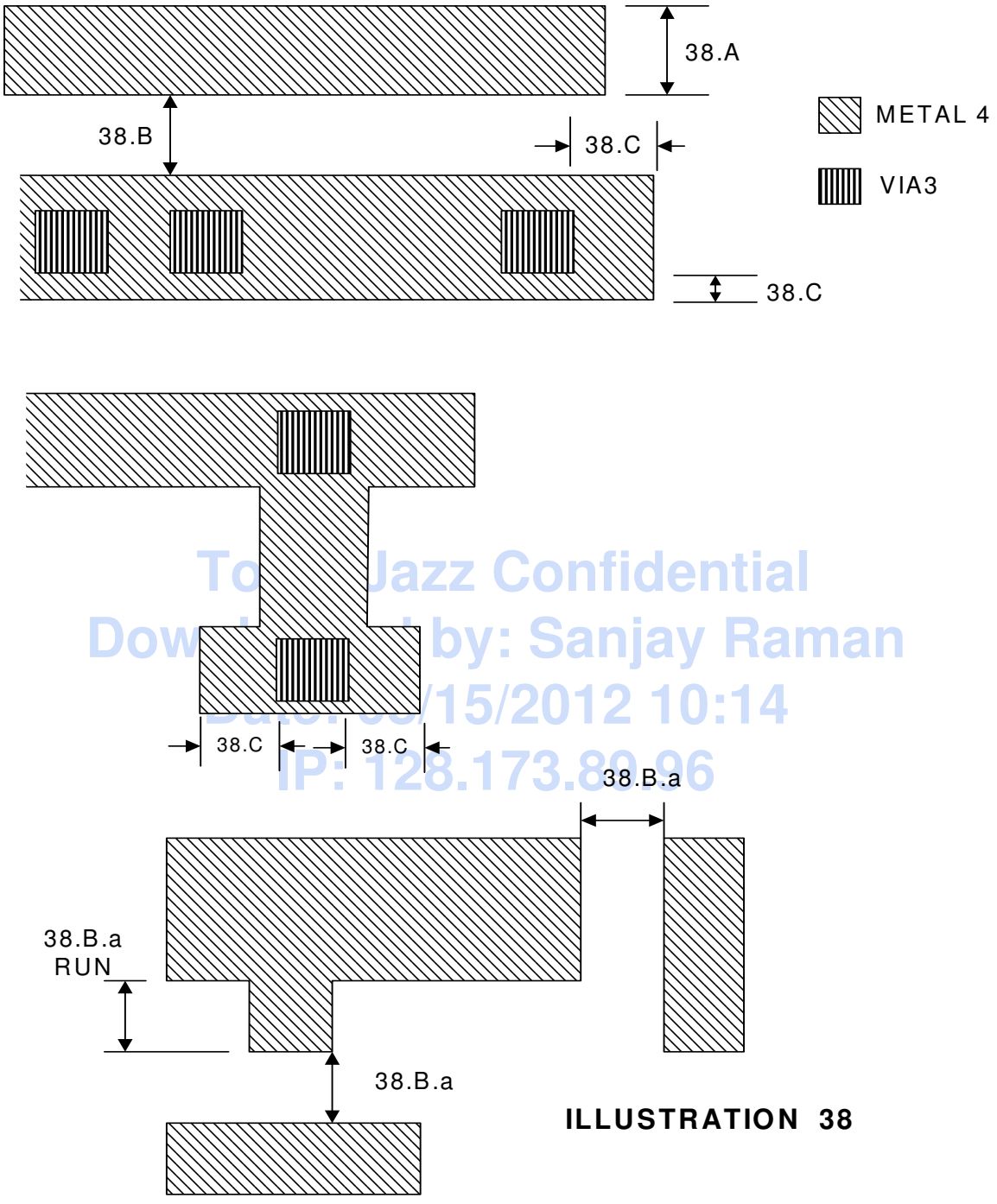


ILLUSTRATION 38

4.21 Via4 "V4" (Layer 47)

Mask 47: This mask defines metal 4 to metal 5 contact areas. This mask is a negative mask and is aligned to the zero layer. Note: Via4s may be placed over contacts, vias.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA, SBC18PT
47.A	Minimum/maximum via4 size	0.5 x 0.5
47.B	Minimum metal 4 overplot of via4	0.35
47.C	Minimum via4 to via4 space	0.50

4.22 Metal 5 (layer 48)

Mask 48: This mask defines the fifth metal interconnect. This mask also defines the bonding pads for SBC18PT process. The mask is a positive tone mask and is aligned to ZL. See Illustration 48.

Rule No.	Rule Name	SBC18HX , SBC18HXL, SBC18HA	SBC18PT,
48.A	Minimum metal 5 width	1.00	2.5
48.B	Minimum metal 5 to metal 5 space	1.25	2.0
48.C	Metal 5 overplot of via 4	0.35	0.35
48.D	Minimum metal 5 density (total metal 5 area / chip area) (see Note 1)	25%	25%
48.E	Minimum metal 5 area	1.44 (μm^2)	6.25 (μm^2)
48.F	Maximum metal 5 density (total metal 5 area / chip area) (see Note 1)	60%	60%

Note 1: **Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements.** See Section 3.5.1 and 3.5.2 for dummy metal fill generation.

Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 95). See section 5.12.

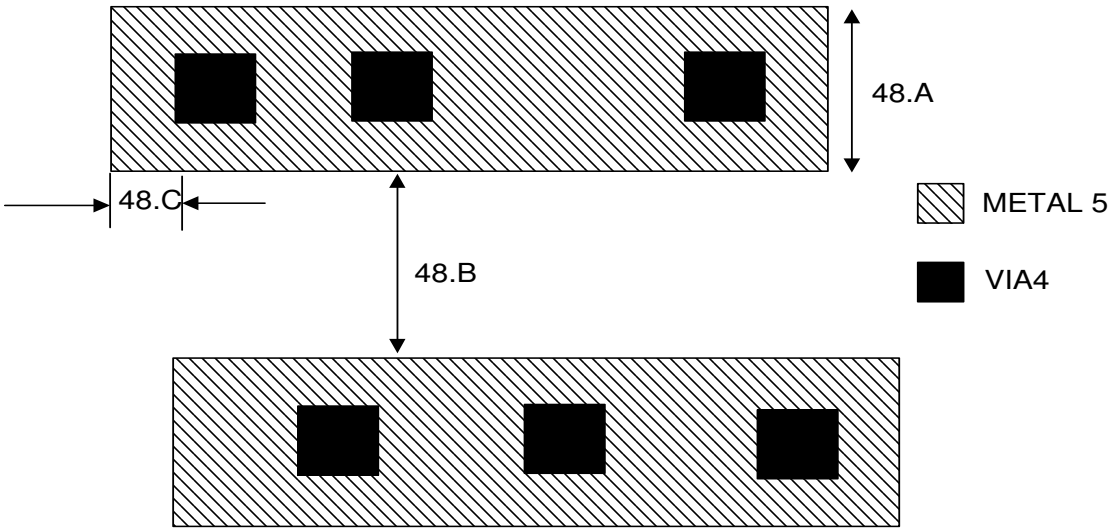


ILLUSTRATION 48

4.23 Via 5 (layer 57)

Mask 57: This mask defines metal 5 to metal 6 contact areas. This mask is a negative mask and is aligned to the zero layer. Note: Via5s may be placed over contacts, vias.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA Only
57.A	Minimum/maximum via5 size	0.5x0.5
57.B	Minimum metal 5 overplot of via5	0.35
57.C	Minimum via5 to via5 space	0.50

4.24 Metal 6 (layer 58)

Mask 58: This mask defines the top (or sixth) metal interconnects, inductors and bonding pads for a circuit. The mask is a positive tone mask and is aligned to ZL. See Illustration 58.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA only
58.A	Minimum metal 6 width	2.50
58.B	Minimum metal 6 to metal 6 space	2.00
58.C	Metal 6 overplot of via 5	0.35
58.D	Minimum metal 6 density (total metal 6 area / chip area). See Note 1	25%
58.E	Minimum metal 6 area	6.25 (μm^2)
58.F	Maximum metal 6 density (total metal 6 area / chip area). See Note 1	60%

Note 1: **Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements.** See Section 3.5.1 and 3.5.2 for dummy metal fill generation.
Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 95). See section 5.12.

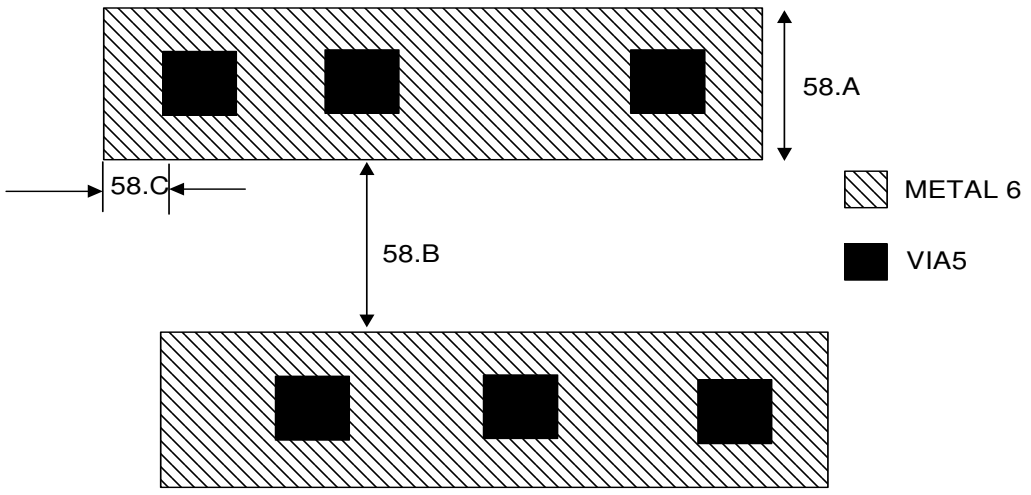


ILLUSTRATION 58

4.25 Protective Overcoat "S" (Layer 9)

Mask 9: This layer provides overcoat protection for the chip. This mask is a negative mask and is aligned to the zero layer. See the section on bonding pads for related rules.

Rule No.	Rule Name	
9.A	Minimum passivation overcoat width	4
9.B	Minimum spacing passivation overcoat to passivation overcoat	4

4.26 Polyimide Protective Overcoat "PO" (Layer 99)

Mask 99: The polyimide overcoat (layer 99) is added on top of the oxide/nitride passivation overcoat for some process variants with greater than 2.5um thick top metal. The polyimide overcoat helps to significantly improve the top planarization of the finished wafers even with the thick patterned top metal features.

Layer 99 is generated from drawn layer 9. See Section 3.5 for layer generation of layer 99. This mask is a negative mask and is aligned to the zero layer. See Illustration POLYIMIDE.

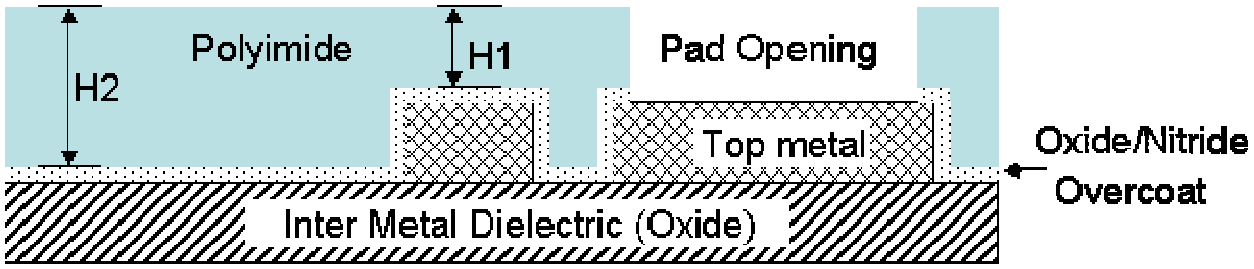


ILLUSTRATION POLYIMIDE

Process variants with polyimide overcoat are identified by the addition of the letter "Z" at the end of the process name. For example, the polyimide overcoat process variant of the process SBC18HX would be called SBC18HXZ process. The following layer 9 rules are applicable for all SBC18**Z processes

Rule No.	Rule Name	SBC18*Z only
9.A	Minimum width of polyimide protective overcoat	20
9.B	Minimum spacing polyimide protective overcoat to polyimide protective overcoat	12
9.C	Layer 9 is not allowed within artifact marking layer (Any drawn layer 9 data within artifact region will be ignored during layer generation)	

Note 1: All checked rules specified for custom wire bond pads are applicable to processes with polyimide overcoat

Note 2: Any opening less than the specification of rule 9.A will be closed during layer generation.

5 Design Rules for RF and Mixed Signal Components

5.1 SiGe NPN Transistor Rules

The SiGe NPN rules are defined in this section. There are three versions of NPNs (a) High speed NPN (b) Standard NPN and (c) High Voltage NPN, in decreasing order of cut-off frequency. See Illustration NPN for standard NPN rules. Rules for the Standard NPN version are shown below. See notes 1 and 2 to obtain the High Speed NPN version and High Voltage NPN versions from the Standard NPN version.

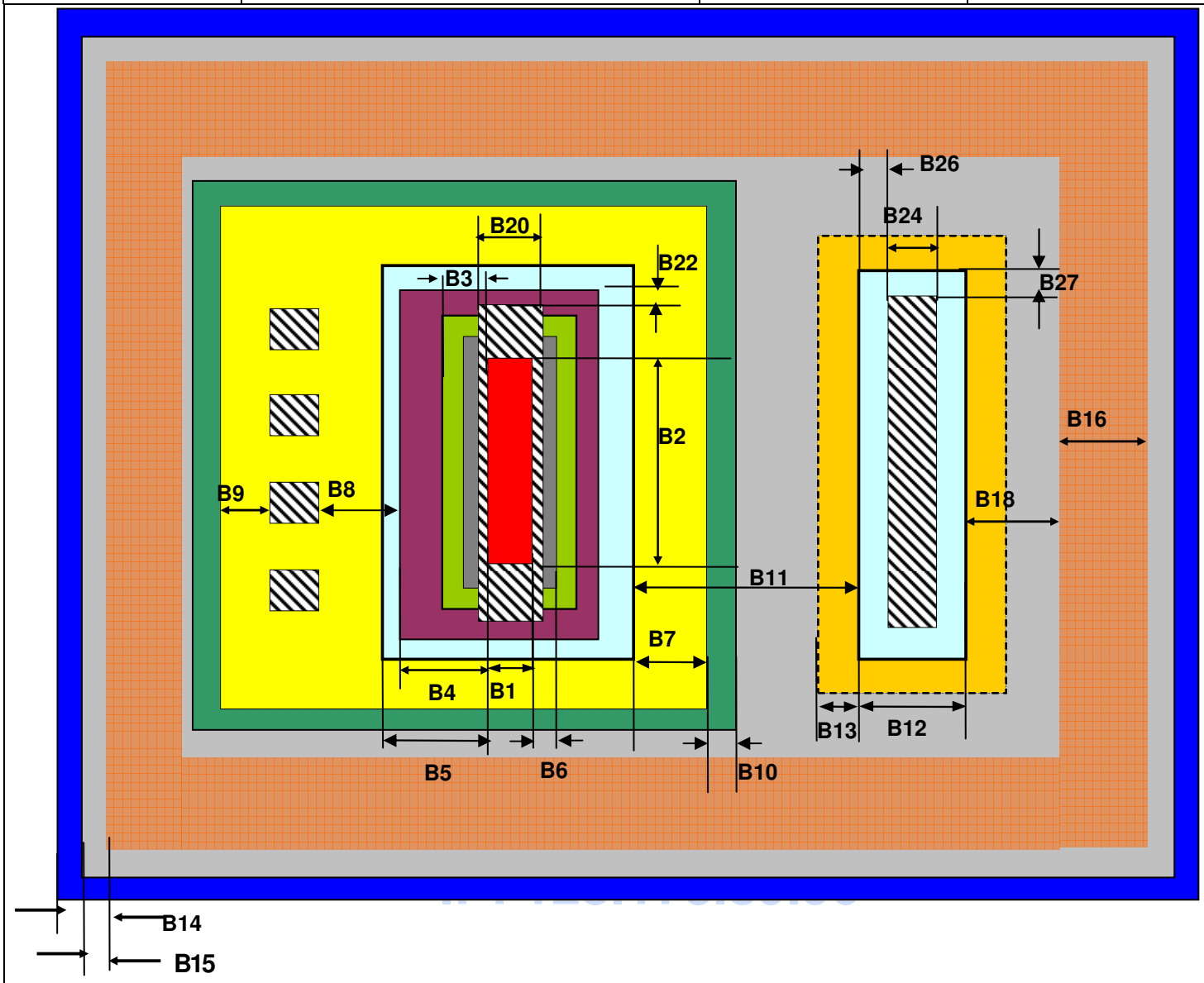
The high speed NPN device is not offered in SBC18PT, SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW, SBC18MW, SBC18MV, SBC18MWD processes

Please note that the deep trench layer (layer 41) is drawn for design rule check reference purposes only for SBC18PT, SBC18QW, SBC18MW processes. No mask is made for layer 41 for SBC18PT, SBC18QW, SBC18MW, SBC18MV processes.

Rule No.	Rule Name	All SBC18
B1	Emitter (EM) widths allowed	0.20, 0.6, 0.9 only
B1.a	Maximum emitter (EM) width for High Speed NPNs only	0.20
B2	Minimum emitter (EM) length	0.76
B3	Minimum/maximum emitter window (EW) overplot of emitter (EM)	0.085
B4	Minimum/Maximum emitter poly (EP) overplot of emitter (EM)	0.25
B5	Minimum/Maximum active overplot of emitter (EM)	0.3
B6	Minimum/Maximum local collector overplot of emitter (EM)	0.05
B7	Minimum base poly (BP) overplot of base active	0.35
B8	Minimum/Maximum distance from base contact to emitter poly (EP)	0.2
B9	Minimum/Maximum base poly (BP) overplot of base contact	0.1

Note 1: For High Voltage NPN version, eliminate the Local Collector (LC) implant (layer 44) from the Standard NPN version; i.e., there is neither layer 34 nor layer 44.

Note 2: For High Speed NPN version replace Local Collector implant (layer 44) from the Standard NPN version with High Speed implant (layer 34); i.e., there is layer 34 but no layer 44. Layer 34 rules are identical to layer 44 rules.



Rule No.	Rule Name	All SBC18
B10	Minimum/Maximum spacer clear overplot of base poly (BP)	0.1
B11	Minimum distance from base active to collector sinker active	0.9
B12	Minimum/Maximum collector sinker active width	0.89
B13	Minimum/Maximum collector sinker implant overplot of collector sinker active	0.15
B14	Minimum/Maximum buried layer overplot of outer edge of deep trench	0.10
B15	Minimum/Maximum Nwell-2 overplot of outer edge of deep trench	0.10
B16	Minimum/Maximum deep trench width	1.20
B17	Minimum space deep trench to deep trench	1.80
B18	Minimum/Maximum deep trench space to active	0.50
B19	Maximum distance between deep trench and substrate contact	30
B20	Minimum/Maximum emitter slot contact width	0.30
B21	Minimum emitter slot contact to emitter slot contact space	0.30
B22	Minimum emitter poly (EP) overplot of emitter slot contact	0.1
B23	The emitter slot contact (or slot contact array) has to be centered with respect to emitter poly (EP)	
B24	Minimum/Maximum collector sinker slot contact width	0.36
B25	Minimum collector sinker slot contact to collector sinker slot contact space	0.30
B26	Minimum/Maximum collector sinker slot contact to active parallel to long edge of collector sinker slot contact	0.265
B27	Minimum/Maximum collector sinker slot contact to active parallel to short edge of collector sinker slot contact	0.15

Note 3: Varactor rules VAR.13 to VAR.18 are derived from NPN rules B24, B25, B26, B27, B28, and B32, respectively.

Note 4: For High Speed NPN version, a maximum of 2 emitter fingers are allowed. This restriction is not applicable to the Standard NPN and High Voltage NPN

Rule No.	Rule Name	All SBC18
B28	Minimum Metal 1 overplot of slot contact (both collector sinker and emitter)	0.1
B29	Minimum/Maximum slot via1 width	0.30
B30	Minimum slot via1 to slot via1 space	0.30
B31	Minimum metal 1 and 2 overplot of slot via1	0.1
B32	Maximum slot emitter contact, slot collector contact and slot via length	25
B33	Analog block border (layer 95) must cover NPN extent	
B34	Slot contacts and vias are allowed only inside collector sinker active and emitter poly	
B35	It is required that all NPNs have (and be surrounded by) substrate contacts	
B36	No first poly (layer 5) is allowed within N_cell marking layer	
B37	Minimum space between first poly and deep trench (not shown in figure below) Note: Poly cannot be placed over deep trench	1.0
B38	Minimum slot emitter contact, slot collector contact and slot via length	1.06
B39	Minimum space ‘slotted contact’ to ‘contact’	0.4
B40	Minimum space ‘slotted via’ to ‘via’	0.5
B41	For dual collector devices, both collectors must be connected together electrically	

5.1.1 Additional rules for devices using bipolar layers

Rule No.	Rule Name	
23.A	Minimum base poly width	1.62
23.B	Minimum base poly space	1.99
23.D	Minimum space base poly to first poly	0.8
29.A	Minimum emitter poly width	0.70
29.B	Minimum emitter poly space^	0.62
29.C	Minimum overplot base poly to emitter poly	0.40
68.A	Minimum Nwell-2 width	4.00
68.B	Minimum Nwell-2 space outside P_cell marking layer	0.9
68.C	Minimum distance Nwell-2 to Nwell	4.00
68.D	Minimum distance Nwell-2 to unrelated N+ active*	4.00
68.E	Minimum distance Nwell-2 to unrelated P+ active*	0.35
68.F	Minimum Nwell-2 space inside P_cell marking layer	1.60
68.G	Substrate contacts must exist directly between Nwell-2, and Nwell placed within 30 um of Nwell-2	
68.H	Substrate contacts must exist directly between Nwell-2 and unrelated N+active* placed within 30 um of Nwell-2	

* N+/P+ active is defined as any active region intersecting N+ or P+ implants.

^ Rule 29.B does not apply to ESD protection devices described in section 6.

Rule No.	Rule Name	
4.A	Minimum buried layer width	4.96
4.B	Minimum space buried layer to buried layer (Within artifact marking layer, minimum space = 2um)	4.60
4.B.a	Minimum space buried layer to buried layer when both buried layers are within Ncell marking layer (for SBC18HX, HXL, QTD, QTR, QTL, MWD only)	1.60
10.A	Minimum collector sinker (CS) width	0.8
10.B	Minimum collector sinker (CS) to collector sinker (CS) space	1.6
31.B	Minimum space emitter (EM) to emitter (EM)	1.12
33.A	Minimum emitter window (EW) width	0.37
33.B	Minimum space emitter window (EW) to emitter window (EW)	0.95
21.A	Minimum spacer clear width	1.82
21.B	Minimum spacer clear space	1.79
40.A	Minimum silicide block width	0.50
41.A	Deep Trench must not exist in SBC18MW, SBC18MV, SBC18QW, SBC18PT processes except within Ncell and Schottky diode marking layers. The deep trench process is not available for these processes	
41.B	T-shaped and cross-shaped deep trenches are not allowed (deep trench sharing is not allowed)	

5.2 PNP Transistor Rules

5.2.1 Lateral PNP Transistors

These guidelines represent a recommended layout to design a unit cell LPNP device. The parasitic Lateral bipolar PNP transistors, for use in analog designs, are formed from a P+ diffusion (emitter), surrounded by an N- epi (base) , and the P+ diffusion collector. The base extent is defined by the P+ implant space extending from the emitter and the collector and is covered by a silicide block layer. The base is connected through a n+ buried layer. See Illustration LP

The fixed cell available in the kit can be replicated as follows: For 2 cells, mirror image the structure along the center line of the top base contacts. This will result in rows of substrate contacts at top and bottom. A maximun of 2 rows of unit cells can be placed between substrate contacts.
For Additional pairs of unit cells, mirror the structure along the center line of the right base contacts.

Note that model support will be given only for devices following this fixed cell approach.

Note that the LPNP has to be covered by the Bipolar Lateral PNP marking layer (layer 66)

Rule No.	Rule Name	All SBC18
LP.A	Minimum/maximum opening of silicide block in emitter area of LPNP	0.6 x 0.6
LP.B	Minimum/maximum width of silicide block in LPNP	2.3
LP.C	Minimum/maximum Emitter P+ Implant overlap of silicide block	0.2
LP.D	Minimum/maximum space between emitter P+ implant and collector P+ implant	1.8
LP.E	Minimum/maximum collector diffusion overplot of silicide block	0.57
LP.F	Minimum/maximum P+ implant overplot of collector diffusion	0.05
LP.G	Minimum/maximum space collector diffusion to base diffusion	0.70
LP.H	Minimum/maximum width of base diffusion	0.50
LP.I	Minimum/maximum overplot of sinker implant to base diffusion	0.15
LP.J	Minimum space of Nwell2 to base diffusion	0.60
LP.K	Minimum space of buried layer to base diffusion	0.60

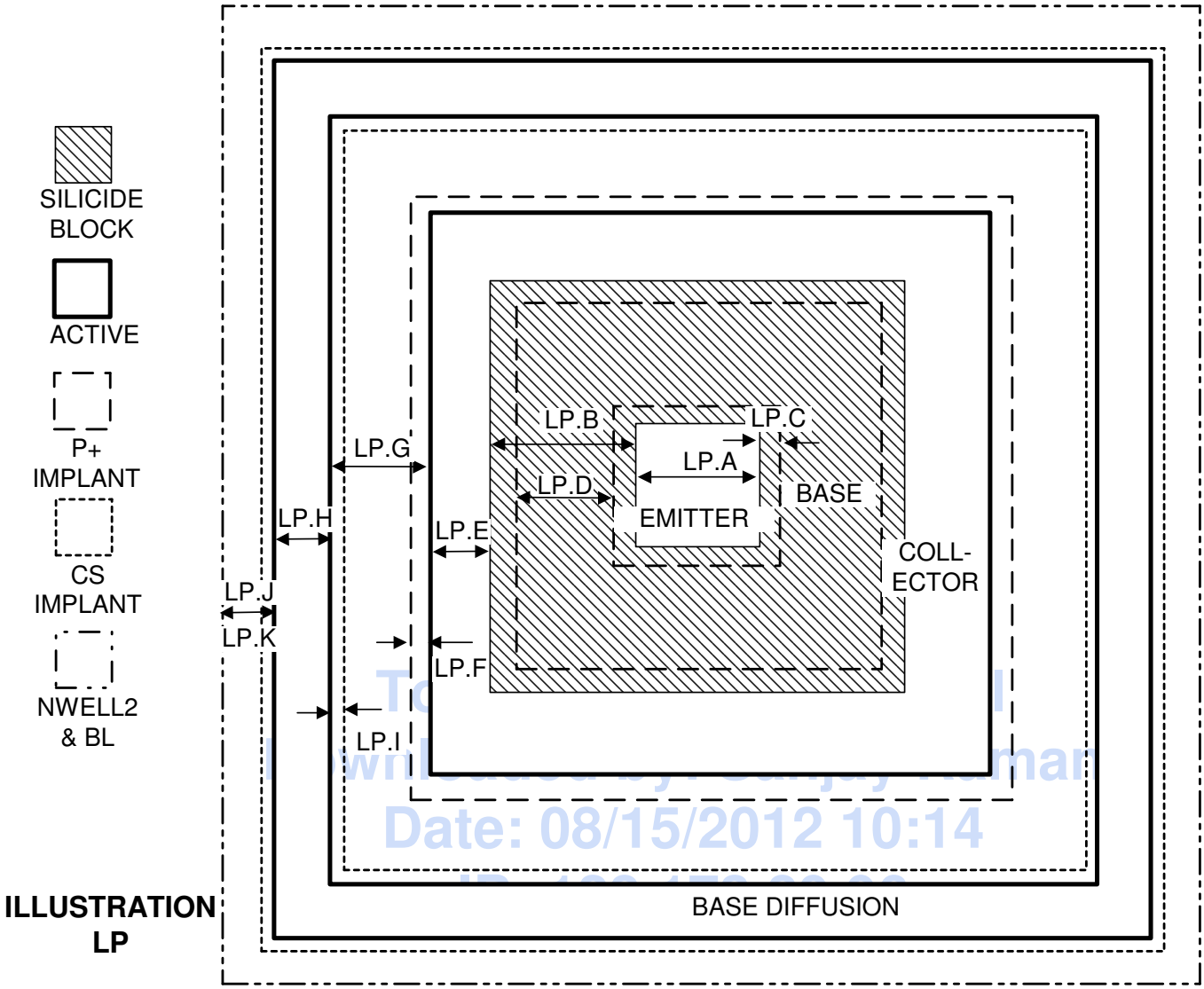


ILLUSTRATION LP

5.2.2 Vertical PNP Transistor

The parasitic vertical bipolar PNP transistors, for use in analog designs, are formed from a P+ diffusion in the N-well (emitter), an N-well (base) with an N+ diffusion guard-ring, and the P- substrate (collector) with a P+ diffusion ring. See figure BP.

Note: The VPNP transistor has to be covered by Bipolar Vertical PNP marking layer (layer 39)

Rule No.	Rule Name	All SBC18
BI.A	Minimum emitter size (P+ diffusion inside N-well). Emitter is always square.*	3.0 x 3.0
BI.B	Minimum spacing P+ emitter diffusion inside N-well to N+ base diffusion.	0.38
BI.C	Minimum N+ base diffusion width	0.42
BI.D	Minimum N-well overplot of N+ base diffusion (Same as rule 2.H)	0.12
BI.E	Minimum spacing N+ base diffusion to P+ collector diffusion in substrate	0.36
BI.F	Minimum P+ collector diffusion width	0.60
BI.G	N+ base diffusion must surround P+ emitter diffusion.	
BI.H	P+ collector diffusion must surround N+ base diffusion.	
BI.J	Maximum space contact to contact in the emitter, base and collector.	0.80

* Note : Only the following emitter sizes are allowed 3x3 um^2, 5.4x5.4 um^2, 11x11 um^2 and 25x25 um^2

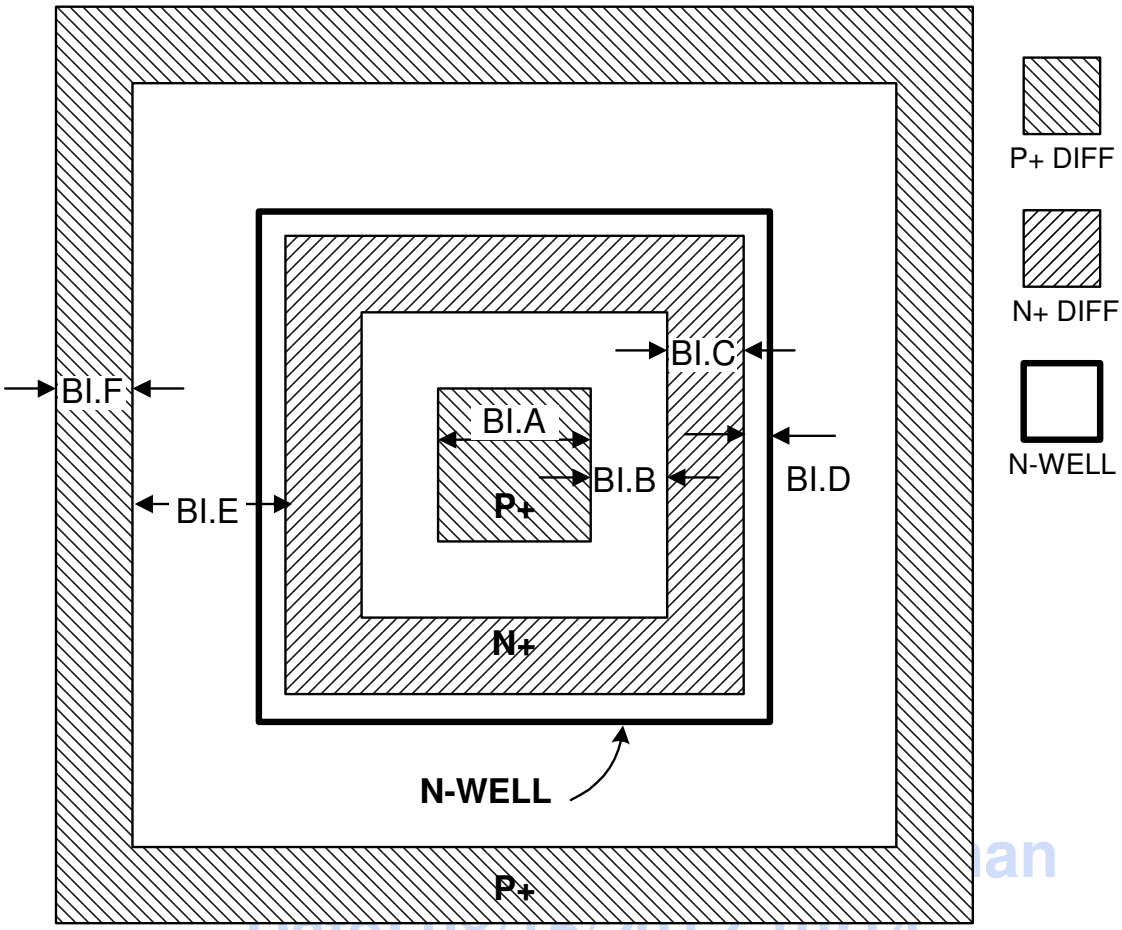


ILLUSTRATION BP

5.3 Resistor Rules:

5.3.1 Metal Resistor Rules:

Metal resistors should be drawn without dogbone ends. The minimum width of metal resistor is determined by minimum Metal Resistor (TR) layer 26 that contains at least one via 3 (See MR.A). For wider resistors, the maximum number of vias in a direction perpendicular to the length should be used to reduce resistance. See Illustration MR for SBC18HX, SBC18HXL, SBC18HA process and Illustration MR1 for SBC18QTR process.

Rule No.	Rule Name	***SBC18HX, SBC18HXL, SBC18HA only***	***SBC18QTR only***
MR.A	Minimum Width of TR	0.56	0.56
MR.B	Minimum Space TR to TR	0.56	0.56
MR.C	Minimum length of Metal Resistor*	2.00	2.00
MR.D	Minimum TR overplot of Via 3 (standard M3 overplot of Via3 rules do not apply here).	0.15	N/A
	Minimum TR overplot of Via 1 (standard M1 overplot of Via1 rules do not apply here).	N/A	0.15
MR.E	Minimum space between TR and Metal 3. No Via 2 or Metal 3 is allowed below TR.	5.00	N/A
	Minimum space between TR and Metal 1. No contact or Metal 1 is allowed below TR.	N/A	5.00
MR.F	Metal resistor is connected to rest of circuit using Via 3 and Metal 4 only**		N/A
	Metal resistor is connected to rest of circuit using Via 1 and Metal 2 only***	N/A	
MR.G	Minimum Analog block border (layer 95) overplot of TR ****	1.00	1.00
MR.H	Non rectangular TR is not allowed		

* The minimum length of TR also includes the size of two vias on either end and their minimum TR overplot of Via1 or via3
** Note: No connections are allowed on metal resistors (layer TR) using metal 3 or via 2.
*** Note: No connections are allowed on metal resistors (layer TR) using metal 1 or contact.
**** Not shown in illustration MR

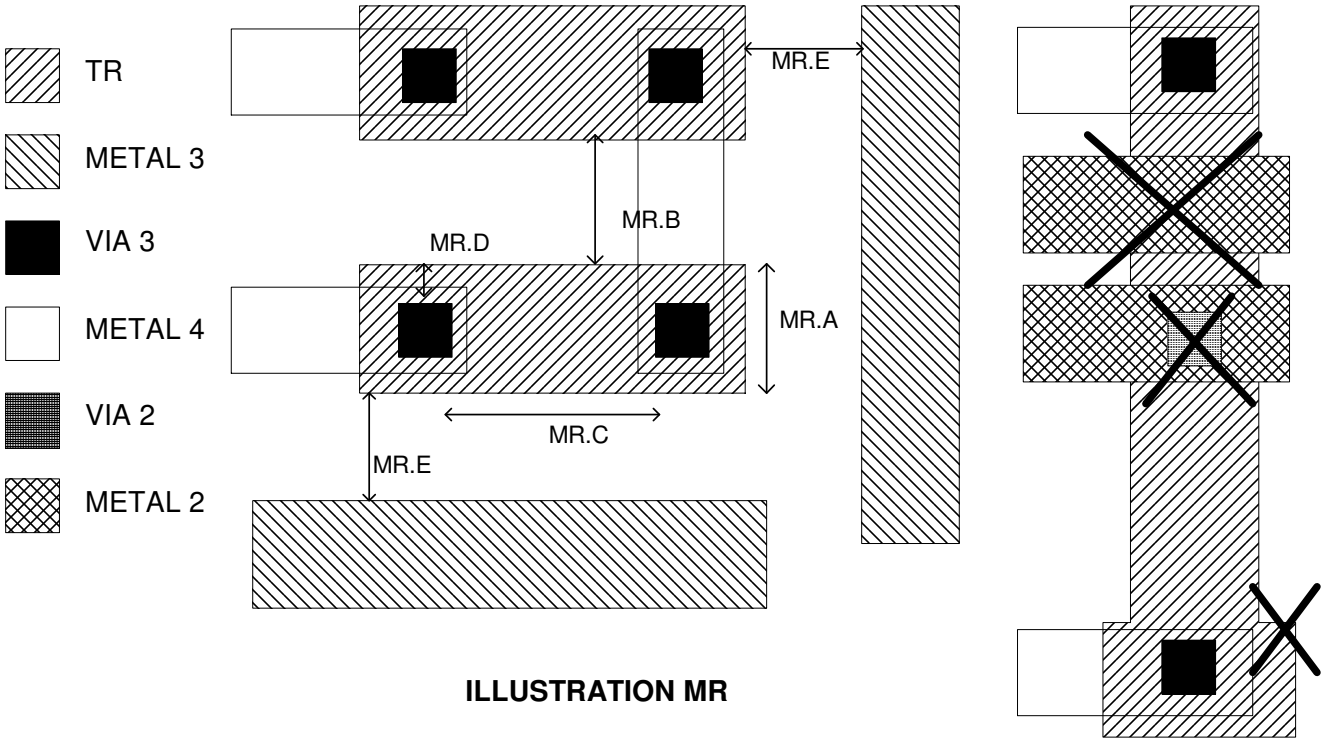


ILLUSTRATION MR

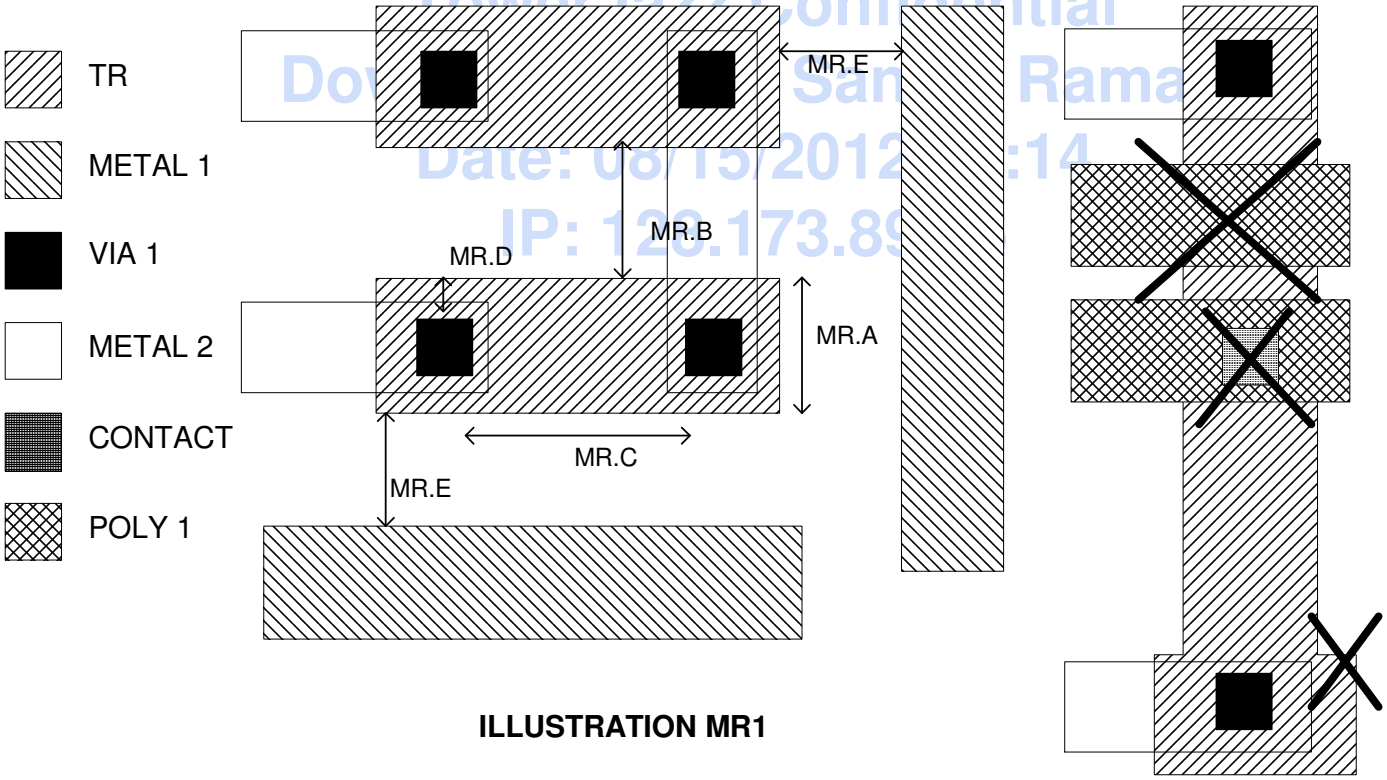


ILLUSTRATION MR1

5.3.2 High Value Unsilicided Poly Resistor Rules

The HR layer defines polysilicon regions over field oxide, which does not receive silicide but receive the HR implant. Silicide Block, which defines the unsilicided p-poly resistor regions, is a positive mask and aligns to ZL. High Value resistor Implant (HR) is a negative mask and aligns to ZL. See Illustration HR.

Rule No.	Rule Name	***SBC18PT, SBC18HA, SBC18QTD, SBC18QTR, SBC18QTL, SBC18MW, SBC18MWD, SBC18MV Only***
HR.A	Minimum Silicide Block overplot of P-poly resistor	0.50
HR.B	Minimum Length Silicide Block	2.00
HR.C	Minimum Space Silicide Block to Active (Note: SB overlap of active is not allowed)	0.50
HR.D	Minimum Space Silicide Block to P-poly resistor contact	0.40
HR.E	Minimum Space Silicide Block to Silicide Block	0.50
HR.G	Minimum HR Implant overplot of P-poly resistor.	0.40
HR.H	Minimum Space HR to HR	0.50
HR.K	Minimum Space Silicide Block to unrelated poly	0.40
HR.L	Minimum space N+ Implant to P-poly resistor.	0.40
HR.N	Minimum space SB to P-poly edge (of resistor) parallel to SB	0.40
HR.O	Minimum Nwell overplotf P-poly resistors (not shown)	0.50
HR.P	Minimum Nwell spacing to P-poly resistors (not shown)	0.50
HR.R	Minimum P-poly resistor length (non silicided region defined by SB mask)	2.00
HR.T	Minimum analog block border (layer 95) overplot of P-poly resistor*	1.00
HR.U	Minimum width of HR	0.7

* Not shown in Illustration HR

Note 1: P-poly resistors are either totally inside Nwell or outside nwell per HR.O and HR.P.

Note 2: Active design rules require additional drawn active to be added near large Poly resistor areas. See Section 5.3.6 for details.

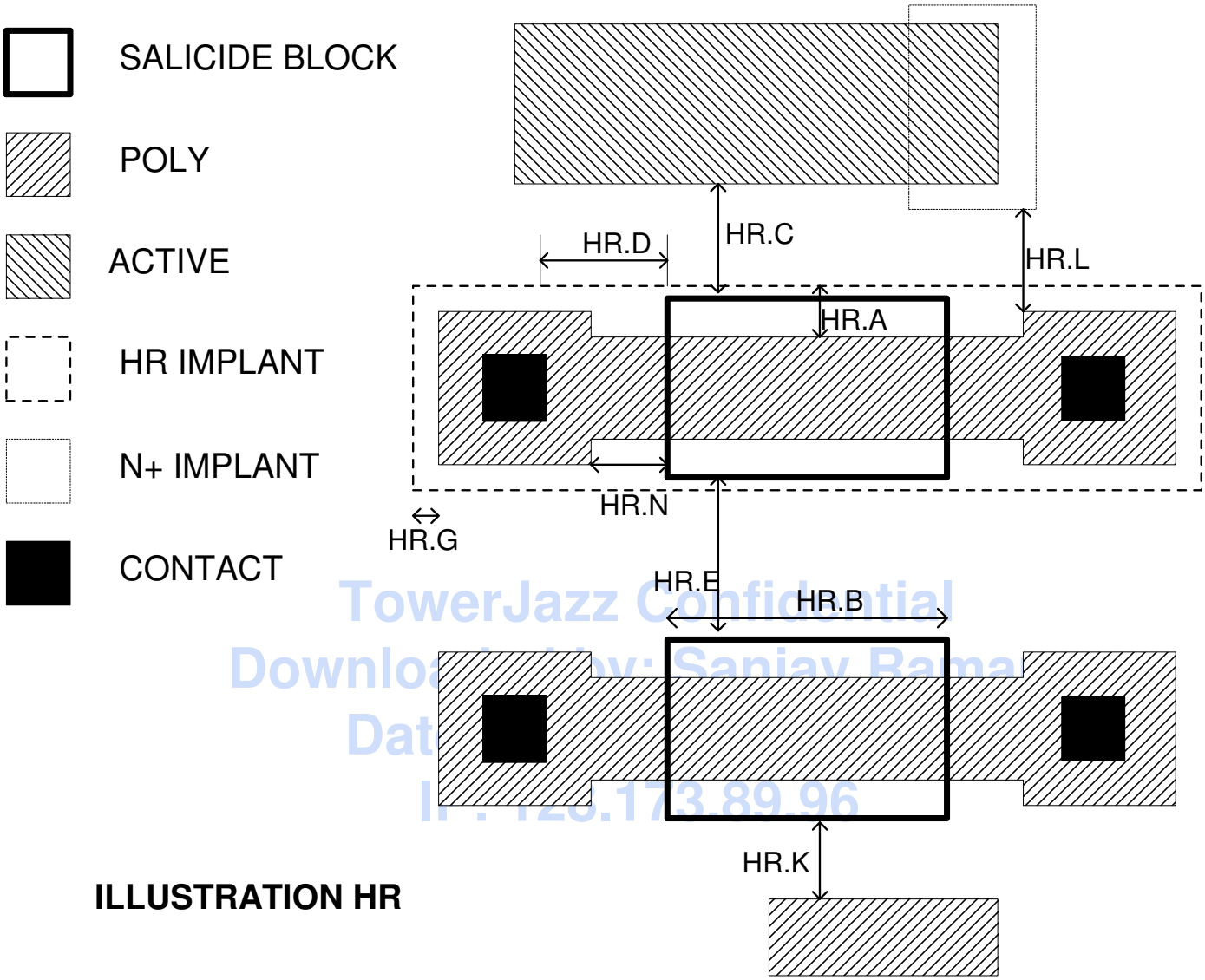


ILLUSTRATION HR

5.3.3 Low value Unsilicided P+ Poly Resistor Rules:

This defines polysilicon regions over field oxide, which do not receive silicide. Silicide Block is used to define the p-poly resistor regions. It is a positive mask and aligns to ZL. See Illustration PR.

Rule No.	Rule Name	All SBC18
PR.A	Minimum Silicide Block overplot of P-poly resistor	0.50
PR.B	Minimum Length Silicide Block	2.00
PR.C	Minimum Space Silicide Block to Active (Note: SB overlap of active is not allowed)	0.50
PR.D	Minimum Space Silicide Block to P-poly resistor contact	0.40
PR.E	Minimum Space Silicide Block to Silicide Block	0.50
PR.G	Minimum P+ Implant overplot of P-poly resistor.	0.40
PR.K	Minimum Space Silicide Block to unrelated poly	0.40
PR.L	Minimum space N+ Implant to P-poly resistor.	0.40
PR.N	Minimum space SB to P-poly edge (of resistor) parallel to SB	0.40
PR.O	Minimum Nwell overplot of P-poly resistors (not shown)	0.50
PR.P	Minimum Nwell spacing to P-poly resistors (not shown)	0.50
PR.R	Minimum P-poly resistor length (non silicided region defined by SB mask)	2.00
PR.T	Minimum Analog block border (layer 95) overplot of P-poly resistor*	1.00

*Not shown in illustration PR

Note 1: P-poly resistors are either totally inside Nwell or outside Nwell per PR.O and PR.P

Note 2: Active design rules require additional drawn active to be added near large Poly resistor areas. See Section 5.3.6 for details.

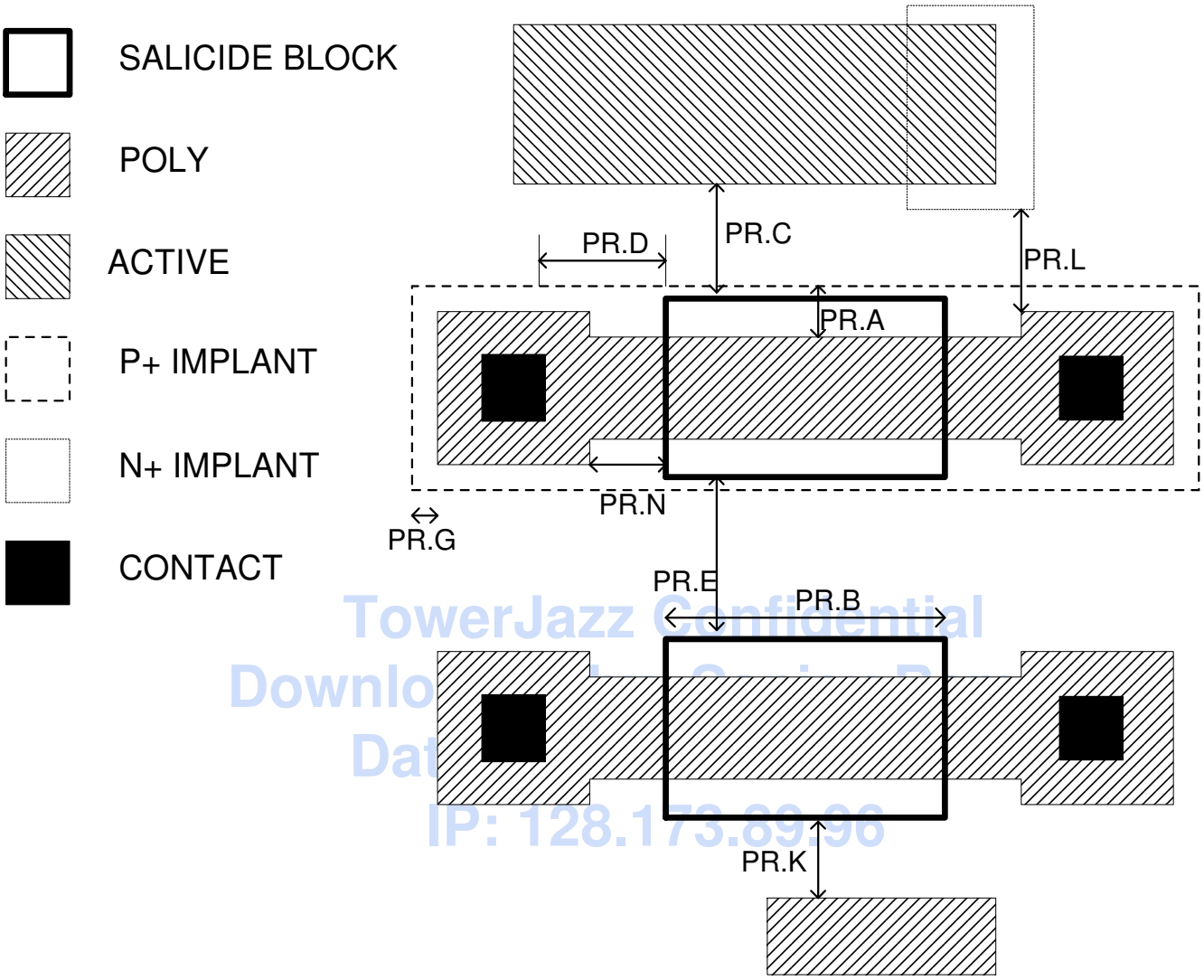


ILLUSTRATION PR

5.3.4 Silicided Poly Resistors

Low sheet resistance silicided poly resistors are fabricated by implanting the entire poly resistor including contact regions with P+ implant and completing the standard silicidation process. This resistor requires no additional masks or process steps.

Silicided resistors should be drawn without dogbone ends, that is, the minimum width is determined by minimum poly that contains at least one contact (see SR.D). For wider resistors, the maximum number of contacts in a direction perpendicular to the length should be used to reduce end resistance. See Illustration SR.

Silicide resistors must be marked with layer 108.

Rule No.	Rule Name	All SBC18
SR.A	Minimum P+ Overplot of Silicided Resistor	0.40
SR.B	Minimum Space N+ Implant to Silicided Resistor	0.40
SR.C	Minimum Space Active to Silicided Resistor	0.40
SR.D	Minimum width Silicided Resistor	0.42
SR.F	Minimum Analog block border (layer 95) overplot of silicided resistor (not shown)	1.00
SR.G	Minimum Nwell overplot of silicided resistor (not shown)	0.50
SR.H	Minimum Nwell spacing to silicided resistor (not shown)	0.50

Note 1: Silicided resistors are either totally inside Nwell or outside Nwell per SR.G and SR.H

Note 2: Active design rules require additional drawn active to be added near large Poly resistor areas. See Section 5.3.6 for details.

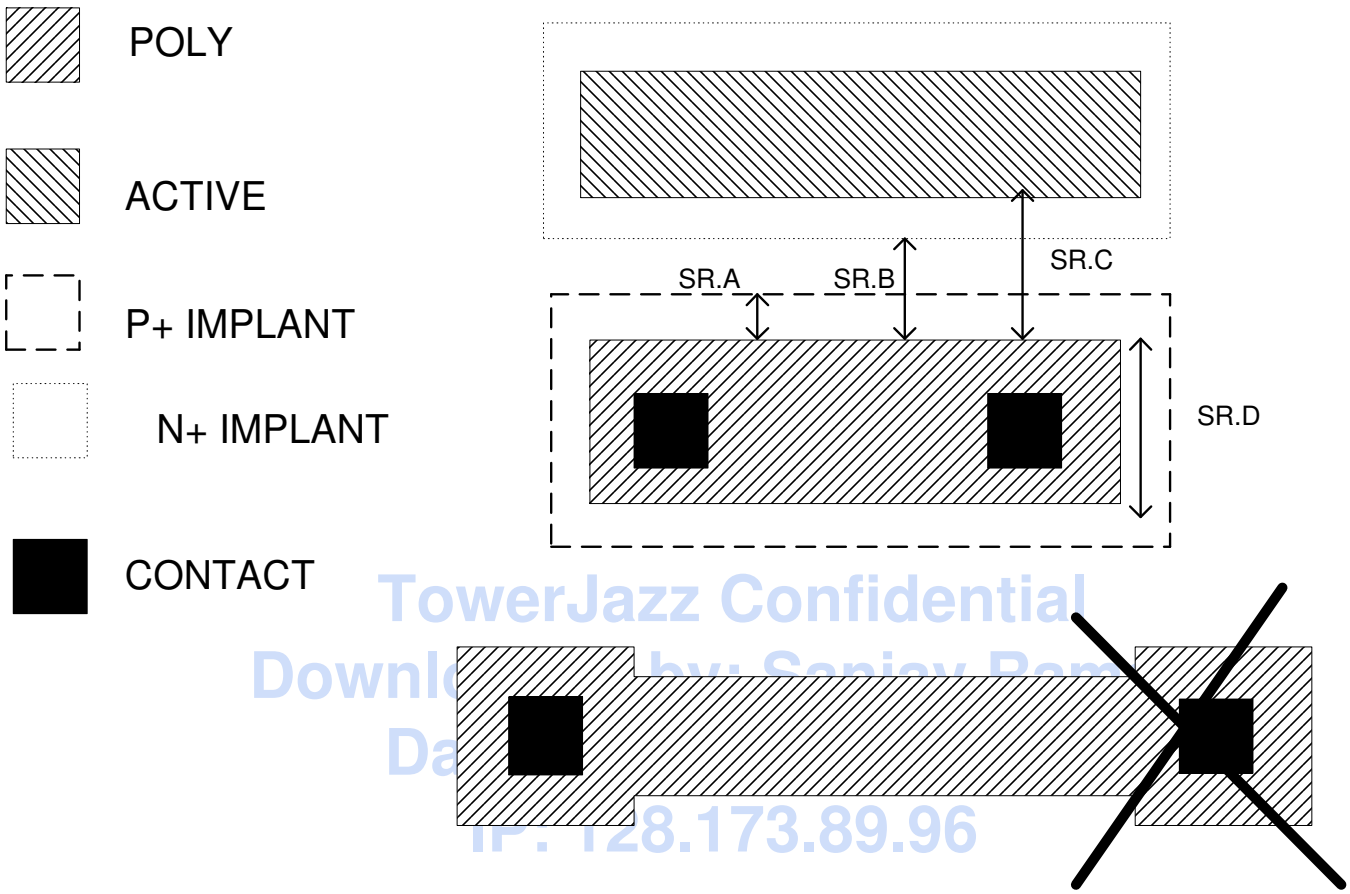


ILLUSTRATION SR

5.3.5 N-well Resistors

High value N-well resistors are fabricated by making n+ implanted active contacts at the end of Nwell implanted layer below the field oxide. See Illustration NWRES.

N-Well resistors must be marked with layer 80.

Rule No.	Rule Name	All SBC18
2.I	Minimum N+ diffusion extension into the N-well as N-well tie for N-well resistors (See Note 1)	0.60
2.I.a	Minimum N+ diffusion overlap area of the N-well as N-well tie for N-well resistors (See Note 1)	0.50 (μm^2)
1.A.a	Minimum N-well width for N-well used as a resistor	2.10

Note 1: 2.I, 2.I.a, 1.A.a: A marking layer (Layer 80) is used to mark all the N-well resistors.

Note 2: Active design rules require additional drawn active to be added near large N-well resistor areas. See Section 5.3.6 for details.

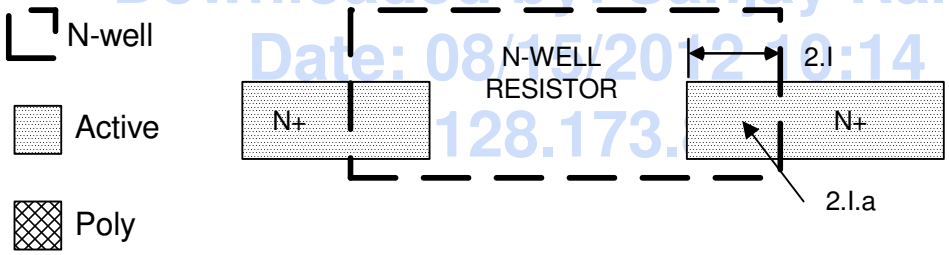


ILLUSTRATION NWRES

5.3.6 Adding drawn active near large poly/nwell resistor areas with no drawn active or dummy active generation

Additional rules are required to insure that a sufficient amount of active area is added near large areas due to the presence of N-well resistors or poly. Both of these features prevent the generation of dummy active fill which would normally occur to prevent CMP related issues. The dummy active fill generation rules are detailed in Section 3.5.3.

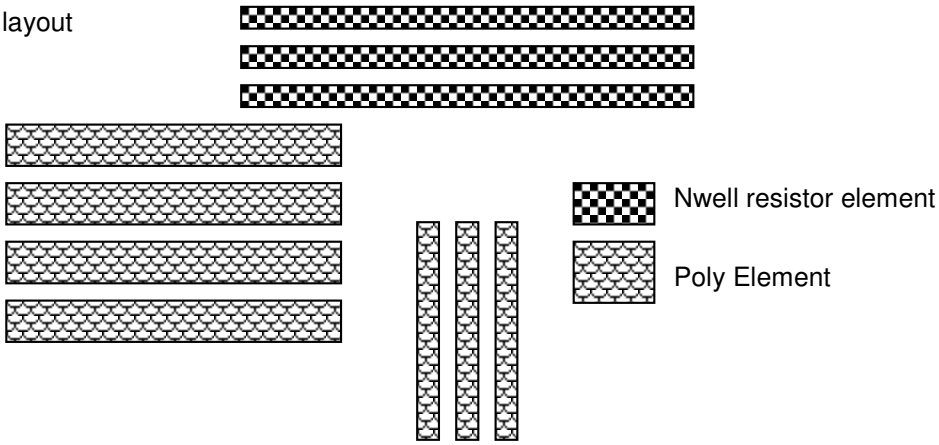
The following rules apply to all merged polygons (merged N-well resistor and poly on field features, see below for algorithm to generate the polygons).

Algorithm to Generate Merged Resistor Polygons

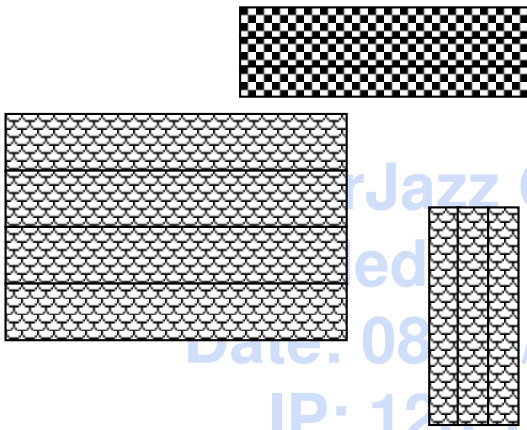
1) Size up drawn active by 2.5um per edge. (data file 1)
2) Identify poly layer (data file 2)
3) Identify N-well resistors (data file 3)
4) Add data file 2 and 3 and subtract data file 1 to obtain polygons, (data file 4) = (data file 2) + (data file 3) – (data file 1)
5) Size up data file 4 by 2.5µm per edge and merge features to obtain the merged polygons (data file 5).

Rule No.	Rule Name	All SBC18
2.L	Minimum width of drawn active stripes between any two merged polygons within 40µm of transistors, with areas between 7,500µm^2 and 15,000µm^2 and spaced less than 30µm apart	5
2.M	Minimum width of drawn active rings surrounding merged polygons, for merged polygons with area < 15,000µm^2, or one of the dimensions (X or Y) < 15µm	0
2.M.a	Minimum width of drawn active rings surrounding merged polygons, for merged polygons within 40µm of transistors, with area between 15,000µm^2 and 50,000µm^2	5
2.M.b	Minimum width of drawn active rings surrounding merged polygons, for merged polygons within 40µm of transistors, with area between 50,000µm^2 and 100,000µm^2	10
2.M.c	Minimum width of drawn active rings surrounding merged polygons, for merged polygons within 40µm of transistors, with area between 100,000µm^2 and 200,000µm^2	20
2.M.d	Merged polygons with area larger than 200,000µm^2 are not allowed.	
2.N	Minimum space between required additional drawn active features (stripes or rings) and corresponding merged polygons.	2
2.O	Maximum space between required additional drawn active features (stripes or rings) and corresponding merged polygons.	10

Example layout



Example layout : Size up to merge features



Resulting " Merged Polygon"

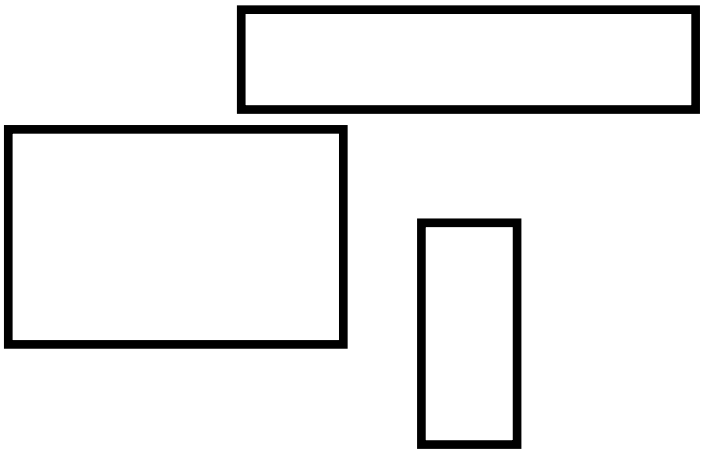


ILLUSTRATION DA

5.4 Capacitor Rules

5.4.1 Rules of 1fF/μm^2 density Metal-Insulator-Metal Capacitor

Applicable to SBC18HX, SBC18HXL only

This defines high unit area capacitor structures (MIM caps) fabricated using metal 4 (Layer 38) as the lower plate and top capacitor metal (TM) as the upper plate. See Illustration MC
Layer 22 is a positive masks.

Rule No.	Rule Name	SBC18HX, SBC18HXL only
MC1	Minimum TM width/length	1.50
MC2	Minimum TM Overplot of Via4	0.50
MC3	Minimum Space TM to Via4	0.50
MC4	Minimum Metal 4 Overplot of TM	1.00
MC5	Minimum Space TM to TM	0.80
MC9	Minimum via4 to via4 space on TM (for TM area > 400um^2)	3.50
MC9.a	Minimum via4 to via4 space on TM (for TM area < 400um^2)	1.00
MC10	Maximum via4 to via4 space on TM	4.50
MC11	Minimum space capacitor TM to via3 (No Via3 is allowed below TM layer)	0.50
MC21	Minimum Analog block border (layer 95) overplot of TM*	2.00

* Not shown in illustration MC

Note 2: For best matching results it is recommended that a minimum via3 to TM space of 2.0 um be maintained.

5.4.2 Rules of 2fF/μm^2 density Metal-Insulator-Metal Capacitor

Applicable to SBC18PT, SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW, SBC18MW, SBC18MV, SBC18MWD processes only

This defines high unit area capacitor structures (MIM caps) fabricated using metal 2 (Layer 18) as the lower plate and top capacitor metal (TM) as the upper plate. See Illustration MCB
Layer 22 is a positive mask. The 2fF/μm^2 density MIM capacitor has to be covered by layer 70 (layer cap2fF) to distinguish it from the 1fF/μm^2 density MIM capacitor.

Rule No.	Rule Name	SBC18PT, SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW, SBC18MW, SBC18MWD, SBC18MV, Only
MCB1	Minimum TM width/length	1.50
MCB2	Minimum TM Overplot of Via2	0.50
MCB3	Minimum Space TM to Via2	0.50
MCB4	Minimum Metal 2 Overplot of TM	1.00
MCB5	Minimum Space TM to TM	0.80
MCB9	Minimum via2 to via2 space on TM (for TM area > 400um^2)	3.50
MCB9.a	Minimum via2 to via2 space on TM (for TM area < 400um^2)	1.00
MCB10	Maximum via2 to via2space on TM	4.50
MCB11	Minimum space capacitor TM to via1 (No Via1 is allowed below TM layer)	0.50
MCB21	Minimum Analog block border (layer 95) overplot of TM*	2.00

* Not shown in illustration MCB
Note 2: For best matching results it is recommended that a minimum via1 to TM space of 2.0 um be maintained.

5.4.3 Rules for 2.8fF/um^2 density Metal-Insulator-Metal Capacitor

Applicable to SBC18HA processes only

This defines high unit area capacitor structures (MIM caps) fabricated using metal 4 (Layer 48) as the lower plate and top capacitor metal (TM) as the upper plate. See Illustration MCC
Layer 22 is a positive mask. The 2.8fF/µm^2 density MIM capacitor has to be covered by layer 70 (layer cap2fF) to distinguish it from the 1fF/µm^2 density MIM capacitor.

Rule No.	Rule Name	SBC18HA
MCC1	Minimum TM width/length	1.50
MCC2	Minimum TM Overplot of Via4	0.50
MCC3	Minimum Space TM to Via4	0.50
MCC4	Minimum Metal 4 Overplot of TM	1.00
MCC5	Minimum Space TM to TM	0.80
MCC9	Minimum via4 to via4 space on TM (for TM area > 400um^2)	3.50
MCC9.a	Minimum via4 to via4 space on TM (for TM area < 400um^2)	1.00
MCC10	Maximum via4 to via4 space on TM	4.50
MCC11	Minimum space capacitor TM to via3 (No Via3 is allowed below TM layer)	0.50
MCC21	Minimum Analog block border (layer 95) overplot of TM*	2.00

* Not shown in illustration MCC
Note 2: For best matching results it is recommended that a minimum via3 to TM space of 2.0 um be maintained.

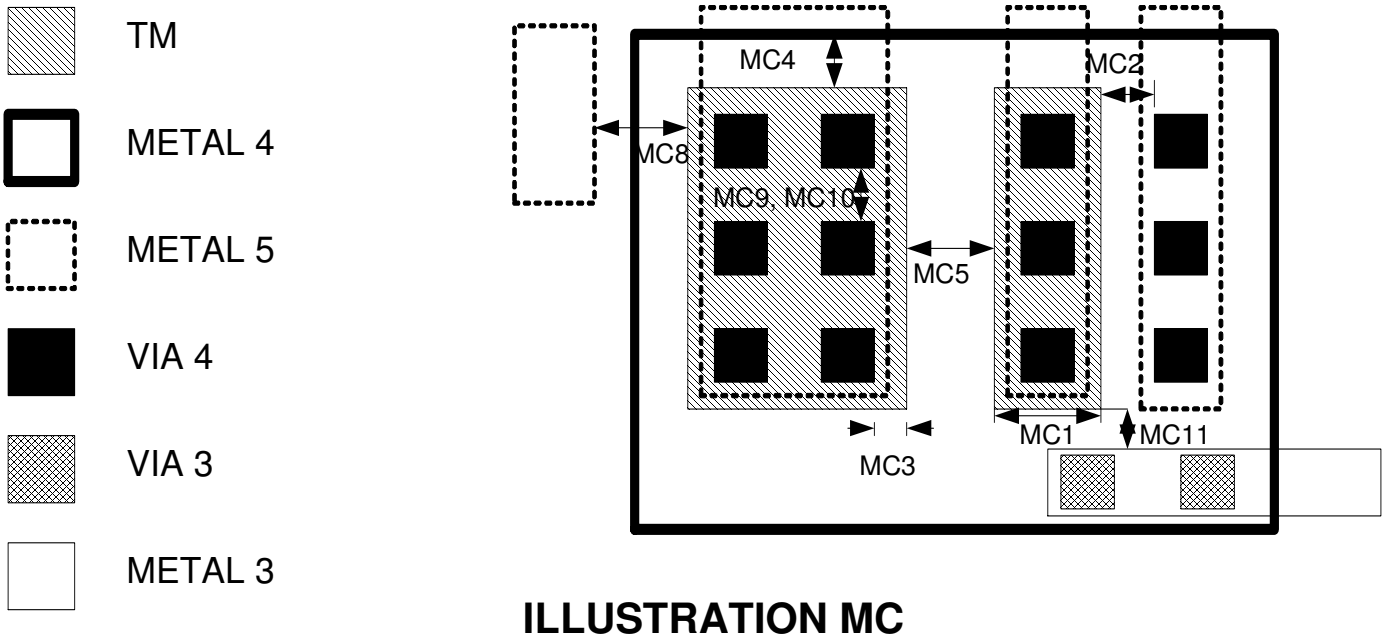


ILLUSTRATION MC

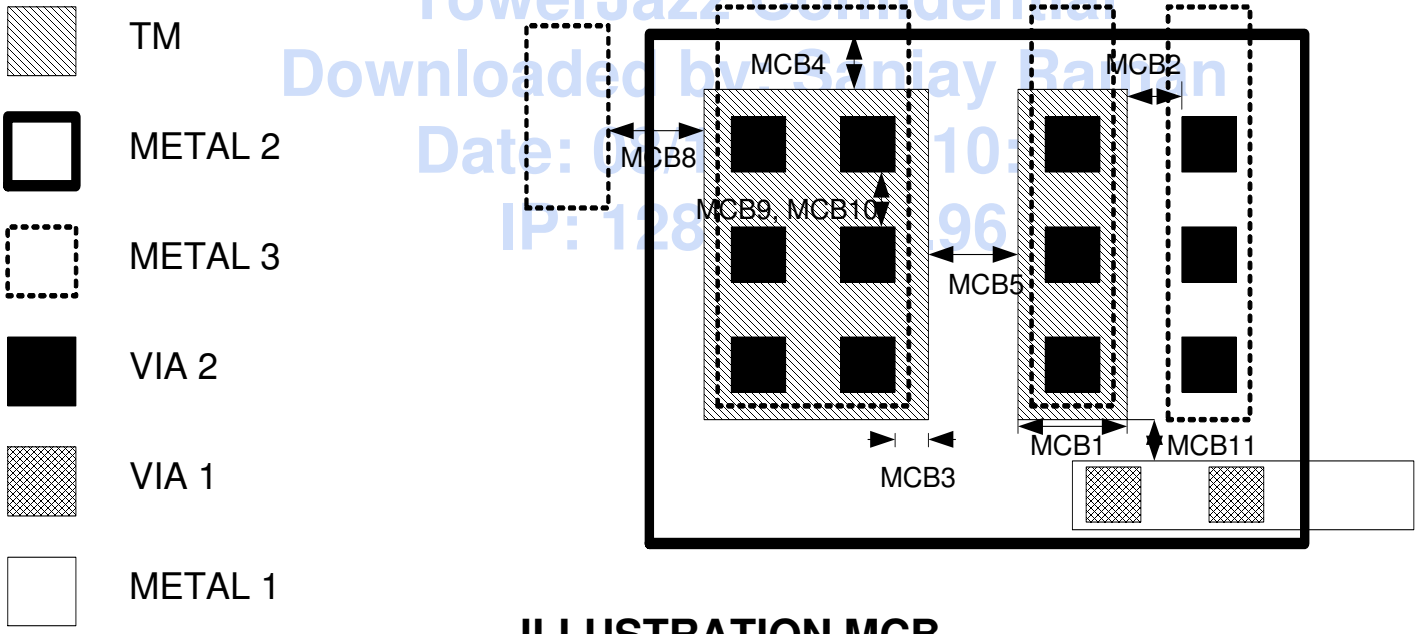


ILLUSTRATION MCB

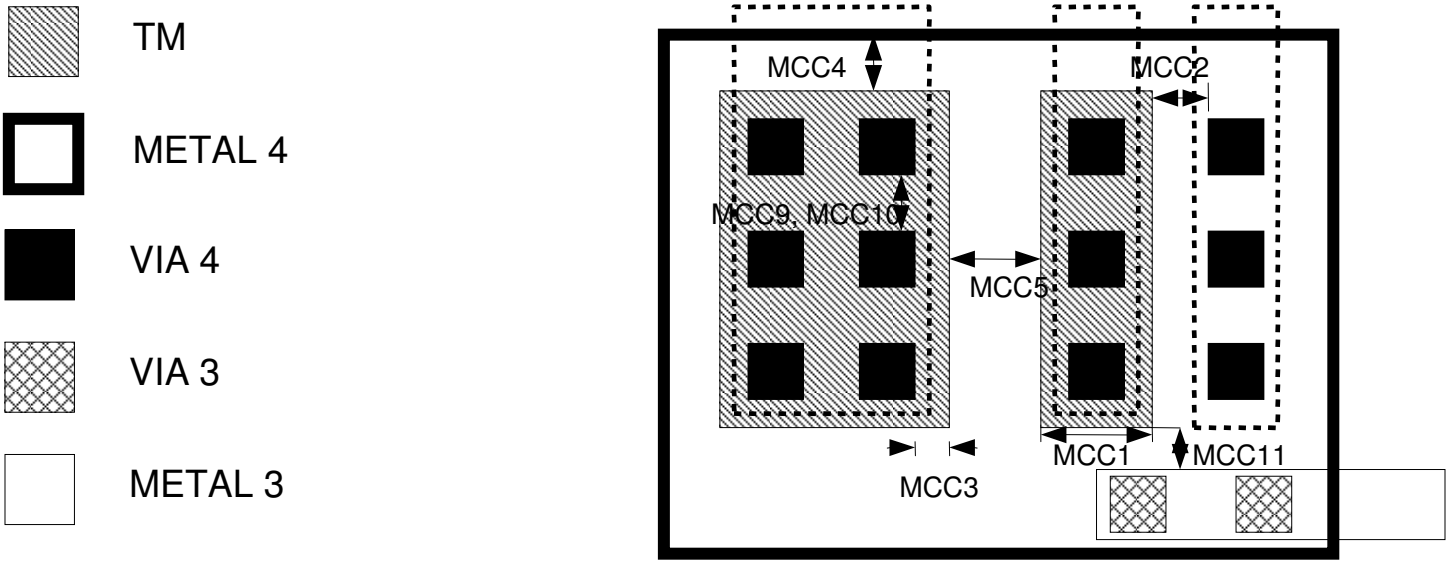
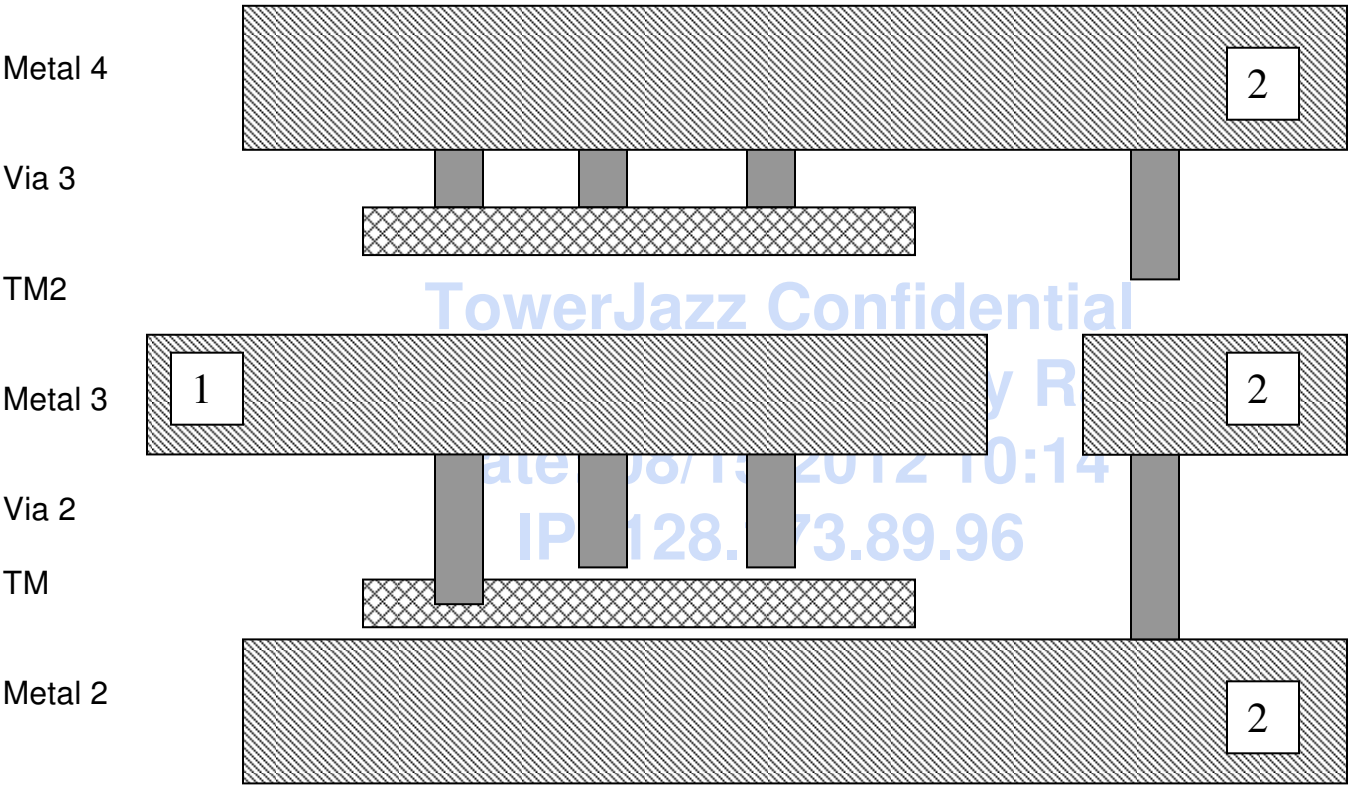


ILLUSTRATION MCC

5.4.4 Rules of 4fF/μm^2 density Stacked Metal-Insulator-Metal capacitor for SBC18PT, SBC18QW only

This defines high unit area capacitor structures (Stacked MIM caps) fabricated using metal 2 (Layer 18) as the lower plate and top capacitor metal (TM, layer 22) as the upper plate of the bottom capacitor of the stacked capacitor and metal 3 (Layer 28) as the lower plate and top capacitor 2 metal (TM2, layer 30) as the upper plate of the upper capacitor of the stacked capacitor. Layer TM is connected to lower plate Metal 3 by an array of Via 2 ‘s and is one node of the capacitor (See Node 1 in the schematic below). Lower plate M2 is connected to related metal 4 (metal 4 connected to TM2 by an array of Via3) and is the second node of the capacitor (See Node 2 in the schematic below).



Schematic of the Stacked 4fF/um2 MIM capacitor

See Illustration SMC

Layer 22 and layer 30 are positive masks. Layer 30 is the additional mask layer needed in stacked MIM capacitors versus regular MIM capacitors between Metal 2 and TM. The stacked 4fF/μm^2 MIM capacitors have to be covered by marking layer 70.

Rule No.	Rule Name	SBC18PT SBC18QW only
SMC1	Minimum TM width/length	1.50
SMC2	Minimum TM Overplot of Via2	0.50
SMC3	Minimum Space TM to Via2	0.50
SMC4	Minimum Metal 2 Overplot of TM	1.00
SMC5	Minimum Space TM to TM	0.80
SMC9	Minimum via2 to via2 space on TM (for TM area > 400um^2)	3.50
SMC9.a	Minimum via2 to via2 space on TM (for TM area < 400um^2)	1.00
SMC10	Maximum via2 space on TM in X and Y direction.	4.50
SMC11	Minimum TM2 width/length	1.50
SMC12	Minimum TM2 Overplot of Via3	0.50
SMC13	Minimum Space TM2 to Via3	0.50
SMC14	Minimum Metal 3 Overplot of TM2	1.00
SMC15	Minimum Space TM2 to TM2	0.80
SMC19	Minimum via3 to via3 space on TM2 (for TM2 area > 400um^2)	3.50
SMC19.a	Minimum via3 to via3 space on TM2 (for TM2 area < 400um^2)	1.00
SMC20	Maximum via3 space on TM2 in X and Y direction.	4.50
SMC21	Minimum Analog block border (layer 95) overplot of TM2*	2.00
SMC22	Minimum space capacitor TM to via1 (No Via1 is allowed below TM layer)	0.50
SMC23	TM2 is allowed only in stacked MIM configuration and TM2 must be coincident with TM. (Note: Standalone capacitor using layers M3 and TM2 is not allowed)	
SMC24	Capacitor bottom plate metal 2 must be connected with related metal 4 (metal 4 connected to TM2	

* Not shown in illustration SMC

TM, TM2

METAL 4

VIA 3

METAL 3

VIA 2

METAL 2

VIA 1

METAL 1

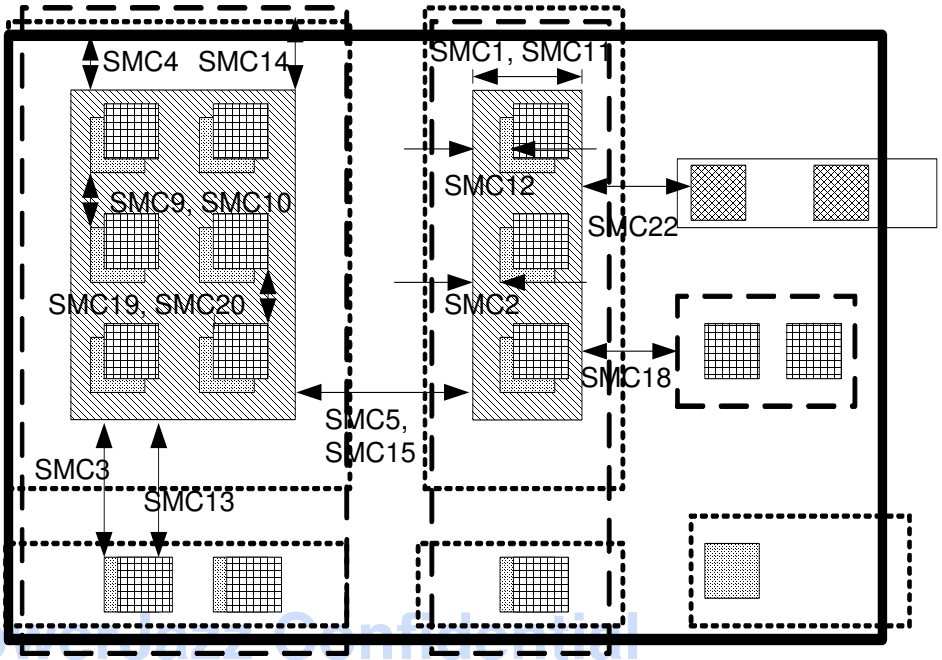
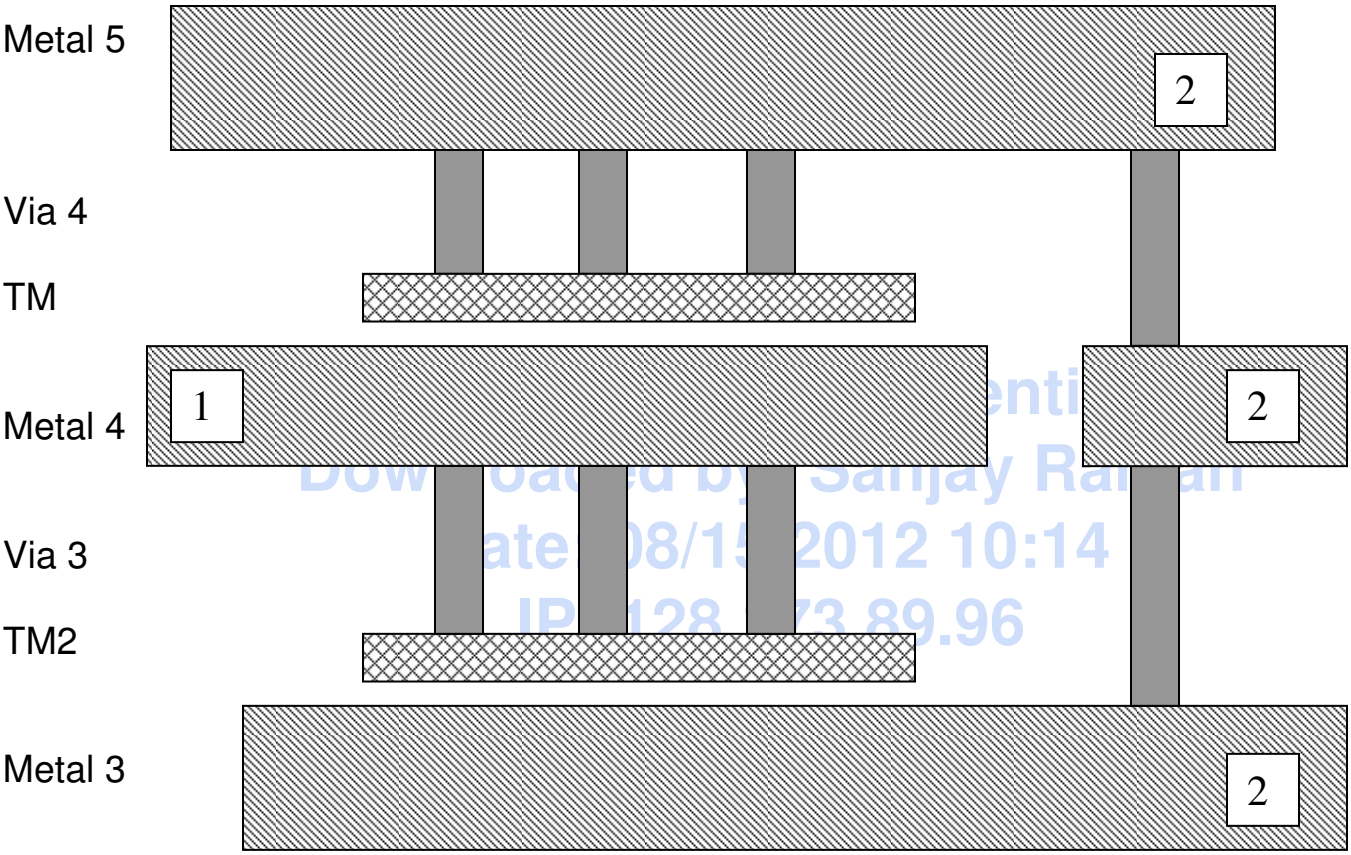


ILLUSTRATION SMC

5.4.5 Rules of 5.6fF/μm2 density Stacked Metal-Insulator-Metal capacitor for SBC18HA

This defines high unit area capacitor structures (Stacked MIM caps) fabricated using metal 3 as the lower plate and top capacitor 2 metal (TM2) as the upper plate of the bottom capacitor of the stacked capacitor and metal 4 as the lower plate and top capacitor metal (TM) as the upper plate of the upper capacitor of the stacked capacitor. Layer TM2 is connected to lower plate Metal 4 by an array of Via 3 ‘s and is one node of the capacitor (See Node 1 in the schematic below). Lower plate M3 is connected to related metal 5 (metal 5 connected to TM by an array of Via4) and is the second node of the capacitor. See Node 2 in the schematic below.



Schematic of the Stacked 5.6fF/um^2 MIM capacitor

See Illustration SMH

Layer 22 and layer 30 are positive masks. Layer 30 is the additional mask layer needed in stacked MIM capacitors versus regular MIM capacitors between Metal 4 and TM. The stacked 5.6fF/μm^2 MIM capacitors have to be covered by marking layer 70.

Rule No.	Rule Name	SBC18HA only
SMH1	Minimum TM width/length	1.50
SMH2	Minimum TM Overplot of Via4	0.50
SMH3	Minimum Space TM to Via4	0.50
SMH4	Minimum Metal 4 Overplot of TM	1.00
SMH5	Minimum Space TM to TM	0.80
SMH9	Minimum via4 to via4 space on TM (for TM area > 400um^2)	3.50
SMH9.a	Minimum via4 to via4 space on TM (for TM area < 400um^2)	1.00
SMH10	Maximum via4 space on TM in X and Y direction.	4.50
SMH11	Minimum TM2 width/length	1.50
SMH12	Minimum TM2 Overplot of Via3	0.50
SMH13	Minimum Space TM2 to Via3	0.50
SMH14	Minimum Metal 3 Overplot of TM2	1.00
SMH15	Minimum Space TM2 to TM2	0.80
SMH19	Minimum via3 to via3 space on TM2 (for TM2 area > 400um^2)	3.50
SMH19.a	Minimum via3 to via3 space on TM2 (for TM2 area < 400um^2)	1.00
SMH20	Maximum via3 space on TM2 in X and Y direction.	4.50
SMH21	Minimum Analog block border (layer 95) overplot of TM2*	2.00
SMH22	Minimum space capacitor TM2 to via2 (No Via2 is allowed below TM2 layer)	0.50
SMH23	TM2 is allowed only in stacked MIM configuration and TM2 must be coincident with TM. (Note: Standalone capacitor using layers M3 and TM2 is not allowed)	
SMH24	Capacitor bottom plate metal 3 must be connected with related metal 5 (metal 4 connected to TM2)	

* Not shown in illustration SMH

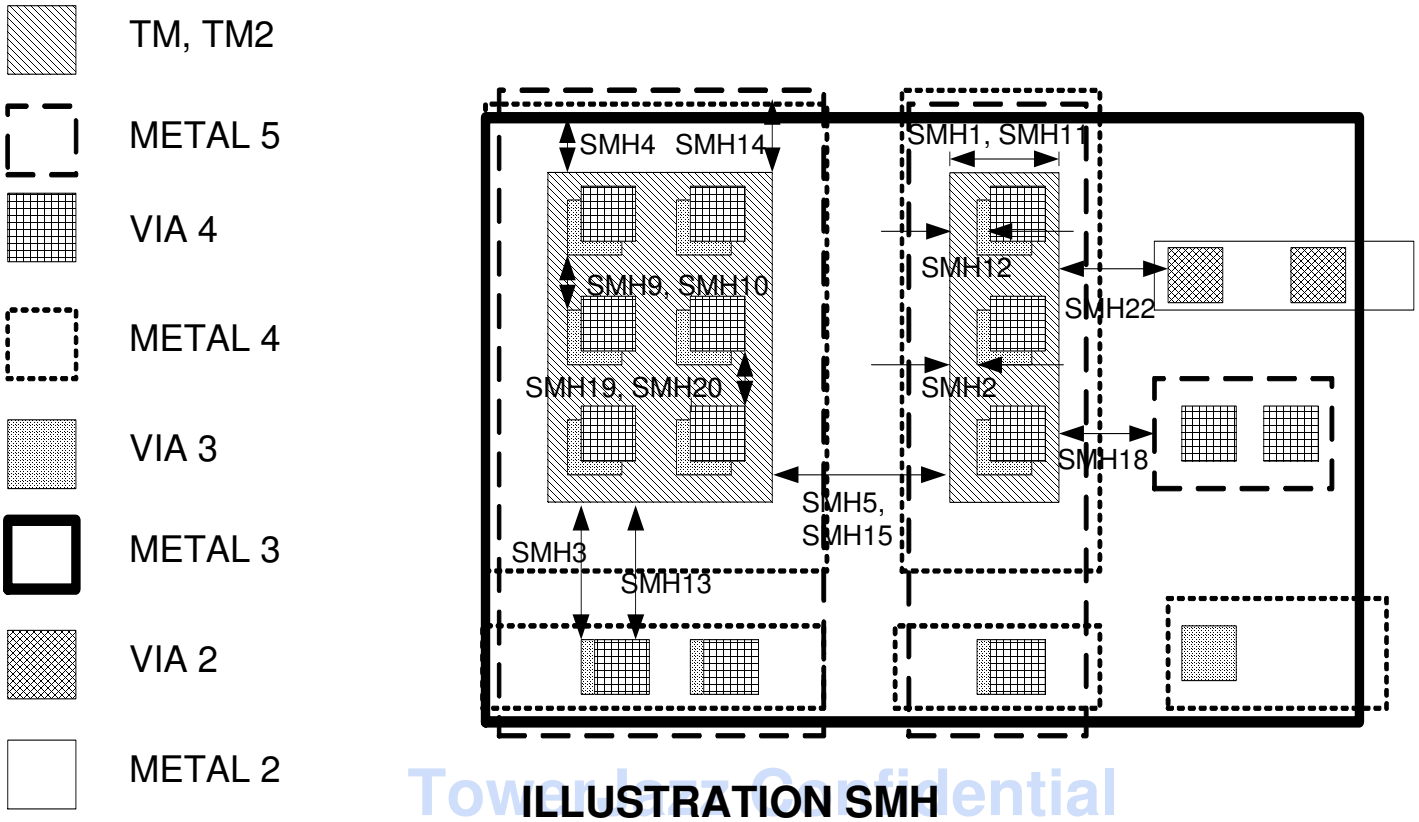


ILLUSTRATION SMH

5.5 Varactor Rules

5.5.1 High Performance Junction Varactor

Applicable to SBC18HX, SBC18HXL, SBC18HA, SBC18PT, SBC18QTD, SBC18QTR, SBC18QTL, SBC18MV, SBC18MWD processes only.

The layout of high performance junction varactor diodes should follow the rules below in order to obtain devices with low series resistance and high Q. This varactor is a multi-finger P/N diode in the form of N(PN…PN). The P+ active region is formed using the varactor implant (cascaded p+/n implant) on active on N- epi. The N+ cathode region is formed by collector sinker implant on active connected to buried layer. See Illustration VAR.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA, SBC18PT, SBC18QTD, SBC18QTR, SBC18QTL, SBC18MWD, SBC18MV only
VAR.1	Minimum/Maximum Varactor implant overplot of anode active	0.15
VAR.2	Minimum Spacing P+ active to Sinker active edge	0.9
VAR.3	Minimum/Maximum P+ active width (recommended width 1.4um)	0.5/10
VAR.4	Minimum/Maximum P+ active length**	20/50
VAR.5	Minimum Sinker active width (NPN rule B9)	0.89
VAR.6	Minimum/Maximum Sinker active length (must be equal to P+ active)**	20/50
VAR.7	Minimum/Maximum Collector Sinker implant overplot of Sinker active (NPN rule B8)	0.15
VAR.9	Minimum/Maximum Substrate contact ring (must be present) space to Nwell2**	1.5/2.0
VAR.10	Minimum/Maximum buried layer overplot of the outermost active	1.8
VAR.12	Minimum/Maximum Nwell-2 overplot of of the outermost active	1.8
VAR.19	Minimum Analog block border (layer 95) overplot of Nwell2 layer enclosing varactor fingers**	1.00
VAR.20	Minimum width of layer 13	0.5
VAR.21	Minimum space layer 13 to layer 13	0.7

Rules B.24, B.25, B.26, B.27, B.28, B.32 in Section 5.1 are applicable for this varactor. See Note 3 in section 5.1.

** not shown below

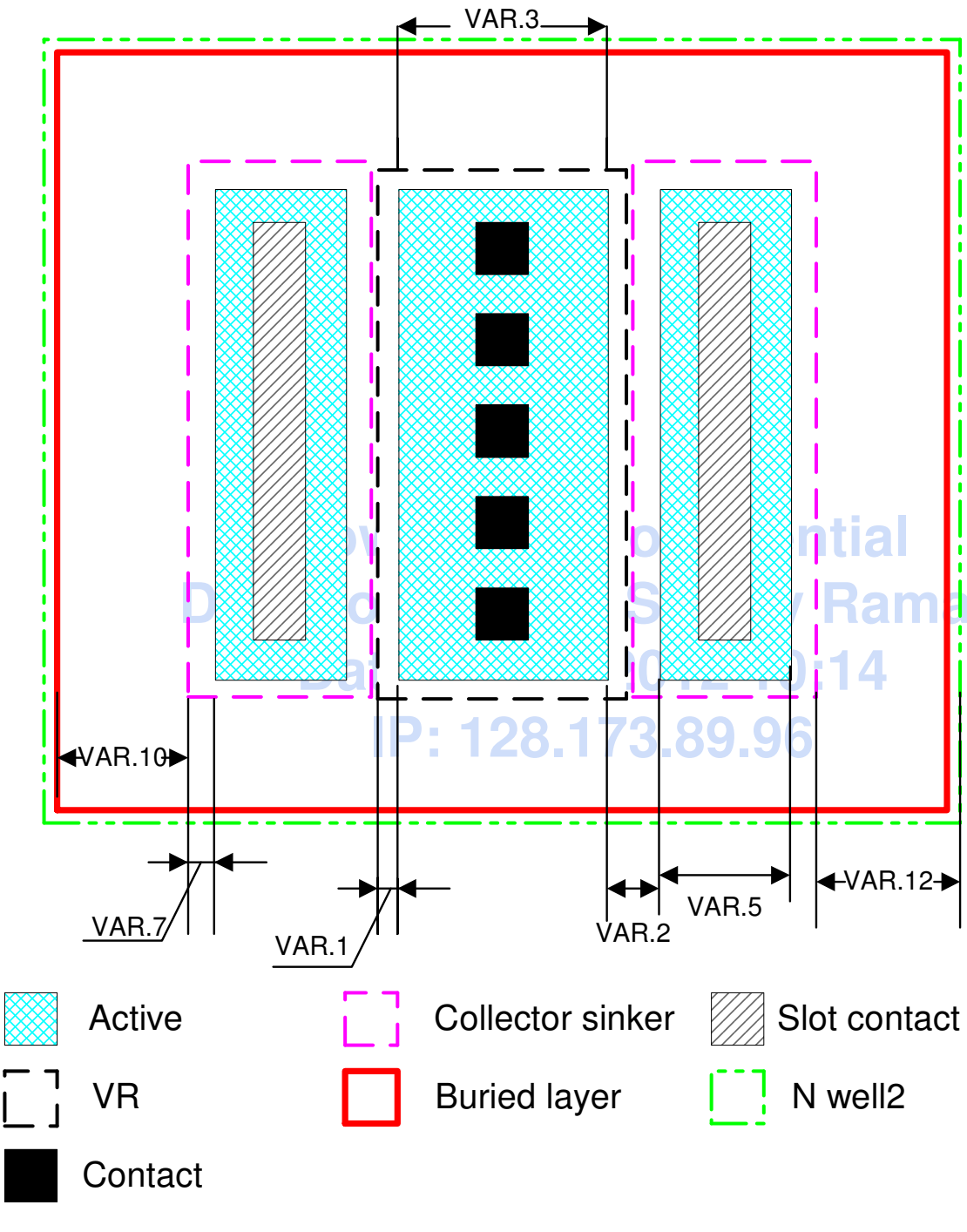


ILLUSTRATION VAR

5.5.2 p+/Nwell Junction Varactor

Applicable to SBC18MW, SBC18QW processes only

The layout of varactor diodes should follow the rules below in order to obtain devices with low series resistance and high Q. SBC18 varactor is a multi-finger P+/N diode in the form of N(PN…PN). See Illustration VR. This varactor does not require any additional varactor implant mask such as the VR mask for the high performance varactor (see previous section).

Rule No.	Rule Name	SBC18QW, SBC18MW only
VR.A	Minimum n+ implant overplot of n active	0.02
VR.B	Minimum spacing n+ implant to p+ active edge	0.26
VR.C	Minimum p+ implant overplot of p active	0.18
VR.D	Minimum spacing p+ implant to n+ active edge	0.10
VR.E	Recommended minimum/maximum anode width for High Q Varactor	1.40
VR.F	Nwell overplot of active for varactors	3.00
VR.G	Maximum anode length for Varactor	30
VR.H	The varactor must be enclosed by varactor marking layer (layer 107)	
VR.I	The varactor must be enclosed by analog block border (layer 95)	
Note	Anodes (P+ IMPLANT) should have N+ on both sides	
Note	Use minimum active spacing for high Q varactors. (s=0.28)	

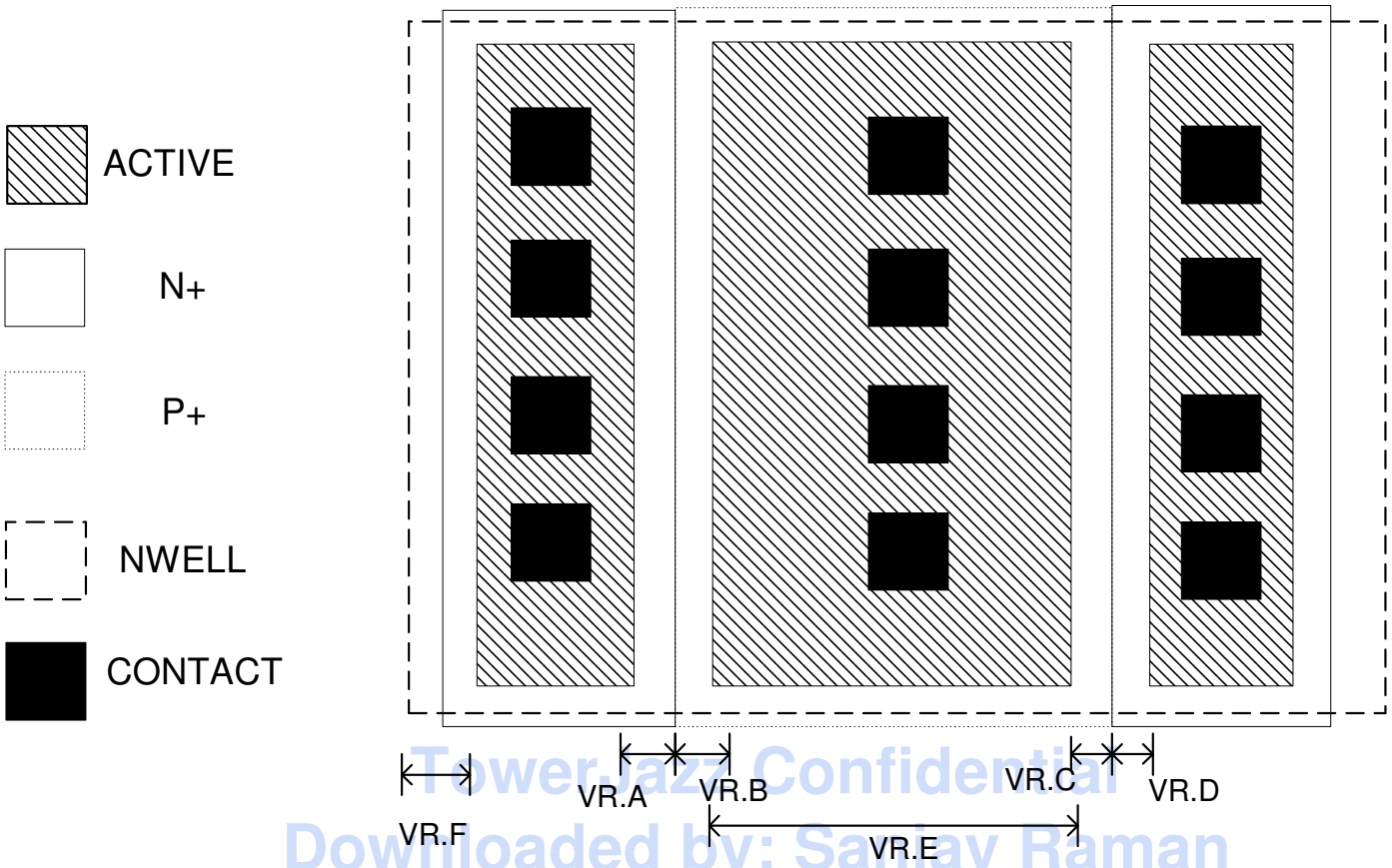


ILLUSTRATION VR

5.5.3 MOS Varactor

Applicable to SBC18PT, SBC18HX, and SBC18HXL, SBC18HA processes only

SBC18 MOS varactor is an array of fixed size capacitors. The MOS varactors have to be covered with varactor marking layer (layer 107). This device is available for SBC18PT, SBC18HX, and SBC18HXL processes only.

Note: This device is applicable for thin gate oxide only

Rule No.	Rule Name	SBC18PT, SBC18HXL, SBC18HX, SBC18HA only
MVAR.1.A	Minimum Gate length	0.5
MVAR.1.B	Maximum Gate length	2.0
MVAR.2.A	Minimum Active width	2.0
MVAR.2.B	Maximum Active width	4.0
MVAR.3	Minimum/Maximum spacing of gate to field edge	0.7
MVAR.4	Minimum NI overplot of active	0.18
MVAR.5	Minimum/Maximum N-well extension from active (along gate length)	0.18
MVAR.6	Minimum/Maximum N-well extension from active (along active width)	0.53
MVAR.7	Minimum/Maximum distance of active contact to gate poly	0.34
MVAR.8	Minimum/Maximum distance of gate contact to active edge	0.21
MVAR.9	Minimum/Maximum width of metal 1 contacted to active	0.5
MVAR.10	Minimum width of metal 1 contacted to gate	0.44
MVAR.11	Minimum/Maximum active spacing between slices (not shown)	0.64
MVAR.12	Minimum/Maximum gate poly spacing between fingers (not shown)	0.9
MVAR.13	DG layer (for thick gate oxide) must not be present within varactor marking layer	

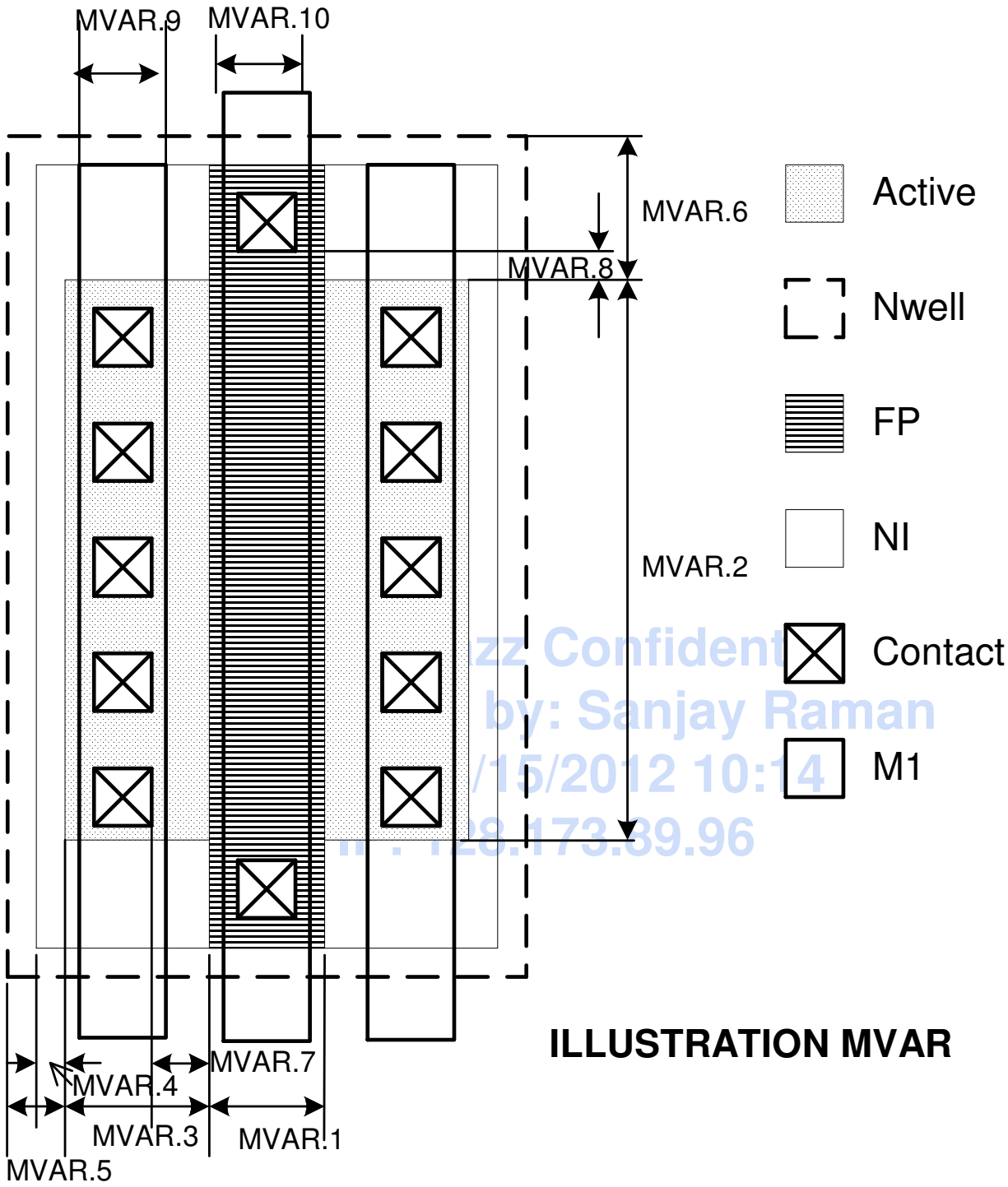


ILLUSTRATION MVAR

5.6 Metal Fuse Rules

These metal fuse design rules are for SBC18 process to trim analog designs. For a N metal layer process, the "fuse metal" is chosen to be metal N-2 layer. The fuses consist of metal 4 for SBC18HX, SBC18HXL, SBC18HA processes, metal 3 for SBC18PT process and metal 2 for SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW processes. The fuse metal is connected to metal N-1 through Via N-2 an subsequently to metal N through ViaN-1. The fuses are marked by fuse marking layer (46) and analog marking layer (95) with 10um overplot. Metal and via overplot rules for analog and RF should be followed. These fus are designed to be programmed with a 5ms 3V (500mA compliance) pulse. See figure MF1.

Rule No.	Rule Name	
MF.A	Fuse metal width (direction perpendicular to current flow)	1.0
MF.B	Fuse metal length (direction parallel to current flow)	5.0
MF.C	Minimum fuse metal shunt fanout length	4.35
MF.D	Minimum fuse metal connection width	9.7
MF.E	Minimum space metal N-1 or metal N to fuse metal edge	4.7
MF.F	Minimum number of via N-2 for fuse metal to metal N-1 fuse connection per termination	40
MF.G	Minimum number of via N-1 for metal N-1 to top metal (metal N) fuse connection per termination	40
MF.H.a	Minimum width of metal N-1 connected to fuse metal	9.7
MF.H.b	Minimum width of metal N connected to fuse metal	9.7
MF.I	Fuse edge must be identified (metal fuse marking layer 46)	
MF.J	Minimum width of fuse metal or metal N-1 or metal N from fuse pad to internal circuitry.	3.0
MF.K	Minimum space fuse edge to unrelated metal 1, metal 2, metal 3, metal 4, metal 5, metal 6, TM or TR	10
MF.L	Minimum space fuse edge to Nwell, active or poly	10
MF.M	Fuse Metal must be metal N-2 layer	

Note: Pads used for fuse programming must follow the bonding pad rules specified in this document. However, if pads are used exclusively for fuse programming and are not bonded out, they do not need to follow rule BD.N.

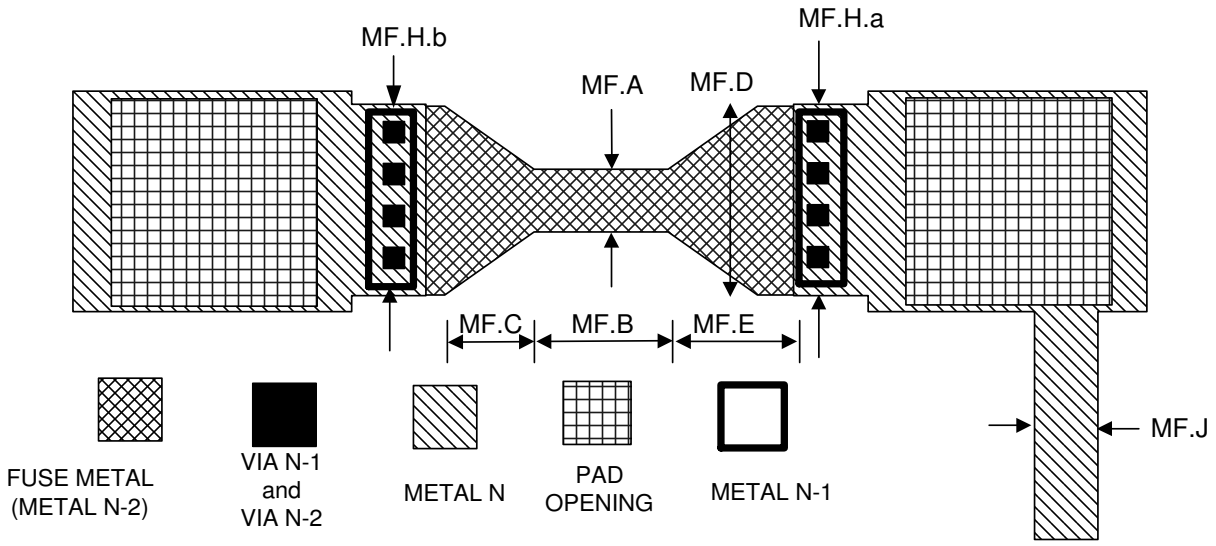


ILLUSTRATION MF1

5.7 Inductors and Baluns

All inductors and baluns must be covered with inductor marking layer (layer 51). Layer 51 is used during layer generation to prevent metal fill from being generated near inductors per the following.

Rule No.	Rule Name	
51.A	IML overplot of Inductors.	5.00
51.B	Minimum space IML to unrelated active, poly, metals, TR, TM and TM2.	25.00

Note 1: Analog block layer (ABLB, layer 95) must be drawn around inductors and baluns in addition to layer 51.

Note 2: Dummy active fill is generated below the inductors as described in Section 4.1.

5.8 Schottky Diode Rules

Applicable to SBC18QTR process only

The layout of the Schottly Diode should follow the rules below. This is an unimplanted silicided active to n- epi junction Schottky Diode. The N+ cathode region is formed by collector sinker implant on active connected to buried layer. See Illustration SCHOTTKY

Rule No.	Description	SBC18QTR
SD.1	Minimum P+ implant overplot of active (inside active)	0.38
SD.2	Minimum overlap silicide block to active (inside active)	0.18
SD.3	Minimum space sinker active to diode active	0.6
SD.4	Minimum/Maximum width of silicide block	0.56
SD.5	Schottky Diode marking layer 106 must extend to cover deep trench	
SD.6	Sinker actives must be electrically connected	

Rules B18, B16, B14, B13, B12 in Section 5.1 are also applicable for this Schottky Diode.

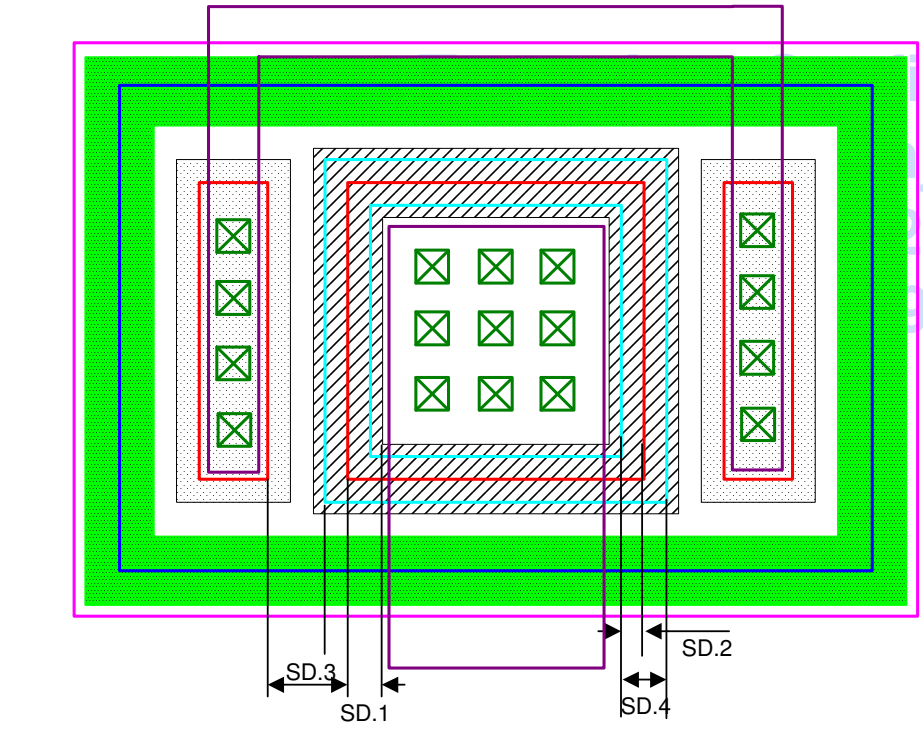
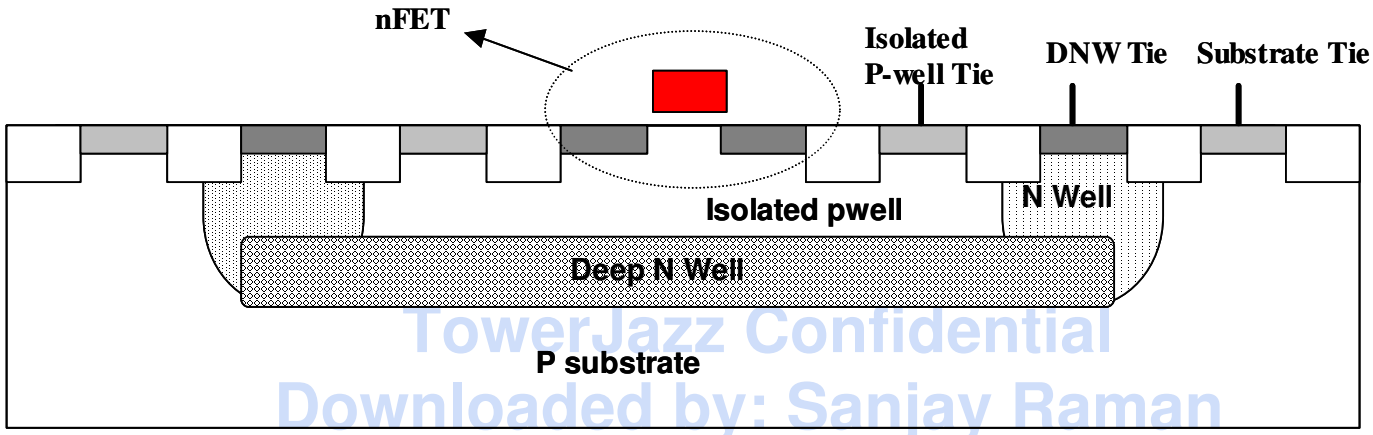


ILLUSTRATION SCHOTTKY

5.9 Triple Well for SBC18HXL, SBC18HA, SBC18QTL only)

The triple well process consists of an additional deep nwell layer using an additional N implant masking step in the p-substrate region. The deep nwell is surrounded by nwell. In this manner, an nFET can be isolated by the triple well consisting of deep nwell and surrounding nwell. In addition, the isolated pwell inside can be biased separately than the common psubstrate outside. See Illustrayion DNW.

The Deep N-well (DNW) mask, layer 36, is used to define the extents of the deep n well region. It is a negative mask and aligns to the buried layer. Isolated pwell by the Deep nwell/nwell can be biased separately using p+ taps. The substrate tie is located outside the deep nwell.



When the triple well process option is available, the DNW layer can be drawn around a circuit block or an element. This allows a different bias to be applied to the isolated pwell than the bias applied to the p-substrate. Inside the drawn DNW layer, the verification rules of the triple well process are implemented for DRC and LVS.

During schematic entry, the triple well may be implemented by specifying or wiring a secondary substrate net that is different from the local substrate. Any required biasing may then be applied to the secondary net that is different from the bias applied to the local substrate.

Rule No.	Rule name	SBC18HXL, SBC18HA, SBC18QTL only
DNW.1	Minimum width of DNW	3.0
DNW.2	Minimum space between DNW	10.0
DNW.3	Minimum NW extension into the DNW	2.0
DNW.4	Minimum/Maximum NW extension out of the DNW (modelling boundary)	2.5
DNW.5	Minimum spacing of physically unrelated NW to DNW	6.0
DNW.6	DNW must be surrounded by NW	
DNW.7	A p+ tie must exist for each isolated pwell	
DNW.8	Each DNW extent must be connected to a n+ tie through its surrounding nwell	
DNW.9	Minimum space DNW to nwell2 layer, pcell marking layer, Ncell marking layer, varactor marking layer, bjtdev (vertical pnp) marking layer	6.0
DNW.11	NPN, PNP, Junction Varactors, MOS Varactor, Nwell Resistor, MOSCAP, Inductors, and Schottky diode devices as well as buried layer are not allowed within and up to 6um of DNW	
DNW.16	Deep Trench (layer 41) is not allowed to intersect DNW	
DNW.17	Analog Marking layer is not allowed to straddle DNW	
DNW.20	Latchup rule – Maximum space in X or Y directions between any point in an N+ active diffusion and its nearest isolated pwell p+ tie	10.0
DNW.21	Latchup rule – A substrate tie of > 0.25um^2 must be placed directly between an Nwell and any Nfet gate within 10um of the Nwell	

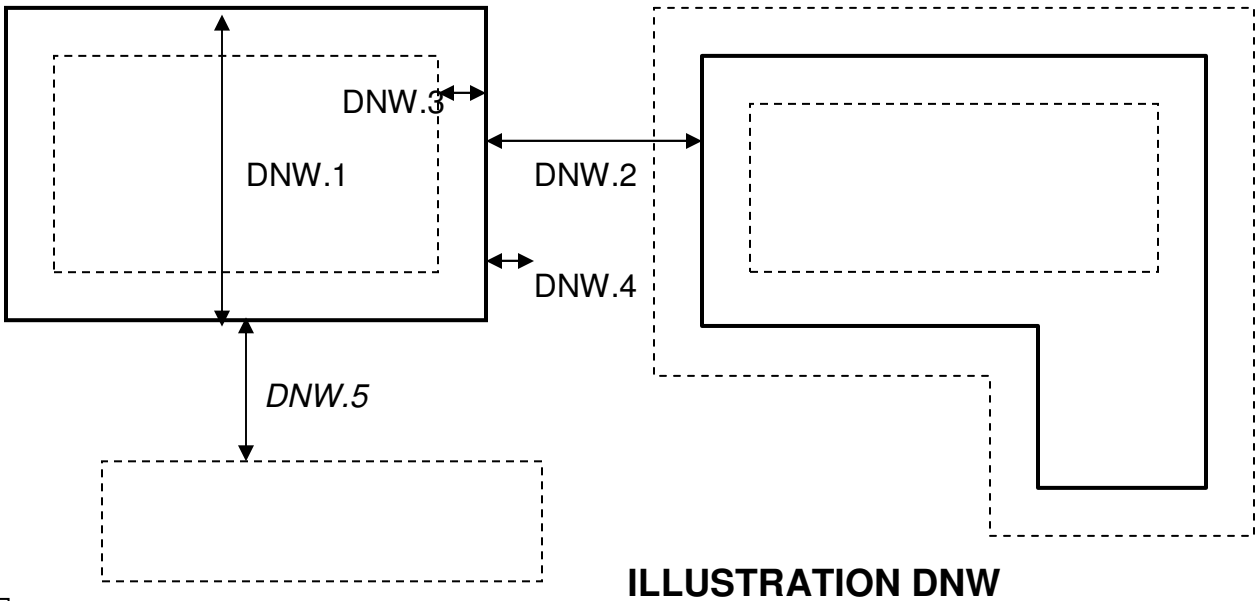


ILLUSTRATION DNW

Deep Nwell

Nwell

5.10 Metal Pin layer rules

These rules are applicable for the metal Pin layers

Rule No.	Rule Name
8.Pin	Metal 1 Pin layer must be covered by metal 1 drawing layer
18.Pin	Metal 2 Pin layer must be covered by metal 2 drawing layer
28.Pin	Metal 3 Pin layer must be covered by metal 3 drawing layer
38.Pin	Metal 4 Pin layer must be covered by metal 4 drawing layer
48.Pin	Metal 5 Pin layer must be covered by metal 5 drawing layer
58.Pin	Metal 6 Pin layer must be covered by metal 6 drawing layer

5.11 Metal overplot of contacts and vias for RF and Analog sections (Inside the Layer ABLB 95 region)

These rules assure consistent low resistance contacts/vias for analog and RF designs.

Rule No.	Rule Name	SBC18HX, SBC18HXL SBC18HA	SBC18PT,	SBC18QTD, SBC18QTL, SBC18QTR, SBC18QW	SBC18MW, SBC18MWD, SBC18MV
OP.A	Metal 1 overplot of contact	0.07 µm	0.07 µm	0.07 µm	0.07 µm
OP.B	Metal 1 overplot of via	0.07 µm	0.07 µm	0.07 µm	0.07 µm
OP.C	Metal 2 overplot of via	0.07 µm	0.07 µm	0.15 µm	0.15 µm
OP.D	Metal 2 overplot of via2	0.07 µm	0.07 µm	0.15 µm	0.15 µm
OP.E	Metal 3 overplot of via2	0.07 µm	0.07 µm	0.15 µm	0.35 µm
OP.F	Metal 3 overplot of via3	0.07 um	0.35 um	0.35 um	
OP.G	Metal 4 overplot of via3	0.1 µm	0.35 µm	0.35 µm	
OP.H	Metal 4 overplot of via4	0.35 µm	0.35 µm		
OP.I	Metal 5 overplot of via4	0.35 µm	0.35 µm		
OP.J	Metal 5 overplot of via5	0.35 µm			
OP.K	Metal 6 overplot of via 5	0.35 µm			
M1A	Minimum Metal 1 area	0.30 μm^2	0.30 μm^2	0.30 μm^2	0.30 μm^2
M2A	Minimum Metal 2 area	0.34 μm^2	0.34 μm^2	0.32 μm^2	0.32 μm^2
M3A	Minimum Metal 3 area	0.34 μm^2	0.34 μm^2	0.32 μm^2	6.25 μm^2
M4A	Minimum Metal 4 area	0.56 μm^2	1.44 μm^2	6.25 μm^2	
M5A	Minimum Metal 5 area	1.44 μm^2	6.25 μm^2		
M6A	Minimum Metal 6 area	6.25 μm^2			

5.12 Metal Dummy Resistor Rules

These rules are applicable for the metal dummy resistor layers of datatype 5. The dummy resistor enables a net to be attached to multiple net names for LVS purpose.

Rule No.	Rule Name
8.R.1, 18.R.1, 28.R.1, 38.R.1, 48.R.1, 58.R.1	Metal dummy resistor layer must be a rectangle
8.R.2, 18.R.2, 28.R.2, 38.R.2, 48.R.2, 58.R.2	Metal dummy resistor layer (datatype 5) must be completely inside the drawn metal (datatype 0)
8.R.3, 18.R.3, 28.R.3, 38.R.3, 48.R.3, 58.R.3	Two edges of metal dummy resistor layer (datatype 5) must be coincident with drawn metal (datatype 0)

Note: The area of the metal dummy resistor must be as small as possible for accurate parasitic extraction. Parasitic capacitance extraction is excluded in regions with dummy metal resistor layer.

Note: The dummy metal resistor is documented here but has not been implemented in August 2004 kit release. It will be implemented in the next kit release.

5.13 Miscellaneous Rules

Additional rules checked in different processes are listed below

Rule No.	Rule Description	sbc18hx	sbc18hxl	Sbc18ha	sbc18pt	sbc18pth	sbc18qtd	sbc18qtl	sbc18qtr	sbc18qw	sbc18mtv	sbc18mv	sbc18mw	sbc18mwd
R.ARTF	data straddling over artifact layer	x	x	X	X	x	x	x	x	x	x	x	x	x
16.Bad.1	Layer not supported by process variant						x	x	x	x	x	x	x	x
61.Bad.1	Layer 61 not supported by process variant						x	x	x	x	x	x	x	x
5.fill	poly fill layer not coinciding with poly polygon	x	x	X	X	x	x	x	x	x	x	x	x	x
6.X1	N+/P+ Implants overlap on field	x	x	X	X	x	x	x	x	x	x	x	x	x
6.X2	N+/P+ Implants overlap on active	x	x	X	X	x	x	x	x	x	x	x	x	x
8.fill	met1 fill layer not coinciding with met1 polygon	x	x	X	X	x	x	x	x	x	x	x	x	x
18.fill	met2 fill layer not coinciding with met2 polygon	x	x	X	X	x	x	x	x	x	x	x	x	x
28.fill	met3 fill layer not coinciding with met3 polygon	x	x	X	X	x	x	x	x	x	x	x	x	x
37.Bad	via3 not supported by process variant										x	x	x	x
38.fill	met4 fill layer not coinciding with met4 polygon	x	x	X	X	x	x	x	x	x				
38.Bad	met4 not supported by process variant										x	x	x	x
47.Bad	via4 not supported by process variant						x	x	x	x	x	x	x	X
48.fill	met5 fill layer not coinciding with met5 polygon	x	x	X	X	x								
48.Bad	met5 not supported by process variant						x	x	x	x	x	x	x	X
57.Bad	via5 not supported by process variant				X	x	x	x	x	x	x	x	x	X
58.fill	met6 fill layer not coinciding with met6 polygon	x	x	X										
58.Bad	met6 not supported by process variant				X	x	x	x	x	x	x	x	x	X

Rule No.	Rule Description	sbc18hx	sbc18hxl	Sbc18ha	sbc18pt	sbc18pth	sbc18qtd	sbc18qtl	sbc18qtr	sbc18qw	sbc18mtv	sbc18mv	sbc18mw	sbc18mwd
DNW.Bad	Badly drawn deep nwell structure		x	X		x		x						
DNW.Bad	Deep nwell not supported by process variant	x			X		x		x	x	x	x	x	x
B.note	High speed bjt is not supported				X	x	x	x	x	x	x	x	x	X
VAR.Bad	process does not support Varactor_bl									x			x	
VR.Bad	process does not support Junction Varactor	x	x	X	X	x	x	x	x		x	x		x
MVAR.Bad	process does not support MOS Varactor						x	x	x	x	x	x	x	x
VP.Bad	process does not support high performance vertical pnp	x	x	X	X	x	x	x	x	x	x	x	x	x
SD.Bad	process does not support Schottky diode	x	x	X	X	x	x	x		x	x	x	x	x
HV.Bad	high voltage fets not supported by process variant	x	x	X	X	x	x	x	x		x	x	x	x
MR.BAD	Non-rectangular TR; TR with no via	x	x	X					x					
MR.BAD	process does not support metal resistor				X	x	x	x		x	x	x	x	x
HR.Bad	high-value poly res not supported by process variant	x	x											
MC.bad	Cap via, TM without top/bottom metal	x	x	X	X	x	x	x	x	x	x	x	x	x
MC_Bad_2fF_cap	Bad 2fF cap- topmm not covered by mim2 marking layer			X	X	x	x	x	x	x	x	x	x	x
MC_Bad_1fF_cap	Bad 1fF cap- topmm covered by mim2 marking layer	x	x											
SMC_Bad_2fF_cap	Bad 2fF cap- topmm not covered by mim2 marking layer			X	X	x				x				
SMC.Bad	process does not support TM2	x	x				x	x	x		x	x	x	x
MF.Bad	fuse marking layer not on metal N-2	x	x	X	X	x	x	x	x	x				
MF.Bad	process not supporting fuse										x	x	x	x

R.ABLB	ablb MUST TOUCH tm, sblk, lpnp, ind_mrk, n_cell layers	x	x	X	X	x	x	x	x	x	x	x	x	x
ptap_no_contact	Bad Ptap- missing contacts	x	x	X	X	x	x	x	x	x	x	x	x	X
ntap_no_contact	Bad Ntap- missing contacts	x	x	X	X	x	x	x	x	x	x	x	x	X
SRAM.bad *	Not using Jazz supplied SRAM	x	x	X	X		x	x	x	x		x	x	X

* Not checked

Rule No.	Rule Description
BAD_npn.01	Improper Bipolar layout- N_CELL does not enclose buried layer
BAD_npn.02	Improper Bipolar layout- N_CELL does not enclose nwel2
BAD_npn.03	Improper Bipolar layout- npn nwel2 does not enclose buried layer
BAD_npn.04	Improper Bipolar layout- npn buried layer does not enclose spacer clear
BAD_npn.05	Improper Bipolar layout- npn buried layer does not enclose sinker
BAD_npn.06	Improper Bipolar layout- npn spacer does not enclose active
BAD_npn.07	Improper Bipolar layout- npn sinker does not enclose active
BAD_npn.08	Improper Bipolar layout- npn collector sinker does not enclose active
BAD_npn.09	Improper Bipolar layout- npn collector sinker active does not enclose contact
BAD_npn.10	Improper Bipolar layout- npn emitter implant does not interact with emitter poly
BAD_npn.11	Improper Bipolar layout- npn emitter does not enclose contact
BAD_npn.12	Improper Bipolar layout- n_cell does not enclose base poly
BAD_npn.13	Improper Bipolar layout- npn base poly does not enclose emitter poly
BAD_npn.14	Improper Bipolar layout- npn base poly does not enclose contact
BAD_npn.15	Improper Bipolar layout- npn emitter poly does not enclose emitter window
BAD_npn.16	Improper Bipolar layout- npn spcaer diffusion does not enclose emitter poly
BAD_npn.17	Improper Bipolar layout- npn emitter window does not contain emitter
BAD_MOS	Improper MOSFET
BAD_NCELL	Merging N_cells
BD.Bad	Wire Bond Pad material error
OBD.error	octagon pad not completely inside Jazz marking layer
BDxx54a	Although Jazz pad marking layer is present, pad is not Jazz Pad
show_dummyactive	Density DRC, the markers represent where dummy active will be applied
show_dummypoly	Density DRC, the markers represent where dummy poly will be applied
show_dummymet1 ... show_dummymet2 ... show_dummymetX	Density DRC, the markers represent where dummy metal will be applied
show_periphery	LUP DRC, the markers represent the region of MOS periphery. This region is used to determine the LUP rules will be applied (inside periphery vs outside periphery)

5.14 Large Die Rules

The large die rules are triggered if the minimum data extent in either X or Y direction exceeds 7mm. For large die, customer must assume low yields or large yield variations for designs that do not meet the *.LD rules. The standard cells may violate these rules and they need to be marked with the standard cell marking layer (layer 118, datatype 36).

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA, SBC18H2
8.E.LD	Minimum large die metal 1 area	0.36 (μm^2)
18.E.LD	Minimum large die metal 2 area	0.40 (μm^2)
28.E.LD	Minimum large die metal 3 area	0.48 (μm^2)
38.E.LD	Minimum large die metal 4 area	NA
48.E.LD	Minimum large die metal 5 area	NA
58.E.LD	Minimum large die metal 6 area	NA
8.C.LD	Minimum large die Metal 1 overplot of contacts	0.03
17.B.LD	Minimum large die Metal 1 overplot of via	0.03
18.C.LD	Minimum large die Metal 2 overplot of via	0.04
27.B.LD	Minimum large die Metal 2 overplot of via2	0.04
28.C.LD	Minimum large die Metal 3 overplot of via2	0.05
37.B.LD	Minimum large die Metal 3 overplot of via3	0.05
38.C.LD	Minimum large die Metal 4 overplot of via3	NA
47.B.LD	Minimum large die Metal 4 overplot of via4	NA
48.C.LD	Minimum large die Metal 5 overplot of via4	NA
57.B.LD	Minimum large die Metal 5 overplot of via5	NA
58.C.LD	Minimum large die Metal 6 overplot of via5	NA
118.36.BAD	Maximum allowed percentage of standard cell marking layer covering circuit data extent.	20%

As an aid to meet the large die design rules, the following two tables, with *.*.LD.a and *.*.LD.b rules, provide intermediate design rule bins between the standard design rules and the large die design rules. These rules help in identifying gross large die design rule violations.

Rule No.	Rule Name	SBC18HX, SBC18HXL, SBC18HA, SBC18H2
8.E.LD.a	Minimum metal 1 area	0.26 (μm^2)
8.E.LD.b	Minimum metal 1 area	0.31 (μm^2)
18.E.LD.a	Minimum metal 2 area	0.28 (μm^2)
18.E.LD.b	Minimum metal 2 area	0.34 (μm^2)
28.E.LD.a	Minimum metal 3 area	0.30 (μm^2)
28.E.LD.b	Minimum metal 3 area	0.39 (μm^2)
38.E.LD.a	Minimum metal 4 area	NA
38.E.LD.b	Minimum metal 4 area	NA
48.E.LD.a	Minimum metal 5 area	NA
48.E.LD.b	Minimum metal 5 area	NA
58.E.LD.a	Minimum metal 6 area	NA
58.E.LD.b	Minimum metal 6 area	NA
8.C.LD.a	Minimum Metal 1 overplot of contacts	0.02
8.C.LD.b	Minimum Metal 1 overplot of contacts	0.025
17.B.LD.a	Minimum Metal 1 overplot of via	0.02
17.B.LD.b	Minimum Metal 1 overplot of via	0.025
18.C.LD.a	Minimum Metal 2 overplot of via	0.02
18.C.LD.b	Minimum Metal 2 overplot of via	0.03
27.B.LD.a	Minimum Metal 2 overplot of via2	0.02

27.B.LD.b	Minimum Metal 2 overplot of via2	0.03
28.C.LD.a	Minimum Metal 3 overplot of via2	0.025
28.C.LD.b	Minimum Metal 3 overplot of via2	0.04
37.B.LD.a	Minimum Metal 3 overplot of via3	0.025
37.B.LD.b	Minimum Metal 3 overplot of via3	0.04
38.C.LD.a	Minimum Metal 4 overplot of via3	NA
38.C.LD.b	Minimum Metal 4 overplot of via3	NA
47.B.LD.a	Minimum Metal 4 overplot of via4	NA
47.B.LD.b	Minimum Metal 4 overplot of via4	NA
48.C.LD.a	Minimum Metal 5 overplot of via4	NA
48.C.LD.b	Minimum Metal 5 overplot of via4	NA
57.B.LD.a	Minimum Metal 5 overplot of via5	NA
57.B.LD.b	Minimum Metal 5 overplot of via5	NA
58.C.LD.a	Minimum Metal 6 overplot of via5	NA
58.C.LD.b	Minimum Metal 6 overplot of via5	NA

6. ESD Rules

Refer to SBC18 ESD Design Manual, Document No. NPB-PS-0411.

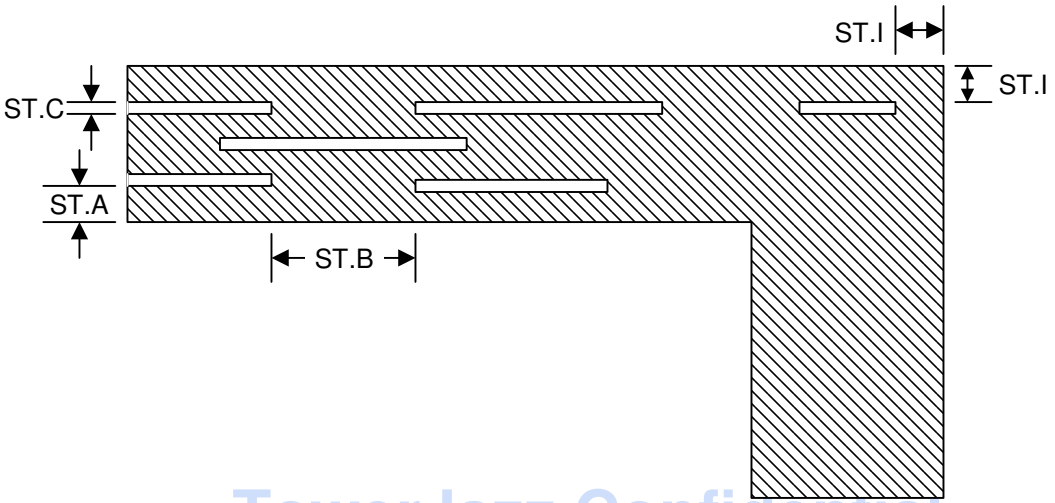
7. Stress Relief Rules

7.1 Metal Stress Relief Rules

Stress relief rules are additional metal rules that reduce stress effects. The inserted slits should be aligned with the long axis parallel to the metal line. These rules do not apply to metal within 17 microns of pad metal. See Illustration ST.

Rule No.	Rule Name	SBC18HX, SBC18HXL SBC18HA	SBC18PT	SBC18QTD, SBC18QTL, SBC18QTR, SBC18QW	SBC18MW, SBC18MWD, SBC18MV
ST.A	Maximum metal bus width without adding slits	35	35	35	35
ST.B	Maximum spacing between coaxial metal slits (recommended minimum = 10µm)	35	35	35	35
ST.C	Minimum slit width:				
	a) metal 1	1.0	1.0	1.0	1.0
	b) metal 2	1.0	1.0	1.0	1.0
	c) metal 3	1.0	1.0	1.0	2.0
	d) metal 4	1.0	1.25	2.0	
	e) metal 5	1.25	2.0		
	f) metal 6	2.0			
ST.E	Minimum spacing from chip corner to metal 1, metal 2, metal 3, metal 4, metal 5 or metal 6 when die size is > 25mm^2	275	275	275	275
ST.E.1	Minimum spacing from chip corner to metal 1, metal 2, metal 3, metal 4, metal 5 or metal 6 when die size is ≤ 25mm^2.	150	150	150	150
ST.F	Metal at the chip corners should be at an angel of 45 degrees. These corners may be designed by using stair stepped polygons with sides of about 5µm per step.				
ST.G	No active circuitry (active layer, poly) is allowed within a square area 200µm X 200µm from chip corner when die size > 25mm^2				

ST.G.1	No active circuitry (active layer, poly) is allowed within a square area 125µm X 125µm from chip corner when die size ≤ 25mm^2				
ST.I	Minimum space between any slit and metal edge	10	10	10	10



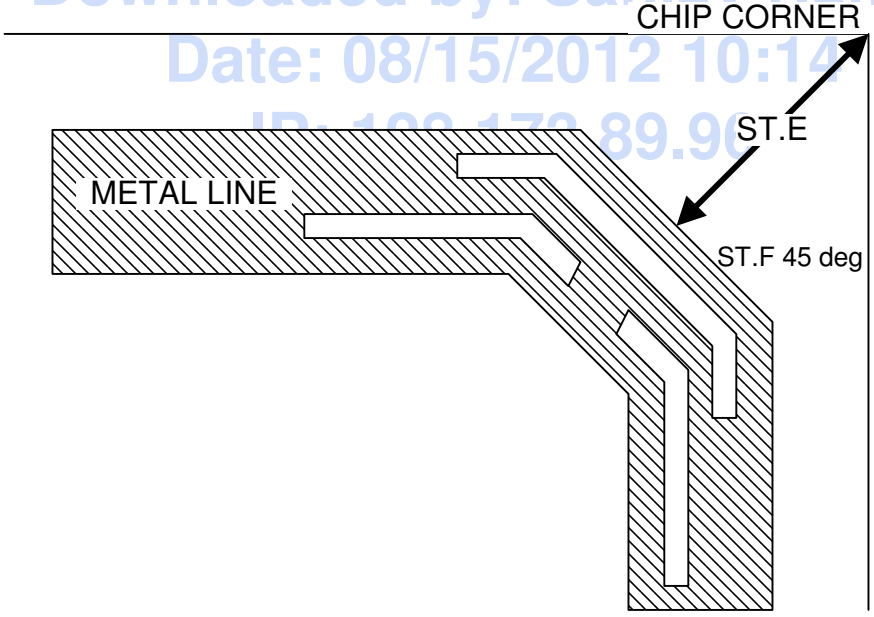


ILLUSTRATION ST

7.2 MIM Capacitor Stress Relief Rules

The stress relief rules of the non stacked MIM capacitor are described below

Rule No.	Rule Name	All SBC18
MC12	Capacitor TM space to die edge	>100
MC13*	Maximum width of bottom metal of capacitor where either die size x or y dimension < 6350um	250 um
MC14*	Maximum width of bottom metal of capacitor where both die size x and y dimension > 6350um	200 um
MC15	Maximum width of TM where either die size x or y dimension < 6350um	250 um
MC16	Maximum width of TM where both die size x and y dimension > 6350um	200 um

* The standard Metal stress relief rules apply beyond the capacitor extent

The stress relief rules of the stacked MIM capacitor are described below

Rule No.	Rule Name	SBC18PT, SBC18QW only
SMC41	Minimum space capacitor TM to die edge	100 um
SMC42*	Maximum width of bottom metal 2 of capacitor	200 um
SMC43	Maximum width of TM	200 um
SMC44	Minimum space capacitor TM2 to die edge	100 um
SMC45*	Maximum width of bottom metal 3 of capacitor	200 um
SMC46	Maximum width of TM2	200 um

* The standard Metal stress relief rules apply beyond the capacitor extent

8. Bonding Pad Design Rules

This section gives the rules for designing bonding pads and their relationships to nearby and connecting conductors.
All customers must have their pad designs and layout verified and approved by their packaging vendor prior to pad layout.
SBC18 may have four types of pads:
The Jazz wire bonding pads are marked with layer 74 only and should follow the rules in Section 8.1.
The custom wire bond pads (not marked with layer 74 or layer 96) should follow rules of Section 8.2.
The Jazz bump pads are marked with layer 96 and layer 74.
The custom bump pads are marked with layer 96 only and should follow rules of Section 8.3.

8.1 Jazz Wire Bond Pads

Notes:
1) The SBC18 wire bond pads do not contain any metal 1, metal 2, metal 3, vias, or via2s. The pads are composed of metal 4 only in quadruple level metal designs, metal 5 only in five level metal designs and metal 6 only in six level metal designs.
2) The minimum pad pitch is 60µm. However, Jazz assembly house and probing house is not qualified yet for 60um pads. Customers must qualify their own assembly and probing house.

8.1.1 Jazz Rectangular Wire Bond Pads

This section describes rules for Jazz rectangular wire bond pads. See illustrations BD, BD2 . These pads are also used in jazz digital I/O cells.

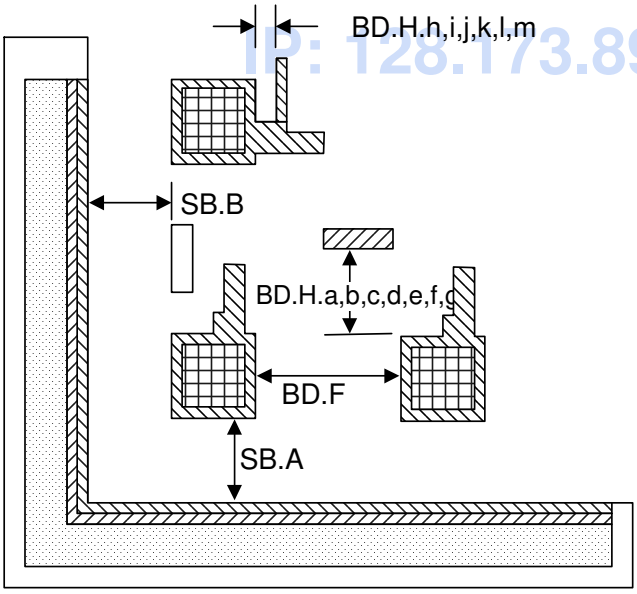


ILLUSTRATION BD2

Rule No.	Rule Name	All SBC18	
		80um pad pitch	60um pad pitch
BD.A.a	Minimum/maximum bond pad opening in protective overcoat layer for single pads. The narrow dimension must be parallel to the chip edge.	105 x 66	94 X 51
BD.A.b	Minimum/maximum bond pad opening in protective overcoat layer for double pads. The long dimension must be parallel to the chip edge.	105 x 132	94 X 102
BD.B	Minimum spacing bond pad opening to bond pad opening	14	12
BD.D.a	Minimum pad metal overplot of pad opening for the dimension perpendicular to the chip edge	4.0	3.0
BD.D.a.1	Maximum pad metal overplot of pad opening (except pad to circuit side)	7.0	3.0
BD.F	Minimum spacing pad metal to pad metal	6	6
BD.J.a	Minimum width of metal 1, metal 2 ,metal 3, metal 4, metal 5, metal 6 connected to and within 10µm of the pad (measured parallel to the pad edge)	42	42
BD.K	Minimum (floating) N-well extension beyond pad metal. Reliability guideline: A floating well must be used under bonding pads to reduce the likelihood of leakage from pad to substrate caused by cracking of the dielectric between the pad metal and the substrate.	2	0.5
BD.L	Minimum spacing between metal connections to the pad and a corner of the bonding pad.	6	6
BD.M.a	All bonding pads shall consist of at least 3 pad corners (defined in rule BD.L)		
BD.M.b	OR bonding pads shall consist of at least two pad corners (as defined in rule BD.L) and an opposite edge length (L) without connections	L=6	L=6
BD.N	Pad metal(s) must have a direct connection to diffusion or a tie.		

Rule No.	Rule Name	SBC18HX, SBC18HXL SBC18HA	SBC18PT,	SBC18QTD, SBC18QTL, SBC18QTR, SBC18QW	SBC18MW, SBC18MWD , SBC18MV
BD.H	Minimum space between pad metal (s) and:				
	a) unrelated poly	10	10	10	10
	b) unrelated metal 1	10	10	10	10
	c) unrelated metal 2	10	10	10	10
	d) unrelated metal 3	10	10	10	10
	e) unrelated metal 4	10	10	10	
	f) unrelated metal 5	10	10		
	g) unrelated metal 6	10			
	h) related metal 1	10	10	10	10
	i) related metal 2	10	10	10	10
	j) related metal 3	10	10	10	10
	k) related metal 4	10	10	10	
	l) related metal 5	10	10		
	m) related metal 6	10			
	n) via	10	10	10	10
	o) via2	10	10	10	10
	p) via3	10	10	10	
	q) via4	10	10		
	r) via5	10			

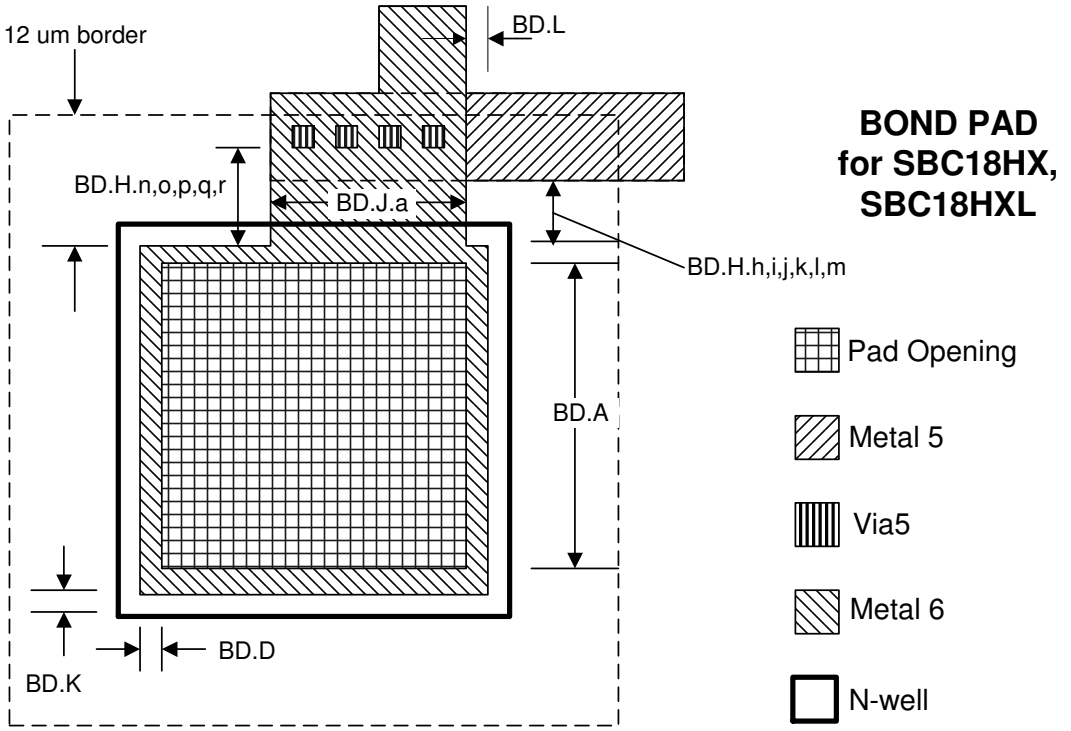


ILLUSTRATION BD (continued)

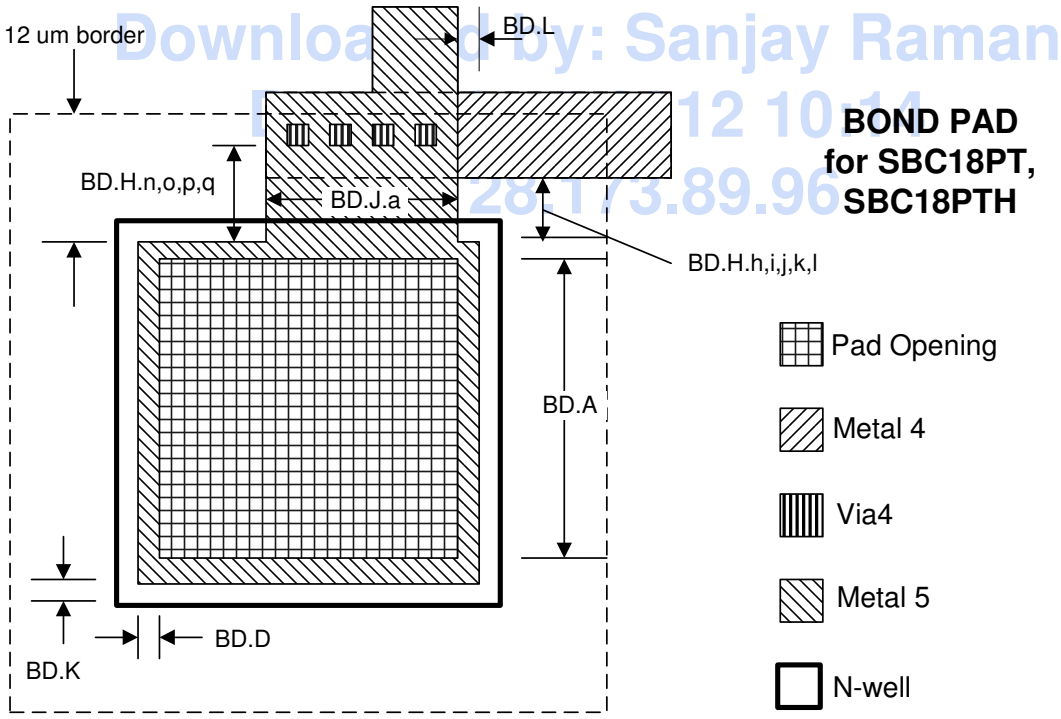


ILLUSTRATION BD (continued)

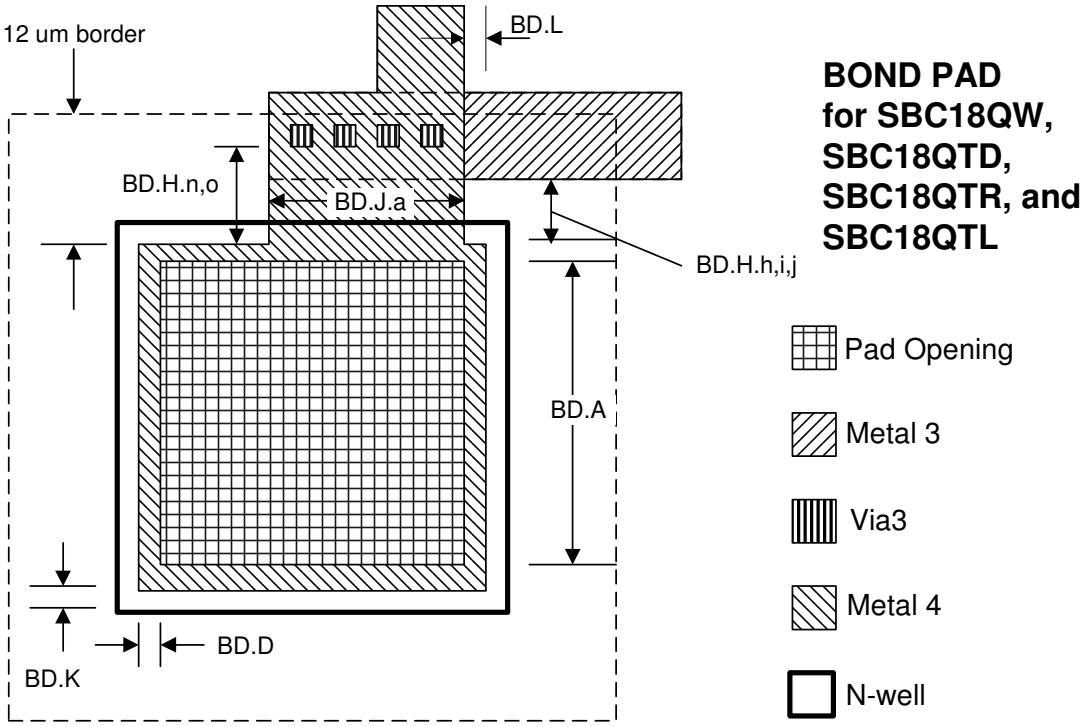
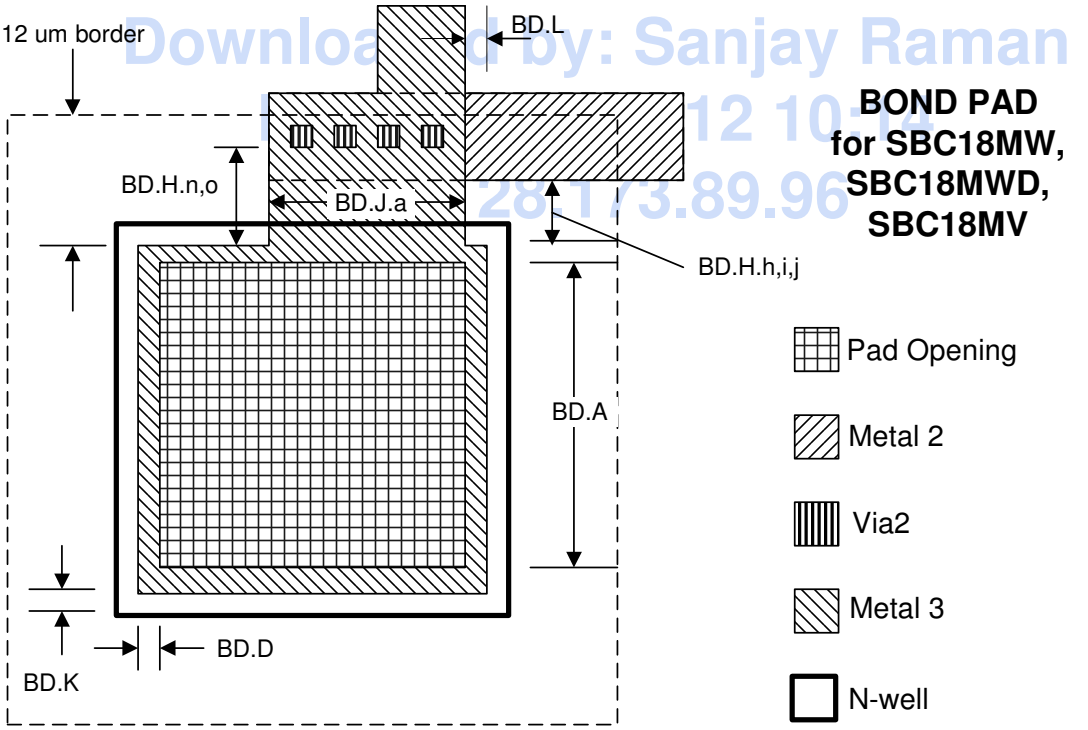


ILLUSTRATION BD (continued)



8.1.2 Octagonal Wire Bond Pads

This section describes rules for octagonal wire bond pads. See illustration OBD.

Rule No.	Rule Name	All SBC18
OBD.A	Minimum/Maximum center portion pad opening in the Y direction	59
OBD.B	Minimum/Maximum total pad opening in the Y direction	105
OBD.C	Minimum top metal overplot pad opening.	4
OBD.D	Minimum/Maximum top/bottom portion pad opening in the Y dimension	23
OBD.E	Minimum/Maximum top edge/bottom edge pad opening in the X dimension	20
OBD.F	Minimum/Maximum center portion pad opening in the X dimension	66
OBD.G	Minimum/Maximum width of top metal connecting metal pad to pad border.	23.4
OBD.H	Minimum (floating) N-well extension beyond pad metal. Reliability guideline: A floating well must be used under bonding pads to reduce the likelihood of leakage from pad to substrate caused by cracking of the dielectric between the pad metal and the substrate.	2

Notes:

1) The bonding pads are composed of metal 6 in the SBC18HX, SBC18HXL, SBC18HA processes, metal 5 in the SBC18PT processes, metal 4 in SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW processes and metal 3 in SBC18MW, SBC18MV, SBC18MWD processes.

3) For the purpose of defining design rules, the octagonal opening is divided into three sections, top, center and bottom (See OBD).

4) The Y dimension is along the longer axis, the X dimension is along the short axis of the pad.

5) Bond pad rules BD.B to BD.P in the previous section apply to octagonal pad layout.

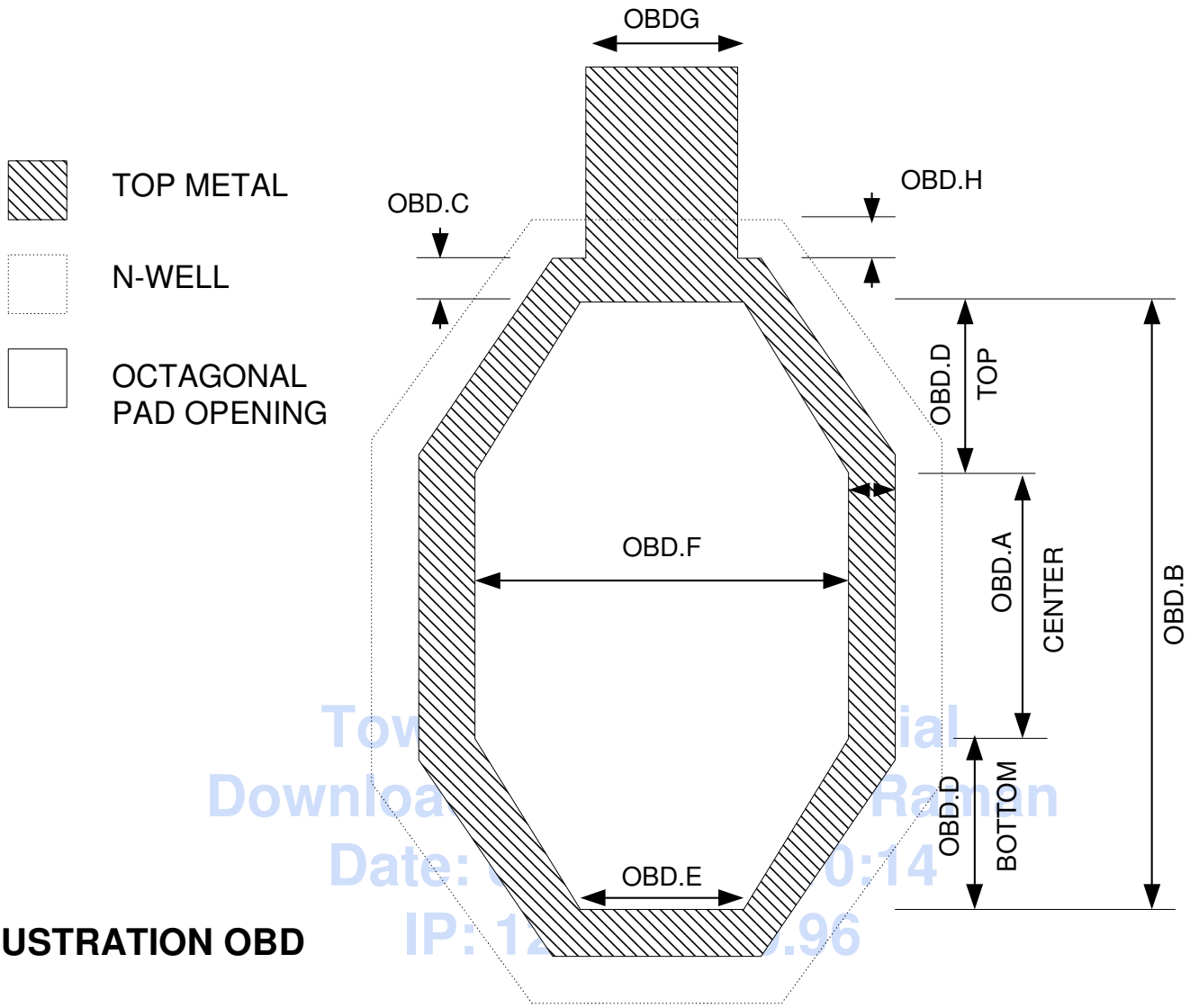


ILLUSTRATION OBD

8.2 Custom Wire Bond Pads

These rules are applied when the Jazz pad marking layer (layer 74) or the bump pad marking layer (layer 96) does not cover the pad. Custom pads may be made using the guidelines provided in this section.

Rule No.	Rule Name	All SBC18
BD.1	Minimum width of bond pad opening.	6
BD.2	Maximum width of bond pad opening.	140
BD.3	Only 90 degree and 135 degree inside corners are allowed for pad opening	
BD.4	Maximum area of bond pad opening per pad	15,000
BD.5	Minimum pad metal overplot opening	3
BD.5.a	Maximum pad metal overplot opening	5
BD.6	Minimum spacing pad metal to pad metal	6

The rules below are unchecked and are for guidelines only

Rule No.	Rule Name	All SBC18
#BD.7	Minimum width of any metal or poly connected to and within 13□m of the pad opening (unchecked rule)	12
#BD.8	Minimum space between pad opening and unrelated poly, and metal layers other than top metal. The top metal is the same metal layer as pad metal layer (unchecked rule)	8
#BD.9	Minimum space between bond pad opening and non-pad-metal top metal (unchecked rule)	13
#BD.10	No vias or contacts are allowed below pad opening (unchecked rule)	
#BD.11	Layers used to provide shielding for RF applications, such as Metal1, poly, and active must enclose the pad opening (unchecked rule)	
#BD.12	In the absense of any shielding layers, Nwell must be present below the pad. Minimum (floating) N-well extension beyond pad metal = 0.5um (unchecked rule)	
#BD.13	Pad metal(s) must have a direct connection to diffusion or a tie (unchecked rule)	

8.3 Custom Bump Pads

These rules are applied when the bump pad marking layer (layer 96) covers the pad and the Jazz pad marking layer (layer 74) does not cover the pad. Custom bump pads may be made using the guidelines provided in this section.

Rule No.	Rule Name	
BMP.1	Minimum width of bump pad opening.	6
BMP.2	Maximum width of bump pad opening.	140
BMP.3	Maximum area of bump pad opening per pad	15,000
BMP.4	Minimum pad metal overplot of bump pad opening	3
BMP.5	Maximum pad metal overplot bump pad opening	25
BMP.6	Minimum N for N-sided polygonal bump pad opening (Circular bump pad opening is recommended)	8 (octagonal)
BMP.7	All sides of the polygonal bump pad opening must have the same length	

The following rules are recommended and are not checked.

Rule No.	Rule Name	
#BMP.8	No top via allowed below bump pad opening	
#BMP.9	Minimum spacing pad metal to pad metal (unchecked rule)	10
#BMP.10	Minimum width of any metal or poly connected to and within 10µm of the bump pad opening (unchecked rule)	12
#BMP.11	Minimum space between bump pad metal and non-pad-metal top metal (unchecked rule).	5
#BMP.12	Pad metal(s) must have a direct connection to diffusion or a tie (unchecked rule)	

9. Antenna Rules

9.1 Restriction of Polysilicon and Metal Areas on Field

Poly, metal 1, metal 2, metal 3, metal 4, metal 5 and metal 6 conductors over field have restrictions. These restrictions are for 1) total area, and 2) ratio of conductor area to gate area provided:

A) the conductors on field are not connected to a diffusion (or tie) directly or through a previous (not subsequent) conductor layer or

B) the conductors on field are connected to a diffusion (or tie) of specific area directly or through a previous (not subsequent) conductor layer (Rules AN.H)

C) and the conductors of A) or B) above are attached to a channel area (poly on active) either directly or through a previous layer.

The term “antenna area” is used to refer to the total conductor area of that layer that meets the conditions A) or B) and C) above a) on field and channel for poly antennas or b) total conductor area for all metal layers. The term connected total gate area refers to the total channel area connected either directly or indirectly to an antenna.

Rules AN.G and AN.H use the following definitions for antenna perimeter area:
Antenna perimeter area= 2 * (Length + Width) * thickness
Using:

(a) For SBC18HX/HXL/HA only: poly thickness=2100A, M1 to M3 thickness=5200A, M4 thickness = 6200A; M5 thickness = 15900A, Top metal thickness = 28100A

(b) For SBC18PT, only: poly thickness=2100A, M1 to M3 thickness=5200A, M4 thickness = 15900A; M5 thickness = 52600A

(c) For SBC18QTD/SBC18QTR/SBC18QTL only : poly thickness=2100A, M1 thickness=5200A; M2 thickness = 6200A; M3 thickness = 6200A; Top metal (M4) thickness= 52600A

(d) For SBC18QW only : poly thickness=2100A, M1 thickness=5200A; M2 thickness = 6200A; M3 thickness = 6200A; Top metal (M4) thickness= 28100A

(e) For SBC18MW/SBC18MWD/SBC18MV only : poly thickness=2100A, M1 thickness=5200A; M2 thickness = 6200A; Top metal (M3) thickness= 28100A

See Illustration AN.

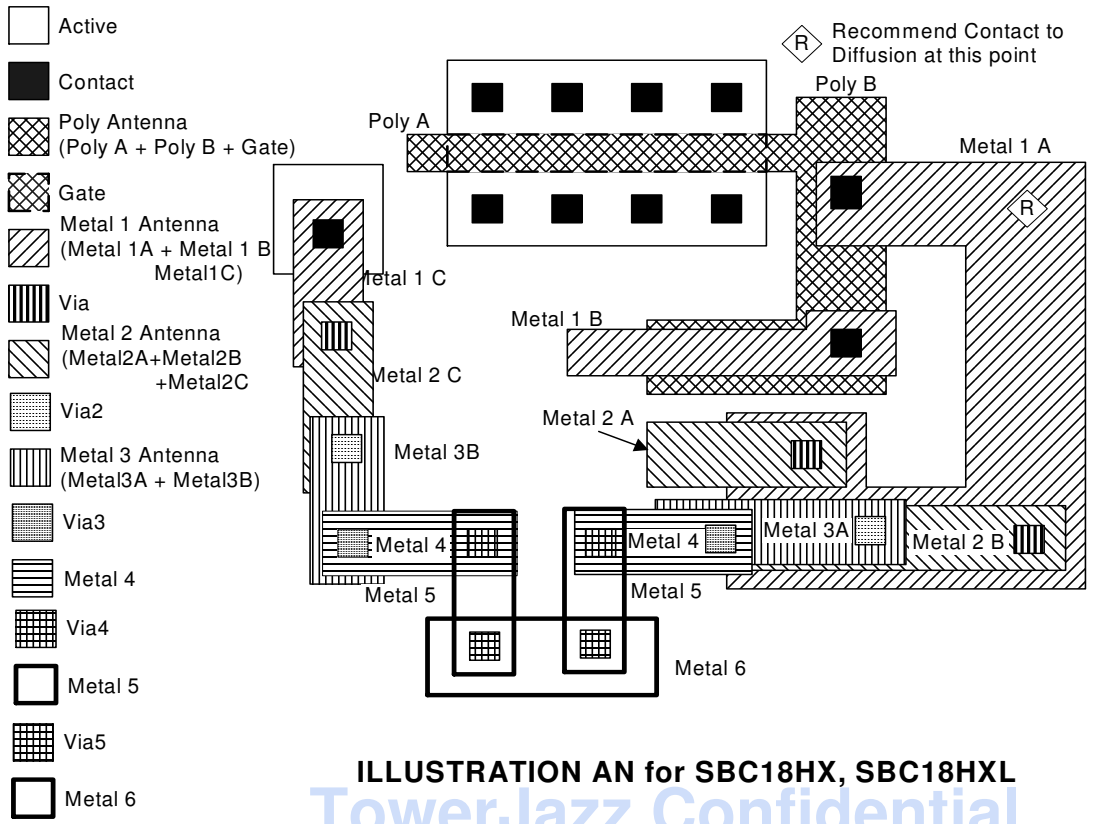


ILLUSTRATION AN for SBC18HX, SBC18HXL

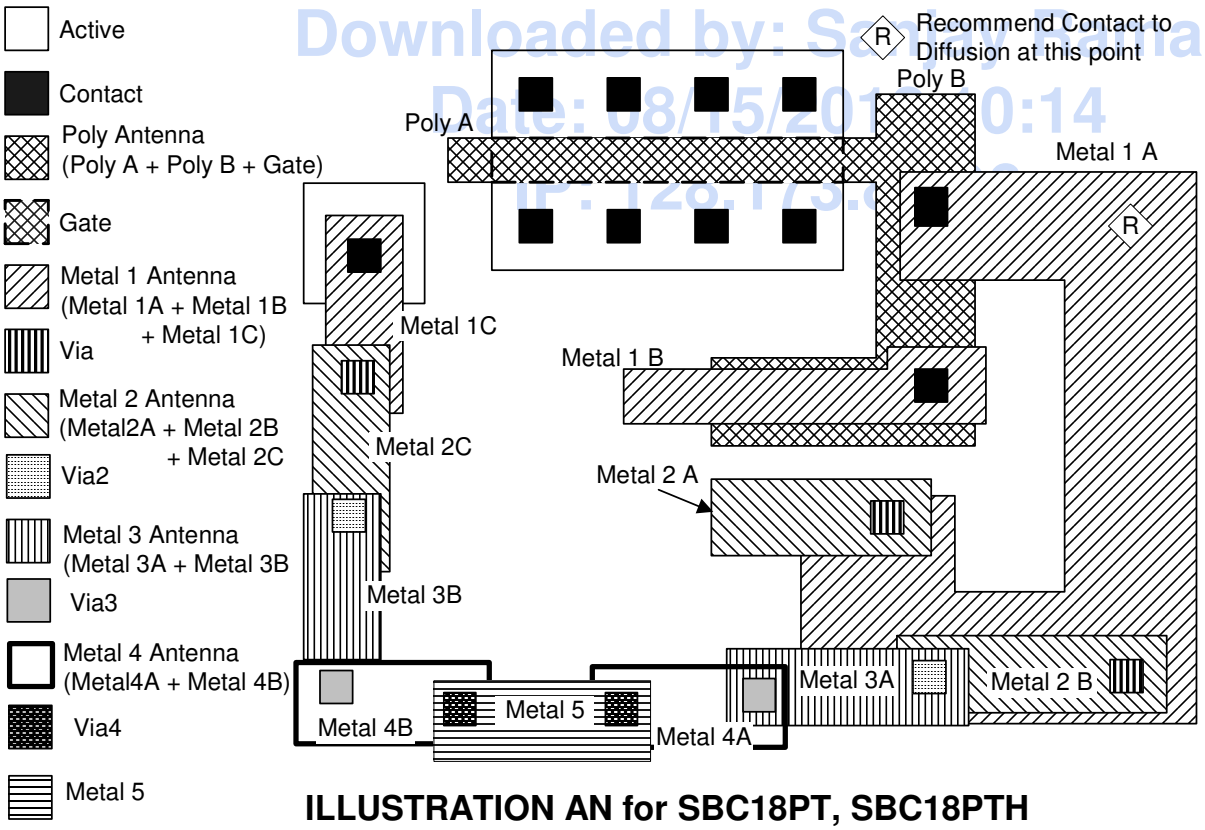


ILLUSTRATION AN for SBC18PT, SBC18PTH

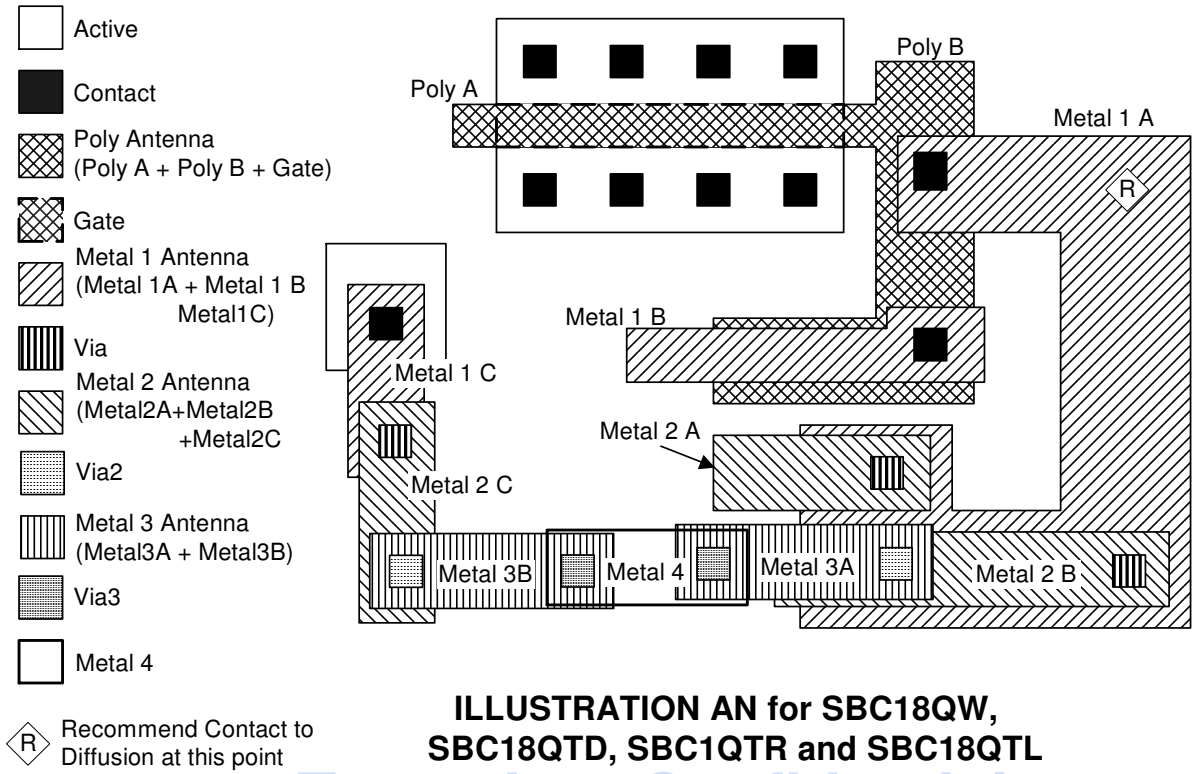


ILLUSTRATION AN for SBC18QW, SBC18QTD, SBC1QTR and SBC18QTL

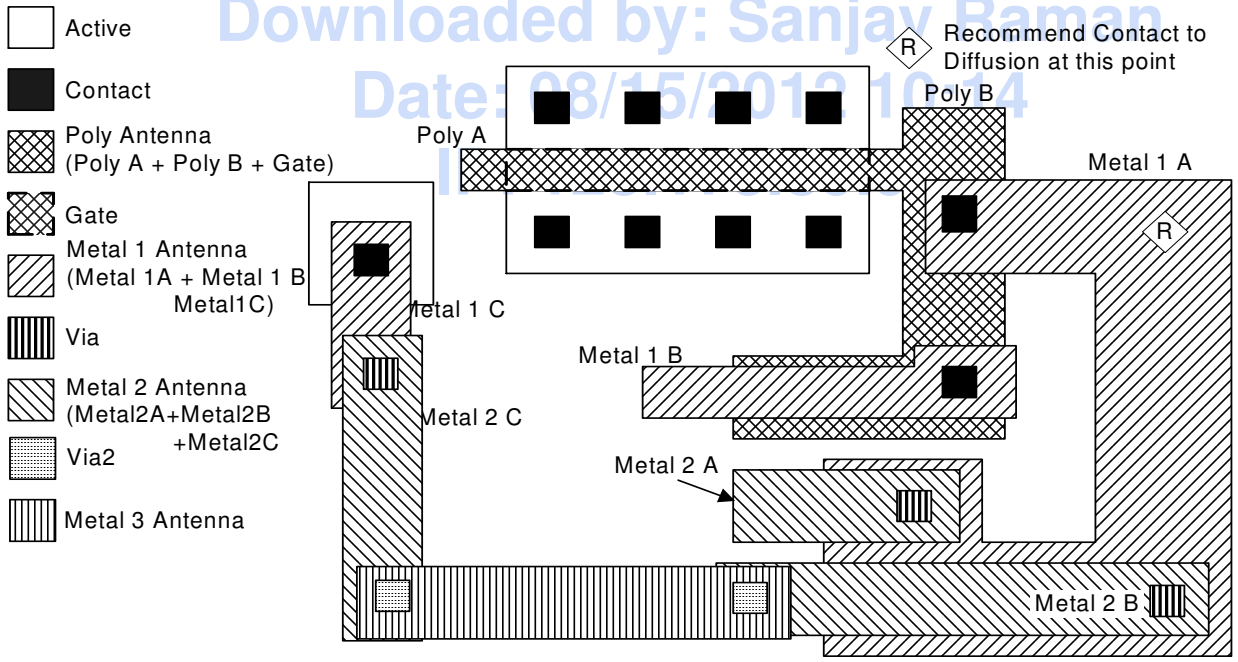


ILLUSTRATION AN for SBC18MW , SBC18MV and SBC18MWD

Rule	Rule Name	All SBC18H*	All SBC18PT*	All SBC18Q*	All SBC18M*	

AN.A	Maximum poly area of poly antenna	15,000	15,000	15,000	15,000	μm^2
AN.B	Maximum metal 1 area of metal 1 antenna	15,000	15,000	15,000	15,000	μm^2
AN.C.a	Maximum metal 2 area of metal 2 antenna	15,000	15,000	15,000	15,000	μm^2
AN.C.b	Maximum metal 3 area of metal 3 antenna	15,000	15,000	15,000	0	μm^2
AN.C.c	Maximum metal 4 area of metal 4 antenna	15,000	5,000	0		μm^2
AN.C.d	Maximum metal 5 area of metal 5 antenna	5,000	0			μm^2
AN.C.e	Maximum metal 6 area of metal 6 antenna	0				μm^2
AN.D	Maximum ratio of poly area of poly antenna to connected total gate area	35	35	35	35	
AN.E.a	Maximum ratio of metal 1 antenna area to total connected gate area (without a protection diode)	200	200	200	200	
AN.E.b	Maximum ratio of metal 2 antenna area to total connected gate area (without a protection diode)	200	200	200	200	
AN.E.c	Maximum ratio of metal 3 antenna area to total connected gate area (without a protection diode)	200	200	200	0	

Rule	Rule Name	All SBC18H*	All SBC18PT*	All SBC18Q*	All SBC18M*	
AN.E.d	Maximum ratio of metal 4 antenna area to total connected gate area (without a protection diode)	200	100	0		
AN.E.e	Maximum ratio of metal 5 antenna area to total connected gate area (without a protection diode)	200	0			
AN.E.f	Maximum ratio of metal 6 antenna area to total connected gate area (without a protection diode)	0				
AN.F	Maximum ratio of poly perimeter area of poly antenna to connected total gate area	200	200	200	200	
AN.G.a	Maximum accumulative ratio of metal 1 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58μm^2)	400	400	400	400	
AN.G.b	Maximum accumulative ratio of metal 2 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58μm^2)	400	400	400	400	
AN.G.c	Maximum accumulative ratio of metal 3 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58μm^2)	400	400	400	0	
AN.G.d	Maximum accumulative ratio of metal 4 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58μm^2)	400	200	0		

Rule	Rule Name	All SBC18H*	All SBC18PT*	All SBC18Q*	All SBC18M*	
AN.G.e	Maximum accumulative ratio of metal 5 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58µm^2)	200	0			
AN.G.f	Maximum accumulative ratio of metal 6 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58µm^2)	0				
AN.H.a	Maximum accumulative ratio of metal 1 perimeter area to total connected gate area, if a diode > 0.58x0.58µm^2 is connected.	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400	
AN.H.b	Maximum accumulative ratio of metal 2 perimeter area to total connected gate area, if a diode > 0.58x0.58µm^2 is connected.	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400	
AN.H.c	Maximum accumulative ratio of metal 3 perimeter area to total connected gate area, if a diode > 0.58x0.58µm^2 is connected.	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400	
AN.H.d	Maximum accumulative ratio of metal 4 perimeter area to total connected gate area, if a diode > 0.58x0.58µm^2 is connected.	400* (diode area-.5) +2400	400* (diode area-.5) +2400	400* (diode area-.5) +2400		
AN.H.e	Maximum accumulative ratio of metal 5 perimeter area to total connected gate area, if a diode > 0.58x0.58µm^2 is connected.	400* (diode area-.5) +2400	400* (diode area-.5) +2400			
AN.H.f	Maximum accumulative ratio of metal 6 perimeter area to total connected gate area, if a diode > 0.58x0.58µm^2 is connected.	400* (diode area-.5) +2400				

9.2 Restriction of Number of Contacts and Vias Attached to the Gate

The total number of contacts, via 1, via 2, via 3, via 4, and via 5 over poly, metal 1, metal 2, metal 3, metal 4, and metal 5 conductors respectively, have restrictions on the ratio of contact/via area to gate area. These restrictions apply provided:

A) the contacts/vias are not connected to a diffusion (or tie) directly or through a previous (not subsequent) conductor layer or

B) the contacts/vias are connected to a diffusion (or tie) of specific area directly or through a previous (not subsequent) conductor layer (Rules AN.K)

C) the contacts/vias of A) or B) above are attached to a channel area (poly on active) either directly or through a previous layers (applicable to bond pads also).

The term antenna area is used to refer to the total contact or via area of that layer that meets the conditions A) or B) and C) above. The term connected total gate area refers to the total channel area connected either directly or indirectly to a contact/via intensive antenna.

Rule No.	Rule Name	All SBC18H*	All SBC18P*	All SBC18Q*	All SBC18M*
AN.I	Maximum ratio of total contact antenna area to total connected gate area	10	10	10	10
AN.J.a	Maximum ratio of total via1 antenna area to total connected gate area when no protection diode is used.	20	20	20	20
AN.J.b	Maximum ratio of total via2 antenna area to total connected gate area when no protection diode is used.	20	20	20	5
AN.J.c	Maximum ratio of total via3 antenna area to total connected gate area when no protection diode is used.	20	5	5	N/A
AN.J.d	Maximum ratio of total via4 antenna area to total connected gate area when no protection diode is used.	5	5	N/A	N/A
AN.J.e	Maximum ratio of total via5 antenna area to total connected gate area when no protection diode is used.	5	N/A	N/A	N/A

AN.J.p	Maximum ratio of stacked via3 and via 4 antenna area to total connected gate area when no protection diode is used.	N/A	5	N/A	N/A
AN.J.q	Maximum ratio of stacked via4 and via 5 antenna area to total connected gate area when no protection diode is used.	5	N/A	N/A	N/A
AN.K.a	Maximum ratio of total via1 antenna area to total connected gate area, if a protection diode > 0.58x0.58µm^2 is implemented	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300
AN.K.b	Maximum ratio of total via2 antenna area to total connected gate area, if a protection diode > 0.58x0.58µm^2 is implemented	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300
AN.K.c	Maximum ratio of total via3 antenna area to total connected gate area, if protection a diode > 0.58x0.58µm^2 is implemented	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	N/A
AN.K.d	Maximum ratio of total via4 antenna area to total connected gate area, if protection a diode > 0.58x0.58µm^2 is implemented	83.3* (diode area–2.7) +300	83.3* (diode area–2.7) +300	N/A	N/A
AN.K.e	Maximum ratio of total via5 antenna area to total connected gate area, if protection a diode > 0.58x0.58µm^2 is implemented	83.3* (diode area–2.7) +300	N/A	N/A	N/A

9.3 Special Antenna Rules for MIM Capacitors

Poly, metal 1, metal 2, metal 3, metal 4, metal 5 and metal 6 conductors over field have restrictions on 1) total area, and 2) ratio of conductor area to TM area provided A) the conductors on field are not connected to a diffusion (or tie) directly or through a previous (not subsequent) conductor layer and B) the conductors are attached to a capacitor area (TM on metal2) either directly or through a previous layer. The term antenna area is used to refer to the total conductor area of that layer that meets the conditions A) and B) above.

Rule No.	Rule Name	All SBC18 HX, HXL	SBC18 HA	All SBC 18P*	All SBC 18Q*	All SBC 18M*
SA.0	Maximum ratio of metal 2 antenna connected to the intersection of the Metal 2 bottom capacitor plate and TM. See Note 3	N/A	N/A	20	20	20
SA.1	Maximum ratio of metal 3 antenna area to total connected TM area or to the intersection area of Metal2 bottom capacitor plate and TM. See Note 3	N/A	20	20	20	0
SA.2	Maximum ratio of metal 4 antenna area to total connected TM area or to the intersection area of Metal4 bottom capacitor plate and TM (for SBC18HX, HA) or to the intersection area of Metal2 bottom capacitor plate and TM (for SBC18PT) . See Note 3	20	20	20	0	N/A
SA.3	Maximum ratio of metal 5 antenna area to total connected TM area or to the intersection area of Metal4 bottom capacitor plate and TM. See Note 3	20	20	0	N/A	N/A
SA.4	Maximum ratio of metal 6 antenna area to total connected TM area or to the intersection area of Metal4 bottom capacitor plate and TM. See Note 3	0	0	N/A	N/A	N/A

Note 3: The connecting path from the metal antenna layer to the MIM capacitor should include all connecting paths through metal layers metal 4, metal 3, metal 2, metal 1, and poly, which are not protected by diodes.

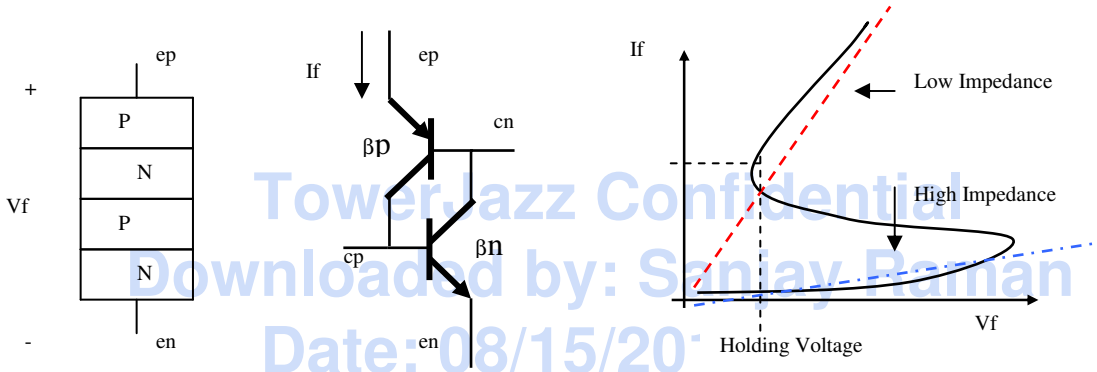
Additional rules for stacked MIM capacitor are described below

Rule No.	Rule Name	SBC18PT, only	SBC18QW only	SBC18HA only
SMA.2	Maximum ratio of metal 4 antenna area to total connected TM2 area.	20	0	20
SMA.3	Maximum ratio of metal 5 antenna area to total connected TM2 area	0	N/A	20

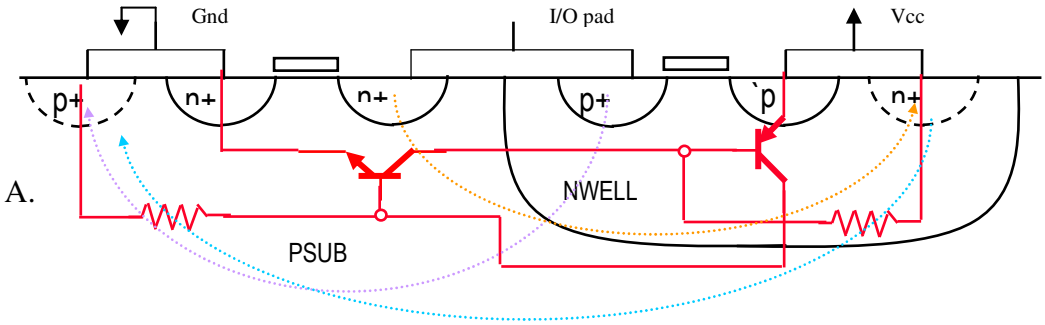
10. Latchup Rules

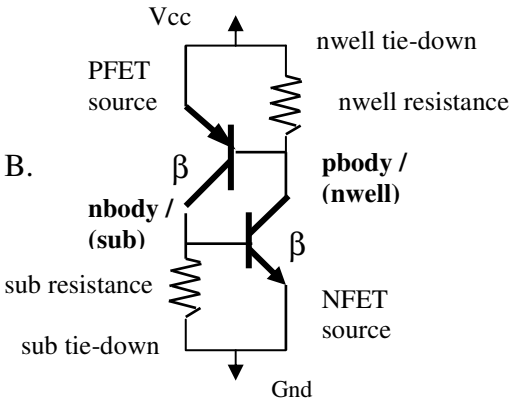
Jazz latch-up rules enforce counter-measures for the over-voltage and forced-IO-current phases of standardized product-level latch-up tests. These tests force hundreds of milliamps into the IO pins and bias supply voltages to 1.5x their maximum rated values, while the voltages of uninvolved IO pins are biased alternatively at their maximum and minimum values. The test may be conducted at elevated temperatures. If a part demonstrates a sustained high current on a supply pin after the stress condition is removed, or is not functional after the test, it is classified as having failed.

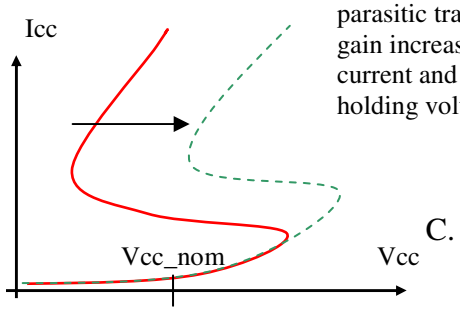
Sustained latch-up is usually caused by strong regenerative feedback in silicon controlled rectifiers (SCRs). These devices consist of parasitic inter-twinned npn and pnp transistors connected between supply and ground, as shown below. They commonly exist in CMOS layouts, but can form in the layouts of any devices that have a similar connectivity and cross section. SCRs can snap back to low voltages and exhibit low impedance. If the snap back holding voltage is lower than the supply value, the SCR may stay in the low impedance mode and draw potentially high currents (one failure criterion of latch-up).



The following figures show how an SCR can form in CMOS layouts. The corresponding schematic indicates the effect of well and substrate debiasing resistance on regenerative feedback between the parasitic transistors. Reducing npn/pnp current gain or reducing substrate/well debiasing resistances can elevate the minimum voltage required to hold the SCR in a sustained low impedance mode.



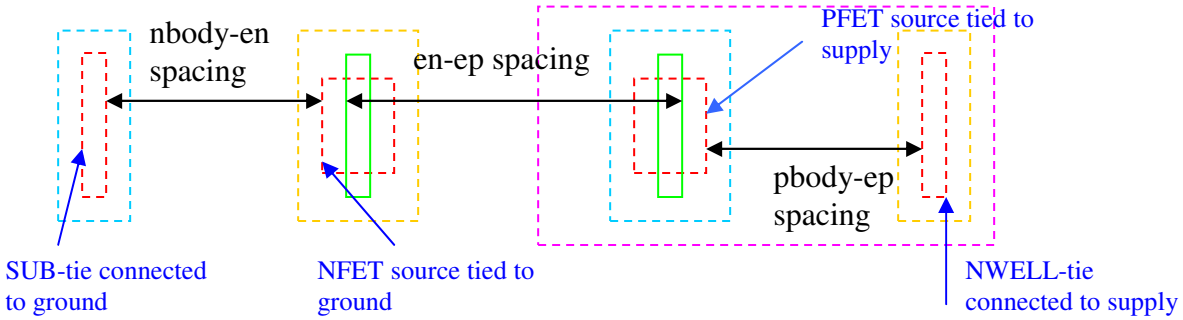




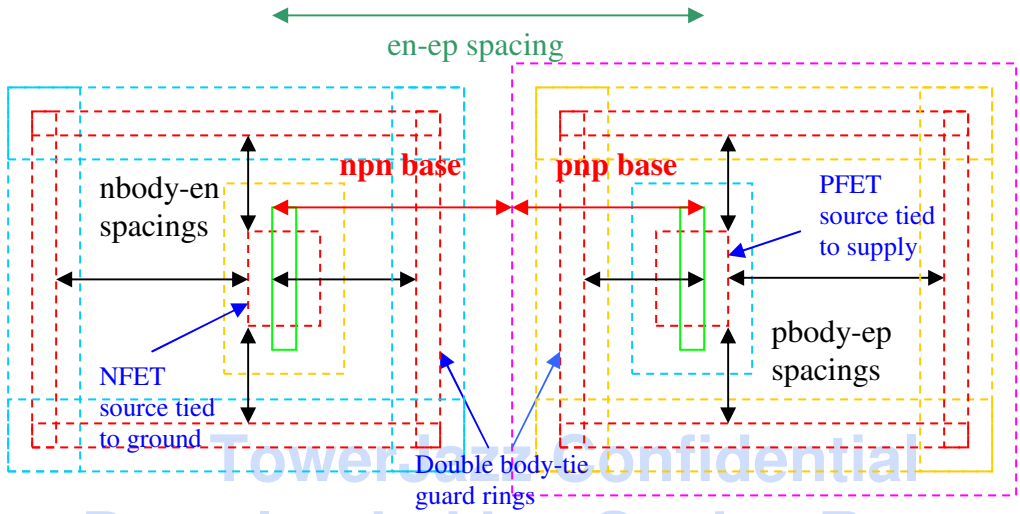
Reducing well resistance or parasitic transistor current gain increases SCR trigger current and snap back holding voltage.

From a layout perspective, closer body (well or substrate) tie-down proximity to the emitters of the parasitic npn/pnp in an SCR can reduce body debiasing resistance. Larger emitter-emitter spacing can reduce parasitic transistor current gain, as can body tie-downs placed in between the emitters.

The figure below shows how outwards facing body-tiedowns (pbody and nbody) should be placed closer to the emitters (MOS sources tied to power domain rails) in order to reduce debiasing resistance for a given emitter-emitter (en-ep) spacing. A global maximum body-tie spacing may be needed just to ensure that a product doesn't latch-up due to inadvertent charging of the nwell and substrate during over-voltage testing and even normal operation.

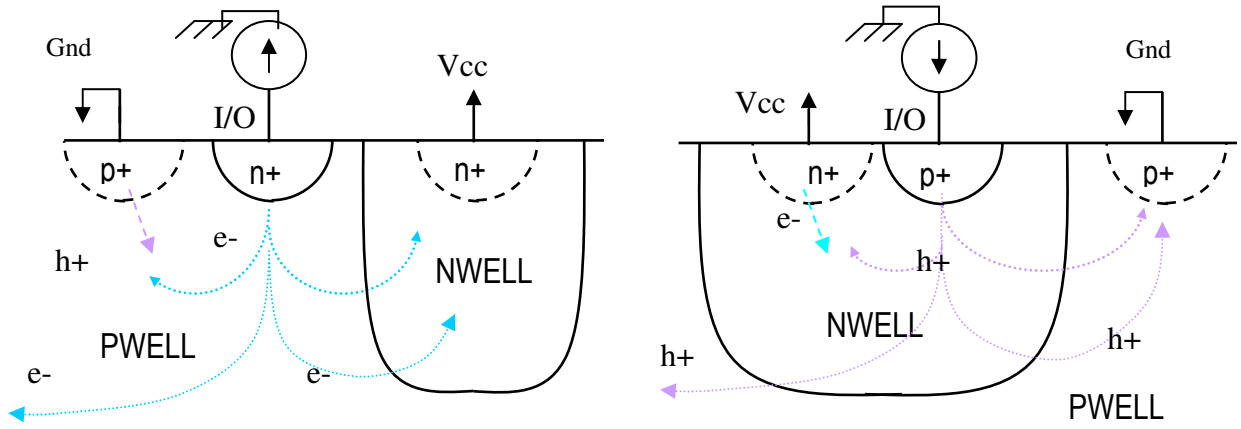


The figure below shows how interior body-tiedowns can be used to simultaneously reduce debiasing resistance and parasitic current gain, especially in small emitter-emitter spacing SCRs that can exist near the perimeter regions of nwell and substrate. Complete ring body tie-downs are effective in passivating SCRs all along the well and substrate perimeters. Such rings are also recognized by the DRC verification tools. While interior body-tiedowns and complete rings may not be necessary everywhere in a chip, they should have benefit in regions of layout where the body potentials are systematically elevated by the forced-IO-current phase of latch-up testing (within 60um of all active tied to IO pad).



Note that for forming an SCR, a MOS capacitor with nwell tied to ground could be equivalent to the NFET source tied to ground. A diode with anode tied to supply could be equivalent to the PFET source tied to supply. SCRs involving these devices should be passivated by surrounding the devices with substrate tie-downs.

Body tie-down rings are effective in preventing nwell and substrate charging during the forced IO-current phase of latch-up testing. Forced current tends to flow thru forward biased pn-junctions, such as the MOS drain junction. As illustrated in the figure below, for example, electrons injected into the substrate by a forward biased drain junction can recombine with holes that are sunk by a substrate tie-down. Hole injected into the nwell can recombine with electrons that are sunk by a well tie-down.

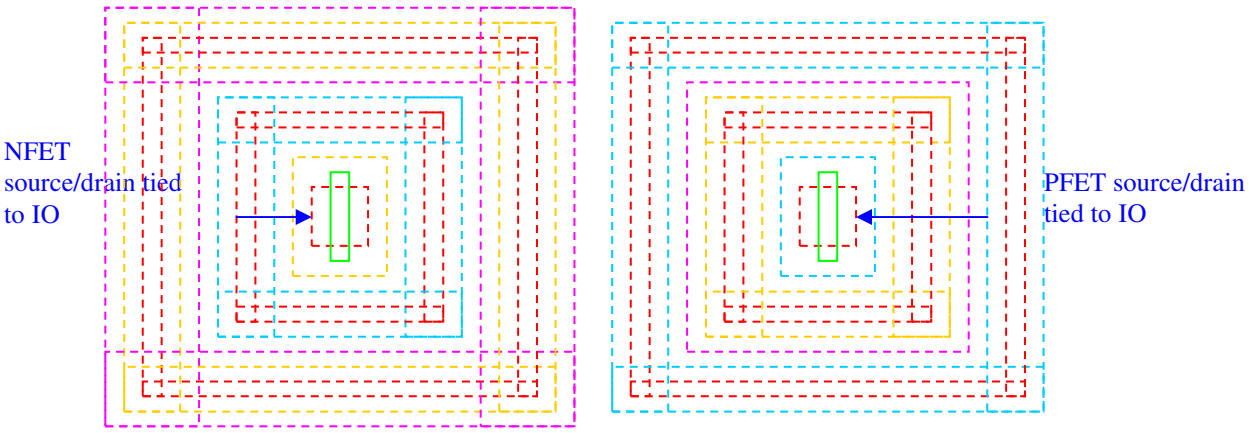


The above figure also indicates that some finite fraction of the forced test current can be captured into adjacent wells. Electrons injected into the substrate can be collected by an adjacent nwell. Holes injected into the nwell can be collected into the surrounding substrate.

Once holes are captured into the substrate, they can diffuse easily to other regions of layout within 60um. If unpassivated CMOS is nearby, it may be advantageous to surround the nwell containing the test diffusion by a substrate tie-down guard ring to sink excess holes. This applies to npn base inputs, for example.

It's found that electrons injected into the substrate may have a range of 20um before entirely recombining into holes. If unpassivated CMOS is nearby within 20um, it may be advantageous to surround the test diffusion with an n-type guard ring (n+ in nwell, as shown above left) to collect excess electrons in the substrate. This applies to npn open collectors tied to IO pins, for example. Otherwise a substrate tie-down guard ring surrounding the n-type diffusion should be adequate.

Examples of these extreme body-tie + collector guard rigns for MOSFET outputs are shown below: They are probably only necessary if nearby CMOS is not passivated with strong body tie-downs.



Suggestions for running DRC verification of the latch-up rules.

Proper evaluation of the LUP DRC rules first requires that IO bonding pads be identified to distinguish active diffusions that are stressed by the forced IO current phase of the standard latch-up test. This is done by adding labels to layouts of power and ground bonding pads, and identifying their values in the Calibre DRC submission form. This means that running the DRC rules on layouts that do not contain properly labeled bonding pads or bonding pads at all will yield a different number of database results than at the top level.

Jazz's position is that it's not possible to follow the physical methodology outlined in the previous sections without knowing what type of pins active diffusions are connected to. A stand-alone subcell can be evaluated for compliance with the latch-up rules by connecting labeled pads to its pins and generating periphery over the cell by placing adjacent test MOS output transistors connected to IO pads.

Since most conservative and difficult-to-satisfy latch-up rules involving guard-ring placement, connectivity and spacings between transistors occur in "periphery" regions of layout that surround within 60um each active diffusion tied to an IO bonding pad, but most regions of layout near active diffusions tied to power or ground do not satisfy such rules, identifying all power and ground pins properly may reduce the number of reported false errors significantly.

By the same token, since probe pads that are not bonded out on a product may also be evaluated by the DRC deck, it's advisable to identify them as power or ground pads. Otherwise, another means of eliminating DRC evaluation of certain subcells is to specify them as Calibre "exclude cell" command line arguments.

One poor design practice is to connect IO pads directly to active diffusions in the digital core. In true digital products, IO pads are always routed thru a buffer circuit that satisfies the latch-up rules. Unbuffered IO lines will create periphery in the core, which usually results in large numbers of LUP.B.c violations.

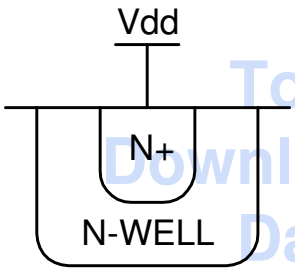
One source of confusion regarding the Jazz LUP DRC rules is the definition of guard ring. Guard rings recognized by Calibre must be completely closed in ACTIVE. This may be more conservative than but is not inconsistent with the physical guidelines above. Metal strapping on the ring can be broken, but a broken active path will not qualify as a guard ring.

10.1 Definition of Terms for Latchup Rules

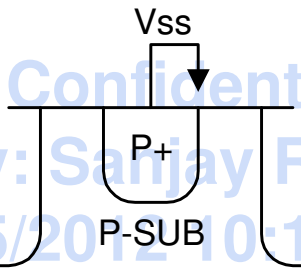
Active diffusion: An active diffusion is any FET source/drain, P+ active in a Nwell, or N+ active in the substrate. NPN base and collector diffusions should be considered active diffusions for the purpose of defining “periphery”.

Guard bar: A guard-bar is defined as a tie-down in well or substrate strapped solidly to the appropriate power bus. See Figures LR.1 and LR.2. A well-tie (see below) qualifies as an n-type guard bar for active diffusions in the same well, provided it lays in between the active in question and the substrate (preferably lining the interior perimeter of the nwell), as does a substrate-tie (see below) for active diffusions in the substrate, provided it lays in between the active in question and any adjacent nwell. Jazz DRC rules only recognize complete ring guard bars.

Double Guardbar: A double guard-bar between p+ active in nwell and n+ active in substrate consists of a p-type guard ring enclosing the n+ active polygons, and an n-type guard ring enclosing the p+ active polygons.

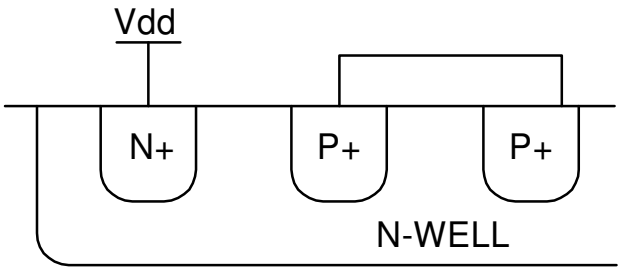


LR.1 N+ GUARD-BAR



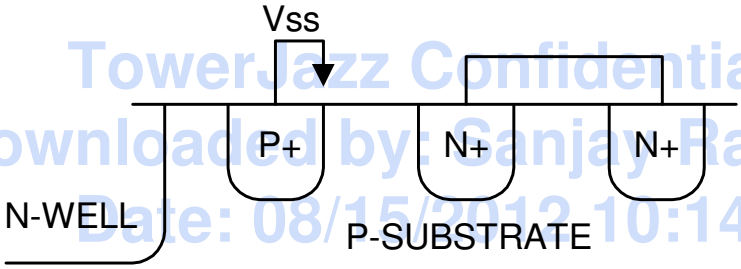
LR.2 P+ GUARD-BAR

Well-tie: An Nwell tie is defined as a N+ active in an N-well solidly strapped to the appropriate power bus, for a N- well containing P+ active diffusion. Figure LR.3



LR.3 N-WELL TIE

Substrate-tie: A substrate-tie is defined as a P+ active in the substrate solidly strapped to the appropriate bus, for the substrate containing N+ active diffusion. Figure LR.4



LR.4 P-SUBSTRATE TIE

Periphery: For the purposes of latch-up, the device periphery is defined as any geometry less than or equal to 60µm from any diffusion directly connected to an I/O pad.

I/O pad: Any pad not identified as connected to power or ground.

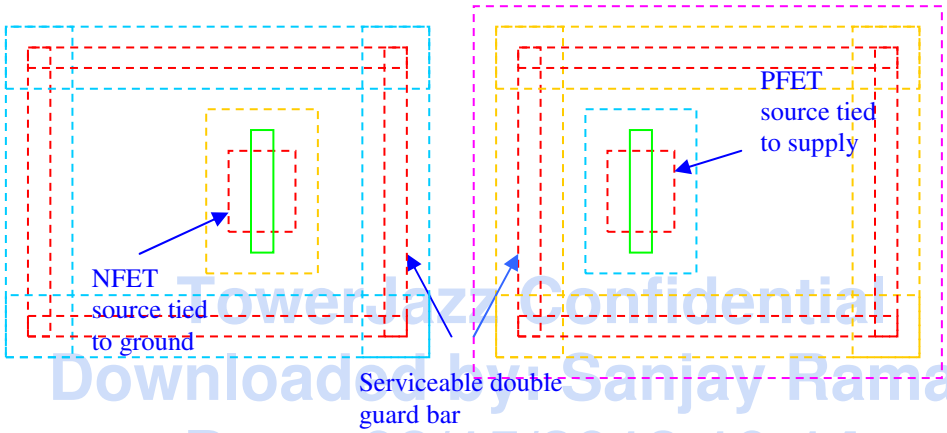
Directly Connected: Connected by metal 1, metal 2, metal 3, metal 4, metal 5, metal 6, poly or diffusion.

Clarifications:

1. Jazz latch-up rules are broken down into groups that apply to “Core” and “Periphery” regions of layout. “Core” rules apply everywhere on the chip. “Periphery” regions are a subset of the core generated 60um about active diffusions tied to IO pad.

2. Guard rings need to be continuous in ACTIVE in order to be recognized as complete rings.

3. It’s not necessary to use isolated guard bars to satisfy rules such as LUP.B.C.c1. It’s acceptable to use body-tie downs lining the interior perimeter of an nwell as serviceable n+ guard bars, instead of a discrete nwell with n+ contact. The figure below illustrates NMOS and PMOS transistors isolated by double body-tie guard rings (relevant to LUP.B.C.c1)



10.2 Latchup Rules

10.2.1 Latch-up Rules for Circuitry in the Device Periphery:

See Illustration LR.1

Rule No.	Rule Name	SBC18
LUP.B.C	Minimum space between an N+ diffusion in the substrate tied to ground to a P+ diffusion in an N-well tied to supply:	
LUP.B.C.a	Tag all periphery N+ diffusions that are in the substrate and connected to the power supply ground or Vss(o).	
LUP.B.C.b	Tag all periphery P+ diffusions that are connected to a high side power supply or Vgg (Vdd for thin oxide I/O) that are also in N Wells tied to Vgg (Vdd).	
LUP.B.C.c	Minimum space between all P+ diffusions tagged in LUP.B.C.b from all N+ diffusions tagged in LUP.B.C.a if not isolated by double guard rings.	35
#LUP.B.C.c1	Minimum space between all P+ tagged in LUP.B.C.b from all N+ diffusions tagged LUP.B.C.a in which there is a “double guardbar” between the aforementioned P+ diffusions and the N+ diffusions. See “double guardbar” in LUP definition section. **Note: This is a recommended rule (not checked)**	15
LUP.D	All wells in the periphery, (except the floating wells under pads and Nwell resistors) must be surrounded by a well-tie ring with a break no greater than 2µm. An external ring of P+ guard-bar is recommended.	
LUP.D.c	Latch-up rule LUP.D does not apply for N-wells which are used as well resistors. An external ring of P+ guard-bar must surround n-well resistors in the periphery.	
LUP.E	A P+ guard bar must surround all substrate areas containing N+ active diffusions in the periphery. An external ring of N+ guard-bar is recommended.	
LUP.F.a	Any P+ diffusion directly connected to an I/O pad must be contained in an isolated well. Well isolation is defined in Rule LUP.D. (A P+ region connected to a pad must be in a well)	

LUP.F.b	Any N+ diffusion directly connected to an I/O pad must be isolated from other N+ diffusions. This isolation is defined in Rule LUP.E. (Does not apply to Nwell drain resistors on an I/O pad)	
LUP.G.a	Maximum separation between adjacent power bus contacts in a guard bar (LUP.G.a.n for well tie, or LUP.G.a.p for substrate-tie diffusion). A maximum of 20µm is recommended.	100
LUP.Q	All nwells tied to ground should be surrounded by a complete ring substrate tie-down	

False violations may be caused by rule over-simplificaton

- LUP.D should apply to nwell tied to supply.
- LUP.E should apply to n+diffusions and nwell tied to ground.

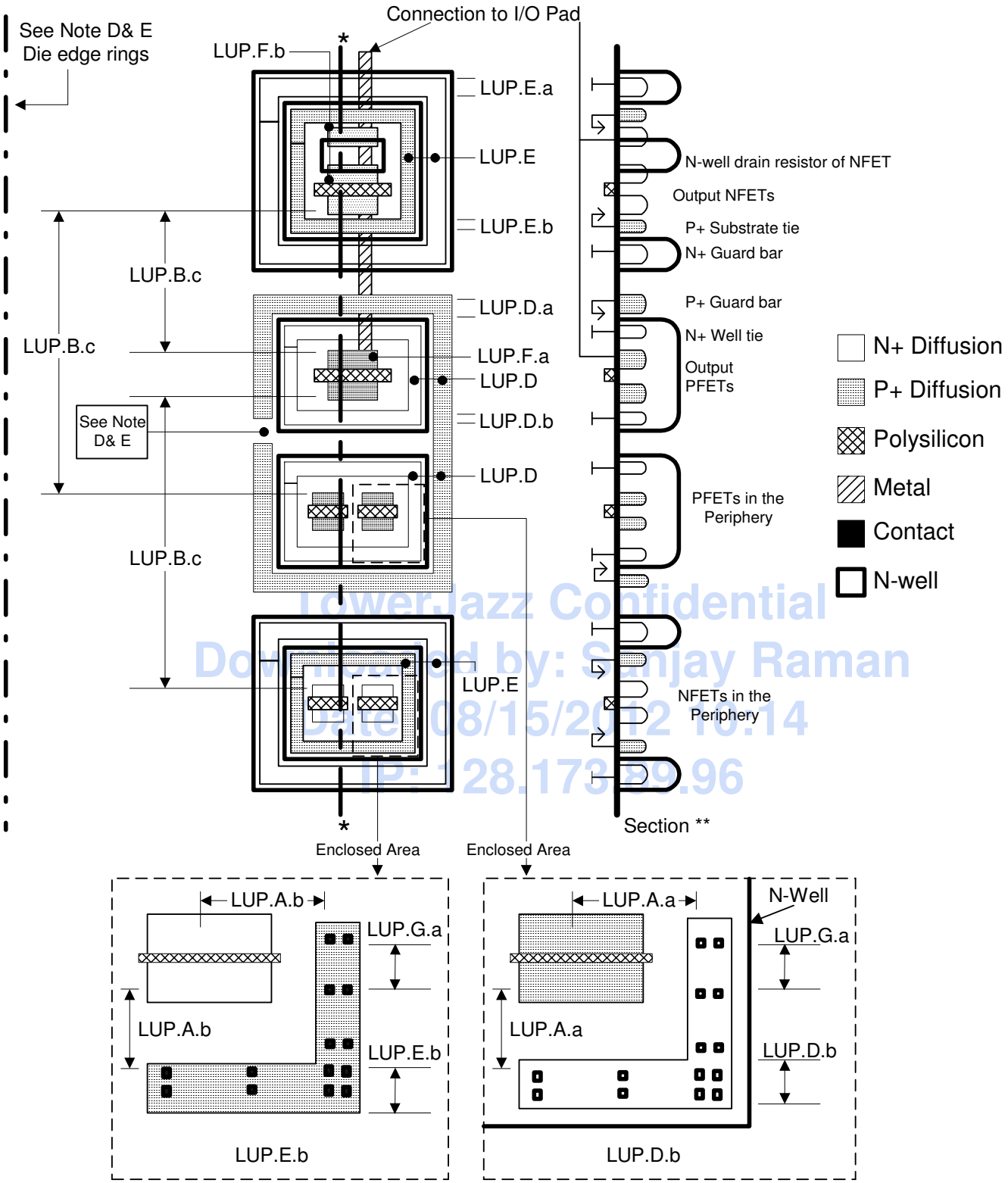


ILLUSTRATION LR.1 Latch-up rules for device periphery

10.2.2 Latch-up Rules for Internal Circuitry

Rule No.	Rule Name	SBC18
LUP.H	All N-wells containing p+ active must contain a guard-bar or a well-tie diffusion except for Nwells under pads.	
LUP.I.a	Maximum space in X or Y directions between any point in a P+ active diffusion and its nearest well-tie contact in the same well	30
LUP.I.b	Maximum space in X or Y directions between any point in an N+ active diffusion and its nearest substrate contact.	30

False violations may be caused by rule over-simplificaton

- LUP.H should apply to nwell tied to supply.

Devices that inject appreciable currents into the substrate during normal operation should be surrounded by strong or complete ring substrate tie-downs.

- P+/nwell diodes under forward bias
- PNP transistors

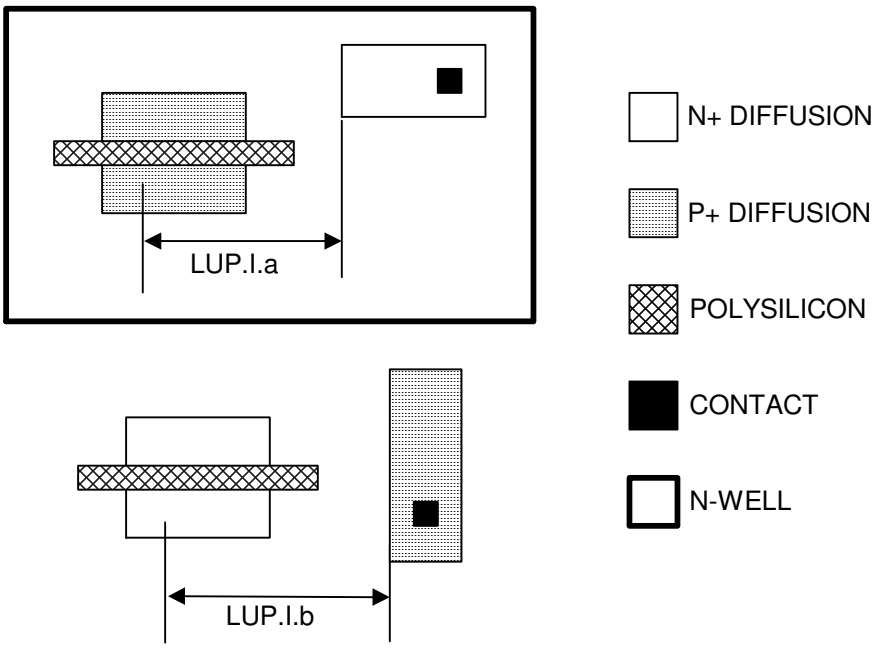
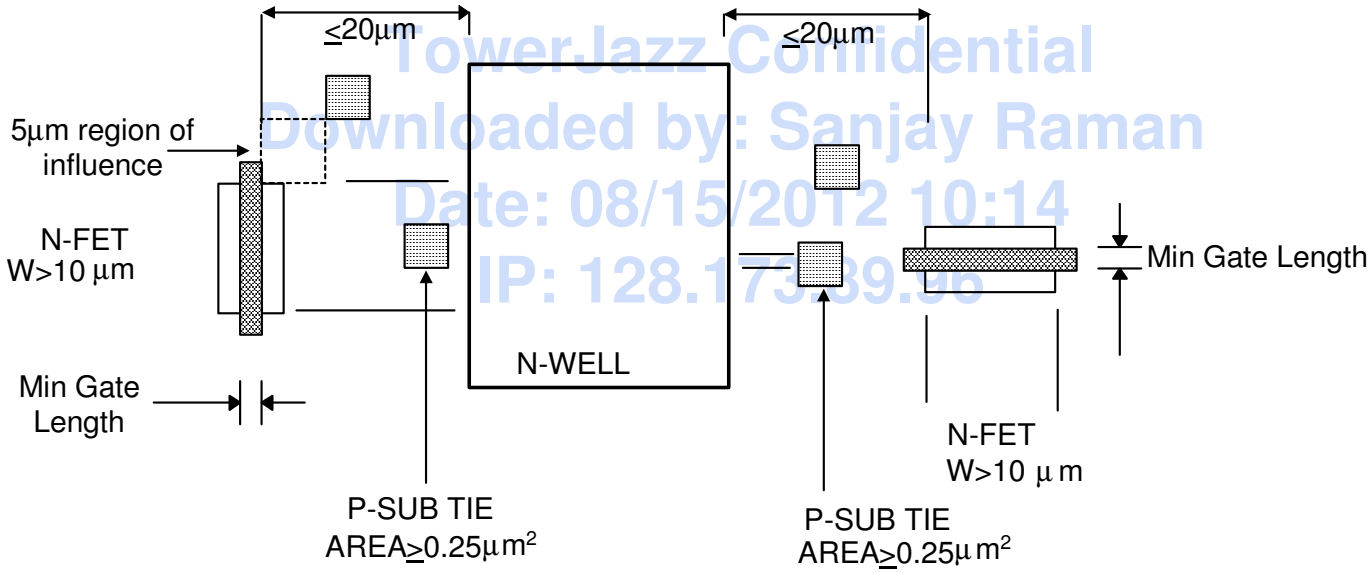


ILLUSTRATION LR.2 Latch-up rules for internal circuitry



LUP.I.d Special Nfet Psub-Tie Rules

11 Soft ERC Rules

The soft ERC checks identify layout topology that could induce electrical failure. Some definitions of terminology include,

Ntap: n+ active inside nwell
Ptap: p+ active inside p substrate
Digital substrate: Substrate region not covered by layer 62
Analog substrate: Substrate region covered by layer 62

Check Name	Check Description
Floating_poly	Poly is not connected to a Jazz supported device terminal or bond pad
Floating_met1_net	Metal 1 is not connected to a Jazz supported device terminal or bond pad
Floating_ met2_net	Metal 2 is not connected to a Jazz supported device terminal or bond pad
Floating_ met3_net	Metal 3 is not connected to a Jazz supported device terminal or bond pad
Floating_ met4_net	Metal 4 is not connected to a Jazz supported device terminal or bond pad
Floating_gate	Gate is not connected to a Jazz supported device terminal or bond pad
Floating_dpsub	Digital substrate with active component does not have ptap
Floating_apsub	Analog substrate with active component does not have ptap
SOFT.N	Ntap has no connection to power, ground, or pFET terminal
Nwell_no_tap	Nwell with active component has no ntap
SOFT.P	Ptap has no connection to ground
SOFT.PC	Ptap has no connection to bonding pad
Ptap_pwr	Ptap is connected to a power pad
Ntap_gnd	Ntap is connected to ground pad
Gate_pwr_gnd	Power or ground is connected to both source and drain of the same transistor
Power_pdiff_in_grounded_nwell	Forward biased diode between power and ground
Shorting_thru_nwell	Ntaps at different potential are shorted thru nwell
Shorting_thru_dpsub	Ptaps at different potential are shorted through digital substrate
Shorting_thru_apsub	Ptaps at different potential are shorted thru analog substrate

12. Artifact Region

Artifact regions are defined to be regions within the artifact marking layer (layer 45, datatype 0). Provision for artifact region is made to allow customers to draw non circuit data such as company logo, part number, revision number or letters. Only basic manufacturing design rules are checked. All other checks, such as LVS, are not performed within artifact regions.

1) Jazz does not require to have any non circuit data such as company logo, part number, revision number or letters

2) Basic manufacturing DRC violations within the artifact regions are flagged by *.artifact design rule checks. All checked rules must pass without violation.

3) As drawn data is preserved within artifact regions. Only reverse active layer generation is performed within the artifact regions. No other layer generation is performed within the artifact regions.

The following guidelines may be used for artifacts.

A) Use minimum number of layers such as metals and/or poly in artifact regions

B) If contact or via layers *must* be used, they must consist of a field of minimum sized contacts and vias (i.e. no large-area contacts or vias), with all poly and metal overplots consistent with the design rules. Text or artifacts on contact and via layers must have an underlying metal or poly plate and an overlying metal plate.

C) According to CMOS mask naming convention, the letters I, O, Q, S, X, and Z are not allowed. The following part number and revision letter/characters are acceptable for symbolic designs:

A B C D E F G H J K L M N P R T U V W Y

1 2 3 4 5 6 7 8 9 0 -

.

12.1 Good Layout Procedures for Enhanced Yields

A. Good circuit layout procedures can enhance yields. Some suggested practices are:
   1) Allow more than minimum spaces for metals and poly wherever possible.
   2) Allow extra overplot of contacts, via via2s, via3s, via4s, and via5s wherever possible.
   3) Allow more than minimum spaces for active wherever possible.
   4) Place extra substrate and well ties in the circuits and it is best to put the ties between transistors and the well boundaries for latchup immunity.
   5) Eliminate or minimize the antennas, including the ROM area.
   6) Do not allow small slivers and slits to be generated on the reticles.
   7) Move the contacts, vias, via2s, via3s, via4s and via5s in from the metal edge by an extra 0.25µm for wide metal lines with a line of many (>4) contacts, vias, via2s, via3s, via4s and via5s.
   8) Avoid the use of angled polygons. Try to step the angled line with large steps, if possible. If you must use angled polygons, try to use only 45-degree sides. These hints will significantly help to reduce the size of the generated Mebes (CATS) data.
   9) Use slits in metal layers (for stress relief reasons) at corner intersection that maintain good current flow.
   10) Design rule ST.D (recommended minimum/maximum slit length of 100/300um), this is an unchecked rule. Please pay attention when tapping large current in/out of a slotted line and make sure that the current loading is even on both sides of the slit.

Procedures 1, 2, 3, 4 and 5 are the most important practices that can improve yields and reliability margin.

B. General practice for analog/RF sections
1) Larger devices match better (except for very large devices which can match worse).
2) Keep matched devices close together, as matching degrades with distance.
3) Use symmetric layouts to improve matching (mirror image layouts do not prevent offsets caused by resist thickness variations).
4) Be aware of offsets caused by temperature variations across the die.
5) Reduce contact and via resistance variations by using extra contacts and vias where possible.
6) Use dummy capacitors to improve capacitor matching. Use common centroid layouts for larger capacitors.
7) Use dummy resistors to improve resistor matching. Use the same orientation and width for matched resistors.
8) Use common centroid FETs to improve matching. Use the same orientation and current flow direction for matched FETs. Be aware that source/drain capacitance can be affected by the presence of adjacent active.
9) Minimize antennas on matched FETs.

C. It is recommended to place the layer identifications on the same side of the chip, within 1,000µm of the design data extends.

13. Scribe Line and Die Seal Rings

This section describes the rules for the scribe lane and the die seal rings. See illustrations BD2 in Section 8.1.1 and SB. All rules in this Scribe Line section are drawn dimensions and polarities.

13.1 Die Seal Rings

Every circuit placed on wafer is required to have a die seal ring. This includes all circuits placed on test chips and MPW (multi project wafers) runs. The die seal rings are made of two components; white space and rings. White space is the separation of the circuit data to the ring data and is 13µm wide – it is truly blank space. The actual ring data is 12µm wide and made of layers: Active, P+ Implant, Contact, Metals and Vias. The final structure looks like a P+ Substrate tie with all layers of metal. The outermost edge of the ring data is line-on-line with the edge of the scribe lane.

The figure below shows the relationship between circuit, scribe, and seal ring data. Seal rings in essence expand the circuit data by 25µm on each edge (13µm white space and 12µm rings).

Die Seal Rings are added by Jazz ONLY to the circuit data. Jazz does not recommend customers to do die seal ring. If absolutely necessary, contact Jazz representative.

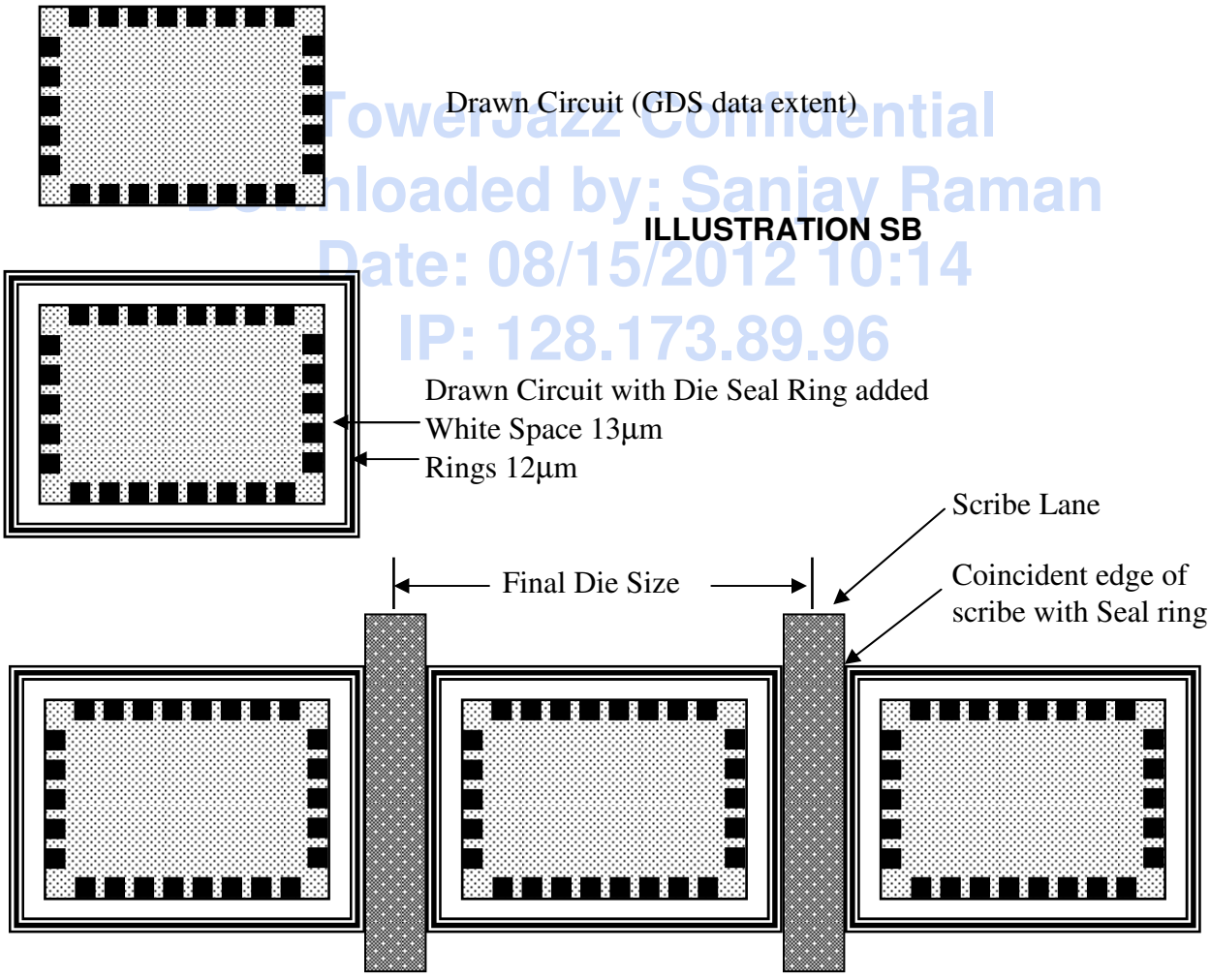


ILLUSTRATION SB

The following rules are not checked and are for reference only

Rule No.	Rule Name		SBC18HX, SBC18HXL ,SBC18HA	SBC18PT	SBC18QTD, SBC18QTR, SBC18QTL, SBC18QW	SBC18MW, SBC18MWD , SBC18MV
SB.A	**Recommended** width of white space (rings to any layer of circuit)		13	13	13	13
SB.B	Total width of white space and rings		25	25	25	25
SB.C	Width of:	a) Active Ring	12	12	12	12
		b) Reverse - Active ring	6	6	6	6
		c) Contact ring	3 contact slots			
		d) Metal 1 ring	6.35	6.35	6.35	6.35
		e) Via ring	2 via slots			
		f) Metal 2 ring	6.35	6.35	6.35	6.35
		g) Via2 ring	3 via2 slots			
		h) Metal 3 ring	6.35	6.35	6.35	6.35
		j) Via3 ring	2 via3 slots			
		k) Metal 4 ring	6.35	6.35	6.35	
		g) Via4 ring	3 via4 slots			
		h) Metal 5 ring	6.35	6.35		
		j) Via5 ring	2 via5 slots			
		k) Metal 6 ring	6.35			
		l) P+ implant ring	12	12	12	12
		m) N+ implant ring	none	None	none	none
		n) N-well ring	none	None	none	none
		o) Field implant ring	none	None	none	none

Note1: The contact and via slot widths are equal to the width of the square contacts or vias allowed in the corresponding process variant

13.2 Scribe Lines

Scribe Lines are spaces between die seal ring for saw cutting. It does not have any circuit data. However, process control and monitoring structures are put in the scribe line. The minimum widths of the scribe lines are limited by the dimensions of these structures. The minimum widths for the vertical scribe and the horizontal scribe are described in the table below.

Note: The scribe lanes do not have the silox opened.

Summary Table for Seal ring, vertical Scribes and Horizontal Scribes

Process variant	Seal ring width (SB.B)	Minimum Vertical Scribe Width	Minimum Horizontal Scribe Width
SBC18*	25	82	82

14. Memory Rules

Jazz provided SRAMs and SRAMs generated by Jazz-provided memory compilers may not follow all design rules in this document. The design rule check (DRC) decks provided by Jazz have special checks for such SRAMs and will pass them without violations. Exceptions in the DRC decks for such SRAMs may only be used with Jazz provided SRAMs and SRAMs generated by Jazz provided memory compilers. Any other structures using these design rule exceptions will be rejected by Jazz.

Non Jazz provided SRAMs should follow Jazz logic rules as specified in Section 4.