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TITLE:

Design Application Note for the SBC18H2 Family of Processes

REV	REVISION DESCRIPTION	DATE
00	Initial release – high risk version. Starting point NPB_PS_0267_Rev8 dated 9/26/03 and NPB-PS-0179 Rev 6 dated 9/26/03.	01/26/04
00.a	1. Update NPN rules: restrict only 0.15um (B1), minimum to 0.76 (B2), base contact – EP to 0.275 (B8), minimum slot contact to 0.86um (B38), minimum BL to 4.76 (4.A), minimum BP to 1.495um (23.A), minimum EP to 0.55um (29.A), minimum SC to 1.695um (21.A). 2. Update HS NPN Espec center in sect. 9.1. 3. Remove all references to PJ/JP layer change (Sec 4)	2/17/04
00.b	1. Removed all reference to DNW version. 2. More verbose descriptions included in Chap 1 and 5. 3. Corrected NPN Illustration in Chap 5.	3/2/04
1.0	1. Remove reference LC and replace with HS. 2. Added 2fF MiM using DUV specifications as starting point. 3. Removed mention of nWell and LVR resistors – no change from SBC18.	5/3/04
2.0	1. L-PNP and BL VAR removed. 2. Nominal NPN specifications updated 3. Specified minimum width and space rules including 4.B, 21.B, 29.B, 29.C, 33.A, and 33.B in Sect 5.2. 4. Updated cautionary disclaimer in footer to meet quality requirements 5. Changed rule B18 to 0.6um.	9/28/2004
3.0	All – Add HV Resistor devices 7 - Updated Bipolar Electrical parameters	03/26/2007
4.0	Add SBC13HA process integration information Update descriptions to use low/medium voltage as primary differentiator	6/15/2007
5.0	4.2 Added NWell2 layer Info in the Additional drawn layers table 5.2 Updated Design Rules 31.B and 33.B for SBC13.	9/13/2007
6.0	7.1 Updated electrical specifications for high speed NPN: Jc at peak Ft, Fmax, Cbe, Cbc, Ccs.	12/02/08
7.0	Updated document to include information on SBC18H2A and SBC18H2B variants	5/17/2011
8.0	1. Eliminated references to SBC13. SBC13 will now have its own document 2. Added information on SBC18H2C variant 3. Updated NPN design rules to allow 0.5um emitter width devices 4. Added Schottky Diode design rules and diagram 5. Added e-specs for 2.8 fF/um2, 5.6 fF/um2 and MIS capacitors for SBC18H2C	04/12/2012

TABLE OF CONTENTS

1 PURPOSE AND SCOPE

This document contains only additional information needed to design into SBC18H2 process variants. These processes are a variation of the SBC18 family of technologies. These processes are grouped together in one document because they share the central feature of a 200GHz SiGe HBT (heterojunction bipolar transistor). The front-end construction of the HBT and associated process modules are designed to offer a significant performance gain for this one device as compared with other existing SiGe BiCMOS technologies while maintaining transparent integration compatibility with all other active and passive components.

The back end metallization strategy is unchanged relative to other SBC18 processes. For the SBC18H2 family the closest process variant is SBC18HXL.

All differentiating information regarding the SBC18H2 process technology is detailed in subsequent chapters. This includes the process sequence, design kit layers, NPN design rules, and finally electrical specifications.

2 DESCRIPTION OF PROCESSES

The SBC18H2 processes have six layers of aluminum metal. The family consists of one standard offering (SBC18H2), and several variants. SBC18H2A and H2C are superset processes with the maximum functionality whereas H2B is a reduced-mask count process for cost savings. They support the following process features:

Device Family	Device	SBC18H2	SBC18H2A	SBC18H2B	SBC18H2C
CMOS	1.8V	X	X	X	X
	3.3V	X	X	X	X
Bipolar	200GHz / 2V SiGe HBT	X	X	X	X
	70GHz / 3.2V SiGe HBT	X	X	X	X
	Lateral PNP		X*		X*
Resistors	235 Ω/sq Poly	X	X	X	X
	1000 Ω/sq Poly	X	X		X
	NWell	X	X	X	X
	Silicided Poly	X	X	X	X
	TiN	X	X		X
Capacitors	2fF/μm^2 MIM	X	X	X	
	4fF/μm^2 Stacked MIM		X		
	2.8fF/μm^2 MIM				X
	5.6fF/μm^2 Stacked MIM				X
	2.3fF/μm^2 MIS				X
Inductors	2.8μm Al Top Metal	X	X	X	X
Diodes	Schottky Diode		X*		X*
	Buried Layer Varactor		X		
	MOS Varactor	X	X	X	X
Isolation	Deep Trench	X	X	X	X
	Deep NWell	X	X		X

* These devices are “free” devices that do not require an additional masking layer. They are only included in the SBC18H2A and H2C design kits for now but eventually will be made available for all SBC18H2 variants since they require no additional processing.

3 APPLICABLE DOCUMENTS

SBC18 Mask Requirement Specification	NPB-PS-0140
SBC18 Design Rules	NPB-PS-0179
SBC18 Electrical Specification	NPB-PS-0267
SBC18 Analog Characterization Report	NPB-PS-0392
SBC18 Design Manual	NPB-PS-0288
SBC18HX Reliability Data	NPB-PS-0449
Digital Design Manual	NPB PS-0402
Spice Data Bank	NPB-PS-0268

4 MASK SET

4.1 Reticle Layers per Process Sequence

Table 1: List of layers in order of process sequence for SBC18H2 and SBC18H2A

Layer No.	Layer Name	Mask Name	Field	Aligns to layer	SBC18H2	SBC18H2A	SBC18H2B	SBC18H2C
4	N+ Buried Layer	BL	Neg	Notch	X	X	X	X
36	Deep N Well	DNW	Neg	BL	X	X		X
0	Zero layer	ZL	Pos	BL	X	X	X	X
2	Active	A	Pos	ZL	X	X	X	X
15	Reverse active	RA	Neg	ZL	X	X	X	X
41	Deep Trench	DT	Neg	ZL	X	X	X	X
10	Collector Sinker	CS	Neg	ZL	X	X	X	X
3	Field Implant	F	Pos	ZL	X	X	X	X
1	Well	W	Neg	ZL	X	X	X	X
12	Dual Gate	DG	Pos	ZL	X	X	X	X
5	First Poly	FP	Pos	ZL	X	X	X	X
14	DN implant	DN	Neg	ZL	X	X	X	X
61	NK implant	NK	Neg	ZL	X	X	X	X
59	PK implant	PK	Neg	ZL	X	X	X	X
16	DP implant	DP	Neg	ZL	X	X	X	X
34	High Speed NPN implant	HS	Neg	ZL	X	X	X	X
21	Spacer Clear	SC	Neg	ZL	X	X	X	X
31	Emitter	EM	Pos	ZL	X	X	X	X
33	Emitter Window	EW	Neg	ZL	X	X	X	X
29	Emitter Poly	EP	Pos	ZL	X	X	X	X
23	Base Poly	BP	Pos	ZL	X	X	X	X
6	N+ Implant	NI	Neg	ZL	X	X	X	X
11	P+ Implant	PI	Neg	ZL	X	X	X	X
54	High Value Resistor Implant	HR	Neg	ZL	X	X		X
13	Varactor Implant	VAR	Neg	ZL		X		
40	Silicide Block	SB	Pos	ZL	X	X	X	X
7	Contact	C	Neg	ZL	X	X	X	X
8	First Metal (Metal 1)	M1	Pos	ZL	X	X	X	X
17	First Via (Via1)	VA	Neg	ZL	X	X	X	X
18	Second Metal (Metal 2)	M2	Pos	ZL	X	X	X	X
27	Second Via (Via2)	V2	Neg	ZL	X	X	X	X
30	2nd Top MIM capacitor plate	TM2	Pos	ZL		X		X
28	Third Metal (Metal 3)	M3	Pos	ZL	X	X	X	X
26	Metal Resistor	TR	Pos	ZL	X	X		X
37	Third Via (Via 3)	V3	Neg	ZL	X	X	X	X
22	Top MIM capacitor plate	TM	Pos	ZL	X	X	X	X
38	Fourth Metal (Metal 4)	M4	Pos	ZL	X	X	X	X
47	Via 4	V4	Neg	ZL	X	X	X	X

Layer No.	Layer Name	Mask Name	Field	Aligns to layer	SBC18H2	SBC18H2A	SBC18H2B	SBC18H2C
48	Fifth Metal (Metal 5)	M5	Pos	ZL	X	X	X	X
57	Via 5	V4	Neg	ZL	X	X	X	X
58	Sixth Metal (Metal 6)	M6	Pos	ZL	X	X	X	X
9	Protective Overcoat	S	Neg	ZL	X	X	X	X
Total Photo Layers					40	42	37	41
Total Reticles					39	41	36	40

4.2 Additional drawn layers:

Table 2: Additional Drawn Layers

Layer No.	Description	Layer Name	H2	H2A	H2B	H2C
5/2	Poly Pin layer	poly/pin	X	X	X	X
5/30	Poly Block (fill block) marking layer	poly/fill	X	X	X	X
5/31	Poly Fill (dummy fill) marking layer	poly/fill	X	X	X	X
8, 18, 28, 38, 48, 58/2	Metal 1-6 Pin layer	metal1/pin metal2/pin etc.	X	X	X	X
8, 18, 28, 38, 48, 58/30	Metal Block (fill block) marking layer	metal1/bk metal2/bk etc.	X	X	X	X
8, 18, 28, 38, 48, 58/31	Metal Fill (dummy fill) marking layer	metal1/fl metal2/fl etc.	X	X	X	X
114/0	Fuse marking layer	fusemrk	X	X	X	X
80/0	Resistor Marking layer. Used for ALL resistors	resdev	X	X	X	X
24/0	MIS Capacitor Marking Layer	C_Cell				X
64	NPN Marking Layer	N_cell	X	X	X	X
45/0	Artifact Layer	artifact	X	X	X	X
191/any	Reserved for Customer Use		X	X	X	X
68/0	PWell and Dummy Fill Block	nwell2	X	X	X	X
106/0	Schottky Diode Marking Layer	Schottky		X		X

5 DESIGN RULES FOR RF AND MIXED SIGNAL COMPONENTS

5.1 SiGe NPN Transistor Rules

The SiGe NPN rules are defined in this section. In SBC18H2, there are only two versions of NPN: (a) low voltage (high speed) NPN and (b) medium voltage (standard speed) NPN. In addition, the NPN modules differ significantly in design rules from the rest of the SBC18 family. To maintain continuity, the definition of the two NPN transistors maintains a consistency from a breakdown voltage standpoint only. One key distinction in the SBC18H2 process is that the medium voltage version no longer requires the LC layer (41) and therefore becomes the default if the Low Voltage version is not selected. In only this perspective, the SBC18H2 medium voltage device is analogous to the high voltage device found in the larger SBC18 family.

Bipolar devices are allowed in the following emitter configurations:

Width	0.15um or 0.5um
Length	Any value between 0.76um and 20um
Emitter Configurations	1 emitter, 2 bases, 1 collectors 1 emitter, 2 bases, 2 collectors 2 emitters, 3 bases, 2 collectors

Design rules for the Low Voltage NPN version are shown below. Also indicated in the note below, the Medium Voltage version can be derived from the Low Voltage version by removing the HS layer.

Table 3: Bipolar Transistor Design Rules

Rule No.	Rule Name	Rule (µm)
B1*	Emitter (EM) widths allowed	0.15,0.5
B2	Minimum emitter (EM) length	0.76
B2.a	Maximum emitter (EM) length	20
B3	Minimum/maximum emitter window (EW) overplot of emitter (EM)	0.1
B4	Minimum/Maximum emitter poly (EP) overplot of emitter (EM)	0.2
B5	Minimum/Maximum active overplot of emitter (EM)	0.2
B6**	Minimum/Maximum high speed (HS) collector overplot of emitter (EM). Applies only to Low Voltage NPN.	0.05
B7	Minimum base poly (BP) overplot of base active	0.35
B8	Minimum/Maximum distance from base contact to emitter poly (EP)	0.275
B9	Minimum/Maximum base poly (BP) overplot of base contact	0.1

* The PDK will allow 0.15 or 0.5um emitter widths for either the HS or MV device but the 0.5um width device is only modeled for the HS device.
**The Medium Voltage NPN version is default. To achieve the Low Voltage (High Speed) NPN, layer 34 must be included.

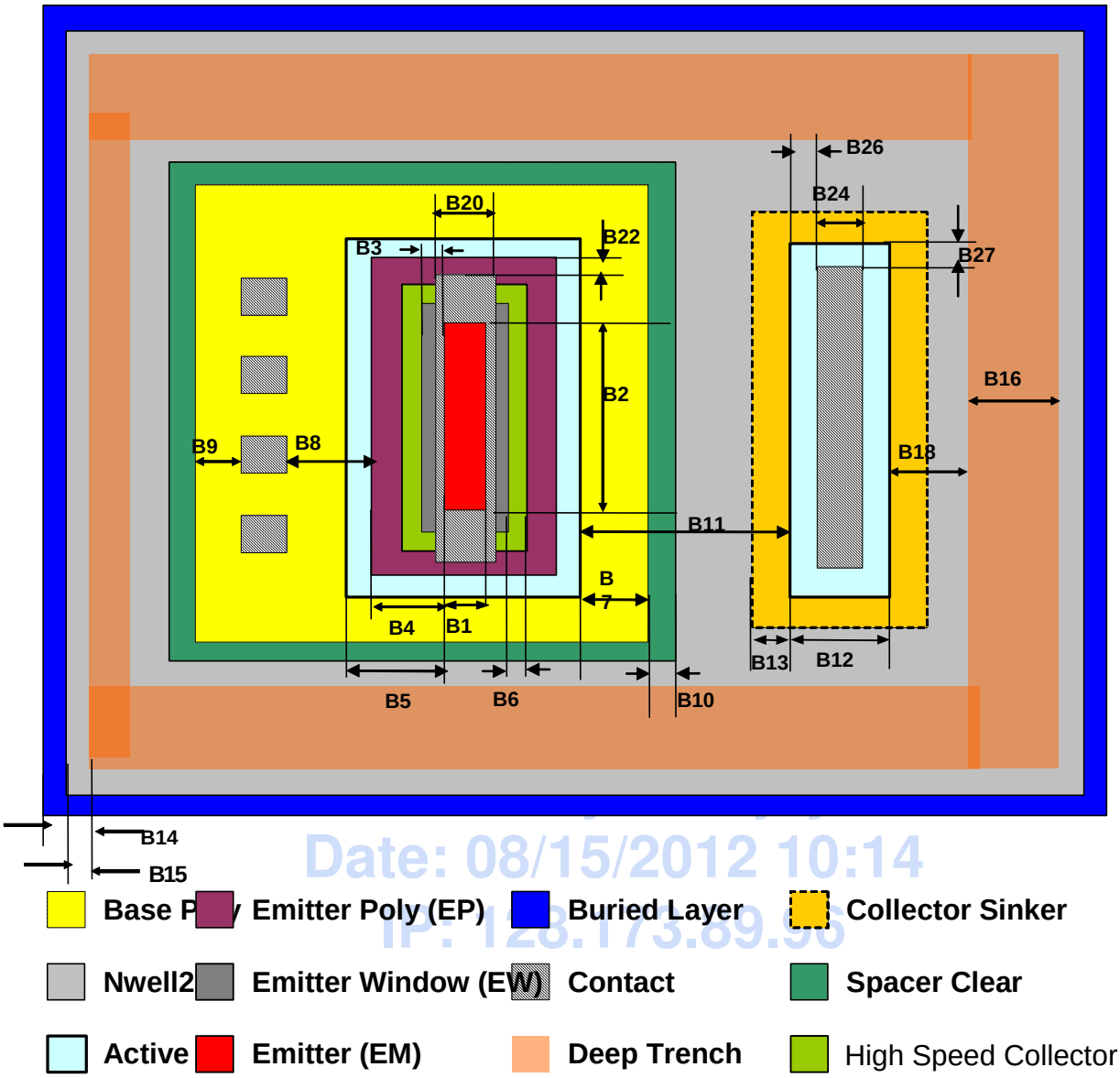

ILLUSTRATION NPN (Low Voltage NPN version)

Rule No.	Rule Name	Rule (µm)
B10	Minimum/Maximum spacer clear overplot of base poly (BP)	0.1
B11	Minimum distance from base active to collector sinker active	0.8
B12	Minimum/Maximum collector sinker active width	0.89
B13	Minimum/Maximum collector sinker implant overplot of collector sinker active	0.15
B14	Minimum/Maximum buried layer overplot of outer edge of deep trench	0.10
B15	Minimum/Maximum Nwell-2 overplot of outer edge of deep trench	0.10
B16	Minimum/Maximum deep trench width	1.20
B17	Minimum space deep trench to deep trench	1.80
B18	Minimum/Maximum deep trench space to active	0.60
B19	Maximum distance between deep trench and substrate contact	30
B20	Minimum/Maximum emitter slot contact width	0.30
B21	Minimum emitter slot contact to emitter slot contact space	0.30
B22	Minimum emitter poly (EP) overplot of emitter slot contact	0.1
B23	The emitter slot contact (or slot contact array) has to be centered with respect to emitter poly (EP)	
B24	Minimum/Maximum collector sinker slot contact width	0.36
B25	Minimum collector sinker slot contact to collector sinker slot contact space	0.30
B26	Minimum/Maximum collector sinker slot contact to active parallel to long edge of collector sinker slot contact	0.265
B27	Minimum/Maximum collector sinker slot contact to active parallel to short edge of collector sinker slot contact	0.15
B28	Minimum Metal 1 overplot of slot contact (both collector sinker and emitter)	0.1
B29	Minimum/Maximum slot via1 width	0.30
B30	Minimum slot via1 to slot via1 space	0.30
B31	Minimum metal 1 and 2 overplot of slot via1	0.1
B32	Maximum slot emitter contact, slot collector contact and slot via length	25
B33	Analog block border (layer 95) must cover NPN extent	
B34	Slot contacts and vias are allowed only inside collector sinker active and emitter poly	
B35	It is required that all NPNs have (and be surrounded by) substrate contacts	
B36	No first poly (layer 5) is allowed within N_cell marking layer	
B37	No first poly (layer 5) is allowed on deep trench (layer 41)	
B38	Minimum slot emitter contact, slot collector contact and slot via length	0.86
B39	Minimum space ‘slotted contact’ to ‘contact’	0.4
B40	Minimum space ‘slotted via’ to ‘via’	0.5

5.2 Additional rules for devices using bipolar layers

Table 4: Additional Design Rules Pertaining to Bipolar Layers

Rule No.	Rule Name	Rule (µm)
4.A	Minimum buried layer (BL) width	4.96
10.A	Minimum collector sinker (CS) width	0.8
4.B	Minimum space buried layer (BL) to buried layer (BL)	1.60
21.A	Minimum spacer clear (SC) width	1.695
21.B	Minimum spacer clear (SC) space	1.79
23.A	Minimum base poly (BP) width	1.495
23.B	Minimum base poly (BP) space	1.99
29.A	Minimum emitter poly (EP) width	0.55
29.B	Minimum emitter poly (EP) space	0.62
29.C	Minimum overplot base poly (BP) to emitter poly (EP)	0.35
31.B	Minimum space emitter (EM) to emitter (EM)	1.12
33.A	Minimum emitter window (EW) width	0.35
33.B	Minimum emitter window (EW) to emitter window (EW) space	0.95
40.A	Minimum silicide block (SB) width	0.50
41.B	T-shaped and cross-shaped deep trenches are not allowed (deep trench sharing is not allowed)	
68.A	Minimum Nwell-2 width	4.00
68.B	Minimum Nwell-2 space outside P_cell marking layer	0.9
68.C	Minimum distance Nwell-2 to Nwell	4.00
68.D	Minimum distance Nwell-2 to unrelated N+ active*	4.00
68.E	Minimum distance Nwell-2 to unrelated P+ active*	0.35
68.F	Minimum Nwell-2 space inside P_cell marking layer	1.60
68.G	Substrate contacts must exist directly between Nwell-2, and Nwell placed within 30 um of Nwell-2	
68.H	Substrate contacts must exist directly between Nwell-2 and unrelated N+active* placed within 30 um of Nwell-2	

* N+/P+ active is defined as any active region intersecting N+ or P+ implants.

5.3 Hyper-Abrupt Junction Varactor (SBC18H2A only)

The layout of hyper-abrupt junction varactor diodes should follow the rules below in order to obtain devices with low series resistance and high Q. This varactor is a multi-finger P/N diode in the form of N(PNPN…P)N. The p+ anode active region is formed using the varactor implant (cascaded p+/n implant) on active on N- epi. The N+ cathode region is formed by the collector sinker implant on active connected to buried layer in the same manner as the collector sinker in the bipolar transistors. See **Error! Reference source not found.** below.

Table 5: Hyper-abrupt junction varactor rules

Rule No.	Rule Name	Value (um)
VAR.1	Min/Max Varactor Implant Overplot of Anode Active	0.15
VAR.2	Min. Spacing Cathode Active to Anode Active	0.9
VAR.3.a	Min Anode Active Width (recommended width=1.4um)	0.5
VAR.3.b	Max Anode Active Width (recommended width=1.4um)	10
VAR.4.a	Min Anode Active Length	20
VAR.4.b	Max Anode Active Length	50
VAR.5	Min Cathode Active Width (equivalent to NPN rule B12)	0.89
VAR.6.a	Min Cathode Active Length (must be equal to anode active length)	20
VAR.6.b	Max Cathode Active Length (must be equal to anode active length)	50
VAR.7	Min/Max Collector Sinker Overplot of Cathode Active (equivalent to NPN rule B13)	0.15
VAR.9.a	Min Space from NWell2 to Substrate Contact Ring (substrate contact ring must be present)	1.5
VAR.9.b	Max Space from NWell2 to Substrate Contact Ring (substrate contact ring must be present)	2
VAR.10	Min/Max BL overplot of outermost active	1.8
VAR.12	Min/Max NW2 overplot of outermost active	1.8
VAR.19	Min Analog Block (layer 95) overplot of NW2 enclosing varactor fingers	1
13.A	Minimum Varactor Implant Mask Width	0.5
13.B	Minimum Varactor Implant Mask Space	0.7

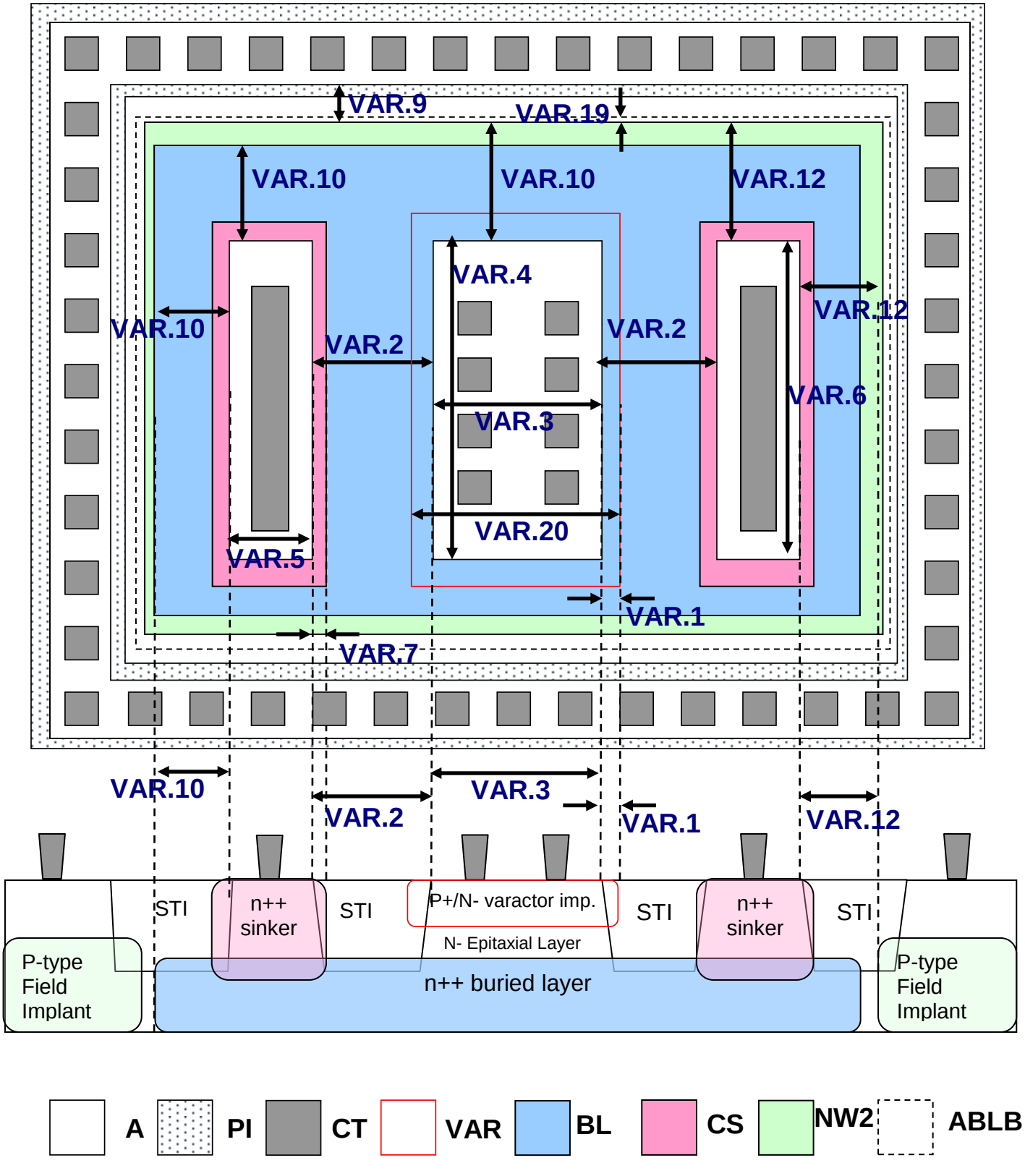

Figure 1: Hyper-abrupt Junction Varactor cross section and layout illustration

5.4 Schottky Diode Design Rules

The Schottky diode rules are defined in this section. The Schottky diode is formed by creating a silicided contact directly onto an area of unimplanted N- epitaxial silicon (by using the NWell2 layer to block the p-type field implant). Rings of both silicide block and P+ implant are used around the circumference of the anode active region in order to minimize parasitic leakage current. The extrinsic cathode is formed in exactly the same manner as the extrinsic collector region in the NPN device; using the collector sinker and BL masks.

Note: Schottky diode anode active areas must be square. The device size is scalable between 2x2µm^2 and 5x5µm^2 and then two larger discrete devices are available at 10x10µm^2 and 20x20µm^2.

Table 6: Schottky Diode Design Rules

Rule No.	Rule Name	Value (um)
SD.1	P+ overplot of anode active	0.38
SD.1.b	P+ extension inside anode active	0.38
SD.2	Extension of silicide block inside anode active	0.18
SD.3	Minimum cathode to anode active spacing	0.6
SD.4	Total silicide block width	0.56
SD.5	Schottky diode marking layer (lay 106) must cover full extent of device including DT	
SD.6	Cathode sinker active regions must be electrically connected by metal	

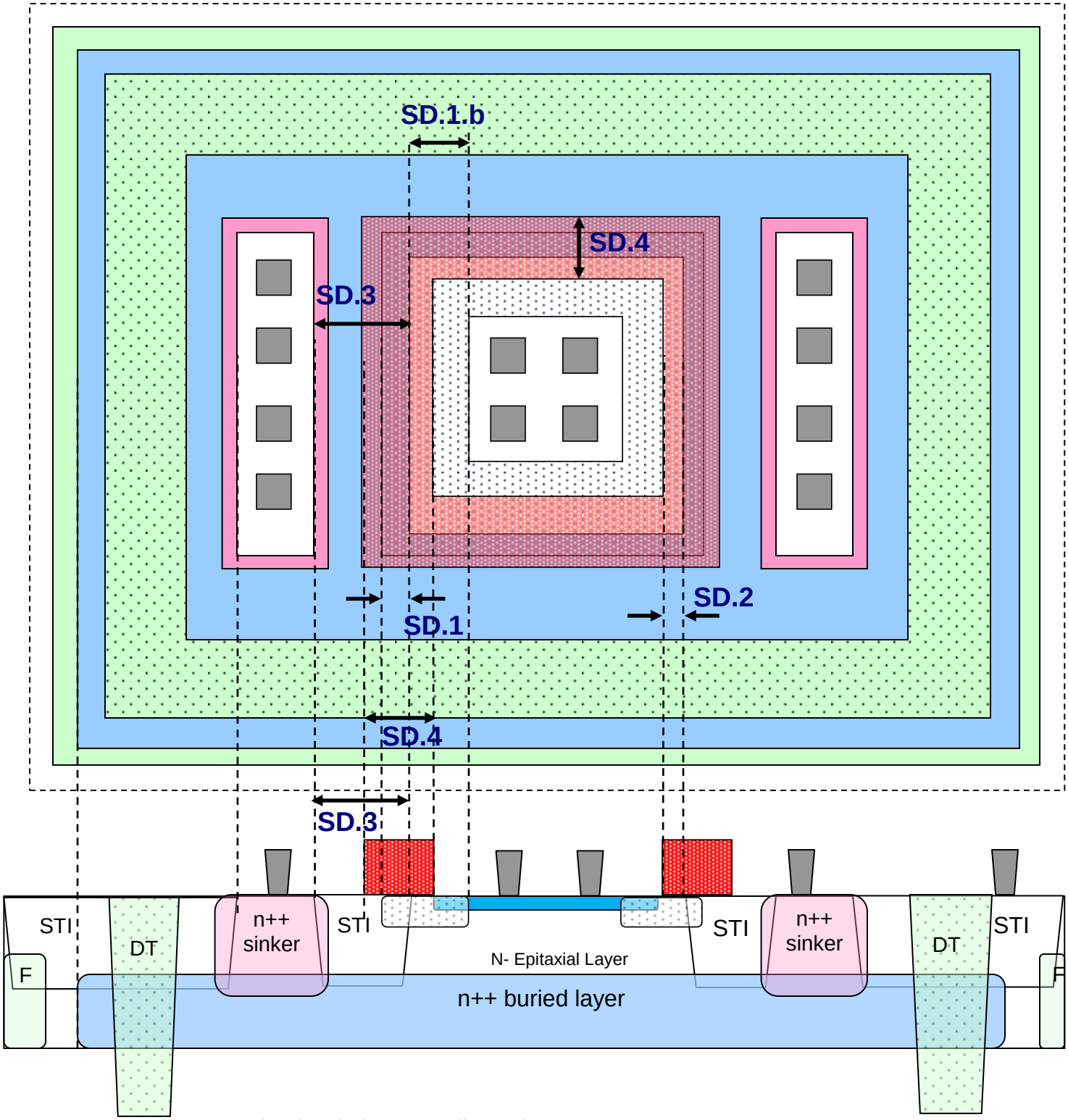

Figure 2: Schottky Diode Layout Illustration

A PI CT CS SB BL DT Schottky Marking Layer

Silicided Silicon

6 PROCESS PARAMETERS

6.1 Dielectric Thicknesses (final thickness)

Table 7: Dielectric Thicknesses

Description	Min.	Nom.	Max.	Units
SiGe poly base to substrate (silicon under STI)	2.1	2.8	3.5	Kangstroms
Poly to substrate (silicon under STI)	2.1	2.8	3.5	Kangstroms
Metal 1 to poly 1	4.5	6.5	8.5	Kangstroms
Metal 1 to diffusion	6.6	8.6	10.6	Kangstroms
Metal 1 to Emitter Poly	1.0	3.1	5.2	Kangstroms
Metal 1 to collector sinker	6.6	8.6	10.6	Kangstroms
Metal 1 to substrate (silicon under STI)	9.3	11.4	13.5	Kangstroms
See SBC18 Electrical Specification document for remaining layer thicknesses				

7 BIPOLAR AND MIXED SIGNAL ELECTRICAL PARAMETERS

7.1 SiGe NPN Transistors

Table 8: Electrical Specifications for SiGe HBTs. Specs are all for 0.15x10um Single Emitter, Double Base, Double Collector configuration.

Description	Low Voltage NPN			Medium Voltage NPN			
	Min	Nom	Max	Min	Nom	Max	Units
Beta (Je = 10mA/um2) Je = 26uA/um2	100	300	600	100	300	600	(none)
Ic at Vbe = 0.7V		10			10		uA
Va (Jc = 0.1mA/um2)	60			100			V
Bvceo	1.5	1.9	2.3	2.5	3.2	3.8	V
Bvebo (Je = 10mA/um2)		1.2			1.2		V
Bvcbo		5.8			10.0		V
Ft* at Vcb = 0.5V	180	200	220	65	75	85	GHz
Jc at peak Ft		10.7			1.5		mA/um2
Fmax** at Vcb = 0.5V		196			200		GHz
Cbe (0 V)	18.8	20.8	22.8	18	20	22	fF
Cbc (0 V)	17.3	18.3	19.3	9.0	9.9	10.8	fF
Ccs (0 V)	9	11.6	14.2	11.7	14.6	17.5	fF

*Ft is extracted from 20dB/dec. of ac gain (h21) measured at 15GHz for the low voltage NPN, and 5GHz for the medium voltage NPN
**Fmax is extracted from 20dB/dec. of unilateral gain (U) measured at 15GHz

7.2 Metal-Insulator-Metal (MIM) Cap. (2fF/μm^2 density)

(SBC18H2, H2B and H2A only) These vertical MIM capacitors are situated between M4 and M5. The TM layer forms the top plate of the capacitor with a thin nitride film as the dielectric.

Table 9: Electrical Specifications for 2fF/μm^2 MIM Cap.

Description	Min.	Nom.	Max.	Units
Area Capacitance	1.7	2.0	2.3	fF/μm^2
Perimeter Capacitance	0.2	0.4	0.6	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.	-60	-40	-20	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient	TBD	20	TBD	ppm/°C
Absolute Applied Voltage Bias			5	V
Leakage current @25C, 10V (area: 60,000um^2)			10	nA

7.3 Stacked Metal-Insulator-Metal (MIM) Cap. (4fF/μm^2 density)

(SBC18H2A only) These vertical MIM capacitors combine the capacitor described in section 7.2 above with another identical capacitor between M3 and M4. The TM2 layer forms the top plate of the second capacitor with a thin nitride film as the dielectric. A sheet of M4 between the two capacitors acts as one of the terminals of the combined capacitor while M5 and M3 must be shorted together to form the opposite terminal.

Table 10: Electrical specifications for 4fF/um2 stacked MIM cap.

Description	Min.	Nom.	Max.	Units
Area Capacitance	3.4	4	4.6	fF/μm^2
Perimeter Capacitance	0.4	0.6	0.8	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.	-20	0	20	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient	TBD	20	TBD	ppm/°C
Absolute Applied Voltage Bias			5	V
Leakage current @25C, 10V (area: 60,000um^2)			10	nA

7.4 Metal-Insulator-Metal (MIM) Cap. (2.8fF/μm^2 density)

(SBC18H2C only) These vertical MIM capacitors are similar to those described in section 7.2 above except they employ a thinner dielectric layer and thus have a higher capacitance density. They are still built between M4 and M5 and obey identical design rules as the 2fF/μm^2 devices.

Table 11: Electrical specifications for 2.8 fF/um2 MIM cap.

Description	Min.	Nom.	Max.	Units
Area Capacitance	2.34	2.75	3.16	fF/μm^2
Perimeter Capacitance	0.05	0.15	0.25	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.	-70	-50	-30	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient		20		ppm/°C
Absolute Applied Voltage Bias			3.6	V
Leakage current @25C, 10V (area: 60,000um^2)			10	nA

7.5 Stacked Metal-Insulator-Metal (MIM) Cap. (5.6fF/μm^2 density)

(SBC18H2C only) These vertical MIM capacitors combine the capacitor described in section 7.4 above with another identical capacitor between M3 and M4. The TM2 layer forms the top plate of the second capacitor with a thin nitride film as the dielectric. A sheet of M4 between the two capacitors acts as one of the terminals of the combined capacitor while M5 and M3 must be shorted to form the opposite terminal.

Table 12: Electrical specifications for 5.6fF/um2 stacked MIM cap.

Description	Min.	Nom.	Max.	Units
Area Capacitance	4.68	5.5	6.33	fF/μm^2
Perimeter Capacitance	0.1	0.3	0.5	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.	-10	0	10	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient		20		ppm/°C
Absolute Applied Voltage Bias			3.6	V
Leakage current @25C, 10V (area: 60,000um^2)			20	nA

7.6 Metal-Insulator-Semiconductor (MIS) Cap.

(SBC18H2C only) This device is formed by using the collector sinker mask from the bipolar transistor layout to implant a heavily-doped region underneath the gate of a 3.3V FET. The added doping serves both to enhance the oxidation rate of the silicon surface during gate oxidation and also to create a highly conductive bottom plate for the capacitor, leading to a much lower capacitance variation across voltage than one would see for a simple MOS capacitor using a standard FET gate.

Table 13: Electrical specifications for the MIS cap.

Description	Min.	Nom.	Max.	Units
Area Capacitance	2	2.3	2.6	fF/μm^2
Perimeter Capacitance	0.07	0.1	0.13	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate.		-1030		ppm/V
Quadratic Voltage Coefficient (QVCC)		-120		ppm/V^2
Temperature Coefficient		25		ppm/°C
BV_{GO} (oxide breakdown voltage)	10			V
Max. Applied Voltage Bias*			5.5	V

* The maximum applied bias is based on a 10 year TDDB lifetime for the device and is thus much lower than BV_{GO}

7.7 Hyper-abrupt junction varactor (SBC18H2A only)

The data below is for a device with 20 1.4um wide x 30um long anode fingers.

Table 14: High Performance BL Varactor Electrical Specifications

Description	Low	Nom	High	Units
Capacitance at 0V	**2.1**	**2.6**	**3.1**	**pF**
Capacitance Sensitivity*	**14**	**16**	**18**	**%**
Q (at 1.9GHz, 0.5V)	**65**	**100**		
Leakage at 2.5V			**20**	**nA**

* Capacitance Sensitivity = (Cap @ 0.5V - Cap @ 2.5V)/(Cap @ 0.5V + Cap @ 2.5V)

7.8 Schottky Diode

The data below is for a 20x20um device.

Table 15: Schottky Diode Electrical Specifications

Description	Low	Nom	High	Units
V_{ON} (I_F=100µA)	**0.26**	**0.305**	**0.35**	**V**
Leakage (V_R=3.3V)			**16**	**nA**
Breakdown	**10.5**			**V**
Capacitance (V=0)	**13.2**	**14.5**	**15.8**	**fF**
R_S		**42**		**Ω**

7.9 Lateral PNP

The data below is for a 1x1um emitter device.

Table 16: Lateral PNP Electrical Specifications

Description	Low	Nom	High	Units
Beta (J_E=10nA/µm^2)	**4.6**	**7.4**	**13.3**	
V_A (J_C=10nA/µm^2)	**20**			**V**