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TITLE:

ANALOG CHARACTERIZATION REPORT OF THE SBC18 PROCESSES: SBC18HX, SBC18PT, SBC18QTD, SBC18QTR, SBC18QW, SBC18MW

REV	Revision Description	Date
01	Initial Release	05/07/2003

TABLE OF CONTENTS

1. Purpose and Scope

This document covers both process and device parameters for the Jazz Semiconductor SBC18 technology family. The specifications shown below are intended to reflect the mean and ±3 sigma variation of parameters at 25ºC unless otherwise specified. This manual documents all SBC18 family devices. Table 1 lists the available devices of each SBC18 process variant.

Devices	SBC18HX	SBC18PT	SBC18QTD	SBC18QTR	SBC18QW	SBC18MW
High Voltage FET	☒	☒	☒	☒	☒	☒
Low Voltage FET	☒	☒	☐	☐	☐	☐
High Speed NPN w/ DT[1]	☒	☐	☐	☐	☐	☐
Standard NPN w/ DT	☒	☐	☒	☒	☐	☐
High Voltage NPN w/ DT	☒	☐	☒	☒	☐	☐
Standard NPN w/o DT	☐	☒	☐	☐	☒	☒
High Voltage NPN w/o DT	☐	☒	☐	☐	☒	☒
Lateral PNP	☒	☒	☒	☒	☒	☒
Low Value Poly Resistor	☒	☒	☒	☒	☒	☒
High Value Poly Resistor	☐	☒	☒	☒	☒	☒
Salicided Poly Resistor	☒	☒	☒	☒	☒	☒
TiN Resistor[2]	☒	☐	☐	☒	☐	☐
Nwell Resistor	☒	☒	☒	☒	☒	☒
Varactor (ni)	☐	☐	☐	☐	☒	☒
Varactor (buried layer)	☒	☒	☒	☒	☐	☐
1fF MIM Capacitor	☒	☐	☐	☐	☐	☐
2fF MIM Capacitor	☐	☒	☒	☒	☒	☒
4fF Stack MIM Capacitor[2]	☐	☒	☐	☐	☒	☐

[1] DT: Deep Trench Isolation
[2] No information available at this time

Table 1: SBC18 device list

2. Applicable Documents

NPB PS-0267 SBC18 HX/PT Electrical Parameters
NPB PS-0174 SBC18 MW/QW/QTD/QTR Electrical Parameters

3. High Voltage FET Matching Characterization

Table of Contents

Summary

A FET matching characterization for the high voltage FETs in the SBC18 process has been performed. These devices are available in all sbc18 process variants. A simple model has been fit to the ∆Id data in order to help support design optimization. The test structures, test procedures, and test conditions are described in the appendix.

Measurement Results

It is important to determine whether the wafers used in this characterization represent the nominal electrical specifications. The following table presents the specifications for some of the most significant device parameters:

	NFET			PFET		
Parameter	Min	Nom	Max	Min	Nom	Max
10μm x 0.36μm 3.3v FET Vt (V)	0.52	0.62	0.72	-0.66	-0.76	-0.86
10μm x 0.36μm 3.3v FET Idsat (mA)	5.0	6.0	7.0	2.05	2.45	2.85

Note: These parameters are taken from the unreleased SBC18 electrical specification NPB PS-0267 Revision 5.

The following tables summarize the electrical characteristics of these lots characterized in this report:

NFET:

Mean Vt	Mean Idsat	3 Sigma Vt	3 Sigma Idsat
0.648	6.015	0.03	0.222

PFET:

Mean Vt	Mean Idsat	3 Sigma Vt	3 Sigma Idsat
-0.747	-2.833	0.027	0.201

For measurements involving a large number of samples, it is almost inevitable that there will be a few “bad points” which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these “bad points,” it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3 sigma limits. The standard deviation is then recalculated for the remaining points, and again, all points outside of the 3 sigma limits are removed. This process continues until all data points are within the 3 sigma limits of the distribution. The 3 sigma limits should only cause problems for very large sample sizes.

The three sigma (3 times the standard deviation) matching results for this characterization are presented in the following tables. Both the delta Vgs and delta Id matching results are a function of bias, and are presented with each bias point for all transistor sizes on a page.

The bias range used for this measurement is as follows:
NFET:

Vds	Vgst = Veff = Vgs - Vt
0.2V, 0.6V, 1.0V, 1.4V	0.1V, 0.3V, 0.5V

PFET:

Vds	Vgst = Veff = Vgs - Vt
-0.2V, -0.6V, -1.0V, -1.4V	-0.1V, -0.3V, -0.5V

The delta Vgs and delta Id results are shown with the associated currents which are the mean measured currents for each device. These currents will deviate from the nominal values presented in the electrical specification and the data bank, and are only provided for reference.

NFET Delta Vgs Results

NFET Standard Matched Pair Delta Vgs

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.2V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.1mV / 2.4uA	68.6mV / 2.2uA					
2um		38.2mV / 8.2uA					
5um	24.6mV / 22.4uA	25.1mV / 21.7uA				5.1mV / 1.3uA	
10um		17.9mV / 43.7uA	12.6mV / 27.9uA	7.3mV / 14.6uA			
20um	12.2mV / 86.2uA	13.2mV / 85.9uA	9.0mV / 54.9uA	5.2mV / 28.9uA	3.8mV / 12.9uA	2.6mV / 5.3uA	1.9mV / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.9mV / 43.4uA					
10um		12.9mV / 85.7uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.1mV / 438.8uA	4.4mV / 300.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.5mV / 26.4uA	
20um					1.2mV / 264.6uA	1.2mV / 106.6uA	1.0mV / 54.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.8mV / 86.5uA	12.9mV / 85.7uA
20 x 20um x 5um	1.0mV / 105.6uA	1.2mV / 106.6uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.6V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.1mV / 2.9uA	69.1mV / 2.6uA					
2um		38.4mV / 9.7uA					
5um	24.9mV / 26.9uA	25.3mV / 25.7uA				5.0mV / 1.3uA	
10um		18.1mV / 52.1uA	12.8mV / 29.9uA	7.2mV / 15.2uA			
20um	12.4mV / 103.1uA	13.4mV / 102.4uA	9.1mV / 58.7uA	5.1mV / 30.0uA	3.8mV / 13.2uA	2.6mV / 5.3uA	1.8mV / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		18.1mV / 51.2uA					
10um		13.0mV / 101.1uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.2mV / 513.9uA	4.5mV / 322.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.5mV / 26.8uA	
20um					1.1mV / 271.4uA	1.2mV / 108.3uA	1.0mV / 54.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	13.0mV / 103.6uA	13.0mV / 101.1uA
20 x 20um x 5um	1.0mV / 107.4uA	1.2mV / 108.3uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.0V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.5mV / 3.2uA	69.1mV / 2.9uA					
2um		38.6mV / 10.5uA					
5um	26.0mV / 29.7uA	25.5mV / 28.1uA				4.9mV / 1.3uA	
10um		18.3mV / 57.0uA	12.9mV / 30.7uA	7.2mV / 15.4uA			
20um	12.5mV / 113.2uA	13.6mV / 112.3uA	9.1mV / 60.4uA	5.1mV / 30.5uA	3.7mV / 13.4uA	2.5mV / 5.4uA	1.8mV / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		18.4mV / 55.7uA					
10um		13.2mV / 110.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.2mV / 556.4uA	4.5mV / 332.3uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.4mV / 27.0uA	
20um					1.1mV / 274.1uA	1.2mV / 109.0uA	1.0mV / 54.9uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	13.4mV / 113.7uA	13.2mV / 110.0uA
20 x 20um x 5um	1.0mV / 108.1uA	1.2mV / 109.0uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.4V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.7mV / 3.5uA	69.6mV / 3.1uA					
2um		38.9mV / 11.2uA					
5um	26.2mV / 32.0uA	25.7mV / 30.1uA				4.9mV / 1.3uA	
10um		18.4mV / 61.3uA	13.0mV / 31.4uA	7.2mV / 15.6uA			
20um	12.6mV / 121.8uA	13.7mV / 120.7uA	9.2mV / 61.8uA	5.1mV / 30.8uA	3.7mV / 13.5uA	2.5mV / 5.4uA	1.8mV / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		18.8mV / 59.5uA					
10um		13.3mV / 117.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.3mV / 592.5uA	4.5mV / 340.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.4mV / 27.1uA	
20um					1.1mV / 276.2uA	1.2mV / 109.5uA	1.0mV / 55.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	13.5mV / 122.3uA	13.3mV / 117.6uA
20 x 20um x 5um	1.0mV / 108.6uA	1.2mV / 109.5uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.2V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.3mV / 11.5uA	74.3mV / 10.9uA					
2um		37.8mV / 39.1uA					
5um	25.1mV / 107.5uA	25.0mV / 105.7uA				4.7mV / 6.3uA	
10um		17.6mV / 214.4uA	12.8mV / 141.3uA	7.6mV / 71.3uA			
20um	12.3mV / 426.3uA	13.2mV / 425.9uA	9.3mV / 280.8uA	5.5mV / 142.9uA	3.8mV / 63.4uA	2.5mV / 25.6uA	1.7mV / 12.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.2mV / 211.1uA					
10um		12.9mV / 422.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.2mV / 2,126.9uA	4.4mV / 1,497.2uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.4mV / 127.9uA	
20um					1.3mV / 1,291.1uA	1.1mV / 518.2uA	1.0mV / 260.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.6mV / 424.1uA	12.9mV / 422.6uA
20 x 20um x 5um	0.6mV / 517.2uA	1.1mV / 518.2uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.6V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	73.4mV / 14.7uA	73.2mV / 13.7uA					
2um		37.3mV / 49.0uA					
5um	25.2mV / 135.5uA	24.7mV / 132.3uA				5.1mV / 6.8uA	
10um		17.6mV / 268.8uA	12.8mV / 166.9uA	7.6mV / 81.3uA			
20um	12.1mV / 534.6uA	13.2mV / 533.5uA	9.2mV / 331.4uA	5.5mV / 162.6uA	4.0mV / 69.9uA	2.7mV / 27.7uA	2.0mV / 13.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.6mV / 263.8uA					
10um		12.8mV / 527.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.1mV / 2,643.8uA	4.4mV / 1,771.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.5mV / 138.4uA	
20um					1.3mV / 1,422.0uA	1.1mV / 559.9uA	1.0mV / 280.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.7mV / 533.4uA	12.8mV / 527.4uA
20 x 20um x 5um	0.7mV / 558.8uA	1.1mV / 559.9uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.0V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	73.8mV / 15.8uA	69.3mV / 14.5uA					
2um		37.6mV / 51.9uA					
5um	25.5mV / 144.4uA	24.9mV / 140.4uA				5.1mV / 6.9uA	
10um		17.8mV / 285.5uA	12.9mV / 171.3uA	7.5mV / 82.4uA			
20um	12.2mV / 568.6uA	13.4mV / 567.1uA	9.2mV / 340.1uA	5.5mV / 164.8uA	4.0mV / 70.5uA	2.7mV / 27.8uA	1.9mV / 14.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.8mV / 279.3uA					
10um		13.0mV / 558.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.2mV / 2,790.8uA	4.4mV / 1,818.6uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.5mV / 139.1uA	
20um					1.3mV / 1,433.9uA	1.1mV / 562.5uA	1.0mV / 280.9uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.9mV / 567.5uA	13.0mV / 558.3uA
20 x 20um x 5um	0.7mV / 561.4uA	1.1mV / 562.5uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.4V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.1mV / 16.6uA	69.7mV / 15.2uA					
2um		37.9mV / 54.1uA					
5um	25.8mV / 151.1uA	25.1mV / 146.5uA				5.1mV / 6.9uA	
10um		17.7mV / 298.2uA	12.9mV / 174.4uA	7.5mV / 83.2uA			
20um	12.4mV / 594.2uA	13.6mV / 592.4uA	9.3mV / 346.1uA	5.5mV / 166.4uA	4.0mV / 70.9uA	2.6mV / 27.9uA	1.9mV / 14.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		18.0mV / 291.0uA					
10um		13.1mV / 581.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		6.2mV / 2,901.8uA	4.5mV / 1,851.6uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.5mV / 139.5uA	
20um					1.2mV / 1,442.0uA	1.1mV / 564.4uA	1.0mV / 281.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	13.1mV / 593.4uA	13.1mV / 581.6uA
20 x 20um x 5um	0.7mV / 563.3uA	1.1mV / 564.4uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.2V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	76.1mV / 23.2uA	75.0mV / 21.8uA					
2um		38.8mV / 78.9uA					
5um	25.3mV / 215.6uA	26.3mV / 212.5uA				4.4mV / 13.4uA	
10um		17.8mV / 430.2uA	13.4mV / 290.1uA	8.0mV / 149.0uA			
20um	12.7mV / 853.5uA	13.7mV / 853.8uA	9.9mV / 575.9uA	5.8mV / 298.7uA	3.7mV / 134.1uA	2.4mV / 54.2uA	1.6mV / 27.3uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.9mV / 424.4uA					
10um		13.4mV / 848.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		5.5mV / 4,366.1uA	4.2mV / 3,134.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.4mV / 271.4uA	
20um					1.3mV / 2,794.8uA	1.2mV / 1,124.7uA	1.2mV / 563.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.9mV / 850.4uA	13.4mV / 848.9uA
20 x 20um x 5um	0.6mV / 1,122.5uA	1.2mV / 1,124.7uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.6V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	73.9mV / 33.7uA	74.0mV / 31.7uA					
2um		37.4mV / 113.7uA					
5um	25.0mV / 309.7uA	25.5mV / 304.5uA				5.3mV / 17.7uA	
10um		17.6mV / 617.0uA	13.0mV / 411.2uA	8.0mV / 207.6uA			
20um	12.3mV / 1,226.7uA	13.3mV / 1,225.5uA	9.6mV / 816.9uA	5.9mV / 415.9uA	4.2mV / 180.9uA	2.8mV / 71.6uA	2.1mV / 36.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.6mV / 609.0uA					
10um		13.0mV / 1,218.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		5.7mV / 6,204.0uA	4.2mV / 4,400.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.6mV / 358.2uA	
20um					1.3mV / 3,730.2uA	1.1mV / 1,473.0uA	1.1mV / 735.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.7mV / 1,224.7uA	13.0mV / 1,218.9uA
20 x 20um x 5um	0.7mV / 1,472.5uA	1.1mV / 1,473.0uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.0V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.2mV / 35.8uA	73.4mV / 33.4uA					
2um		37.5mV / 119.7uA					
5um	25.4mV / 327.0uA	25.2mV / 320.5uA				5.3mV / 17.7uA	
10um		17.7mV / 649.9uA	13.1mV / 422.9uA	8.0mV / 211.0uA			
20um	12.4mV / 1,292.8uA	13.5mV / 1,291.3uA	9.5mV / 839.9uA	5.9mV / 422.6uA	4.2mV / 182.5uA	2.8mV / 71.9uA	2.0mV / 36.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		17.8mV / 640.2uA					
10um		13.1mV / 1,280.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		5.6mV / 6,508.3uA	4.2mV / 4,522.3uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.6mV / 359.9uA	
20um					1.3mV / 3,762.3uA	1.1mV / 1,479.8uA	1.0mV / 738.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	12.9mV / 1,291.9uA	13.1mV / 1,280.9uA
20 x 20um x 5um	0.7mV / 1,479.3uA	1.1mV / 1,479.8uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.4V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	74.5mV / 37.1uA	72.8mV / 34.6uA					
2um		37.8mV / 123.5uA					
5um	25.6mV / 338.3uA	25.4mV / 331.0uA				5.3mV / 17.8uA	
10um		17.9mV / 671.2uA	13.2mV / 429.5uA	7.9mV / 212.8uA			
20um	12.5mV / 1,335.6uA	13.6mV / 1,333.8uA	9.6mV / 853.1uA	5.8mV / 426.4uA	4.2mV / 183.4uA	2.7mV / 72.1uA	2.0mV / 36.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		18.0mV / 660.1uA					
10um		13.3mV / 1,320.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		5.7mV / 6,702.5uA	4.3mV / 4,591.3uA				

Standard Matched Pairs: 20 Fingers

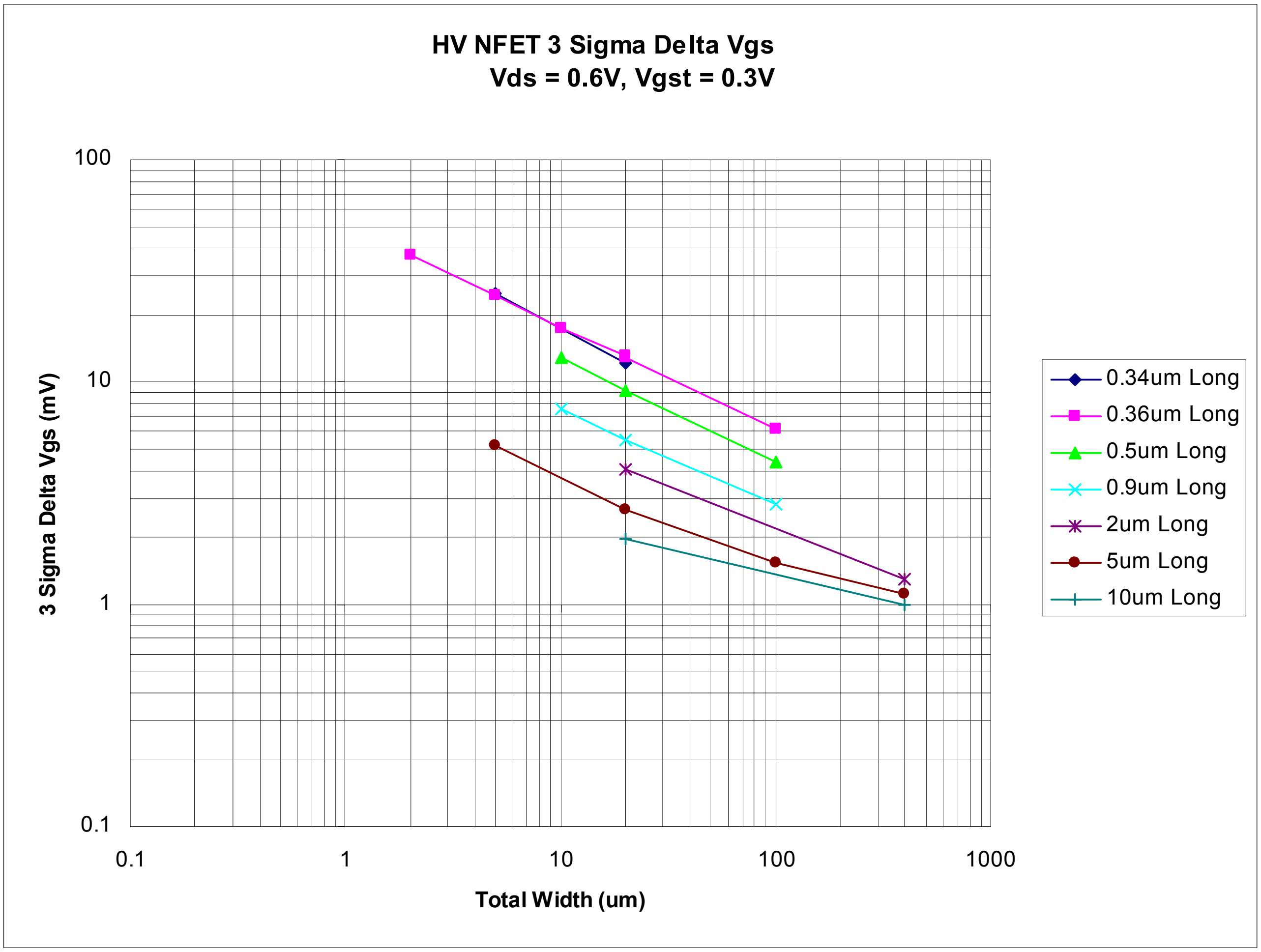
Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.6mV / 360.9uA	
20um					1.3mV / 3,780.2uA	1.1mV / 1,483.8uA	1.0mV / 739.3uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	13.1mV / 1,334.9uA	13.3mV / 1,320.4uA
20 x 20um x 5um	0.7mV / 1,483.3uA	1.1mV / 1,483.8uA

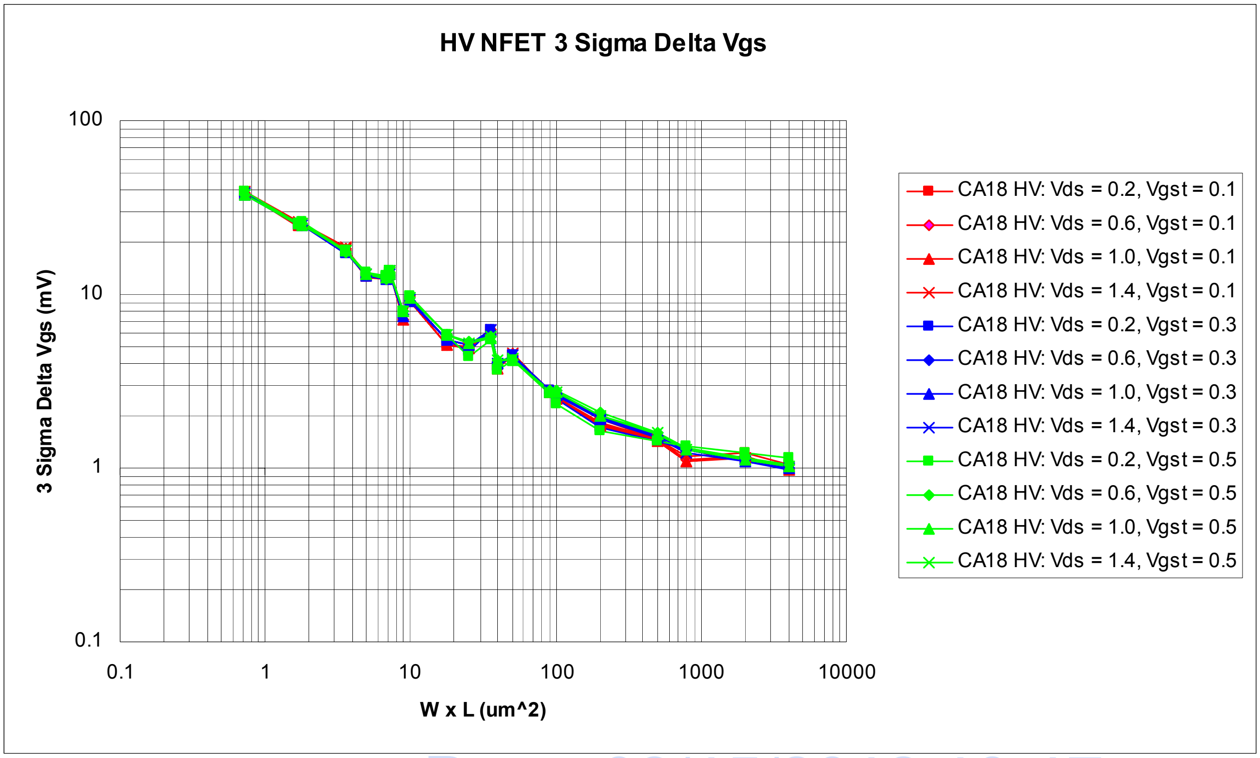
NFET Vgs Matching versus Device Size Plot

The following plot shows the Vgs matching versus device size for a representative (Vds = 0.6V and Vgst = 0.3V) bias point:



NFET Vgs Matching versus Device Area Plot

The following plot shows the Vgs matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ΔW and ΔL.

Fingers	Width	Length	Effective Drawn Area
1	2	0.36	0.72
1	5	0.34	1.7
1	5	0.36	1.8
2	5	0.36	3.6
1	10	0.36	3.6
1	10	0.50	5
1	20	0.34	6.8
2	10	0.36	7.2
1	20	0.36	7.2
1	10	0.90	9
1	20	0.50	10
1	20	0.90	18

Fingers	Width	Length	Effective Drawn Area
1	5	5.00	25
10	10	0.36	36
1	20	2.00	40
10	10	0.50	50
10	10	0.90	90
1	20	5.00	100
1	20	10.00	200
20	5	5.00	500
20	20	2.00	800
20	20	5.00	2000
20	20	10.00	4000

NFET Delta Id Results

NFET Standard Matched Pair Delta Id

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.2V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	94.4% / 2.4uA	79.8% / 2.2uA					
2um		43.9% / 8.2uA					
5um	29.4% / 22.4uA	29.4% / 21.7uA				5.7% / 1.3uA	
10um		21.4% / 43.7uA	15.4% / 27.9uA	8.4% / 14.6uA			
20um	14.7% / 86.2uA	16.0% / 85.9uA	11.1% / 54.9uA	6.1% / 28.9uA	4.4% / 12.9uA	3.0% / 5.3uA	2.1% / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		21.4% / 43.4uA					
10um		15.4% / 85.7uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		7.2% / 438.8uA	5.3% / 300.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.7% / 26.4uA	
20um					1.3% / 264.6uA	1.4% / 106.6uA	1.1% / 54.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	15.4% / 86.5uA	15.4% / 85.7uA
20 x 20um x 5um	1.1% / 105.6uA	1.4% / 106.6uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.6V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	95.6% / 2.9uA	79.4% / 2.6uA					
2um		44.1% / 9.7uA					
5um	29.1% / 26.9uA	29.6% / 25.7uA				5.7% / 1.3uA	
10um		21.5% / 52.1uA	15.6% / 29.9uA	8.5% / 15.2uA			
20um	14.7% / 103.1uA	16.1% / 102.4uA	11.4% / 58.7uA	6.1% / 30.0uA	4.4% / 13.2uA	2.9% / 5.3uA	2.0% / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		21.7% / 51.2uA					
10um		15.6% / 101.1uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		7.2% / 513.9uA	5.5% / 322.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.7% / 26.8uA	
20um					1.3% / 271.4uA	1.3% / 108.3uA	1.1% / 54.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	15.6% / 103.6uA	15.6% / 101.1uA
20 x 20um x 5um	1.1% / 107.4uA	1.3% / 108.3uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.0V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	93.0% / 3.2uA	78.3% / 2.9uA					
2um		43.7% / 10.5uA					
5um	28.8% / 29.7uA	29.2% / 28.1uA				5.6% / 1.3uA	
10um		20.6% / 57.0uA	15.7% / 30.7uA	8.5% / 15.4uA			
20um	14.5% / 113.2uA	16.0% / 112.3uA	11.4% / 60.4uA	6.1% / 30.5uA	4.3% / 13.4uA	2.9% / 5.4uA	2.0% / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		21.6% / 55.7uA					
10um		15.4% / 110.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		7.2% / 556.4uA	5.5% / 332.3uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.6% / 27.0uA	
20um					1.3% / 274.1uA	1.3% / 109.0uA	1.1% / 54.9uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	15.5% / 113.7uA	15.4% / 110.0uA
20 x 20um x 5um	1.1% / 108.1uA	1.3% / 109.0uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.4V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	91.0% / 3.5uA	77.0% / 3.1uA					
2um		44.0% / 11.2uA					
5um	28.5% / 32.0uA	28.9% / 30.1uA				5.6% / 1.3uA	
10um		20.4% / 61.3uA	15.8% / 31.4uA	8.4% / 15.6uA			
20um	14.4% / 121.8uA	15.8% / 120.7uA	11.4% / 61.8uA	6.1% / 30.8uA	4.3% / 13.5uA	2.8% / 5.4uA	2.0% / 2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		21.4% / 59.5uA					
10um		15.3% / 117.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		7.1% / 592.5uA	5.5% / 340.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.6% / 27.1uA	
20um					1.3% / 276.2uA	1.3% / 109.5uA	1.1% / 55.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	15.4% / 122.3uA	15.3% / 117.6uA
20 x 20um x 5um	1.1% / 108.6uA	1.3% / 109.5uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.2V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	37.2% / 11.5uA	34.8% / 10.9uA					
2um		19.0% / 39.1uA					
5um	12.2% / 107.5uA	12.4% / 105.7uA				2.4% / 6.3uA	
10um		8.7% / 214.4uA	6.5% / 141.3uA	3.9% / 71.3uA			
20um	6.1% / 426.3uA	6.6% / 425.9uA	4.7% / 280.8uA	2.8% / 142.9uA	2.0% / 63.4uA	1.3% / 25.6uA	0.9% / 12.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		8.7% / 211.1uA					
10um		6.4% / 422.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.1% / 2,126.9uA	2.2% / 1,497.2uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.8% / 127.9uA	
20um					0.7% / 1,291.1uA	0.6% / 518.2uA	0.5% / 260.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	6.3% / 424.1uA	6.4% / 422.6uA
20 x 20um x 5um	0.3% / 517.2uA	0.6% / 518.2uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.6V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	40.8% / 14.7uA	38.4% / 13.7uA					
2um		20.8% / 49.0uA					
5um	13.5% / 135.5uA	13.5% / 132.3uA				3.1% / 6.8uA	
10um		9.5% / 268.8uA	7.5% / 166.9uA	4.5% / 81.3uA			
20um	6.7% / 534.6uA	7.3% / 533.5uA	5.4% / 331.4uA	3.3% / 162.6uA	2.4% / 69.9uA	1.6% / 27.7uA	1.2% / 13.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		9.8% / 263.8uA					
10um		7.1% / 527.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.4% / 2,643.8uA	2.6% / 1,771.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.9% / 138.4uA	
20um					0.8% / 1,422.0uA	0.7% / 559.9uA	0.6% / 280.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	7.0% / 533.4uA	7.1% / 527.4uA
20 x 20um x 5um	0.4% / 558.8uA	0.7% / 559.9uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.0V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	40.8% / 15.8uA	37.6% / 14.5uA					
2um		20.7% / 51.9uA					
5um	13.6% / 144.4uA	13.5% / 140.4uA				3.0% / 6.9uA	
10um		9.5% / 285.5uA	7.6% / 171.3uA	4.5% / 82.4uA			
20um	6.6% / 568.6uA	7.3% / 567.1uA	5.5% / 340.1uA	3.3% / 164.8uA	2.4% / 70.5uA	1.6% / 27.8uA	1.1% / 14.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		9.8% / 279.3uA					
10um		7.1% / 558.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.3% / 2,790.8uA	2.6% / 1,818.6uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.9% / 139.1uA	
20um					0.7% / 1,433.9uA	0.7% / 562.5uA	0.6% / 280.9uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	7.0% / 567.5uA	7.1% / 558.3uA
20 x 20um x 5um	0.4% / 561.4uA	0.7% / 562.5uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.4V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	40.2% / 16.6uA	37.3% / 15.2uA					
2um		20.6% / 54.1uA					
5um	13.6% / 151.1uA	13.4% / 146.5uA				3.0% / 6.9uA	
10um		9.4% / 298.2uA	7.6% / 174.4uA	4.5% / 83.2uA			
20um	6.6% / 594.2uA	7.3% / 592.4uA	5.5% / 346.1uA	3.3% / 166.4uA	2.4% / 70.9uA	1.6% / 27.9uA	1.1% / 14.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		9.8% / 291.0uA					
10um		7.1% / 581.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.3% / 2,901.8uA	2.6% / 1,851.6uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.9% / 139.5uA	
20um					0.7% / 1,442.0uA	0.6% / 564.4uA	0.6% / 281.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	7.0% / 593.4uA	7.1% / 581.6uA
20 x 20um x 5um	0.4% / 563.3uA	0.6% / 564.4uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.2V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	18.5% / 23.2uA	17.8% / 21.8uA					
2um		9.5% / 78.9uA					
5um	6.1% / 215.6uA	6.3% / 212.5uA				1.2% / 13.4uA	
10um		4.3% / 430.2uA	3.4% / 290.1uA	2.1% / 149.0uA			
20um	3.0% / 853.5uA	3.3% / 853.8uA	2.5% / 575.9uA	1.5% / 298.7uA	1.0% / 134.1uA	0.6% / 54.2uA	0.4% / 27.3uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		4.3% / 424.4uA					
10um		3.2% / 848.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.3% / 4,366.1uA	1.0% / 3,134.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.4% / 271.4uA	
20um					0.4% / 2,794.8uA	0.3% / 1,124.7uA	0.3% / 563.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	3.1% / 850.4uA	3.2% / 848.9uA
20 x 20um x 5um	0.1% / 1,122.5uA	0.3% / 1,124.7uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.6V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	23.3% / 33.7uA	22.5% / 31.7uA					
2um		12.0% / 113.7uA					
5um	7.8% / 309.7uA	7.7% / 304.5uA				2.0% / 17.7uA	
10um		5.5% / 617.0uA	4.5% / 411.2uA	3.0% / 207.6uA			
20um	3.9% / 1,226.7uA	4.2% / 1,225.5uA	3.3% / 816.9uA	2.2% / 415.9uA	1.6% / 180.9uA	1.1% / 71.6uA	0.8% / 36.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		5.6% / 609.0uA					
10um		4.1% / 1,218.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.7% / 6,204.0uA	1.4% / 4,400.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / 358.2uA	
20um					0.5% / 3,730.2uA	0.4% / 1,473.0uA	0.4% / 735.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	4.0% / 1,224.7uA	4.1% / 1,218.9uA
20 x 20um x 5um	0.2% / 1,472.5uA	0.4% / 1,473.0uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.0V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	23.6% / 35.8uA	22.6% / 33.4uA					
2um		12.0% / 119.7uA					
5um	7.9% / 327.0uA	7.9% / 320.5uA				2.0% / 17.7uA	
10um		5.5% / 649.9uA	4.5% / 422.9uA	3.0% / 211.0uA			
20um	3.9% / 1,292.8uA	4.2% / 1,291.3uA	3.4% / 839.9uA	2.2% / 422.6uA	1.6% / 182.5uA	1.1% / 71.9uA	0.8% / 36.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		5.6% / 640.2uA					
10um		4.1% / 1,280.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.7% / 6,508.3uA	1.4% / 4,522.3uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / 359.9uA	
20um					0.5% / 3,762.3uA	0.4% / 1,479.8uA	0.4% / 738.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	4.1% / 1,291.9uA	4.1% / 1,280.9uA
20 x 20um x 5um	0.2% / 1,479.3uA	0.4% / 1,479.8uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.4V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	23.4% / 37.1uA	22.5% / 34.6uA					
2um		12.0% / 123.5uA					
5um	7.9% / 338.3uA	7.7% / 331.0uA				2.0% / 17.8uA	
10um		5.5% / 671.2uA	4.5% / 429.5uA	2.9% / 212.8uA			
20um	3.8% / 1,335.6uA	4.2% / 1,333.8uA	3.3% / 853.1uA	2.2% / 426.4uA	1.6% / 183.4uA	1.0% / 72.1uA	0.8% / 36.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		5.6% / 660.1uA					
10um		4.1% / 1,320.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.7% / 6,702.5uA	1.4% / 4,591.3uA				

Standard Matched Pairs: 20 Fingers

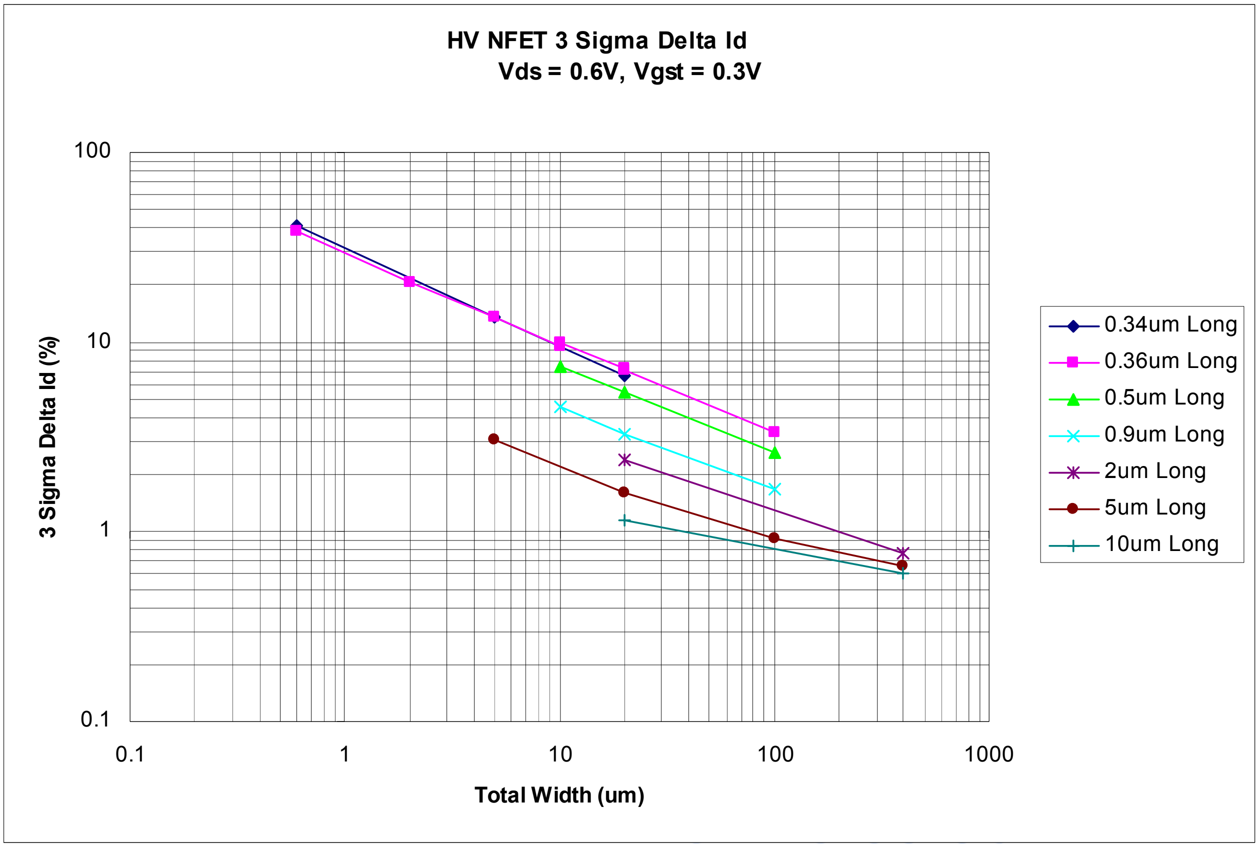
Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / 360.9uA	
20um					0.5% / 3,780.2uA	0.4% / 1,483.8uA	0.4% / 739.3uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	4.1% / 1,334.9uA	4.1% / 1,320.4uA
20 x 20um x 5um	0.2% / 1,483.3uA	0.4% / 1,483.8uA

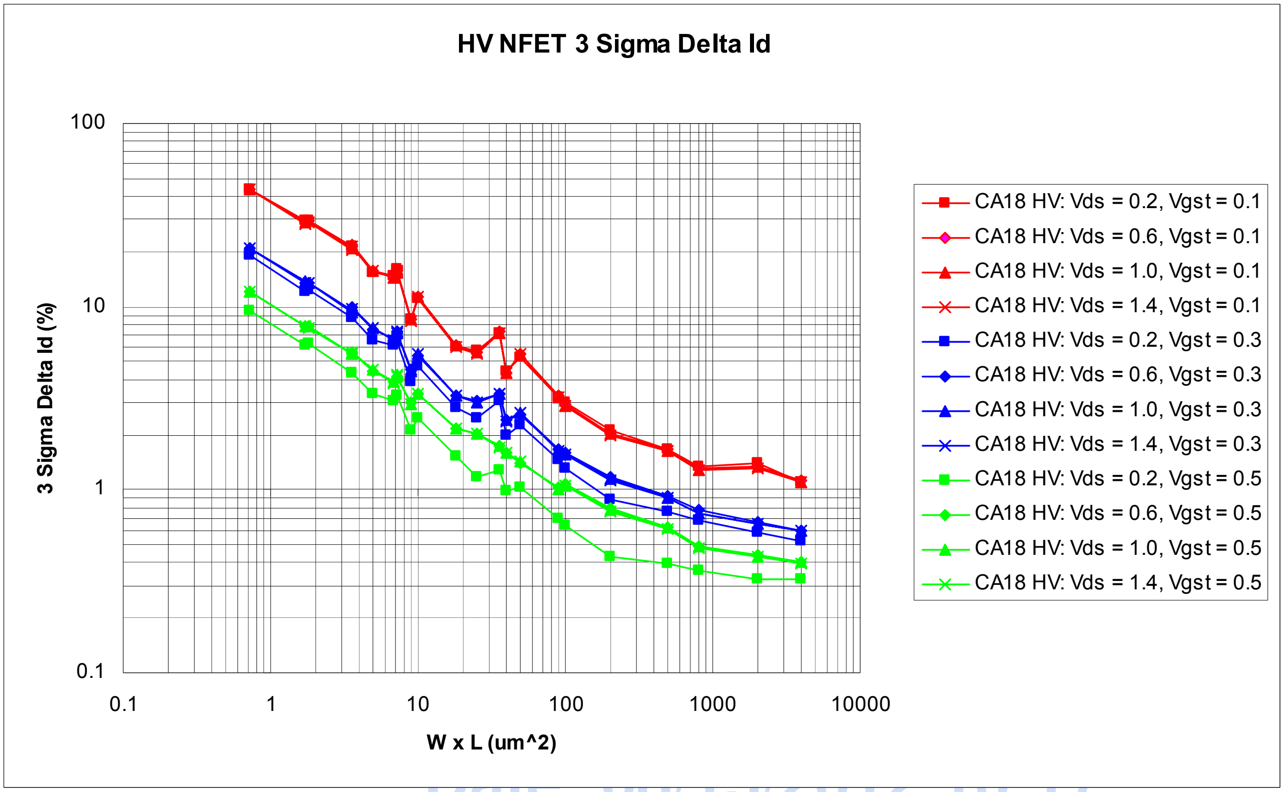
NFET Id Matching versus Device Size Plot

The following plot shows the Id matching versus device size for a representative (Vds = 0.6V and Vgst = 0.3V) bias point:



NFET Id Matching versus Device Area Plot

The following plot shows the Id matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ΔW and ΔL.

Fingers	Width	Length	Effective Drawn Area
1	2	0.36	0.72
1	5	0.34	1.7
1	5	0.36	1.8
2	5	0.36	3.6
1	10	0.36	3.6
1	10	0.50	5
1	20	0.34	6.8
2	10	0.36	7.2
1	20	0.36	7.2
1	10	0.90	9
1	20	0.50	10
1	20	0.90	18

Fingers	Width	Length	Effective Drawn Area
1	5	5.00	25
10	10	0.36	36
1	20	2.00	40
10	10	0.50	50
10	10	0.90	90
1	20	5.00	100
1	20	10.00	200
20	5	5.00	500
20	20	2.00	800
20	20	5.00	2000
20	20	10.00	4000

PFET Delta Vgs Results

PFET Standard Matched Pair Delta Vgs

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.2V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	55.2mV / -0.7uA	42.0mV / -0.5uA					
2um		26.2mV / -2.0uA					
5um	19.2mV / -7.0uA	17.1mV / -5.5uA				3.3mV / -0.3uA	
10um		11.3mV / -11.4uA	8.6mV / -7.1uA	5.8mV / -3.5uA			
20um	10.1mV / -29.0uA	9.4mV / -23.3uA	6.3mV / -14.5uA	4.3mV / -7.0uA	2.6mV / -2.9uA	1.8mV / -1.1uA	1.5mV / -0.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		11.7mV / -10.1uA					
10um		8.3mV / -21.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.6mV / -93.9uA	3.2mV / -62.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -5.1uA	
20um					0.9mV / -52.4uA	1.2mV / -21.2uA	1.7mV / -10.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.2mV / -22.8uA	8.3mV / -21.0uA

20 x 20um x 5um	0.6mV / -21.2uA	1.2mV / -21.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.6mV / -93.9uA	3.8mV / -95.1uA	4.4mV / -95.3uA	4.7mV / -96.8uA
20 x 20um x 5um	1.2mV / -21.2uA	1.1mV / -21.2uA	1.5mV / -21.2uA	1.9mV / -21.4uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.6V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	56.1mV / -0.8uA	43.1mV / -0.6uA					
2um		26.9mV / -2.1uA					
5um	19.3mV / -8.0uA	17.3mV / -6.0uA				3.3mV / -0.3uA	
10um		11.4mV / -12.6uA	8.8mV / -7.5uA	5.8mV / -3.5uA			
20um	10.2mV / -33.3uA	9.5mV / -25.6uA	6.4mV / -15.2uA	4.3mV / -7.2uA	2.6mV / -3.0uA	1.8mV / -1.1uA	1.5mV / -0.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		11.8mV / -11.1uA					
10um		8.5mV / -23.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.7mV / -102.6uA	3.2mV / -65.1uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -5.1uA	
20um					0.9mV / -53.0uA	1.2mV / -21.3uA	1.7mV / -10.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.4mV / -25.0uA	8.5mV / -23.0uA
20 x 20um x 5um	0.6mV / -21.4uA	1.2mV / -21.3uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.7mV / -102.6uA	3.8mV / -103.9uA	4.5mV / -104.1uA	4.7mV / -105.8uA
20 x 20um x 5um	1.2mV / -21.3uA	1.1mV / -21.3uA	1.5mV / -21.4uA	1.9mV / -21.5uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.0V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	57.6mV / -0.8uA	43.8mV / -0.6uA					
2um		27.1mV / -2.2uA					
5um	19.6mV / -8.6uA	17.5mV / -6.3uA				3.3mV / -0.3uA	
10um		11.6mV / -13.2uA	8.9mV / -7.6uA	5.9mV / -3.6uA			
20um	10.4mV / -35.8uA	9.7mV / -26.8uA	6.4mV / -15.5uA	4.4mV / -7.3uA	2.6mV / -3.0uA	1.8mV / -1.1uA	1.5mV / -0.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		11.9mV / -11.6uA					
10um		8.6mV / -24.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.7mV / -107.1uA	3.2mV / -66.5uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -5.2uA	
20um					0.9mV / -53.2uA	1.2mV / -21.4uA	1.7mV / -10.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.5mV / -26.3uA	8.6mV / -24.0uA
20 x 20um x 5um	0.6mV / -21.4uA	1.2mV / -21.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.7mV / -107.1uA	3.9mV / -108.5uA	4.5mV / -108.8uA	4.7mV / -110.5uA
20 x 20um x 5um	1.2mV / -21.4uA	1.1mV / -21.4uA	1.5mV / -21.4uA	1.9mV / -21.5uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.4V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	58.3mV / -0.9uA	44.5mV / -0.6uA					
2um		27.3mV / -2.3uA					
5um	19.9mV / -9.1uA	17.7mV / -6.5uA				3.2mV / -0.3uA	
10um		11.8mV / -13.6uA	9.0mV / -7.8uA	6.0mV / -3.6uA			
20um	10.5mV / -37.9uA	9.7mV / -27.8uA	6.5mV / -15.8uA	4.4mV / -7.3uA	2.6mV / -3.0uA	1.8mV / -1.1uA	1.5mV / -0.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		11.9mV / -12.0uA					
10um		8.8mV / -24.8uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.8mV / -110.8uA	3.3mV / -67.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -5.2uA	
20um					0.9mV / -53.3uA	1.2mV / -21.4uA	1.7mV / -10.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.6mV / -27.2uA	8.8mV / -24.8uA
20 x 20um x 5um	0.6mV / -21.4uA	1.2mV / -21.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.8mV / -110.8uA	3.9mV / -112.3uA	4.5mV / -112.5uA	4.8mV / -114.3uA
20 x 20um x5um	1.2mV / -21.4uA	1.1mV / -21.4uA	1.5mV / -21.4uA	1.9mV / -21.5uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.2V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	56.6mV / -3.2uA	42.4mV / -2.5uA					
2um		27.1mV / -9.5uA					
5um	19.5mV / -33.4uA	17.6mV / -26.3uA				3.5mV / -1.2uA	
10um		12.1mV / -55.4uA	8.8mV / -34.4uA	6.1mV / -16.5uA			
20um	10.3mV / -139.2uA	9.6mV / -112.9uA	6.7mV / -69.9uA	4.6mV / -33.4uA	2.9mV / -13.7uA	1.9mV / -5.2uA	1.6mV / -2.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		12.3mV / -49.1uA					
10um		8.6mV / -102.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.7mV / -459.2uA	3.2mV / -301.5uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -23.9uA	
20um					0.9mV / -249.1uA	1.1mV / -99.7uA	1.6mV / -49.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.4mV / -111.2uA	8.6mV / -102.2uA
20 x 20um x 5um	0.5mV / -100.0uA	1.1mV / -99.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.7mV / -459.2uA	3.9mV / -460.1uA	4.9mV / -460.4uA	5.2mV / -463.6uA
20 x 20um x 5um	1.1mV / -99.7uA	1.2mV / -100.2uA	1.7mV / -100.3uA	2.0mV / -100.5uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.6V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	55.2mV / -3.9uA	42.8mV / -3.0uA					
2um		27.5mV / -11.2uA					
5um	19.7mV / -41.1uA	17.8mV / -31.2uA				3.6mV / -1.3uA	
10um		11.9mV / -65.9uA	8.9mV / -39.0uA	6.2mV / -18.0uA			
20um	10.3mV / -171.0uA	9.6mV / -134.3uA	6.7mV / -79.4uA	4.7mV / -36.6uA	2.9mV / -14.6uA	2.0mV / -5.5uA	1.6mV / -2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		12.3mV / -58.3uA					
10um		8.6mV / -121.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.8mV / -544.5uA	3.2mV / -343.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -25.3uA	
20um					0.9mV / -266.0uA	1.2mV / -105.4uA	1.6mV / -52.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.5mV / -132.3uA	8.6mV / -121.3uA
20 x 20um x 5um	0.6mV / -105.7uA	1.2mV / -105.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.8mV / -544.5uA	3.9mV / -546.3uA	4.8mV / -546.7uA	5.2mV / -551.0uA
20 x 20um x 5um	1.2mV / -105.4uA	1.2mV / -105.9uA	1.6mV / -106.0uA	1.9mV / -106.4uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.0V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	55.7mV / -4.2uA	43.4mV / -3.1uA					
2um		27.6mV / -11.7uA					
5um	20.0mV / -43.7uA	18.1mV / -32.6uA				3.6mV / -1.3uA	
10um		12.0mV / -68.8uA	9.0mV / -39.9uA	6.3mV / -18.2uA			
20um	10.5mV / -181.6uA	9.7mV / -140.2uA	6.7mV / -81.2uA	4.7mV / -36.9uA	2.9mV / -14.7uA	2.0mV / -5.5uA	1.6mV / -2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		12.4mV / -60.8uA					
10um		8.7mV / -126.5uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.8mV / -567.3uA	3.2mV / -351.1uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -25.3uA	
20um					0.9mV / -267.1uA	1.2mV / -105.5uA	1.6mV / -52.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.6mV / -138.2uA	8.7mV / -126.5uA
20 x 20um x 5um	0.6mV / -105.8uA	1.2mV / -105.5uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.8mV / -567.3uA	4.0mV / -569.3uA	4.8mV / -570.0uA	5.2mV / -574.2uA
20 x 20um x 5um	1.2mV / -105.5uA	1.2mV / -106.1uA	1.6mV / -106.2uA	2.0mV / -106.6uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.4V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	57.3mV / -4.4uA	43.9mV / -3.2uA					
2um		27.8mV / -12.0uA					
5um	20.3mV / -45.6uA	18.3mV / -33.6uA				3.7mV / -1.3uA	
10um		12.1mV / -71.0uA	8.9mV / -40.6uA	6.3mV / -18.3uA			
20um	10.6mV / -189.7uA	9.8mV / -144.6uA	6.9mV / -82.5uA	4.7mV / -37.2uA	2.9mV / -14.7uA	2.0mV / -5.5uA	1.6mV / -2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		12.4mV / -62.6uA					
10um		8.8mV / -130.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.9mV / -584.4uA	3.3mV / -356.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -25.4uA	
20um					0.9mV / -267.9uA	1.2mV / -105.7uA	1.6mV / -52.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.7mV / -142.6uA	8.8mV / -130.4uA
20 x 20um x 5um	0.6mV / -106.0uA	1.2mV / -105.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.9mV / -584.4uA	4.0mV / -586.3uA	4.8mV / -587.0uA	5.2mV / -591.4uA
20 x 20um x 5um	1.2mV / -105.7uA	1.2mV / -106.3uA	1.6mV / -106.4uA	2.0mV / -106.7uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.2V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	58.7mV / -6.7uA	45.2mV / -5.2uA					
2um		29.4mV / -19.8uA					
5um	21.4mV / -69.1uA	19.5mV / -54.9uA				3.7mV / -2.7uA	
10um		13.6mV / -115.7uA	9.2mV / -72.8uA	6.7mV / -35.2uA			
20um	11.0mV / -287.7uA	10.3mV / -235.6uA	7.5mV / -147.9uA	4.9mV / -71.5uA	3.1mV / -29.4uA	2.1mV / -11.2uA	1.7mV / -5.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.4mV / -102.7uA					
10um		9.5mV / -213.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.9mV / -982.0uA	3.2mV / -652.6uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -51.5uA	
20um					0.9mV / -548.8uA	1.1mV / -219.9uA	1.5mV / -110.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	9.2mV / -232.2uA	9.5mV / -213.6uA
20 x 20um x 5um	0.1mV / -220.5uA	1.1mV / -219.9uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.9mV / -982.0uA	4.6mV / -963.1uA	5.6mV / -963.4uA	6.2mV / -966.9uA
20 x 20um x 5um	1.1mV / -219.9uA	3.9mV / -252.0uA	5.2mV / -252.2uA	5.7mV / -252.8uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.6V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	57.2mV / -9.6uA	44.1mV / -7.3uA					
2um		28.8mV / -27.7uA					
5um	20.5mV / -99.2uA	18.7mV / -77.0uA				4.0mV / -3.4uA	
10um		12.8mV / -162.4uA	9.1mV / -98.4uA	6.7mV / -45.8uA			
20um	10.7mV / -412.3uA	10.0mV / -330.6uA	7.3mV / -200.0uA	4.9mV / -92.9uA	3.2mV / -37.2uA	2.1mV / -13.9uA	1.8mV / -6.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.0mV / -144.5uA					
10um		9.1mV / -300.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.8mV / -1,376.0uA	3.2mV / -881.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -64.2uA	
20um					0.9mV / -689.9uA	1.1mV / -272.8uA	1.5mV / -136.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	8.9mV / -326.2uA	9.1mV / -300.4uA
20 x 20um x 5um	0.5mV / -273.7uA	1.1mV / -272.8uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.8mV / -1,376.0uA	4.3mV / -1,357.6uA	5.3mV / -1,358.3uA	5.8mV / -1,364.4uA
20 x 20um x 5um	1.1mV / -272.8uA	2.7mV / -307.9uA	3.8mV / -308.2uA	4.1mV / -309.0uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.0V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	57.8mV / -10.2uA	44.6mV / -7.7uA					
2um		28.8mV / -29.0uA					
5um	20.7mV / -105.5uA	19.0mV / -80.7uA				4.0mV / -3.4uA	
10um		12.8mV / -170.3uA	9.3mV / -101.1uA	6.7mV / -46.3uA			
20um	10.8mV / -438.2uA	10.0mV / -346.5uA	7.4mV / -205.5uA	5.0mV / -94.1uA	3.2mV / -37.3uA	2.2mV / -14.0uA	1.8mV / -6.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.1mV / -151.3uA					
10um		9.3mV / -314.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.9mV / -1,440.5uA	3.3mV / -906.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -64.3uA	
20um					0.9mV / -693.3uA	1.1mV / -273.4uA	1.5mV / -136.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	9.0mV / -342.0uA	9.3mV / -314.6uA
20 x 20um x 5um	0.5mV / -274.2uA	1.1mV / -273.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.9mV / -1,440.5uA	4.3mV / -1,421.1uA	5.3mV / -1,421.9uA	5.9mV / -1,428.3uA
20 x 20um x 5um	1.1mV / -273.4uA	2.8mV / -310.3uA	3.9mV / -310.6uA	4.3mV / -311.5uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.4V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	57.5mV / -10.6uA	45.1mV / -7.9uA					
2um		28.9mV / -29.8uA					
5um	20.9mV / -109.7uA	19.5mV / -83.1uA				4.0mV / -3.4uA	
10um		12.8mV / -175.3uA	9.2mV / -102.8uA	6.7mV / -46.7uA			
20um	11.0mV / -455.6uA	10.1mV / -356.8uA	7.4mV / -209.0uA	5.0mV / -94.8uA	3.2mV / -37.5uA	2.2mV / -14.0uA	1.8mV / -6.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.1mV / -155.7uA					
10um		9.4mV / -323.8uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		3.9mV / -1,482.3uA	3.3mV / -922.3uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.1mV / -64.4uA	
20um					0.9mV / -695.4uA	1.1mV / -273.7uA	1.5mV / -136.2uA

Common Centroid Matched Pairs

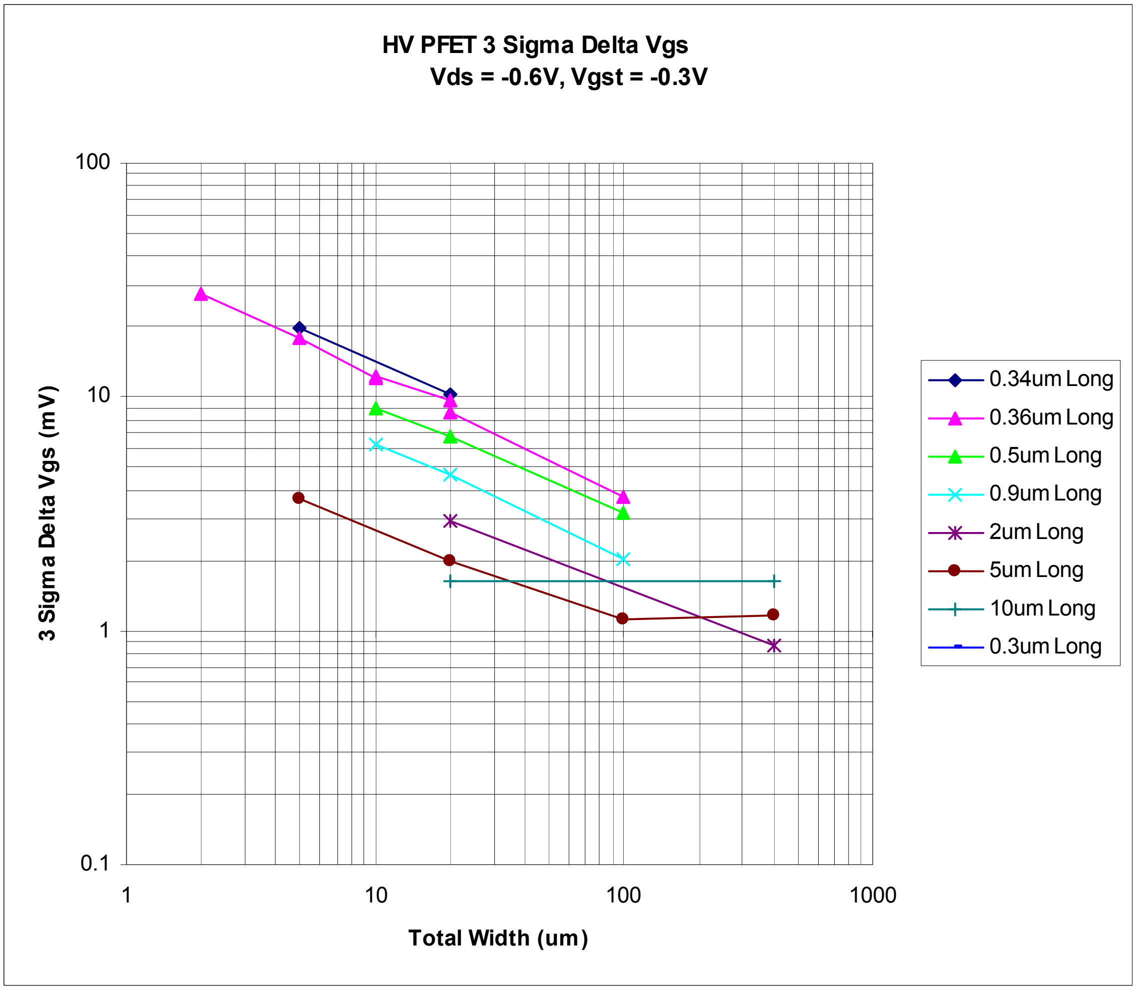
Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	9.1mV / -352.3uA	9.4mV / -323.8uA
20 x 20um x 5um	0.5mV / -274.5uA	1.1mV / -273.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	3.9mV / -1,482.3uA	4.3mV / -1,462.0uA	5.3mV / -1,463.1uA	5.9mV / -1,470.0uA
20 x 20um x 5um	1.1mV / -273.7uA	3.0mV / -312.2uA	4.0mV / -312.5uA	4.4mV / -313.4uA

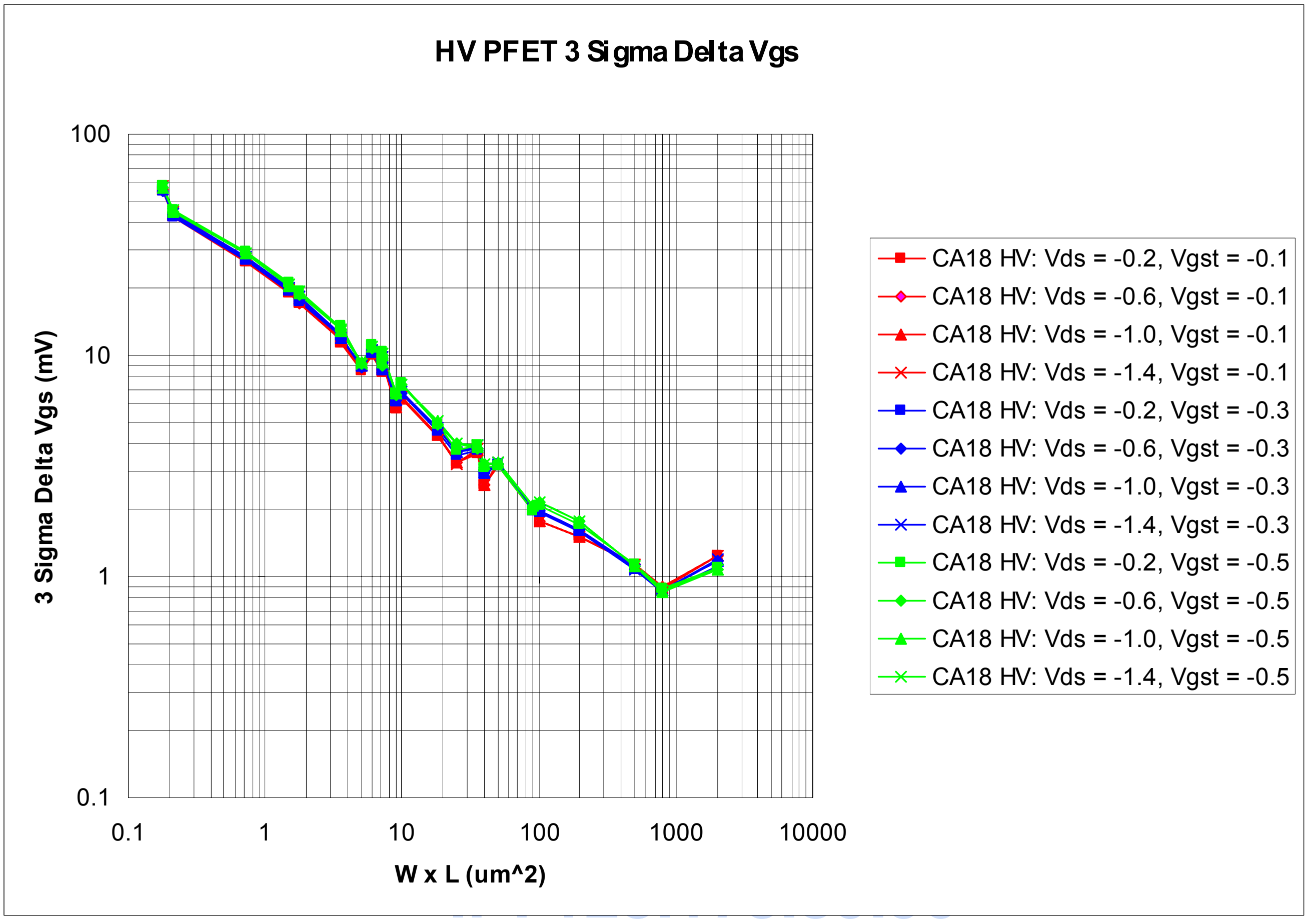
PFET Vgs Matching versus Device Size Plot

The following plot shows the Vgs matching versus device size for a representative (Vds = -0.6V and Vgst = -0.3V) bias point:



PFET Vgs Matching versus Device Area Plot

The following plot shows the Vgs matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ΔW and ΔL.

Fingers	Width	Length	Effective Drawn Area
1	2	0.36	0.72
1	5	0.34	1.7
1	5	0.36	1.8
2	5	0.36	3.6
1	10	0.36	3.6
1	10	0.50	5
1	20	0.34	6.8
2	10	0.36	7.2
1	20	0.36	7.2
1	10	0.90	9
1	20	0.50	10
1	20	0.90	18

Fingers	Width	Length	Effective Drawn Area
1	5	5.00	25
10	10	0.36	36
1	20	2.00	40
10	10	0.50	50
10	10	0.90	90
1	20	5.00	100
1	20	10.00	200
20	5	5.00	500
20	20	2.00	800
20	20	5.00	2000
20	20	10.00	4000

PFET Delta Id Results

PFET Standard Matched Pair Delta Id

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.2V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	65.3% / -0.7uA	46.4% / -0.5uA					
2um		30.4% / -2.0uA					
5um	21.6% / -7.0uA	19.3% / -5.5uA				3.6% / -0.3uA	
10um		13.0% / -11.4uA	9.8% / -7.1uA	6.4% / -3.5uA			
20um	11.4% / -29.0uA	10.9% / -23.3uA	7.2% / -14.5uA	4.8% / -7.0uA	2.9% / -2.9uA	2.0% / -1.1uA	1.7% / -0.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.4% / -10.1uA					
10um		9.6% / -21.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		4.2% / -93.9uA	3.6% / -62.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.3% / -5.1uA	
20um					1.0% / -52.4uA	1.3% / -21.2uA	1.9% / -10.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	9.6% / -22.8uA	9.6% / -21.0uA
20 x 20um x 5um	0.7% / -21.2uA	1.3% / -21.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	4.2% / -93.9uA	4.2% / -95.1uA	4.9% / -95.3uA	5.0% / -96.8uA
20 x 20um x 5um	1.3% / -21.2uA	1.2% / -21.2uA	1.6% / -21.2uA	2.0% / -21.4uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.6V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	68.1% / -0.8uA	48.5% / -0.6uA					
2um		31.2% / -2.1uA					
5um	22.2% / -8.0uA	20.0% / -6.0uA				3.6% / -0.3uA	
10um		13.4% / -12.6uA	10.1% / -7.5uA	6.5% / -3.5uA			
20um	11.7% / -33.3uA	11.3% / -25.6uA	7.3% / -15.2uA	4.9% / -7.2uA	2.9% / -3.0uA	2.0% / -1.1uA	1.7% / -0.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.7% / -11.1uA					
10um		9.9% / -23.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		4.3% / -102.6uA	3.6% / -65.1uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.3% / -5.1uA	
20um					1.0% / -53.0uA	1.3% / -21.3uA	1.9% / -10.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	9.9% / -25.0uA	9.9% / -23.0uA
20 x 20um x 5um	0.7% / -21.4uA	1.3% / -21.3uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	4.3% / -102.6uA	4.4% / -103.9uA	5.1% / -104.1uA	5.1% / -105.8uA
20 x 20um x 5um	1.3% / -21.3uA	1.2% / -21.3uA	1.6% / -21.4uA	2.0% / -21.5uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.0V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	68.3% / -0.8uA	49.3% / -0.6uA					
2um		31.4% / -2.2uA					
5um	22.7% / -8.6uA	20.2% / -6.3uA				3.6% / -0.3uA	
10um		13.5% / -13.2uA	10.3% / -7.6uA	6.6% / -3.6uA			
20um	12.0% / -35.8uA	11.4% / -26.8uA	7.4% / -15.5uA	4.9% / -7.3uA	2.9% / -3.0uA	2.0% / -1.1uA	1.7% / -0.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.8% / -11.6uA					
10um		10.2% / -24.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		4.4% / -107.1uA	3.7% / -66.5uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.3% / -5.2uA	
20um					1.0% / -53.2uA	1.4% / -21.4uA	1.9% / -10.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	10.0% / -26.3uA	10.2% / -24.0uA
20 x 20um x 5um	0.7% / -21.4uA	1.4% / -21.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	4.4% / -107.1uA	4.4% / -108.5uA	5.1% / -108.8uA	5.2% / -110.5uA
20 x 20um x5um	1.4% / -21.4uA	1.2% / -21.4uA	1.6% / -21.4uA	2.0% / -21.5uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.4V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	67.4% / -0.9uA	49.9% / -0.6uA					
2um		31.6% / -2.3uA					
5um	22.8% / -9.1uA	20.4% / -6.5uA				3.6% / -0.3uA	
10um		13.6% / -13.6uA	10.4% / -7.8uA	6.6% / -3.6uA			
20um	12.0% / -37.9uA	11.4% / -27.8uA	7.4% / -15.8uA	4.9% / -7.3uA	2.9% / -3.0uA	2.0% / -1.1uA	1.7% / -0.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		13.8% / -12.0uA					
10um		10.2% / -24.8uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		4.4% / -110.8uA	3.8% / -67.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						1.3% / -5.2uA	
20um					1.0% / -53.3uA	1.4% / -21.4uA	1.9% / -10.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	10.1% / -27.2uA	10.2% / -24.8uA
20 x 20um x 5um	0.7% / -21.4uA	1.4% / -21.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	4.4% / -110.8uA	4.4% / -112.3uA	5.1% / -112.5uA	5.2% / -114.3uA
20 x 20um x 5um	1.4% / -21.4uA	1.2% / -21.4uA	1.6% / -21.4uA	2.0% / -21.5uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.2V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	29.0% / -3.2uA	21.3% / -2.5uA					
2um		14.2% / -9.5uA					
5um	9.9% / -33.4uA	9.1% / -26.3uA				1.9% / -1.2uA	
10um		6.2% / -55.4uA	4.6% / -34.4uA	3.2% / -16.5uA			
20um	5.3% / -139.2uA	4.8% / -112.9uA	3.6% / -69.9uA	2.4% / -33.4uA	1.5% / -13.7uA	1.0% / -5.2uA	0.8% / -2.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		6.3% / -49.1uA					
10um		4.4% / -102.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.9% / -459.2uA	1.7% / -301.5uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / -23.9uA	
20um					0.5% / -249.1uA	0.6% / -99.7uA	0.9% / -49.8uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	4.3% / -111.2uA	4.4% / -102.2uA
20 x 20um x 5um	0.3% / -100.0uA	0.6% / -99.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	1.9% / -459.2uA	2.0% / -460.1uA	2.5% / -460.4uA	2.6% / -463.6uA
20 x 20um x5um	0.6% / -99.7uA	0.6% / -100.2uA	0.9% / -100.3uA	1.0% / -100.5uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.6V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	33.0% / -3.9uA	24.5% / -3.0uA					
2um		16.0% / -11.2uA					
5um	11.1% / -41.1uA	10.4% / -31.2uA				2.1% / -1.3uA	
10um		6.9% / -65.9uA	5.2% / -39.0uA	3.6% / -18.0uA			
20um	5.8% / -171.0uA	5.5% / -134.3uA	4.0% / -79.4uA	2.7% / -36.6uA	1.7% / -14.6uA	1.2% / -5.5uA	1.0% / -2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		7.2% / -58.3uA					
10um		5.0% / -121.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		2.2% / -544.5uA	1.9% / -343.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / -25.3uA	
20um					0.5% / -266.0uA	0.7% / -105.4uA	1.0% / -52.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	5.0% / -132.3uA	5.0% / -121.3uA
20 x 20um x 5um	0.3% / -105.7uA	0.7% / -105.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	2.2% / -544.5uA	2.3% / -546.3uA	2.8% / -546.7uA	2.9% / -551.0uA
20 x 20um x 5um	0.7% / -105.4uA	0.7% / -105.9uA	0.9% / -106.0uA	1.1% / -106.4uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.0V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	33.3% / -4.2uA	25.0% / -3.1uA					
2um		16.1% / -11.7uA					
5um	11.3% / -43.7uA	10.6% / -32.6uA				2.1% / -1.3uA	
10um		7.0% / -68.8uA	5.3% / -39.9uA	3.7% / -18.2uA			
20um	5.9% / -181.6uA	5.6% / -140.2uA	4.0% / -81.2uA	2.8% / -36.9uA	1.7% / -14.7uA	1.2% / -5.5uA	1.0% / -2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		7.2% / -60.8uA					
10um		5.1% / -126.5uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		2.2% / -567.3uA	1.9% / -351.1uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / -25.3uA	
20um					0.5% / -267.1uA	0.7% / -105.5uA	1.0% / -52.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	5.0% / -138.2uA	5.1% / -126.5uA
20 x 20um x 5um	0.3% / -105.8uA	0.7% / -105.5uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	2.2% / -567.3uA	2.3% / -569.3uA	2.8% / -570.0uA	2.9% / -574.2uA
20 x 20um x 5um	0.7% / -105.5uA	0.7% / -106.1uA	0.9% / -106.2uA	1.1% / -106.6uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.4V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	33.4% / -4.4uA	25.3% / -3.2uA					
2um		16.2% / -12.0uA					
5um	11.4% / -45.6uA	10.6% / -33.6uA				2.1% / -1.3uA	
10um		7.0% / -71.0uA	5.4% / -40.6uA	3.7% / -18.3uA			
20um	6.0% / -189.7uA	5.7% / -144.6uA	4.1% / -82.5uA	2.8% / -37.2uA	1.7% / -14.7uA	1.2% / -5.5uA	1.0% / -2.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		7.3% / -62.6uA					
10um		5.2% / -130.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		2.3% / -584.4uA	1.9% / -356.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.6% / -25.4uA	
20um					0.5% / -267.9uA	0.7% / -105.7uA	1.0% / -52.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	5.0% / -142.6uA	5.2% / -130.4uA
20 x 20um x 5um	0.3% / -106.0uA	0.7% / -105.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	2.3% / -584.4uA	2.3% / -586.3uA	2.8% / -587.0uA	2.9% / -591.4uA
20 x 20um x 5um	0.7% / -105.7uA	0.7% / -106.3uA	0.9% / -106.4uA	1.1% / -106.7uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.2V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	15.5% / -6.7uA	11.8% / -5.2uA					
2um		7.7% / -19.8uA					
5um	5.5% / -69.1uA	5.1% / -54.9uA				1.0% / -2.7uA	
10um		3.5% / -115.7uA	2.5% / -72.8uA	1.8% / -35.2uA			
20um	2.8% / -287.7uA	2.7% / -235.6uA	2.0% / -147.9uA	1.3% / -71.5uA	0.9% / -29.4uA	0.6% / -11.2uA	0.5% / -5.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		3.5% / -102.7uA					
10um		2.5% / -213.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.0% / -982.0uA	0.8% / -652.6uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.3% / -51.5uA	
20um					0.2% / -548.8uA	0.3% / -219.9uA	0.4% / -110.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	2.4% / -232.2uA	2.5% / -213.6uA
20 x 20um x 5um	0.1% / -220.5uA	0.3% / -219.9uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	1.0% / -982.0uA	1.2% / -963.1uA	1.5% / -963.4uA	1.6% / -966.9uA
20 x 20um x 5um	0.3% / -219.9uA	0.9% / -252.0uA	1.2% / -252.2uA	1.3% / -252.8uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.6V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	20.2% / -9.6uA	15.5% / -7.3uA					
2um		10.2% / -27.7uA					
5um	7.0% / -99.2uA	6.6% / -77.0uA				1.5% / -3.4uA	
10um		4.5% / -162.4uA	3.4% / -98.4uA	2.5% / -45.8uA			
20um	3.6% / -412.3uA	3.4% / -330.6uA	2.6% / -200.0uA	1.8% / -92.9uA	1.2% / -37.2uA	0.8% / -13.9uA	0.7% / -6.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		4.6% / -144.5uA					
10um		3.2% / -300.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.3% / -1,376.0uA	1.2% / -881.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.4% / -64.2uA	
20um					0.3% / -689.9uA	0.4% / -272.8uA	0.5% / -136.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	3.1% / -326.2uA	3.2% / -300.4uA
20 x 20um x 5um	0.2% / -273.7uA	0.4% / -272.8uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	1.3% / -1,376.0uA	1.5% / -1,357.6uA	1.8% / -1,358.3uA	2.0% / -1,364.4uA
20 x 20um x 5um	0.4% / -272.8uA	0.9% / -307.9uA	1.2% / -308.2uA	1.3% / -309.0uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.0V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	20.7% / -10.2uA	15.9% / -7.7uA					
2um		10.3% / -29.0uA					
5um	7.1% / -105.5uA	6.9% / -80.7uA				1.5% / -3.4uA	
10um		4.5% / -170.3uA	3.4% / -101.1uA	2.5% / -46.3uA			
20um	3.7% / -438.2uA	3.5% / -346.5uA	2.7% / -205.5uA	1.9% / -94.1uA	1.2% / -37.3uA	0.8% / -14.0uA	0.7% / -6.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		4.7% / -151.3uA					
10um		3.3% / -314.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.4% / -1,440.5uA	1.2% / -906.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.4% / -64.3uA	
20um					0.3% / -693.3uA	0.4% / -273.4uA	0.5% / -136.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	3.2% / -342.0uA	3.3% / -314.6uA
20 x 20um x 5um	0.2% / -274.2uA	0.4% / -273.4uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	1.4% / -1,440.5uA	1.5% / -1,421.1uA	1.9% / -1,421.9uA	2.0% / -1,428.3uA
20 x 20um x 5um	0.4% / -273.4uA	0.9% / -310.3uA	1.3% / -310.6uA	1.3% / -311.5uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.4V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
0.6um	20.8% / -10.6uA	16.1% / -7.9uA					
2um		10.4% / -29.8uA					
5um	7.2% / -109.7uA	7.0% / -83.1uA				1.5% / -3.4uA	
10um		4.5% / -175.3uA	3.5% / -102.8uA	2.5% / -46.7uA			
20um	3.7% / -455.6uA	3.6% / -356.8uA	2.7% / -209.0uA	1.9% / -94.8uA	1.2% / -37.5uA	0.8% / -14.0uA	0.7% / -6.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um		4.7% / -155.7uA					
10um		3.3% / -323.8uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
10um		1.4% / -1,482.3uA	1.2% / -922.3uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.34um	0.36um	0.5um	0.9um	2um	5um	10um
5um						0.4% / -64.4uA	
20um					0.3% / -695.4uA	0.4% / -273.7uA	0.5% / -136.2uA

Common Centroid Matched Pairs

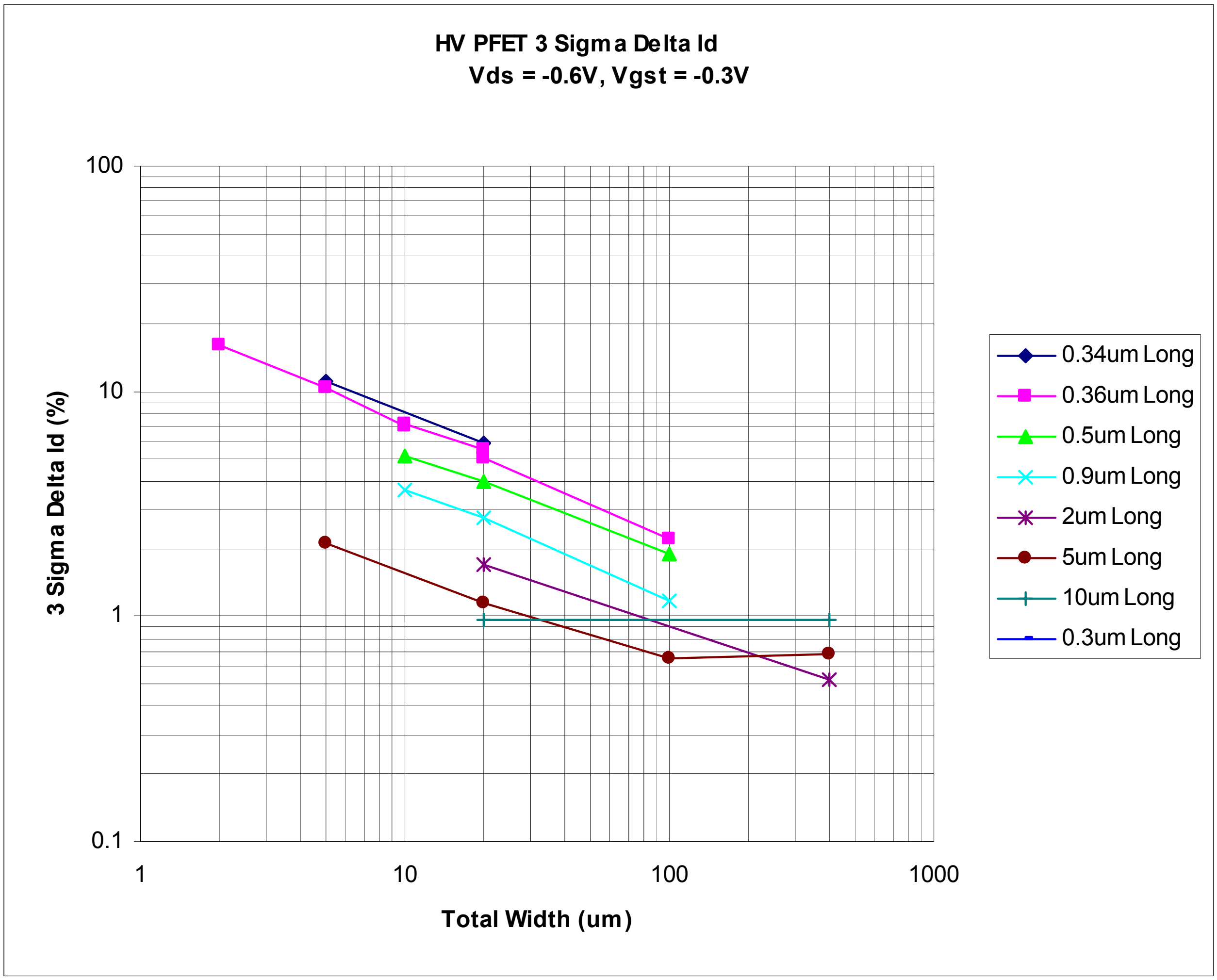
Fingers x Width x Length	CC	Std
2 x 10um x 0.36um	3.2% / -352.3uA	3.3% / -323.8uA
20 x 20um x 5um	0.2% / -274.5uA	0.4% / -273.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.36um	1.4% / -1,482.3uA	1.5% / -1,462.0uA	1.9% / -1,463.1uA	2.1% / -1,470.0uA
20 x 20um x 5um	0.4% / -273.7uA	0.9% / -312.2uA	1.3% / -312.5uA	1.4% / -313.4uA

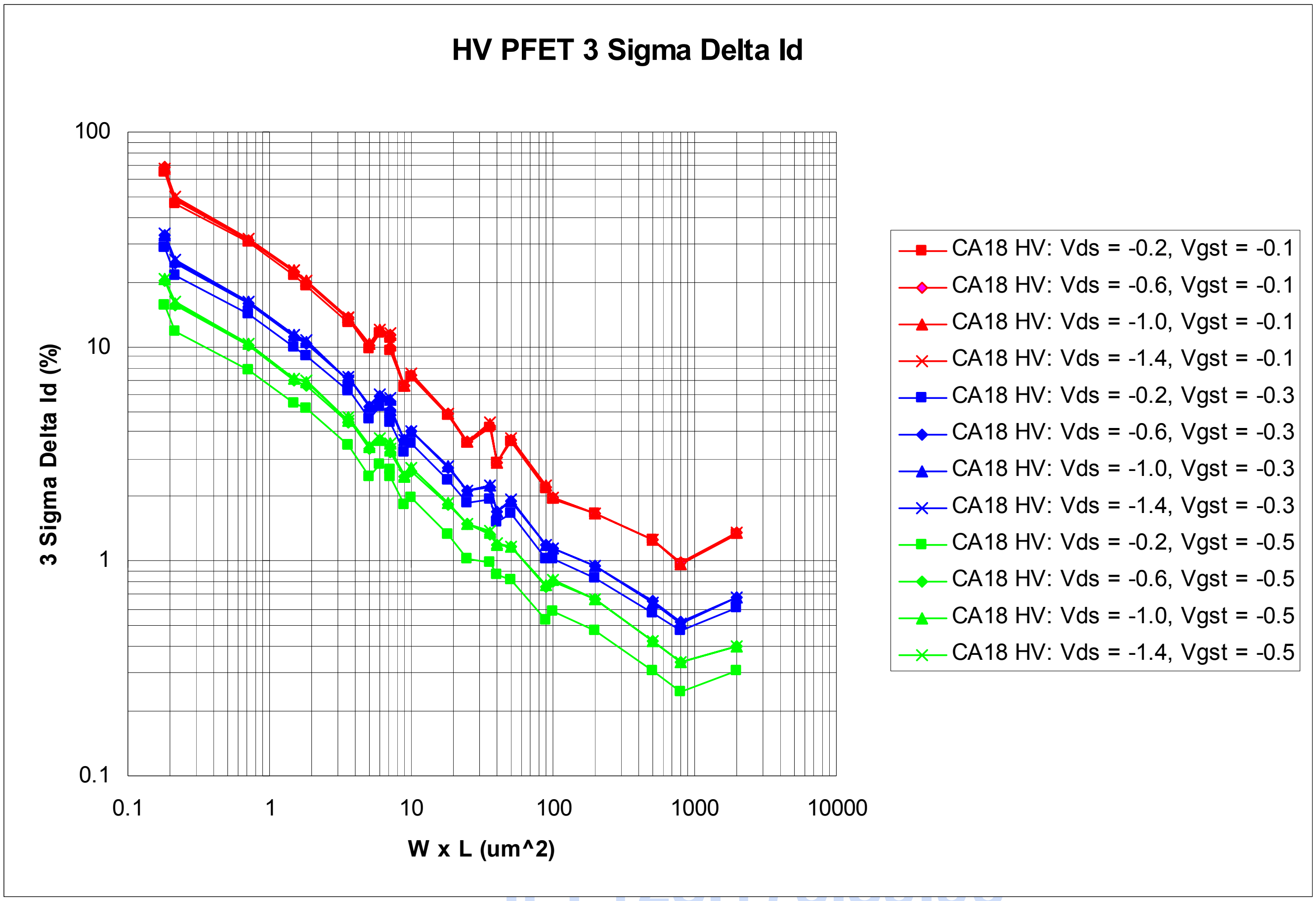
PFET Id Matching versus Device Size Plot

The following plot shows the Id matching versus device size for a representative (Vds = -0.6V and Vgst = -0.3V) bias point:



PFET Id Matching versus Device Area Plot

The following plot shows the Id matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ∆W and ∆L.

Fingers	Width	Length	Effective Drawn Area
1	2	0.36	0.72
1	5	0.34	1.7
1	5	0.36	1.8
2	5	0.36	3.6
1	10	0.36	3.6
1	10	0.50	5
1	20	0.34	6.8
2	10	0.36	7.2
1	20	0.36	7.2
1	10	0.90	9
1	20	0.50	10
1	20	0.90	18

Fingers	Width	Length	Effective Drawn Area
1	5	5.00	25
10	10	0.36	36
1	20	2.00	40
10	10	0.50	50
10	10	0.90	90
1	20	5.00	100
1	20	10.00	200
20	5	5.00	500
20	20	2.00	800
20	20	5.00	2000
20	20	10.00	4000

Delta Id Matching Model

The following simple first order saturation model has been used to the model delta Id results:

$$Id = \beta(Vgs - Vt)^2 \text{ where } \beta = \frac{\mu_o \cdot Cox}{2} \cdot \frac{W}{L}$$

$$\Delta_{Id} = \Delta_\beta \left[\frac{\delta Id}{\delta \beta}\right] + \Delta_{Vt}\left[\frac{\delta Id}{\delta Vt}\right]$$

$$\Delta_{Id} = \Delta_\beta (Vgs - Vt)^2 + \Delta_{Vt}(-2 \cdot \beta \cdot (Vgs - Vt))$$

$$\frac{\Delta_{Id}}{Id} = \frac{\Delta_\beta}{\beta} + \Delta_{Vt}\left(-\frac{2}{Vgs - Vt}\right)$$

$$\sigma_{\frac{\Delta_{Id}}{Id}}{}^2 = \frac{\sigma_\beta{}^2}{\beta^2} + \sigma_{Vt}{}^2\left[\frac{2}{Vgs - Vt}\right]^2$$

$$\sigma_\beta = \frac{A_\beta}{\sqrt{W \cdot L}}$$

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{W \cdot L}}$$

Note that it is easier to express the β dependence as a function of σ_β/β in percent, as then one does not need to know the value of β, and the Vgs – Vt term can be expressed as Vgst. The equation can be rewritten in the following manner, which is independent of the model parameters:

$$\sigma_{\frac{\Delta_{Id}}{Id}}{}^2 = \left(\frac{\sigma_{\beta\%}}{100}\right)^2 + \sigma_{Vt}{}^2\left[\frac{2}{Vgst}\right]^2$$

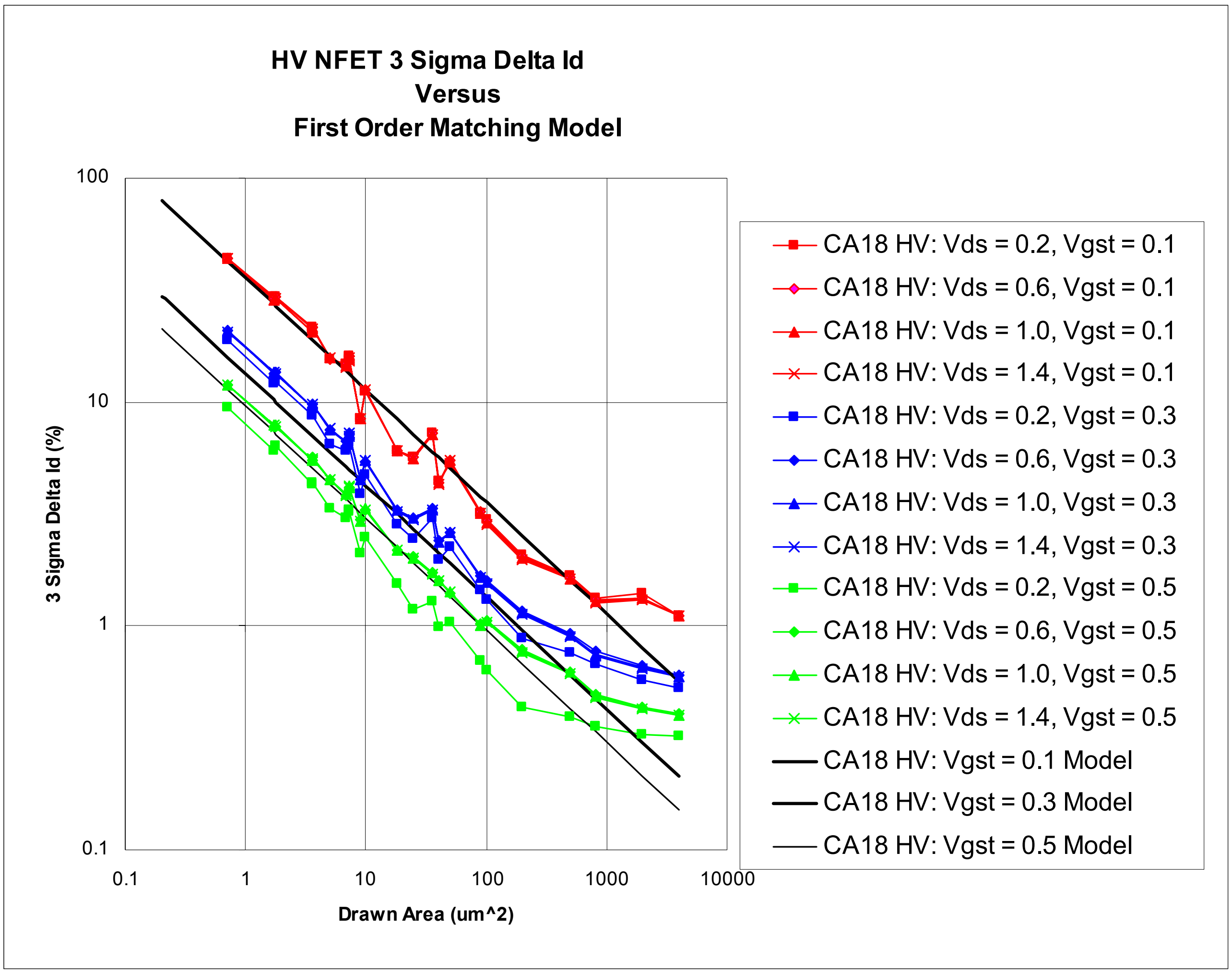
$$\sigma_{\beta\%} = \frac{A_{\beta\%}}{\sqrt{W \cdot L}}$$

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{W \cdot L}}$$

NFET Delta Id Model

The equations used to calculate $\sigma_{\beta\%}$ and σ_{Vt} are intended to model the standard deviation of the model parameters as a function of device size. The fitting constants are determined empirically by optimization of all sizes with effective areas less than 100μm^2.

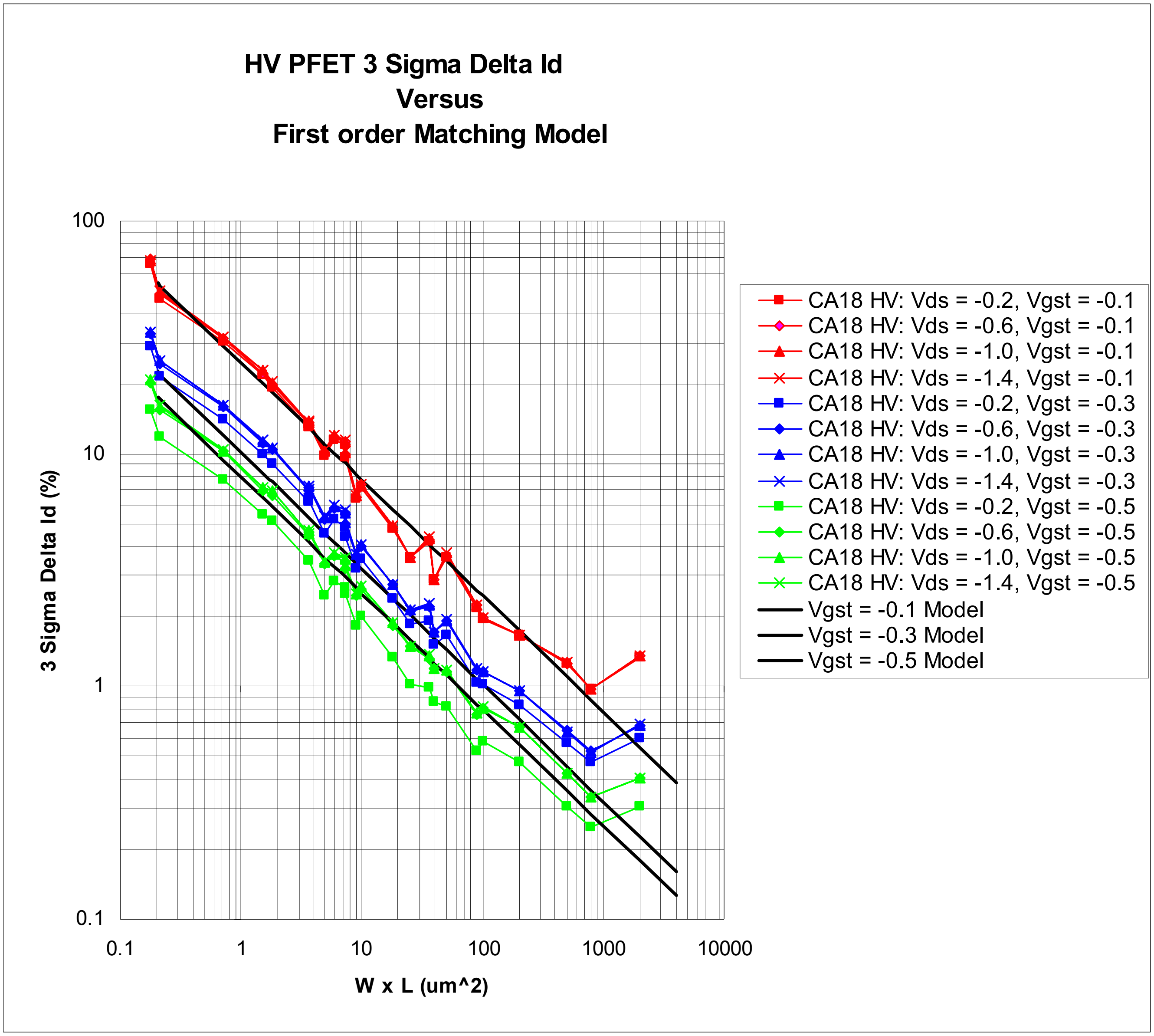
Parameter	Value
$A_{\beta\%}$ (%-μm)	2.17
A_{Vt} (mV-μm)	5.87



PFET Delta Id Model

The equations used to calculate $\sigma_{\beta\%}$ and σ_{Vt} are intended to model the standard deviation of the model parameters as a function of device size. The fitting constants are determined empirically by optimization of all sizes with effective areas less than 100μm^2.

Parameter	Value
$A_{\beta\%}$ (%-μm)	2.13
A_{Vt} (mV-μm)	3.94



Test Structures

This test chip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 3 NFET and 3 PFET modules devoted to FET matching (low and high voltage). NFET and PFET modules are identical except for the change in polarity between the devices. The following tables summarize the structures available for high voltage FET matching characterization:

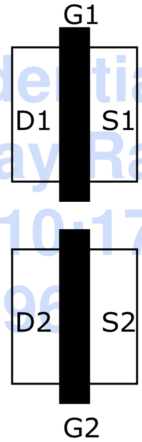
Low Voltage Standard Matched Pairs:

Width\Length	0.34μm	0.36μm	0.5μm	0.9μm	2μm	5μm	10μm
0.6μm	1	1					
2μm		1					
5μm	1	1, 2				1, 20	
10μm		1, 2, 10	1, 10	1, 10			
20μm	1	1	1	1	1, 20	1, 20	1, 20

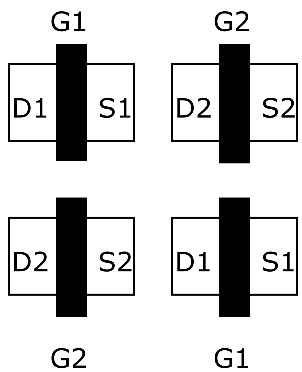
Note: The values in each box are the number of fingers per FET (total width is number of fingers x width).

Low Voltage Common Centroid Matched Pairs:

Width\Length	0.36μm	5μm
10μm	2	
20μm		20



Note: The device specification represents the size and configuration for each of the 4 FETs in the common centroid.



Low Voltage Matched Pairs with Various Spacings (140µm, 560µm, and 1260µm spacings):

Width\Length	0.36µm	5µm
10µm	10	
20µm		20

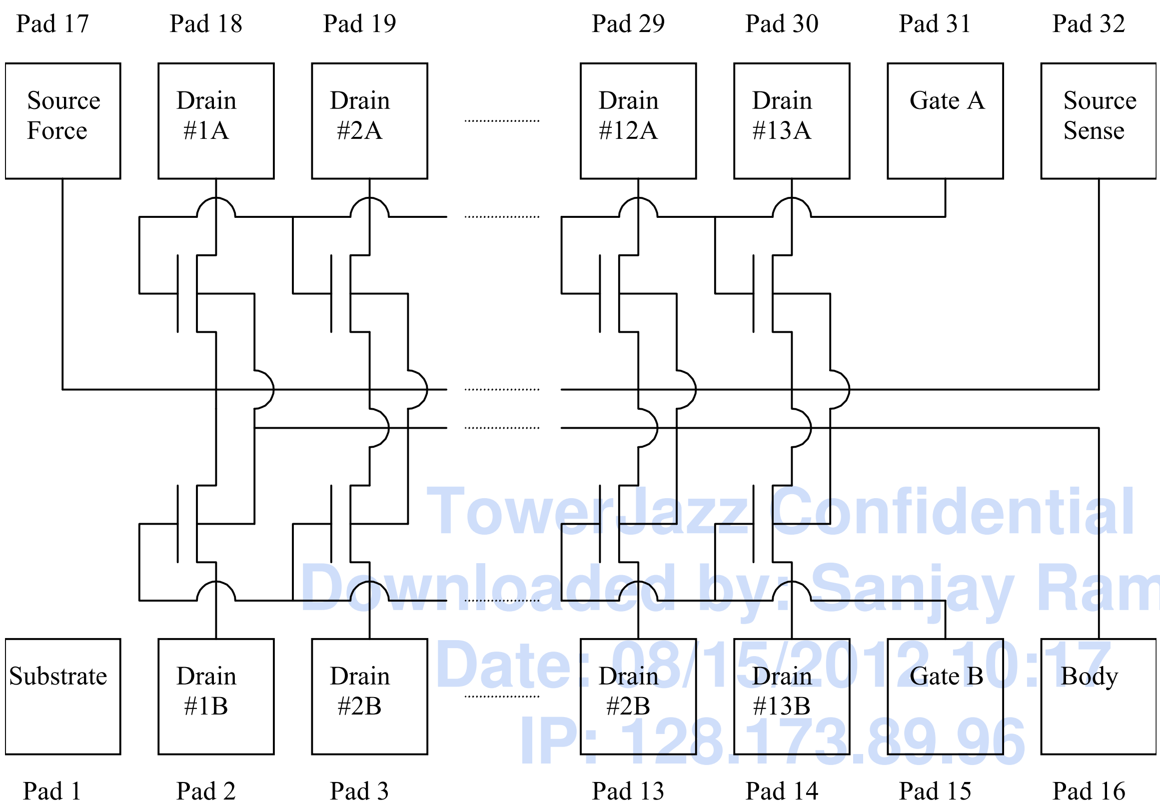


Figure 1: Schematic Diagram of FET Matching Module

The matched pairs are organized into modules as shown in figure 1. All of the transistors in the module share a common source bus, which has both force and sense pads to allow kelvin biasing of the source to maintain a known Vgs. It is important to use a common source pad for both transistors, as the variability in pad resistance will cause corresponding variablities in the effective Vgs for the two transistors if different pads are used. Since Id is a power function of Vgs in the saturation region, it is very sensitive to changes in Vgs. There are two gate buses which allow ΔVgs measurements (these have single pads each, since they should have essentially no current there should not be any concerns regarding pad resistance). There is also a single body tie for all of the transistors, as we want a consistent body voltage for both transistors in the matched pair and the current should be low enough to that pad resistance is not a concern. A single substrate tie is located between pads 1 and 17. Even though the non-kelvin drain pads can cause differences in Vds between the transistors, the transistors are usually biased in saturation for matching measurements, so the Id should be a weak function of Vds (certainly Id should be less sensitive to differences in Vds than in Vgs).

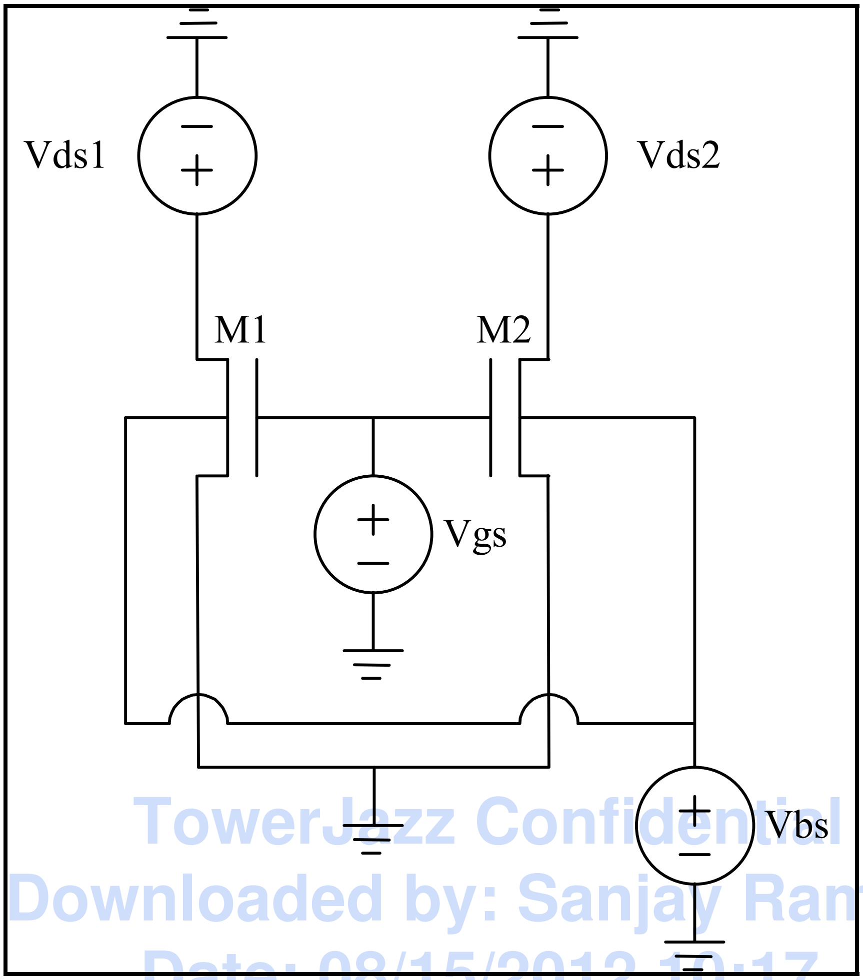


Figure 2: Circuit Configuration for Average Vt and DeltaIdVeff Tests

Test Description

The MOSFET matching test was performed on the "Analog Tester". The analog tester is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. All of the cabling between the HP4156, switch matrix, and probe card is guarded through the use of triaxial cable. The HP4156 is composed of 4 SMUs (Source Measure Units), 2 VSUs (Voltage Source Units), and 2 VMUs (Voltage Source Units). The SMUs are used to simultaneously force voltages and measure currents. They also support kelvin biasing, which allows voltages to be maintained at the DUT (Device Under Test) despite voltage offsets due to series resistance. The measurement resolution of the HP4156 SMUs is approximately 6 digits. All of the test equipment is controlled by a PC using a Visual Basic test program. The test program (WaferTest) is designed to provide a relatively open framework for implementing custom analog tests, and it places the measurement results directly into an Excel spreadsheet. Some of the tests use the term Veff, which stands for the effective gate voltage and is equal to Vgs - Vt (also called Vgst). The following tests were used in this characterization:

Contact - Measures the contact resistance of the probe tips. We have a module on the testchip which is designed specifically to check whether the probes are properly contacting the pads. This module has small metal 1 resistors between the adjacent pads in each row (e.g. pad 1 is connected to pad 17, pad 2 is

connected to pad 18, etc.). The contact test is usually the first test in the test program, and it verifies that the resistance of each pair of pads is less than a set value. If the probe resistance is greater than the set value, the tester stops to allow the probes to be checked.

AverageVt - Measures the Vt of both transistors in a matched pair simultaneously using the maximum transconductance method, and provides the average Vt value for use in subsequent tests. The test setup provides for connection inputs (Drain #1, Gate #1, Drain #2, Gate #2, Source Force, Source Sense, Body, Substrate), bias inputs (Start Vgs, Stop Vgs, Step Vgs, Vds, Vbs, Integration Time), and the ability to save the raw Id data. The setup for this test is described in figure 2. Both of the gate nodes and body nodes are connected to single voltage sources, thus there should not be any offsets between the two devices. The drains are connected to separate SMUs, which can result in Vds and Id offsets. The maximum transconductance method of calculating Vt is implemented in the following steps:

Perform the IdVg measurement on both transistors simultaneously.
Calculate the transconductance of each FET by taking the derivative of a 3 point second order polynomial fit of the IdVg curve.
Find the Vgs points which represent the maximum transconductances.
Perform linear least squares regressions (5 points centered at the point of maximum transconductance) to obtain the Vgs intercepts.
Subtract one-half of the Vds from the Vgs intercepts to obtain the Vts.
Calculate the average Vt.
Pass the average Vt to other tests.

This test also reports the individual Vts, delta Vt, and optionally the raw IdVg data.

DeltaVgsId - Measures both the delta Id and delta Vgs for a transistor pair for a range of Vds and Veff (Vgst or Vgs - Vt). The test setup provides for connection inputs (Drain #1, Gate #1, Drain #2, Gate #2, Source Force, Source Sense, Body, Substrate), bias inputs (Start Veff, Stop Veff, Step Veff, Start Vds, Stop Vds, Step Vds, Vbs), and the ability to save the raw Id data. Delta Id is defined as the percent difference in Id normalized by Id, and is taken from the first part of delta Vgs test.

$$\Delta Id = 100 * \frac{Id_2 - Id_1}{Id_1}$$

The delta Id results represent the error between the currents in a simple current mirror. Delta Vgs is determined by applying the same Veff and Vds to both transistors and then varying the Vgs of one of the transistors until the drain current is equal to the other transistor.

$$\Delta Vgs = Vgs_2 - Vgs_1$$

Delta Vgs represents the input offset voltage for a differential pair, and it is usually reported in milivolts (mV). The setup for this test is described in figure 3. Since the goal of this test is to look for small differences in Vgs between the two transistors, it would be difficult to obtain the required accuracy if the gates were biased independently through two voltage sources. The voltage offset and linearity differences between two voltage supplies would introduce errors, and the requirement of approximately 0.01mV precision cannot be met with our test system. In order to alleviate this problem, we have biased the gates of the transistors at ground level, and applied a -Vgs potential to the common source. The gate of the reference transistor (M1) is tied directly to ground, and the gate of the matched transistor (M2) is tied to a voltage source through a resistor divider. The resistor divider is used to increase the precision of the

voltage source by approximately 100 times. The voltage source is not ideal, and will have an offset voltage (~0.1mV), but the offset is divided down to a small value (~0.001mV) and should only cause a small fixed offset in the mean of the measurement results (we are interested in the 3 Sigma). The linearity of the voltage source is not very critical in this configuration, as we only have to supply the voltage offset magnified by ~100 about 0V rather than the absolute Vgs. The drains are connected to separate SMUs, which supply (Vds – Vgs) to bias the drains at the desired Vds. Since the drains are connected to separate SMUs, there will be offsets in both the Vds and Id between the devices.

The flow chart shown in figure 4 describes the algorithm used to perform the DeltaVgsId test. While the flow chart excludes several practical implementation details, it does represent the general flow which is followed for the test.

Test Conditions

The following test conditions were used for this characterization:

Average Vt

Device	Start Vgs	Stop Vgs	Step Vgs	Vds	Vbs	Integration	Delay	Hold	Save Id Data
NFET	0.4	1.5	0.05	0.1	0	M	0	0	1
PFET	-0.5	-1.6	-0.05	-0.1	0	M	0	0	1

DeltaVgsId

Device	Start Veff	Stop Veff	Step Veff	Start Vds	Stop Vds	Step Vds	Vbs	Save Id Data
NFET	0.1	0.5	0.2	0.2	1.4	0.4	0	1
PFET	-0.1	-0.5	-0.2	-0.2	-1.4	-0.4	0	1

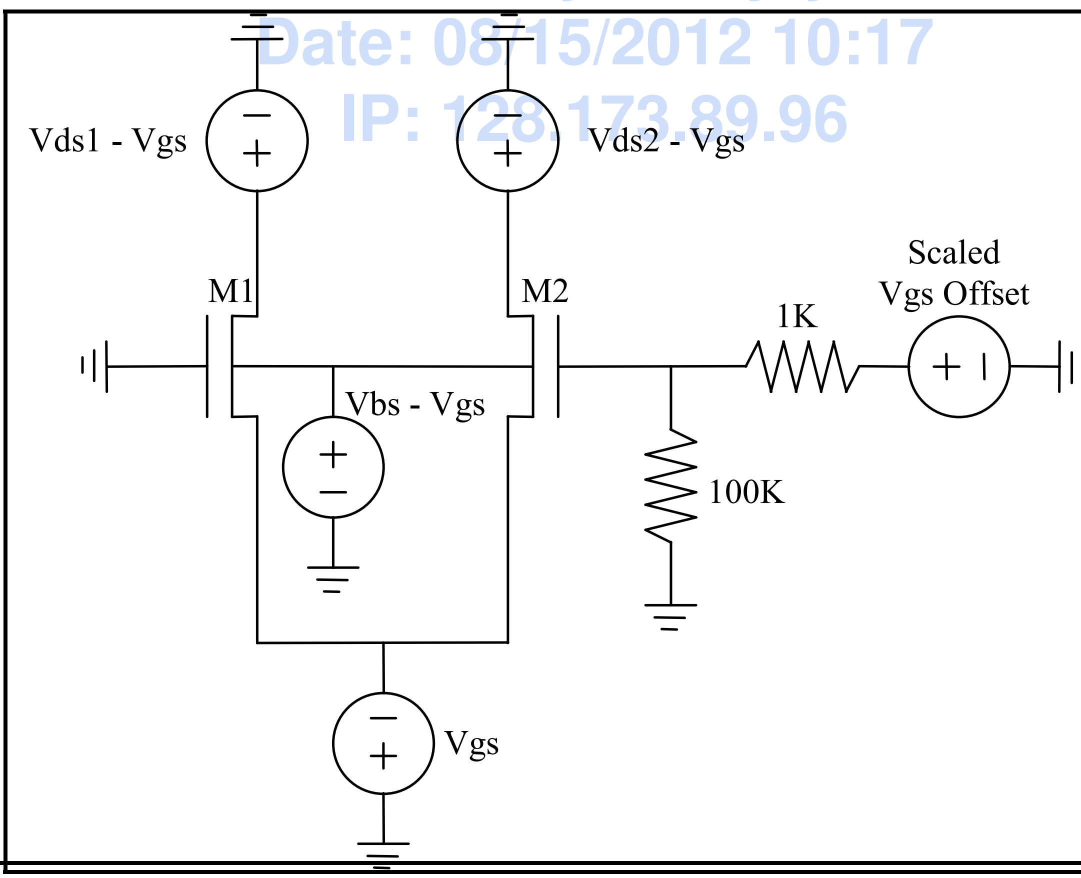


Figure 3: Circuit Configuration for DeltaVgsId Test

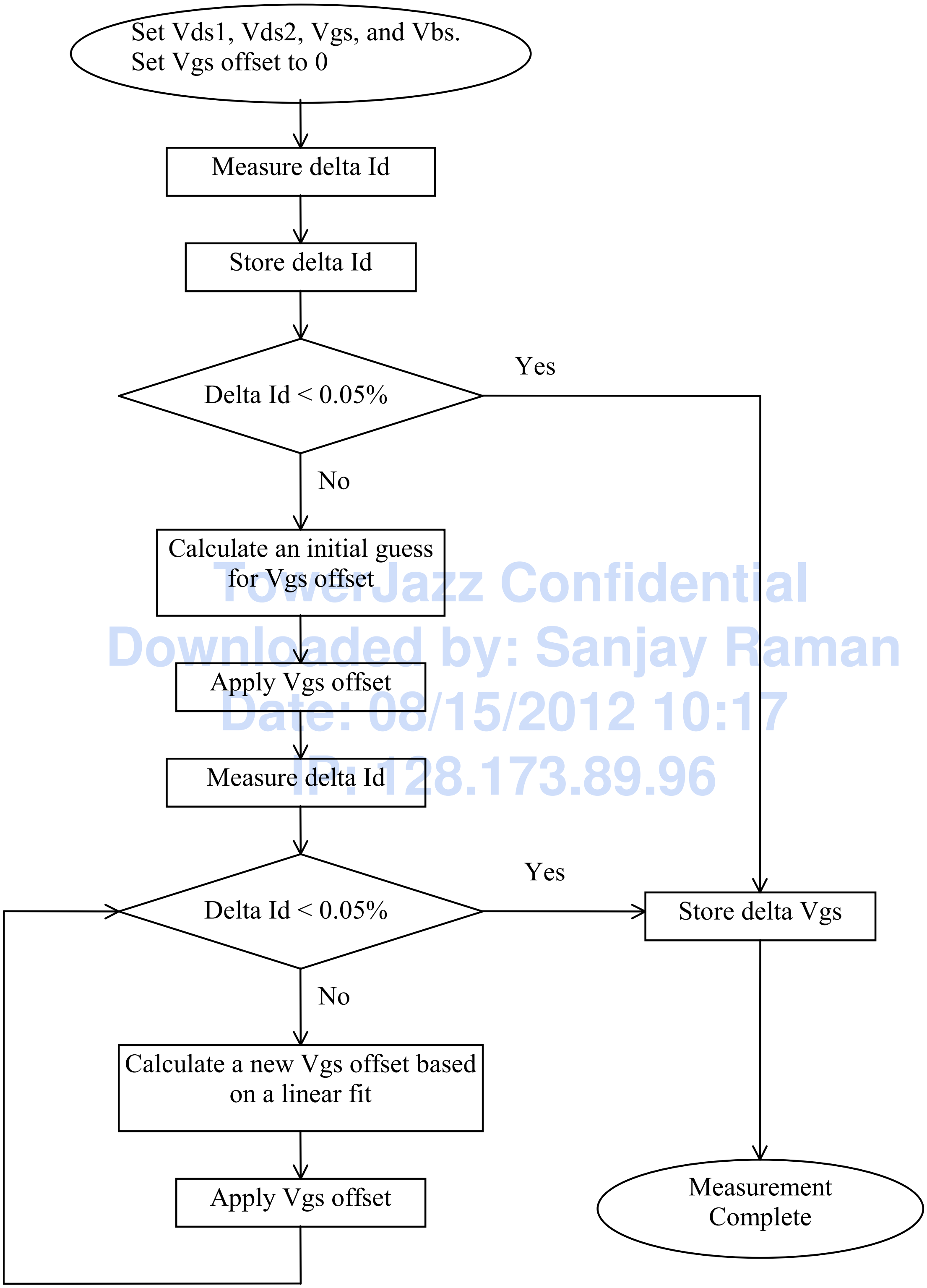


Figure 4: Delta Vgs Test Flowchart

4. Low Voltage FET Matching Characterization

Table of Contents

Summary

A FET matching characterization for the low voltage FETs in the SBC18 process has been performed. These devices are available in sbc18hx and sbc18pt. A simple model has been fit to the ΔId data in order to help support design optimization. The test structures, test procedures, and test conditions are described in the appendix.

Measurement Results

It is important to determine whether the wafers used in this characterization represent the nominal electrical specifications. The following table presents the specifications for some of the most significant device parameters:

	NFET			PFET		
Parameter	Min	Nom	Max	Min	Nom	Max
10μm x 0.18μm 1.8v FET Vt (V)	0.30	0.36	0.42	-0.33	-0.41	-0.49
10μm x 0.18μm 1.8v FET Idsat (mA)	5.1	6.0	6.9	2.1	2.55	3.0
10μm x 0.18μm 1.8v FET Leff (μm)	0.15	0.17	0.19	0.13	0.15	0.17

Note: These parameters are taken from the unreleased SBC18 electrical specification NPB PS-0267 Revision 5.

The following tables summarize the electrical characteristics of these lots characterized in this report:

NFET:

Mean Vt	Mean K	Mean Leff	Mean Idsat	3 Sigma Vt	3 Sigma Leff	3 Sigma Idsat
0.50	9087	0.156	6.32	0.04	0.012	0.51

PFET:

Mean Vt	Mean K	Mean Leff	Mean Idsat	3 Sigma Vt	3 Sigma Leff	3 Sigma Idsat
-0.45	2019	0.144	-2.54.	0.03	0.012	0.32

For measurements involving a large number of samples, it is almost inevitable that there will be a few "bad points" which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these "bad points," it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3 sigma limits. The standard deviation is then recalculated for the remaining points, and again, all points outside of the 3 sigma limits are removed. This process continues until all data points are within the 3 sigma limits of the distribution. The 3 sigma limits should only cause problems for very large sample sizes.

The three sigma (3 times the standard deviation) matching results for this characterization are presented in the following tables. Both the delta Vgs and delta Id matching results are a function of bias, and are presented with each bias point for all transistor sizes on a page.

The bias range used for this measurement is as follows:
NFET:

Vds	Vgst = Veff = Vgs - Vt
0.2V, 0.6V, 1.0V, 1.4V	0.1V, 0.3V, 0.5V

PFET:

Vds	Vgst = Veff = Vgs - Vt
-0.2V, -0.6V, -1.0V, -1.4V	-0.1V, -0.3V, -0.5V

The delta Vgs and delta Id results are shown with the associated currents which are the mean measured currents for each device. These currents will deviate from the nominal values presented in the electrical specification and the data bank, and are only provided for reference.

NFET Delta Vgs Results

NFET Standard Matched Pair Delta Vgs

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.2V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	68.2mV / 7.9uA	58.6mV / 7.0uA					
2um		34.8mV / 27.2uA					
5um	22.4mV / 71.0uA	21.4mV / 69.2uA				5.3mV / 1.8uA	
10um		15.7mV / 135.3uA	10.0mV / 66.9uA	6.7mV / 32.8uA			
20um	10.9mV / 253.6uA	11.6mV / 253.8uA	6.5mV / 127.9uA	4.4mV / 64.2uA	3.6mV / 18.3uA	2.6mV / 7.3uA	1.8mV / 3.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.0mV / 129.5uA					
10um		10.1mV / 248.5uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.5mV / 1,229.7uA	3.7mV / 707.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.5mV / 36.8uA	
20um					1.0mV / 381.5uA		0.7mV / 74.3uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.2mV / 268.4uA	10.1mV / 248.5uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.6V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	69.1mV / 11.1uA	57.5mV / 9.2uA					
2um		34.6mV / 37.4uA					
5um	21.9mV / 100.5uA	21.8mV / 96.5uA				4.7mV / 1.9uA	
10um		16.1mV / 188.8uA	10.2mV / 75.9uA	6.5mV / 35.8uA			
20um	11.2mV / 356.0uA	11.6mV / 354.9uA	6.5mV / 145.0uA	4.3mV / 70.0uA	3.4mV / 19.4uA	2.3mV / 7.6uA	1.6mV / 3.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.1mV / 174.5uA					
10um		9.5mV / 336.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.7mV / 1,663.3uA	3.8mV / 799.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.4mV / 38.3uA	
20um					0.9mV / 402.8uA		0.7mV / 76.4uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.3mV / 380.6uA	9.5mV / 336.4uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.0V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	70.3mV / 13.9uA	60.3mV / 11.0uA					
2um		35.2mV / 46.3uA					
5um	21.5mV / 127.0uA	22.4mV / 120.7uA				4.3mV / 1.9uA	
10um		16.4mV / 236.8uA	10.4mV / 81.7uA	6.4mV / 37.6uA			
20um	11.6mV / 448.8uA	11.7mV / 446.0uA	6.6mV / 156.1uA	4.2mV / 73.4uA	3.2mV / 20.0uA	2.2mV / 7.7uA	1.5mV / 3.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.4mV / 213.0uA					
10um		10.0mV / 413.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.9mV / 2,038.0uA	3.9mV / 858.4uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.3mV / 39.1uA	
20um					0.9mV / 414.9uA		0.7mV / 77.5uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.4mV / 482.1uA	10.0mV / 413.0uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.4V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	71.4mV / 16.7uA	62.2mV / 12.9uA					
2um		36.2mV / 55.3uA					
5um	21.8mV / 154.1uA	22.9mV / 145.4uA				4.1mV / 2.0uA	
10um		16.8mV / 285.7uA	10.5mV / 86.5uA	6.2mV / 38.9uA			
20um	11.9mV / 544.0uA	11.9mV / 539.3uA	6.9mV / 165.2uA	4.2mV / 76.0uA	3.1mV / 20.5uA	2.1mV / 7.9uA	1.4mV / 3.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.7mV / 251.8uA					
10um		10.5mV / 490.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.1mV / 2,417.1uA	3.9mV / 908.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.3mV / 39.7uA	
20um					0.8mV / 423.9uA		0.7mV / 78.4uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.6mV / 587.1uA	10.5mV / 490.6uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.2V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	72.8mV / 35.1uA	60.4mV / 31.8uA					
2um		36.0mV / 121.5uA					
5um	23.1mV / 317.2uA	21.8mV / 312.2uA				4.6mV / 10.3uA	
10um		16.3mV / 618.3uA	10.6mV / 335.4uA	7.0mV / 169.3uA			
20um	11.8mV / 1,192.2uA	12.0mV / 1,186.9uA	7.0mV / 659.1uA	4.7mV / 335.1uA	3.4mV / 102.7uA	2.2mV / 41.6uA	1.4mV / 21.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.1mV / 598.0uA					
10um		10.8mV / 1,171.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.7mV / 5,722.7uA	3.9mV / 3,547.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.4mV / 210.0uA	
20um					0.8mV / 2,110.6uA		0.6mV / 423.6uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.6mV / 1,230.2uA	10.8mV / 1,171.6uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.6V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	71.7mV / 47.2uA	59.1mV / 41.8uA					
2um		35.6mV / 161.7uA					
5um	22.2mV / 425.4uA	21.6mV / 415.9uA				4.7mV / 11.3uA	
10um		16.1mV / 822.9uA	10.6mV / 411.4uA	7.0mV / 200.1uA			
20um	11.8mV / 1,589.6uA	11.6mV / 1,581.5uA	6.8mV / 806.2uA	4.7mV / 395.5uA	3.5mV / 114.8uA	2.4mV / 45.5uA	1.7mV / 22.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.7mV / 787.1uA					
10um		10.6mV / 1,544.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.8mV / 7,562.9uA	3.8mV / 4,342.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.4mV / 229.7uA	
20um					0.9mV / 2,357.8uA		0.6mV / 459.4uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.4mV / 1,652.4uA	10.6mV / 1,544.9uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.0V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	72.9mV / 53.8uA	62.3mV / 46.8uA					
2um		36.3mV / 182.7uA					
5um	22.9mV / 484.4uA	22.5mV / 471.3uA				4.4mV / 11.5uA	
10um		16.5mV / 932.6uA	10.8mV / 435.4uA	6.9mV / 207.9uA			
20um	12.2mV / 1,803.9uA	12.0mV / 1,792.8uA	6.7mV / 853.0uA	4.6mV / 410.7uA	3.3mV / 117.3uA	2.3mV / 46.2uA	1.6mV / 23.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.1mV / 881.2uA					
10um		11.0mV / 1,732.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.0mV / 8,468.9uA	3.9mV / 4,577.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.3mV / 232.7uA	
20um					0.9mV / 2,405.0uA		0.6mV / 463.6uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	11.6mV / 1,882.2uA	11.0mV / 1,732.3uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.4V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	74.1mV / 59.6uA	63.2mV / 51.0uA					
2um		37.0mV / 201.4uA					
5um	23.3mV / 537.5uA	23.1mV / 521.0uA				4.2mV / 11.6uA	
10um		16.9mV / 1,031.1uA	11.0mV / 454.4uA	6.9mV / 213.8uA			
20um	12.6mV / 1,996.8uA	12.4mV / 1,982.9uA	6.7mV / 890.1uA	4.5mV / 422.2uA	3.2mV / 119.1uA	2.1mV / 46.6uA	1.5mV / 23.2uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.4mV / 965.3uA					
10um		11.1mV / 1,899.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.3mV / 9,275.6uA	4.0mV / 4,765.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.2mV / 234.9uA	
20um					0.8mV / 2,439.3uA		0.6mV / 466.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.8mV / 2,089.5uA	11.1mV / 1,899.6uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.2V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	80.7mV / 68.0uA	71.6mV / 62.0uA					
2um		39.9mV / 234.6uA					
5um	26.7mV / 609.4uA	24.2mV / 600.9uA				3.7mV / 21.8uA	
10um		17.8mV / 1,187.9uA	12.2mV / 671.3uA	7.6mV / 347.4uA			
20um	16.0mV / 2,284.8uA	13.5mV / 2,274.6uA	8.6mV / 1,319.4uA	5.1mV / 686.9uA	3.2mV / 216.1uA	1.9mV / 88.1uA	1.2mV / 44.3uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		18.1mV / 1,153.2uA					
10um		13.2mV / 2,254.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.8mV / 11,284.1uA	3.8mV / 7,209.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.4mV / 443.3uA	
20um					0.8mV / 4,486.6uA		0.6mV / 906.1uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	13.9mV / 2,355.9uA	13.2mV / 2,254.4uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 0.6V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	76.2mV / 97.8uA	62.1mV / 88.9uA					
2um		37.9mV / 333.7uA					
5um	24.7mV / 866.6uA	22.7mV / 852.3uA				4.9mV / 29.9uA	
10um		16.6mV / 1,689.1uA	11.2mV / 959.2uA	7.6mV / 499.6uA			
20um	12.6mV / 3,281.0uA	12.1mV / 3,266.5uA	7.5mV / 1,888.3uA	5.3mV / 988.8uA	3.6mV / 300.6uA	2.5mV / 120.6uA	1.8mV / 60.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.6mV / 1,640.8uA					
10um		11.1mV / 3,231.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.4mV / 16,144.9uA	3.8mV / 10,206.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.5mV / 608.4uA	
20um					0.9mV / 6,209.2uA		0.6mV / 1,232.5uA

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	13.5mV / 2,991.3uA	11.9mV / 2,821.8uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.0V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	76.2mV / 107.6uA	65.4mV / 96.7uA					
2um		38.8mV / 365.0uA					
5um	24.8mV / 952.0uA	23.2mV / 933.5uA				4.6mV / 30.3uA	
10um		17.1mV / 1,849.2uA	11.3mV / 1,007.0uA	7.5mV / 517.0uA			
20um	13.0mV / 3,594.3uA	12.4mV / 3,576.4uA	7.2mV / 1,981.3uA	5.1mV / 1,022.7uA	3.4mV / 306.1uA	2.3mV / 122.0uA	1.7mV / 61.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.0mV / 1,782.8uA					
10um		11.5mV / 3,512.8uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.5mV / 17,580.4uA	3.8mV / 10,665.2uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.4mV / 614.9uA	
20um					0.9mV / 6,310.9uA		0.6mV / 1,241.7uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	12.0mV / 3,721.0uA	11.5mV / 3,512.8uA

NFET 3 Sigma Delta Vgs and Mean Id (Vds = 1.4V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	77.5mV / 115.6uA	68.0mV / 102.9uA					
2um		39.7mV / 390.4uA					
5um	25.4mV / 1,022.0uA	23.9mV / 999.6uA				4.4mV / 30.5uA	
10um		17.5mV / 1,979.8uA	11.5mV / 1,041.5uA	7.4mV / 529.1uA			
20um	13.4mV / 3,849.5uA	12.8mV / 3,828.8uA	7.2mV / 2,048.4uA	5.0mV / 1,046.4uA	3.3mV / 309.8uA	2.2mV / 123.0uA	1.6mV / 61.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.6mV / 1,896.8uA					
10um		11.8mV / 3,738.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.6mV / 18,750.4uA	3.8mV / 10,987.3uA				

Standard Matched Pairs: 20 Fingers

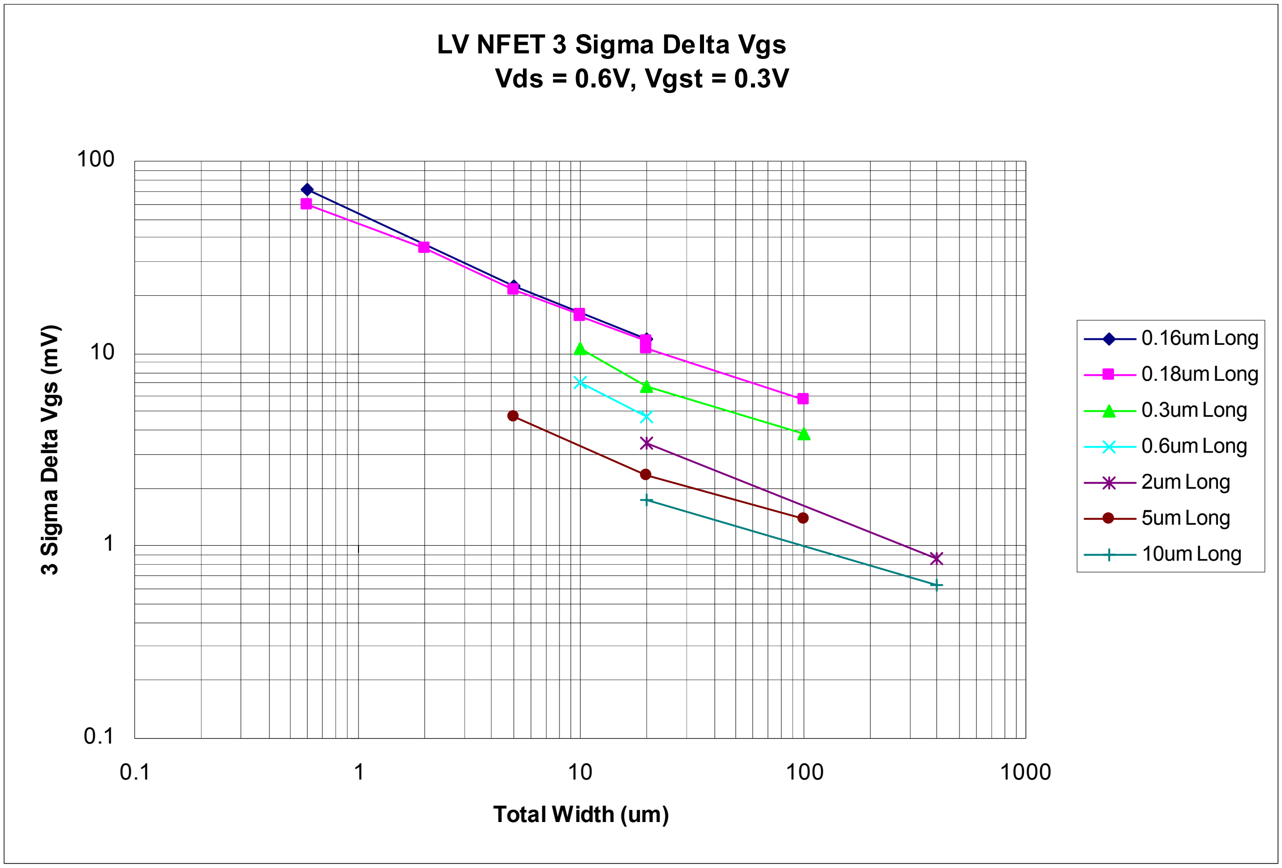
Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.3mV / 619.2uA	
20um					0.8mV / 6,380.7uA		0.6mV / 1,247.7uA

Common Centroid Matched Pairs

Width x Length x Fingers	CC	Std
2 x 10um x 0.18um	12.3mV / 3,993.9uA	11.8mV / 3,738.0uA

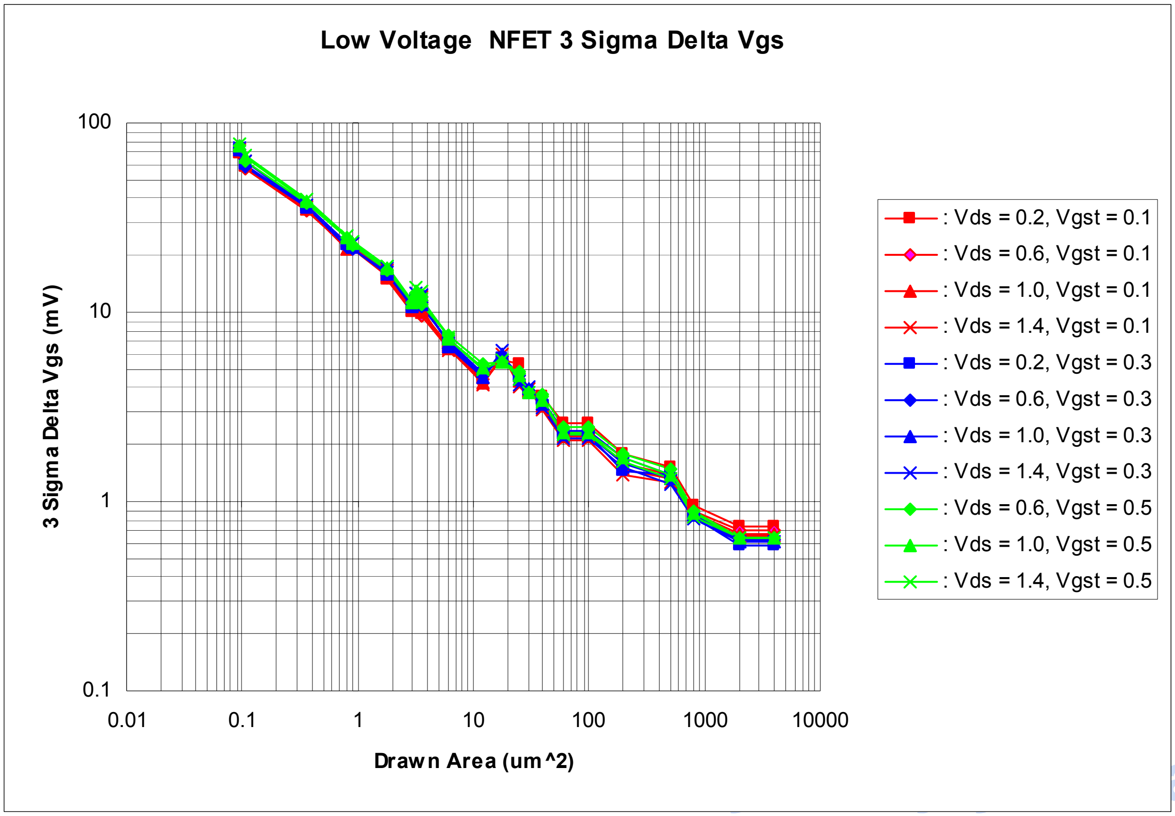
NFET Vgs Matching versus Device Size Plot

The following plot shows the Vgs matching versus device size for a representative (Vds = 0.6V and Vgst = 0.3V) bias point:



NFET Vgs Matching versus Device Area Plot

The following plot shows the Vgs matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ΔW and ΔL.

Fingers	Width	Length	Effective Drawn Area
1	0.6	0.16	0.096
1	0.6	0.18	0.108
1	2	0.18	0.36
1	5	0.16	0.8
1	5	0.18	0.9
1	10	0.18	1.8
2	5	0.18	1.8
1	10	0.30	3
1	20	0.16	3.2
1	20	0.18	3.6
2	10	0.18	3.6
1	10	0.60	6
1	20	0.30	6

Fingers	Width	Length	Effective Drawn Area
1	20	0.60	12
10	10	0.18	18
1	5	5.00	25
10	10	0.30	30
1	20	2.00	40
10	10	0.60	60
1	20	5.00	100
1	20	10.00	200
20	5	5.00	500
20	20	2.00	800
20	20	5.00	2000
20	20	10.00	4000

NFET Delta Id Results

NFET Standard Matched Pair Delta Id

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.2V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	77.6% / 7.9uA	64.5% / 7.0uA					
2um		39.6% / 27.2uA					
5um	25.0% / 71.0uA	25.0% / 69.2uA				7.0% / 1.8uA	
10um		18.5% / 135.3uA	12.6% / 66.9uA	8.3% / 32.8uA			
20um	13.3% / 253.6uA	13.7% / 253.8uA	8.2% / 127.9uA	5.6% / 64.2uA	4.8% / 18.3uA	3.4% / 7.3uA	2.3% / 3.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.5% / 129.5uA					
10um		11.7% / 248.5uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.5% / 1,229.7uA	4.6% / 707.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						2.0% / 36.8uA	
20um					1.2% / 381.5uA		1.0% / 74.3uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.9% / 268.4uA	11.7% / 248.5uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.6V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	75.3% / 11.1uA	59.7% / 9.2uA					
2um		37.3% / 37.4uA					
5um	23.3% / 100.5uA	23.9% / 96.5uA				6.1% / 1.9uA	
10um		17.7% / 188.8uA	12.8% / 75.9uA	8.1% / 35.8uA			
20um	12.8% / 356.0uA	13.2% / 354.9uA	8.3% / 145.0uA	5.5% / 70.0uA	4.4% / 19.4uA	3.0% / 7.6uA	2.1% / 3.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.9% / 174.5uA					
10um		10.9% / 336.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.4% / 1,663.3uA	4.7% / 799.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.8% / 38.3uA	
20um					1.1% / 402.8uA		0.9% / 76.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.1% / 380.6uA	10.9% / 336.4uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.0V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	73.3% / 13.9uA	58.7% / 11.0uA					
2um		36.0% / 46.3uA					
5um	21.4% / 127.0uA	22.7% / 120.7uA				5.6% / 1.9uA	
10um		16.7% / 236.8uA	13.0% / 81.7uA	7.9% / 37.6uA			
20um	12.2% / 448.8uA	12.4% / 446.0uA	8.4% / 156.1uA	5.4% / 73.4uA	4.2% / 20.0uA	2.9% / 7.7uA	1.9% / 3.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.2% / 213.0uA					
10um		10.6% / 413.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.1% / 2,038.0uA	4.8% / 858.4uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.7% / 39.1uA	
20um					1.1% / 414.9uA		0.9% / 77.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.3% / 482.1uA	10.6% / 413.0uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.4V, Vgst = 0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	69.3% / 16.7uA	56.2% / 12.9uA					
2um		34.3% / 55.3uA					
5um	19.8% / 154.1uA	21.6% / 145.4uA				5.3% / 2.0uA	
10um		15.9% / 285.7uA	13.1% / 86.5uA	7.8% / 38.9uA			
20um	11.7% / 544.0uA	11.8% / 539.3uA	8.5% / 165.2uA	5.3% / 76.0uA	4.0% / 20.5uA	2.7% / 7.9uA	1.8% / 3.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.5% / 251.8uA					
10um		10.1% / 490.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.9% / 2,417.1uA	4.8% / 908.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.6% / 39.7uA	
20um					1.1% / 423.9uA		0.8% / 78.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	10.7% / 587.1uA	10.1% / 490.6uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.2V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	33.4% / 35.1uA	28.4% / 31.8uA					
2um		16.6% / 121.5uA					
5um	10.7% / 317.2uA	10.3% / 312.2uA				2.5% / 10.3uA	
10um		7.6% / 618.3uA	5.3% / 335.4uA	3.6% / 169.3uA			
20um	5.6% / 1,192.2uA	5.6% / 1,186.9uA	3.5% / 659.1uA	2.4% / 335.1uA	1.8% / 102.7uA	1.2% / 41.6uA	0.8% / 21.0uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		7.5% / 598.0uA					
10um		5.1% / 1,171.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		2.7% / 5,722.7uA	1.9% / 3,547.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.8% / 210.0uA	
20um					0.4% / 2,110.6uA		0.3% / 423.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	5.4% / 1,230.2uA	5.1% / 1,171.6uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.6V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	35.7% / 47.2uA	30.0% / 41.8uA					
2um		17.2% / 161.7uA					
5um	10.6% / 425.4uA	10.4% / 415.9uA				2.9% / 11.3uA	
10um		7.8% / 822.9uA	6.0% / 411.4uA	4.1% / 200.1uA			
20um	5.8% / 1,589.6uA	5.7% / 1,581.5uA	3.9% / 806.2uA	2.8% / 395.5uA	2.1% / 114.8uA	1.4% / 45.5uA	1.1% / 22.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		7.7% / 787.1uA					
10um		5.3% / 1,544.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		2.9% / 7,562.9uA	2.2% / 4,342.0uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.9% / 229.7uA	
20um					0.5% / 2,357.8uA		0.4% / 459.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	5.5% / 1,652.4uA	5.3% / 1,544.9uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.0V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	34.3% / 53.8uA	29.5% / 46.8uA					
2um		16.9% / 182.7uA					
5um	10.1% / 484.4uA	10.2% / 471.3uA				2.7% / 11.5uA	
10um		7.5% / 932.6uA	6.0% / 435.4uA	4.1% / 207.9uA			
20um	5.7% / 1,803.9uA	5.5% / 1,792.8uA	3.7% / 853.0uA	2.7% / 410.7uA	2.0% / 117.3uA	1.4% / 46.2uA	1.0% / 23.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		7.5% / 881.2uA					
10um		5.2% / 1,732.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		2.8% / 8,468.9uA	2.2% / 4,577.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.8% / 232.7uA	
20um					0.5% / 2,405.0uA		0.4% / 463.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	5.2% / 1,882.2uA	5.2% / 1,732.3uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.4V, Vgst = 0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	33.0% / 59.6uA	29.1% / 51.0uA					
2um		16.3% / 201.4uA					
5um	9.5% / 537.5uA	9.9% / 521.0uA				2.6% / 11.6uA	
10um		7.3% / 1,031.1uA	6.1% / 454.4uA	4.0% / 213.8uA			
20um	5.5% / 1,996.8uA	5.4% / 1,982.9uA	3.7% / 890.1uA	2.7% / 422.2uA	1.9% / 119.1uA	1.3% / 46.6uA	0.9% / 23.2uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		7.3% / 965.3uA					
10um		5.0% / 1,899.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		2.8% / 9,275.6uA	2.2% / 4,765.8uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.8% / 234.9uA	
20um					0.5% / 2,439.3uA		0.4% / 466.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	5.0% / 2,089.5uA	5.0% / 1,899.6uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.2V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	18.5% / 68.0uA	16.0% / 62.0uA					
2um		9.1% / 234.6uA					
5um	6.0% / 609.4uA	5.5% / 600.9uA				0.9% / 21.8uA	
10um		4.0% / 1,187.9uA	2.9% / 671.3uA	1.9% / 347.4uA			
20um	3.6% / 2,284.8uA	3.0% / 2,274.6uA	2.0% / 1,319.4uA	1.3% / 686.9uA	0.8% / 216.1uA	0.5% / 88.1uA	0.3% / 44.3uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		4.1% / 1,153.2uA					
10um		3.0% / 2,254.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.3% / 11,284.1uA	0.9% / 7,209.7uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.4% / 443.3uA	
20um					0.2% / 4,486.6uA		0.2% / 906.1uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	3.1% / 2,355.9uA	3.0% / 2,254.4uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 0.6V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	21.2% / 97.8uA	17.7% / 88.9uA					
2um		10.1% / 333.7uA					
5um	6.5% / 866.6uA	6.1% / 852.3uA				1.9% / 29.9uA	
10um		4.5% / 1,689.1uA	3.6% / 959.2uA	2.7% / 499.6uA			
20um	3.5% / 3,281.0uA	3.3% / 3,266.5uA	2.4% / 1,888.3uA	1.9% / 988.8uA	1.4% / 300.6uA	0.9% / 120.6uA	0.7% / 60.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		4.5% / 1,640.8uA					
10um		3.1% / 3,231.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.5% / 16,144.9uA	1.2% / 10,206.9uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.6% / 608.4uA	
20um					0.3% / 6,209.2uA		0.2% / 1,232.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	3.2% / 3,387.2uA	3.1% / 3,231.6uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.0V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	20.7% / 107.6uA	18.0% / 96.7uA					
2um		10.2% / 365.0uA					
5um	6.4% / 952.0uA	6.0% / 933.5uA				1.8% / 30.3uA	
10um		4.4% / 1,849.2uA	3.6% / 1,007.0uA	2.6% / 517.0uA			
20um	3.4% / 3,594.3uA	3.3% / 3,576.4uA	2.3% / 1,981.3uA	1.8% / 1,022.7uA	1.3% / 306.1uA	0.9% / 122.0uA	0.6% / 61.1uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		4.5% / 1,782.8uA					
10um		3.1% / 3,512.8uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.4% / 17,580.4uA	1.2% / 10,665.2uA				

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.5% / 614.9uA	
20um					0.3% / 6,310.9uA		0.2% / 1,241.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	3.1% / 3,721.0uA	3.1% / 3,512.8uA

NFET 3 Sigma Delta Id and Mean Id (Vds = 1.4V, Vgst = 0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	20.3% / 115.6uA	17.9% / 102.9uA					
2um		10.0% / 390.4uA					
5um	6.2% / 1,022.0uA	6.0% / 999.6uA				1.7% / 30.5uA	
10um		4.4% / 1,979.8uA	3.6% / 1,041.5uA	2.6% / 529.1uA			
20um	3.4% / 3,849.5uA	3.2% / 3,828.8uA	2.3% / 2,048.4uA	1.8% / 1,046.4uA	1.3% / 309.8uA	0.9% / 123.0uA	0.6% / 61.5uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		4.4% / 1,896.8uA					
10um		2.9% / 3,738.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.4% / 18,750.4uA	1.1% / 10,987.3uA				

Standard Matched Pairs: 20 Fingers

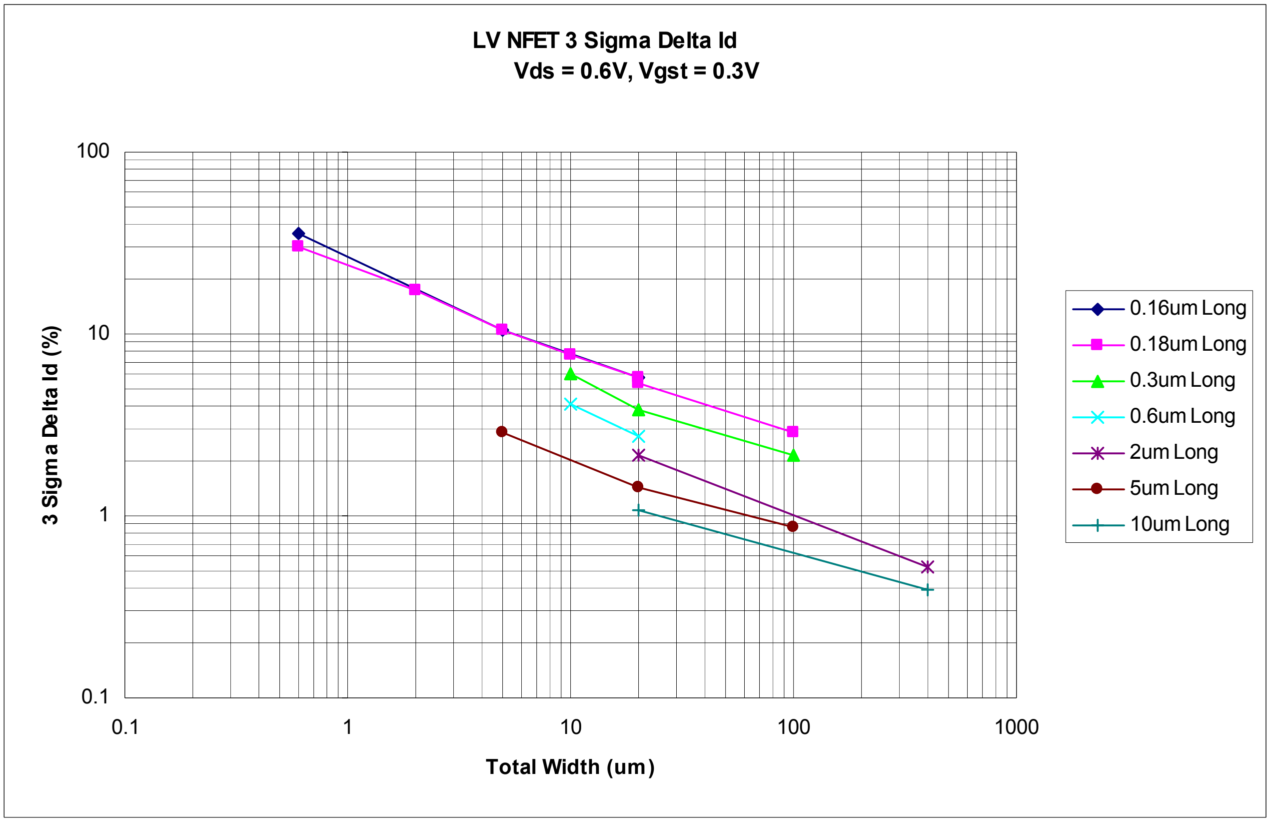
Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.5% / 619.2uA	
20um					0.3% / 6,380.7uA		0.2% / 1,247.7uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	3.0% / 3,993.9uA	2.9% / 3,738.0uA

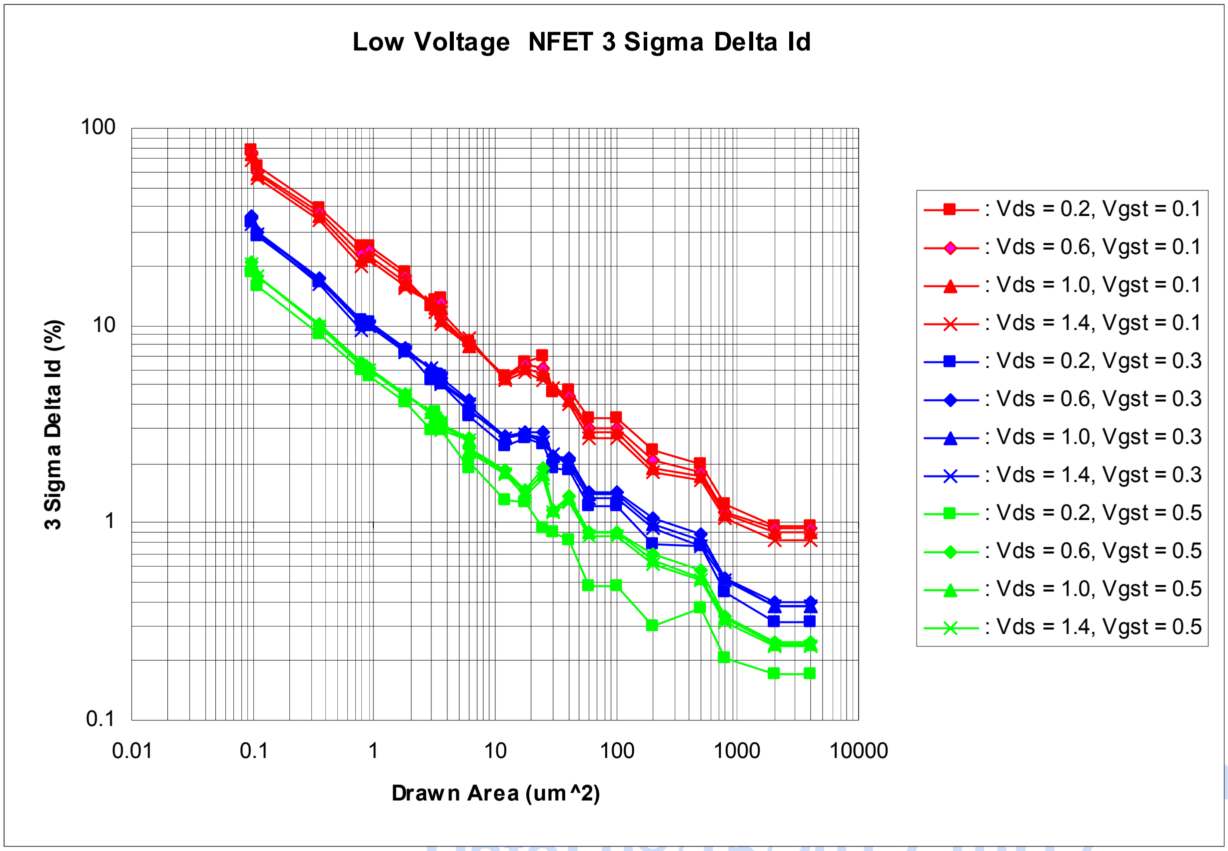
NFET Id Matching versus Device Size Plot

The following plot shows the Id matching versus device size for a representative (Vds = 0.6V and Vgst = 0.3V) bias point:



NFET Id Matching versus Device Area Plot

The following plot shows the Id matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ΔW and ΔL.

Fingers	Width	Length	Effective Drawn Area
1	0.6	0.16	0.096
1	0.6	0.18	0.108
1	2	0.18	0.36
1	5	0.16	0.8
1	5	0.18	0.9
1	10	0.18	1.8
2	5	0.18	1.8
1	10	0.3	3
1	20	0.16	3.2
1	20	0.18	3.6
2	10	0.18	3.6
1	10	0.6	6
1	20	0.3	6

Fingers	Width	Length	Effective Drawn Area
1	20	0.6	12
10	10	0.18	18
1	5	5	25
10	10	0.3	30
1	20	2	40
10	10	0.6	60
1	20	5	100
1	20	10	200
20	5	5	500
20	20	2	800
20	20	5	2000
20	20	10	4000

PFET Delta Vgs Results

PFET Standard Matched Pair Delta Vgs

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.2V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	60.2mV / -2.0uA	51.9mV / -1.7uA					
2um		32.2mV / -6.7uA					
5um	24.3mV / -19.2uA	22.3mV / -18.1uA				2.5mV / -0.4uA	
10um		17.6mV / -37.2uA	8.3mV / -17.1uA	5.3mV / -7.9uA			
20um	12.3mV / -74.2uA	11.3mV / -74.3uA	5.9mV / -34.5uA	3.6mV / -16.0uA	2.1mV / -4.4uA	1.3mV / -1.7uA	1.3mV / -0.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.3mV / -31.2uA					
10um		10.4mV / -64.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		4.7mV / -284.4uA	2.8mV / -147.6uA	1.8mV / -66.6uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.5mV / -7.9uA	
20um					0.9mV / -78.0uA	1.0mV / -32.2uA	1.6mV / -16.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.2mV / -75.9uA	10.4mV / -64.4uA
20 x 20um x	0.5mV / -	1.0mV / -

5um	32.2uA	32.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -66.6uA	2.4mV / -67.7uA	2.9mV / -67.7uA	3.3mV / -68.3uA
20 x 20um x 5um	1.0mV / -32.2uA	1.2mV / -31.9uA	1.4mV / -31.9uA	1.8mV / -31.8uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.6V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	61.4mV / -2.6uA	53.2mV / -2.1uA					
2um		32.8mV / -8.7uA					
5um	24.4mV / -26.1uA	23.0mV / -23.9uA				2.4mV / -0.4uA	
10um		18.0mV / -49.5uA	8.2mV / -19.0uA	5.1mV / -8.4uA			
20um	12.7mV / -98.7uA	11.6mV / -98.7uA	5.9mV / -38.3uA	3.5mV / -17.0uA	2.0mV / -4.5uA	1.2mV / -1.7uA	1.2mV / -0.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.6mV / -39.5uA					
10um		10.6mV / -82.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		4.9mV / -358.4uA	2.8mV / -163.1uA	1.7mV / -70.3uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.6mV / -8.0uA	
20um					0.9mV / -79.7uA	1.0mV / -32.6uA	1.6mV / -16.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.4mV / -102.3uA	10.6mV / -82.2uA
20 x 20um x 5um	0.5mV / -32.5uA	1.0mV / -32.6uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.7mV / -70.3uA	2.4mV / -71.4uA	2.9mV / -71.5uA	3.3mV / -72.2uA
20 x 20um x 5um	1.0mV / -32.6uA	1.2mV / -32.3uA	1.4mV / -32.3uA	1.8mV / -32.2uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.0V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	62.6mV / -2.9uA	53.9mV / -2.3uA					
2um		33.4mV / -10.0uA					
5um	24.9mV / -30.5uA	23.6mV / -27.5uA				2.4mV / -0.4uA	
10um		18.5mV / -57.3uA	8.1mV / -19.9uA	5.1mV / -8.6uA			
20um	13.1mV / -114.2uA	11.9mV / -114.3uA	6.0mV / -40.1uA	3.5mV / -17.4uA	2.0mV / -4.5uA	1.2mV / -1.7uA	1.2mV / -0.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.8mV / -44.4uA					
10um		10.8mV / -92.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.1mV / -403.2uA	2.7mV / -170.4uA	1.8mV / -71.8uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.5mV / -8.0uA	
20um					0.9mV / -80.3uA	1.0mV / -32.7uA	1.6mV / -16.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.6mV / -119.5uA	10.8mV / -92.9uA
20 x 20um x 5um	0.5mV / -32.7uA	1.0mV / -32.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -71.8uA	2.4mV / -73.0uA	2.9mV / -73.1uA	3.3mV / -73.8uA
20 x 20um x 5um	1.0mV / -32.7uA	1.2mV / -32.5uA	1.4mV / -32.4uA	1.8mV / -32.3uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.4V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	63.4mV / -3.3uA	54.6mV / -2.5uA					
2um		33.5mV / -11.1uA					
5um	25.3mV / -34.5uA	24.5mV / -30.8uA				2.4mV / -0.4uA	
10um		18.9mV / -64.1uA	8.1mV / -20.6uA	5.0mV / -8.8uA			
20um	13.5mV / -127.9uA	12.1mV / -128.2uA	6.1mV / -41.5uA	3.5mV / -17.7uA	2.0mV / -4.5uA	1.2mV / -1.7uA	1.2mV / -0.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.0mV / -48.7uA					
10um		11.0mV / -102.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.2mV / -442.3uA	2.8mV / -175.9uA	1.8mV / -73.0uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.5mV / -8.0uA	
20um					0.9mV / -80.7uA	1.0mV / -32.8uA	1.6mV / -16.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.8mV / -134.7uA	11.0mV / -102.2uA
20 x 20um x 5um	0.5mV / -32.7uA	1.0mV / -32.8uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -73.0uA	2.4mV / -74.2uA	2.9mV / -74.2uA	3.3mV / -75.0uA
20 x 20um x 5um	1.0mV / -32.8uA	1.2mV / -32.5uA	1.4mV / -32.5uA	1.8mV / -32.4uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.2V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	60.6mV / -8.7uA	52.6mV / -7.7uA					
2um		33.7mV / -30.4uA					
5um	24.8mV / -86.0uA	22.2mV / -82.0uA				2.5mV / -2.1uA	
10um		18.7mV / -168.9uA	8.7mV / -83.9uA	5.8mV / -39.1uA			
20um	12.5mV / -335.7uA	11.7mV / -338.9uA	6.4mV / -170.2uA	4.0mV / -79.2uA	2.2mV / -21.8uA	1.3mV / -8.5uA	1.2mV / -4.2uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.5mV / -146.9uA					
10um		10.7mV / -304.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.4mV / -1,373.4uA	3.0mV / -743.1uA	1.8mV / -339.4uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.0mV / -39.8uA	
20um					0.7mV / -402.1uA	0.7mV / -163.9uA	1.1mV / -82.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.6mV / -345.7uA	10.7mV / -304.0uA
20 x 20um x 5um	0.4mV / -164.5uA	0.7mV / -163.9uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -339.4uA	2.3mV / -341.7uA	2.9mV / -341.8uA	3.5mV / -343.2uA
20 x 20um x 5um	0.7mV / -163.9uA	0.9mV / -163.5uA	1.2mV / -163.4uA	1.8mV / -163.1uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.6V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	60.7mV / -12.2uA	53.3mV / -10.4uA					
2um		33.8mV / -41.9uA					
5um	25.1mV / -121.4uA	22.9mV / -114.0uA				2.7mV / -2.2uA	
10um		19.0mV / -235.4uA	8.5mV / -102.9uA	5.7mV / -45.2uA			
20um	12.9mV / -469.0uA	12.0mV / -472.2uA	6.3mV / -208.7uA	3.8mV / -91.6uA	2.2mV / -24.0uA	1.4mV / -9.3uA	1.2mV / -4.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.5mV / -199.2uA					
10um		10.8mV / -413.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.5mV / -1,855.3uA	2.9mV / -908.9uA	1.8mV / -389.5uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.1mV / -43.2uA	
20um					0.8mV / -440.9uA	0.8mV / -177.8uA	1.2mV / -89.2uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.5mV / -485.2uA	10.8mV / -413.6uA
20 x 20um x 5um	0.4mV / -178.4uA	0.8mV / -177.8uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -389.5uA	2.4mV / -394.1uA	2.9mV / -394.1uA	3.5mV / -396.1uA
20 x 20um x 5um	0.8mV / -177.8uA	1.0mV / -177.4uA	1.3mV / -177.3uA	1.8mV / -176.9uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.0V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	62.8mV / -13.4uA	54.1mV / -11.3uA					
2um		34.5mV / -46.4uA					
5um	25.6mV / -135.9uA	24.0mV / -126.5uA				2.7mV / -2.3uA	
10um		19.5mV / -261.5uA	8.4mV / -107.5uA	5.6mV / -46.3uA			
20um	13.1mV / -521.7uA	11.9mV / -524.8uA	6.3mV / -218.1uA	3.9mV / -93.8uA	2.2mV / -24.2uA	1.4mV / -9.3uA	1.2mV / -4.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		15.8mV / -217.9uA					
10um		11.1mV / -453.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.5mV / -2,028.0uA	3.0mV / -948.4uA	1.8mV / -398.0uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.1mV / -43.4uA	
20um					0.8mV / -444.3uA	0.8mV / -178.5uA	1.2mV / -89.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	11.8mV / -541.6uA	11.1mV / -453.3uA
20 x 20um x 5um	0.4mV / -179.1uA	0.8mV / -178.5uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -398.0uA	2.4mV / -404.2uA	2.9mV / -404.3uA	3.7mV / -406.3uA
20 x 20um x 5um	0.8mV / -178.5uA	1.0mV / -178.2uA	1.3mV / -178.0uA	1.8mV / -177.7uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.4V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	63.9mV / -14.4uA	53.9mV / -11.9uA					
2um		35.1mV / -49.7uA					
5um	25.7mV / -147.1uA	24.6mV / -136.0uA				2.6mV / -2.3uA	
10um		19.9mV / -281.6uA	8.4mV / -110.7uA	5.6mV / -47.1uA			
20um	13.5mV / -561.8uA	12.2mV / -565.0uA	6.3mV / -224.6uA	3.9mV / -95.3uA	2.2mV / -24.3uA	1.3mV / -9.3uA	1.2mV / -4.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.0mV / -231.9uA					
10um		11.3mV / -483.1uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.7mV / -2,158.0uA	2.9mV / -975.5uA	1.8mV / -403.8uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.1mV / -43.5uA	
20um					0.8mV / -446.6uA	0.8mV / -178.9uA	1.2mV / -89.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.0mV / -585.2uA	11.3mV / -483.1uA
20 x 20um x 5um	0.4mV / -179.5uA	0.8mV / -178.9uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -403.8uA	2.5mV / -411.7uA	3.0mV / -411.8uA	3.9mV / -413.9uA
20 x 20um x 5um	0.8mV / -178.9uA	1.0mV / -178.7uA	1.3mV / -178.6uA	1.8mV / -178.2uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.2V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	66.9mV / -17.4uA	56.9mV / -15.6uA					
2um		38.2mV / -60.5uA					
5um	27.0mV / -170.0uA	24.5mV / -162.7uA				2.7mV / -4.3uA	
10um		21.1mV / -334.9uA	9.8mV / -172.2uA	6.7mV / -81.7uA			
20um	15.2mV / -666.1uA	13.2mV / -670.8uA	7.5mV / -348.8uA	4.3mV / -165.4uA	2.3mV / -45.8uA	1.4mV / -17.9uA	1.3mV / -8.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.1mV / -292.8uA					
10um		12.4mV / -604.5uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.0mV / -2,793.3uA	3.3mV / -1,553.6uA	1.9mV / -722.7uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.7mV / -83.7uA	
20um					0.6mV / -863.3uA	0.0mV / -352.1uA	0.7mV / -177.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	13.6mV / -682.3uA	12.4mV / -604.5uA
20 x 20um x 5um	0.1mV / -353.2uA	0.0mV / -352.1uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.9mV / -722.7uA	8.4mV / -824.4uA	8.8mV / -824.5uA	12.4mV / -827.4uA
20 x 20um x 5um	0.0mV / -352.1uA	4.2mV / -381.8uA	5.1mV / -381.6uA	6.2mV / -381.0uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -0.6V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	64.4mV / -27.9uA	54.8mV / -24.5uA					
2um		36.3mV / -96.5uA					
5um	25.7mV / -274.0uA	24.2mV / -260.1uA				3.1mV / -5.8uA	
10um		20.3mV / -535.6uA	9.4mV / -254.6uA	6.5mV / -114.9uA			
20um	13.8mV / -1,068.1uA	12.3mV / -1,073.8uA	6.9mV / -516.7uA	4.3mV / -232.5uA	2.5mV / -61.6uA	1.6mV / -23.8uA	1.3mV / -11.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.4mV / -464.8uA					
10um		11.7mV / -961.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.8mV / -4,426.5uA	3.1mV / -2,299.1uA	1.8mV / -1,008.8uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.9mV / -111.5uA	
20um					0.7mV / -1,153.8uA	0.5mV / -466.2uA	0.8mV / -233.9uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.4mV / -1,098.1uA	11.7mV / -961.3uA
20 x 20um x 5um	0.1mV / -467.9uA	0.5mV / -466.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -1,008.8uA	6.8mV / -1,167.8uA	7.3mV / -1,167.4uA	10.0mV / -1,173.0uA
20 x 20um x 5um	0.5mV / -466.2uA	3.1mV / -506.3uA	3.7mV / -506.0uA	4.7mV / -505.1uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.0V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	64.6mV / -30.8uA	55.5mV / -26.6uA					
2um		36.8mV / -106.4uA					
5um	26.2mV / -304.8uA	25.0mV / -287.5uA				3.0mV / -5.8uA	
10um		20.8mV / -592.4uA	9.2mV / -267.6uA	6.3mV / -118.0uA			
20um	14.1mV / -1,182.2uA	12.6mV / -1,187.5uA	6.9mV / -542.9uA	4.2mV / -238.9uA	2.5mV / -62.3uA	1.5mV / -24.0uA	1.3mV / -11.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.7mV / -508.5uA					
10um		12.0mV / -1,052.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.9mV / -4,844.3uA	3.1mV / -2,413.7uA	1.8mV / -1,034.3uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.9mV / -112.0uA	
20um					0.7mV / -1,164.1uA	0.6mV / -468.2uA	0.8mV / -234.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.6mV / -1,218.6uA	12.0mV / -1,052.9uA
20 x 20um x 5um	0.1mV / -469.9uA	0.6mV / -468.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.8mV / -1,034.3uA	8.2mV / -1,239.8uA	8.9mV / -1,240.1uA	12.0mV / -1,245.6uA
20 x 20um x 5um	0.6mV / -468.2uA	3.5mV / -517.2uA	4.2mV / -516.9uA	5.3mV / -515.9uA

PFET 3 Sigma Delta Vgs and Mean Id (Vds = -1.4V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	65.8mV / -32.7uA	56.3mV / -27.9uA					
2um		37.4mV / -112.7uA					
5um	26.7mV / -324.8uA	25.2mV / -305.0uA				3.0mV / -5.8uA	
10um		21.3mV / -628.9uA	9.2mV / -275.1uA	6.2mV / -119.8uA			
20um	14.6mV / -1,255.2uA	12.9mV / -1,260.5uA	6.9mV / -558.1uA	4.2mV / -242.5uA	2.4mV / -62.6uA	1.5mV / -24.0uA	1.3mV / -11.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		16.9mV / -535.7uA					
10um		12.3mV / -1,110.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		6.1mV / -5,109.6uA	3.2mV / -2,479.0uA	1.9mV / -1,048.9uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.9mV / -112.3uA	
20um					0.7mV / -1,169.9uA	0.5mV / -469.3uA	0.8mV / -234.7uA

Common Centroid Matched Pairs

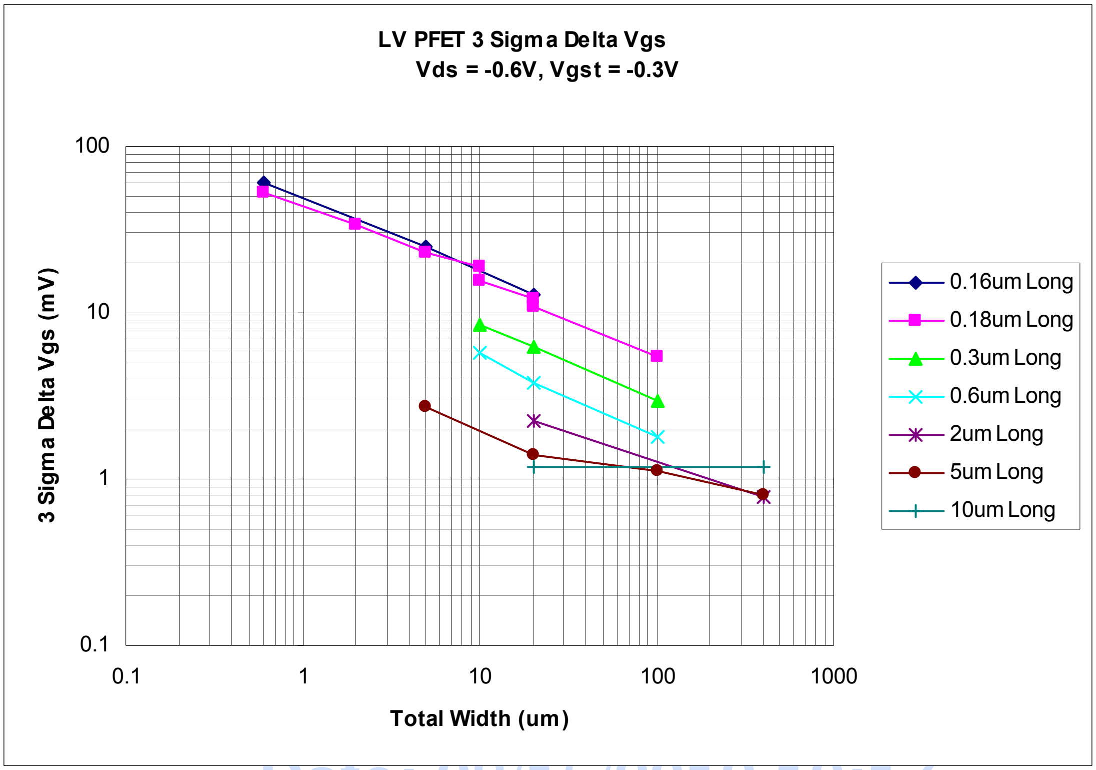
Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.9mV / -1,296.8uA	12.3mV / -1,110.2uA
20 x 20um x 5um	0.1mV / -471.1uA	0.5mV / -469.3uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.9mV / -1,048.9uA	9.7mV / -1,301.0uA	10.5mV / -1,301.2uA	14.1mV / -1,307.2uA
20 x 20um x 5um	0.5mV / -469.3uA	4.1mV / -526.7uA	4.7mV / -526.4uA	5.9mV / -525.4uA

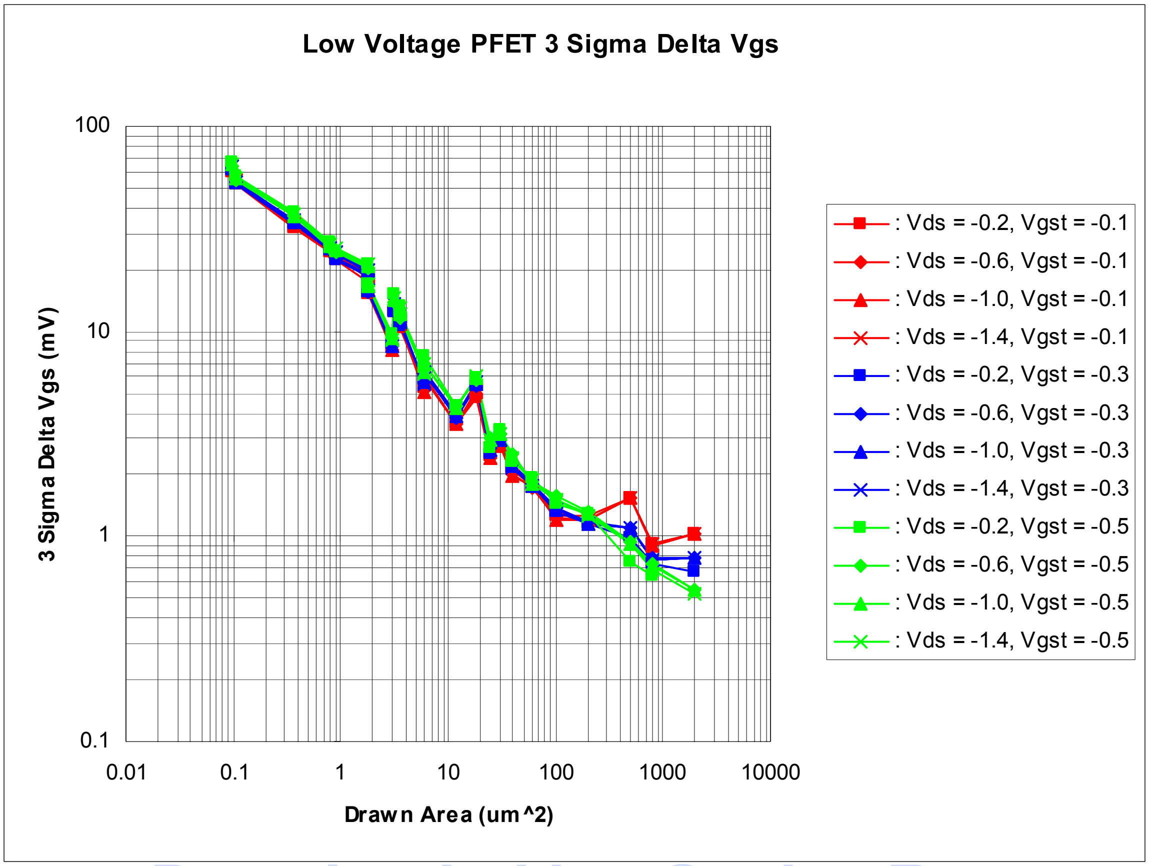
PFET Vgs Matching versus Device Size Plot

The following plot shows the Vgs matching versus device size for a representative (Vds = -0.6V and Vgst = -0.3V) bias point:



PFET Vgs Matching versus Device Area Plot

The following plot shows the Vgs matching results versus device area for all bias points:



Fingers	Width	Length	Effective Drawn Area
1	0.6	0.16	0.096
1	0.6	0.18	0.108
1	2	0.18	0.36
1	5	0.16	0.8
1	5	0.18	0.9
1	10	0.18	1.8
2	5	0.18	1.8
1	10	0.3	3
1	20	0.16	3.2
1	20	0.18	3.6
2	10	0.18	3.6
1	10	0.6	6
1	20	0.3	6

Fingers	Width	Length	Effective Drawn Area
1	20	0.6	12
10	10	0.18	18
1	5	5	25
10	10	0.3	30
1	20	2	40
10	10	0.6	60
1	20	5	100
1	20	10	200
20	5	5	500
20	20	2	800
20	20	5	2000
20	20	10	4000

PFET Delta Id Results

PFET Standard Matched Pair Delta Id

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.2V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	65.8% / -2.0uA	58.6% / -1.7uA					
2um		34.9% / -6.7uA					
5um	26.3% / -19.2uA	25.1% / -18.1uA				2.9% / -0.4uA	
10um		19.4% / -37.2uA	9.8% / -17.1uA	6.2% / -7.9uA			
20um	13.6% / -74.2uA	12.6% / -74.3uA	7.1% / -34.5uA	4.2% / -16.0uA	2.4% / -4.4uA	1.5% / -1.7uA	1.4% / -0.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.6% / -31.2uA					
10um		11.8% / -64.4uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.6% / -284.4uA	3.4% / -147.6uA	2.1% / -66.6uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.8% / -7.9uA	
20um					1.1% / -78.0uA	1.2% / -32.2uA	1.9% / -16.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.8% / -75.9uA	11.8% / -64.4uA

20 x 20um x 5um	0.5% / -32.2uA	1.2% / -32.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	2.1% / -66.6uA	2.8% / -67.7uA	3.3% / -67.7uA	3.7% / -68.3uA
20 x 20um x 5um	1.2% / -32.2uA	1.4% / -31.9uA	1.7% / -31.9uA	2.2% / -31.8uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.6V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	66.4% / -2.6uA	60.3% / -2.1uA					
2um		34.7% / -8.7uA					
5um	26.4% / -26.1uA	26.2% / -23.9uA				2.8% / -0.4uA	
10um		19.1% / -49.5uA	9.8% / -19.0uA	6.1% / -8.4uA			
20um	14.1% / -98.7uA	12.4% / -98.7uA	7.2% / -38.3uA	4.2% / -17.0uA	2.4% / -4.5uA	1.4% / -1.7uA	1.4% / -0.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.9% / -39.5uA					
10um		12.2% / -82.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.8% / -358.4uA	3.4% / -163.1uA	2.1% / -70.3uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.8% / -8.0uA	
20um					1.1% / -79.7uA	1.2% / -32.6uA	1.9% / -16.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.4% / -102.3uA	12.2% / -82.2uA
20 x 20um x 5um	0.6% / -32.5uA	1.2% / -32.6uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	2.1% / -70.3uA	2.8% / -71.4uA	3.4% / -71.5uA	3.7% / -72.2uA
20 x 20um x 5um	1.2% / -32.6uA	1.5% / -32.3uA	1.7% / -32.3uA	2.2% / -32.2uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.0V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	65.5% / -2.9uA	61.0% / -2.3uA					
2um		34.3% / -10.0uA					
5um	25.9% / -30.5uA	25.7% / -27.5uA				2.8% / -0.4uA	
10um		19.3% / -57.3uA	9.8% / -19.9uA	6.0% / -8.6uA			
20um	14.1% / -114.2uA	12.1% / -114.3uA	7.2% / -40.1uA	4.1% / -17.4uA	2.3% / -4.5uA	1.4% / -1.7uA	1.4% / -0.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.8% / -44.4uA					
10um		12.2% / -92.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.8% / -403.2uA	3.4% / -170.4uA	2.1% / -71.8uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.8% / -8.0uA	
20um					1.1% / -80.3uA	1.2% / -32.7uA	1.9% / -16.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.2% / -119.5uA	12.2% / -92.9uA
20 x 20um x 5um	0.5% / -32.7uA	1.2% / -32.7uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	2.1% / -71.8uA	2.8% / -73.0uA	3.3% / -73.1uA	3.7% / -73.8uA
20 x 20um x 5um	1.2% / -32.7uA	1.5% / -32.5uA	1.7% / -32.4uA	2.2% / -32.3uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.4V, Vgst = -0.1V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	64.8% / -3.3uA	60.9% / -2.5uA					
2um		33.9% / -11.1uA					
5um	25.4% / -34.5uA	25.5% / -30.8uA				2.8% / -0.4uA	
10um		19.1% / -64.1uA	9.8% / -20.6uA	6.0% / -8.8uA			
20um	14.1% / -127.9uA	12.0% / -128.2uA	7.4% / -41.5uA	4.2% / -17.7uA	2.3% / -4.5uA	1.4% / -1.7uA	1.4% / -0.9uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		17.6% / -48.7uA					
10um		12.1% / -102.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		5.9% / -442.3uA	3.4% / -175.9uA	2.1% / -73.0uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						1.8% / -8.0uA	
20um					1.1% / -80.7uA	1.2% / -32.8uA	1.9% / -16.6uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	12.0% / -134.7uA	12.1% / -102.2uA
20 x 20um x 5um	0.5% / -32.7uA	1.2% / -32.8uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	2.1% / -73.0uA	2.8% / -74.2uA	3.3% / -74.2uA	3.7% / -75.0uA
20 x 20um x 5um	1.2% / -32.8uA	1.5% / -32.5uA	1.7% / -32.5uA	2.2% / -32.4uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.2V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	28.6% / -8.7uA	25.9% / -7.7uA					
2um		16.2% / -30.4uA					
5um	11.7% / -86.0uA	10.8% / -82.0uA				1.3% / -2.1uA	
10um		8.9% / -168.9uA	4.4% / -83.9uA	3.0% / -39.1uA			
20um	6.2% / -335.7uA	5.7% / -338.9uA	3.3% / -170.2uA	2.1% / -79.2uA	1.1% / -21.8uA	0.7% / -8.5uA	0.6% / -4.2uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		7.6% / -146.9uA					
10um		5.2% / -304.0uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		2.6% / -1,373.4uA	1.5% / -743.1uA	0.9% / -339.4uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.5% / -39.8uA	
20um					0.4% / -402.1uA	0.4% / -163.9uA	0.6% / -82.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	5.6% / -345.7uA	5.2% / -304.0uA
20 x 20um x 5um	0.2% / -164.5uA	0.4% / -163.9uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	0.9% / -339.4uA	1.2% / -341.7uA	1.5% / -341.8uA	1.8% / -343.2uA
20 x 20um x 5um	0.4% / -163.9uA	0.5% / -163.5uA	0.6% / -163.4uA	0.9% / -163.1uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.6V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	31.6% / -12.2uA	29.4% / -10.4uA					
2um		18.2% / -41.9uA					
5um	13.0% / -121.4uA	12.4% / -114.0uA				1.6% / -2.2uA	
10um		10.2% / -235.4uA	5.0% / -102.9uA	3.4% / -45.2uA			
20um	7.0% / -469.0uA	6.4% / -472.2uA	3.7% / -208.7uA	2.3% / -91.6uA	1.3% / -24.0uA	0.8% / -9.3uA	0.7% / -4.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		8.8% / -199.2uA					
10um		6.0% / -413.6uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		3.1% / -1,855.3uA	1.8% / -908.9uA	1.1% / -389.5uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.7% / -43.2uA	
20um					0.5% / -440.9uA	0.5% / -177.8uA	0.7% / -89.2uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	6.2% / -485.2uA	6.0% / -413.6uA
20 x 20um x 5um	0.3% / -178.4uA	0.5% / -177.8uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.1% / -389.5uA	1.4% / -394.1uA	1.7% / -394.1uA	2.0% / -396.1uA
20 x 20um x 5um	0.5% / -177.8uA	0.6% / -177.4uA	0.8% / -177.3uA	1.1% / -176.9uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.0V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	33.9% / -13.4uA	29.7% / -11.3uA					
2um		18.3% / -46.4uA					
5um	12.8% / -135.9uA	12.7% / -126.5uA				1.6% / -2.3uA	
10um		10.3% / -261.5uA	5.0% / -107.5uA	3.3% / -46.3uA			
20um	7.2% / -521.7uA	6.4% / -524.8uA	3.7% / -218.1uA	2.3% / -93.8uA	1.3% / -24.2uA	0.8% / -9.3uA	0.7% / -4.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		8.8% / -217.9uA					
10um		6.1% / -453.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		3.1% / -2,028.0uA	1.8% / -948.4uA	1.1% / -398.0uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.7% / -43.4uA	
20um					0.5% / -444.3uA	0.5% / -178.5uA	0.7% / -89.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	6.2% / -541.6uA	6.1% / -453.3uA
20 x 20um x 5um	0.3% / -179.1uA	0.5% / -178.5uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.1% / -398.0uA	1.4% / -404.2uA	1.7% / -404.3uA	2.1% / -406.3uA
20 x 20um x 5um	0.5% / -178.5uA	0.6% / -178.2uA	0.8% / -178.0uA	1.1% / -177.7uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.4V, Vgst = -0.3V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	33.4% / -14.4uA	29.8% / -11.9uA					
2um		18.2% / -49.7uA					
5um	12.8% / -147.1uA	12.6% / -136.0uA				1.6% / -2.3uA	
10um		10.3% / -281.6uA	4.9% / -110.7uA	3.3% / -47.1uA			
20um	7.2% / -561.8uA	6.4% / -565.0uA	3.7% / -224.6uA	2.3% / -95.3uA	1.3% / -24.3uA	0.8% / -9.3uA	0.7% / -4.6uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		8.7% / -231.9uA					
10um		6.1% / -483.1uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		3.1% / -2,158.0uA	1.7% / -975.5uA	1.1% / -403.8uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.7% / -43.5uA	
20um					0.5% / -446.6uA	0.5% / -178.9uA	0.7% / -89.5uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	6.2% / -585.2uA	6.1% / -483.1uA
20 x 20um x 5um	0.2% / -179.5uA	0.5% / -178.9uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	1.1% / -403.8uA	1.4% / -411.7uA	1.8% / -411.8uA	2.2% / -413.9uA
20 x 20um x 5um	0.5% / -178.9uA	0.6% / -178.7uA	0.8% / -178.6uA	1.1% / -178.2uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.2V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	15.8% / -17.4uA	14.1% / -15.6uA					
2um		9.0% / -60.5uA					
5um	6.3% / -170.0uA	5.9% / -162.7uA				0.7% / -4.3uA	
10um		5.0% / -334.9uA	2.5% / -172.2uA	1.7% / -81.7uA			
20um	3.6% / -666.1uA	3.1% / -670.8uA	1.9% / -348.8uA	1.1% / -165.4uA	0.6% / -45.8uA	0.4% / -17.9uA	0.3% / -8.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		4.1% / -292.8uA					
10um		2.9% / -604.5uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.4% / -2,793.3uA	0.8% / -1,553.6uA	0.5% / -722.7uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.2% / -83.7uA	
20um					0.2% / -863.3uA	0.1% / -352.1uA	0.2% / -177.0uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	3.2% / -682.3uA	2.9% / -604.5uA
20 x 20um x 5um	0.1% / -353.2uA	0.1% / -352.1uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	0.5% / -722.7uA	1.8% / -824.4uA	1.9% / -824.5uA	2.5% / -827.4uA
20 x 20um x 5um	0.1% / -352.1uA	1.0% / -381.8uA	1.2% / -381.6uA	1.4% / -381.0uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -0.6V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	20.4% / -27.9uA	18.2% / -24.5uA					
2um		11.3% / -96.5uA					
5um	7.9% / -274.0uA	7.5% / -260.1uA				1.1% / -5.8uA	
10um		6.3% / -535.6uA	3.3% / -254.6uA	2.3% / -114.9uA			
20um	4.4% / -1,068.1uA	3.9% / -1,073.8uA	2.4% / -516.7uA	1.6% / -232.5uA	1.0% / -61.6uA	0.6% / -23.8uA	0.5% / -11.7uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		5.3% / -464.8uA					
10um		3.8% / -961.3uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.8% / -4,426.5uA	1.1% / -2,299.1uA	0.7% / -1,008.8uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.4% / -111.5uA	
20um					0.3% / -1,153.8uA	0.2% / -466.2uA	0.3% / -233.9uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	3.9% / -1,098.1uA	3.8% / -961.3uA
20 x 20um x 5um	0.2% / -467.9uA	0.2% / -466.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	0.7% / -1,008.8uA	2.1% / -1,167.8uA	2.2% / -1,167.4uA	2.9% / -1,173.0uA
20 x 20um x 5um	0.2% / -466.2uA	1.0% / -506.3uA	1.2% / -506.0uA	1.6% / -505.1uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.0V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	21.1% / -30.8uA	18.5% / -26.6uA					
2um		11.7% / -106.4uA					
5um	8.1% / -304.8uA	7.8% / -287.5uA				1.1% / -5.8uA	
10um		6.5% / -592.4uA	3.3% / -267.6uA	2.3% / -118.0uA			
20um	4.6% / -1,182.2uA	4.0% / -1,187.5uA	2.5% / -542.9uA	1.6% / -238.9uA	0.9% / -62.3uA	0.6% / -24.0uA	0.5% / -11.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		5.4% / -508.5uA					
10um		3.9% / -1,052.9uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.9% / -4,844.3uA	1.1% / -2,413.7uA	0.7% / -1,034.3uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.4% / -112.0uA	
20um					0.3% / -1,164.1uA	0.2% / -468.2uA	0.3% / -234.4uA

Common Centroid Matched Pairs

Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	4.0% / -1,218.6uA	3.9% / -1,052.9uA
20 x 20um x 5um	0.2% / -469.9uA	0.2% / -468.2uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	0.7% / -1,034.3uA	2.4% / -1,239.8uA	2.6% / -1,240.1uA	3.3% / -1,245.6uA
20 x 20um x 5um	0.2% / -468.2uA	1.2% / -517.2uA	1.4% / -516.9uA	1.8% / -515.9uA

PFET 3 Sigma Delta Id and Mean Id (Vds = -1.4V, Vgst = -0.5V)

Standard Matched Pairs: 1 Finger

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
0.6um	21.3% / -32.7uA	18.7% / -27.9uA					
2um		11.7% / -112.7uA					
5um	8.1% / -324.8uA	7.9% / -305.0uA				1.1% / -5.8uA	
10um		6.6% / -628.9uA	3.2% / -275.1uA	2.3% / -119.8uA			
20um	4.7% / -1,255.2uA	4.0% / -1,260.5uA	2.4% / -558.1uA	1.6% / -242.5uA	0.9% / -62.6uA	0.6% / -24.0uA	0.5% / -11.8uA

Standard Matched Pairs: 2 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um		5.5% / -535.7uA					
10um		4.0% / -1,110.2uA					

Standard Matched Pairs: 10 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
10um		1.9% / -5,109.6uA	1.1% / -2,479.0uA	0.7% / -1,048.9uA			

Standard Matched Pairs: 20 Fingers

Width\Length	0.16um	0.18um	0.3um	0.6um	2um	5um	10um
5um						0.4% / -112.3uA	
20um					0.3% / -1,169.9uA	0.2% / -469.3uA	0.3% / -234.7uA

Common Centroid Matched Pairs

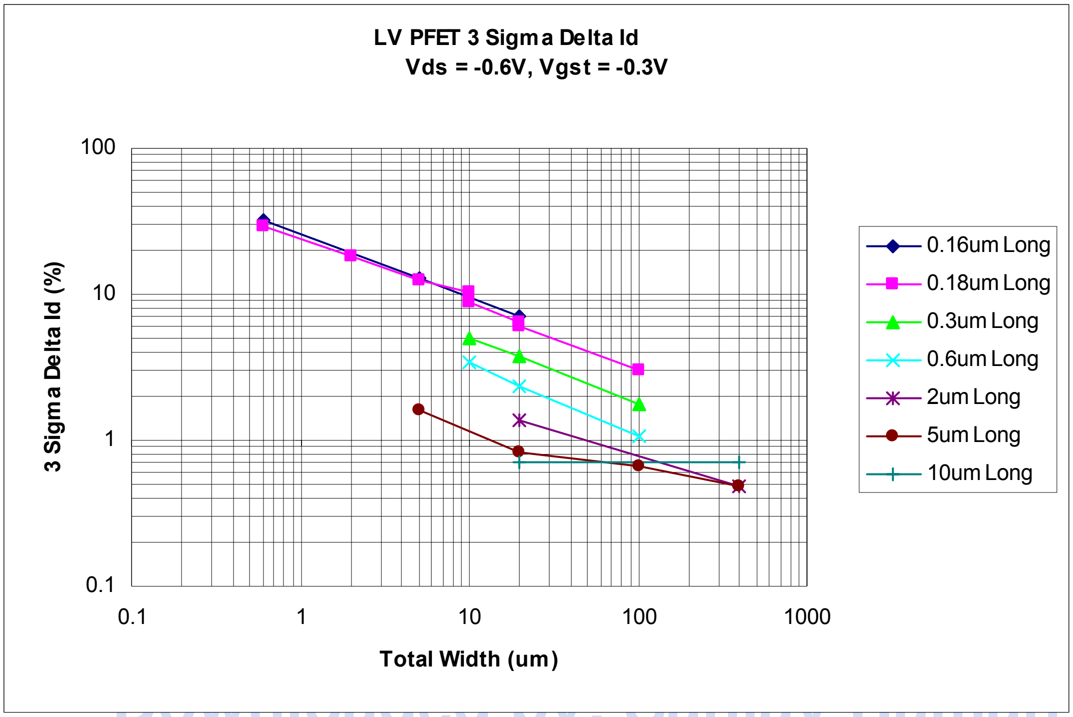
Fingers x Width x Length	CC	Std
2 x 10um x 0.18um	4.0% / -1,296.8uA	4.0% / -1,110.2uA
20 x 20um x 5um	0.2% / -471.1uA	0.2% / -469.3uA

Standard Matched Pairs Versus Separation Distance

Fingers x Width x Length	10um	140um	560um	1260um
10 x 10um x 0.6um	0.7% / -1,048.9uA	2.8% / -1,301.0uA	3.0% / -1,301.2uA	3.7% / -1,307.2uA
20 x 20um x 5um	0.2% / -469.3uA	1.3% / -526.7uA	1.5% / -526.4uA	1.9% / -525.4uA

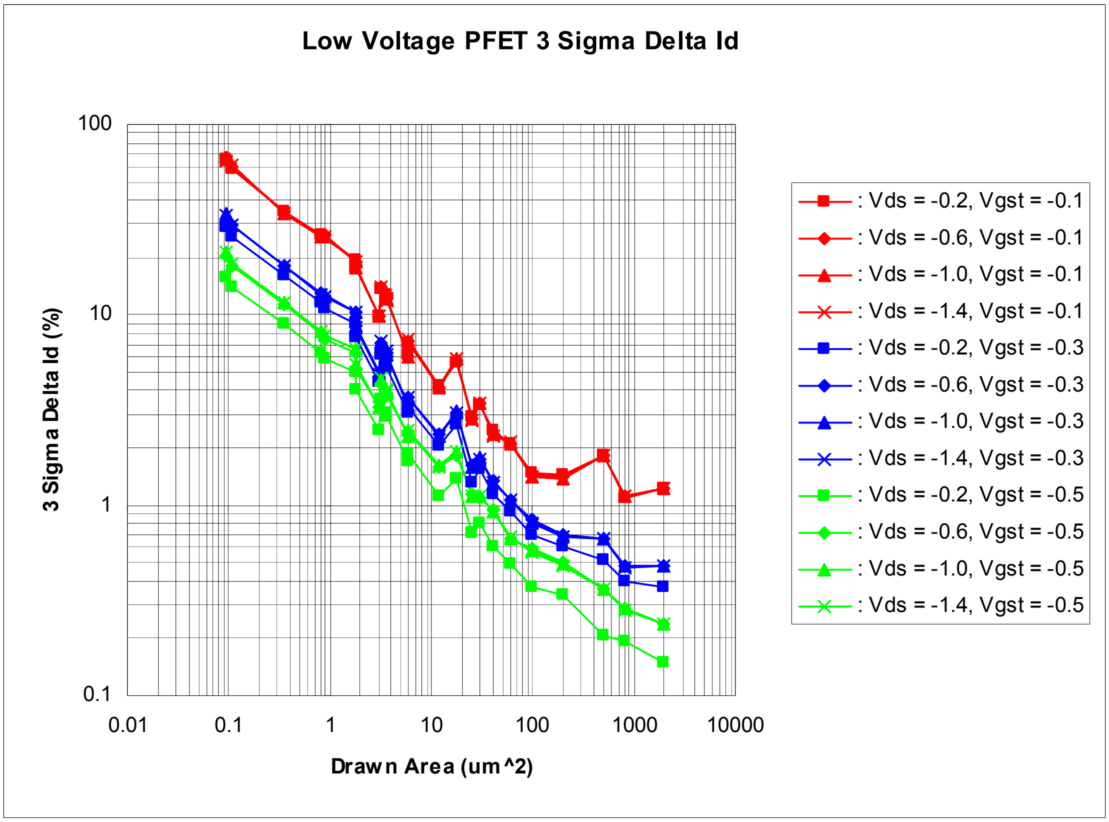
PFET Id Matching versus Device Size Plot

The following plot shows the Id matching versus device size for a representative (Vds = -0.6V and Vgst = -0.3V) bias point:



PFET Id Matching versus Device Area Plot

The following plot shows the Id matching results versus device area for all bias points:



Note: The drawn area has not been corrected for ΔW and ΔL.

Fingers	Width	Length	Effective Drawn Area
1	0.6	0.16	0.096
1	0.6	0.18	0.108
1	2	0.18	0.36
1	5	0.16	0.8
1	5	0.18	0.9
1	10	0.18	1.8
2	5	0.18	1.8
1	10	0.3	3
1	20	0.16	3.2
1	20	0.18	3.6
2	10	0.18	3.6
1	10	0.6	6
1	20	0.3	6

Fingers	Width	Length	Effective Drawn Area
1	20	0.6	12
10	10	0.18	18
1	5	5	25
10	10	0.3	30
1	20	2	40
10	10	0.6	60
1	20	5	100
1	20	10	200
20	5	5	500
20	20	2	800
20	20	5	2000
20	20	10	4000

Delta Id Matching Model

The following simple first order saturation model has been used to the model delta Id results:

$$Id = \beta(Vgs - Vt)^2 \text{ where } \beta = \frac{\mu_o \cdot Cox}{2} \cdot \frac{W}{L}$$

$$\Delta_{Id} = \Delta_\beta \left[\frac{\delta Id}{\delta \beta}\right] + \Delta_{Vt}\left[\frac{\delta Id}{\delta Vt}\right]$$

$$\Delta_{Id} = \Delta_\beta (Vgs - Vt)^2 + \Delta_{Vt}(-2 \cdot \beta \cdot (Vgs - Vt))$$

$$\frac{\Delta_{Id}}{Id} = \frac{\Delta_\beta}{\beta} + \Delta_{Vt}\left(-\frac{2}{Vgs - Vt}\right)$$

$$\sigma_{\frac{\Delta_{Id}}{Id}}{}^2 = \frac{\sigma_\beta{}^2}{\beta^2} + \sigma_{Vt}{}^2\left[\frac{2}{Vgs - Vt}\right]^2$$

$$\sigma_\beta = \frac{A_\beta}{\sqrt{W \cdot L}}$$

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{W \cdot L}}$$

Note that it is easier to express the β dependence as a function of σ_β/β in percent, as then one does not need to know the value of β, and the Vgs – Vt term can be expressed as Vgst. The equation can be rewritten in the following manner, which is independent of the model parameters:

$$\sigma_{\frac{\Delta_{Id}}{Id}}{}^2 = \left(\frac{\sigma_{\beta\%}}{100}\right)^2 + \sigma_{Vt}{}^2\left[\frac{2}{Vgst}\right]^2$$

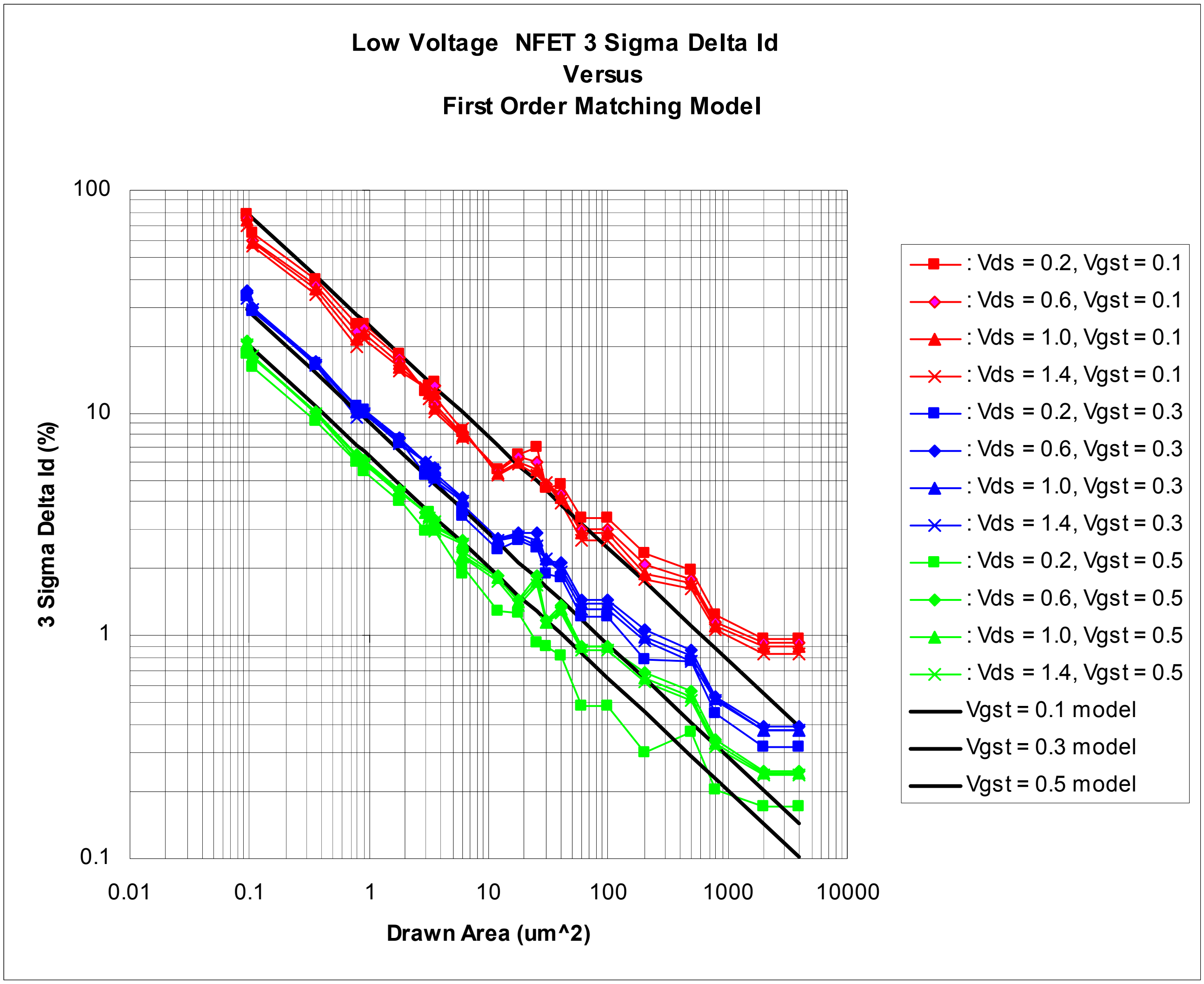
$$\sigma_{\beta\%} = \frac{A_{\beta\%}}{\sqrt{W \cdot L}}$$

$$\sigma_{Vt} = \frac{A_{Vt}}{\sqrt{W \cdot L}}$$

NFET Delta Id Model

The equations used to calculate $\sigma_{\beta\%}$ and σ_{Vt} are intended to model the standard deviation of the model parameters as a function of device size. The fitting constants are determined empirically by optimization of all sizes with effective areas less than 100μm^2.

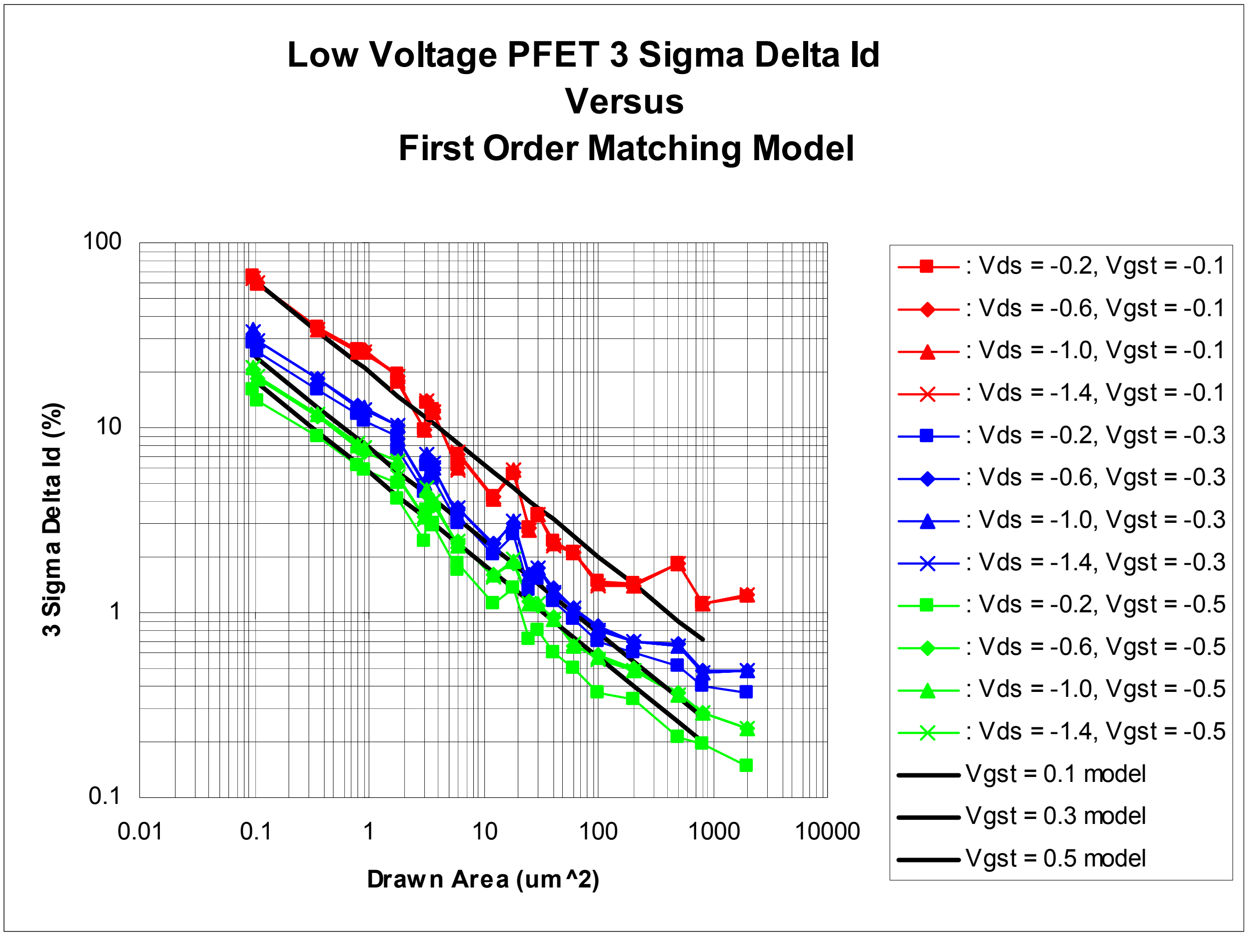
Parameter	Value
$A_{\beta\%}$ (%-μm)	1.40
A_{Vt} (mV-μm)	4.05



PFET Delta Id Model

The equations used to calculate $\sigma_{\beta\%}$ and σ_{Vt} are intended to model the standard deviation of the model parameters as a function of device size. The fitting constants are determined empirically by optimization of all sizes with effective areas less than 100μm^2.

Parameter	Value
$A_{\beta\%}$ (%-μm)	1.39
A_{Vt} (mV-μm)	3.26



Test Structures

This testchip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 3 NFET and 3 PFET modules devoted to FET matching (low and high voltage). The NFET and PFET modules are identical except for the change in polarity between the devices. The following tables summarize the structures available for low voltage FET matching characterization:

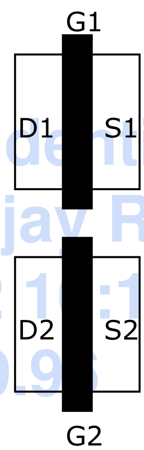
Low Voltage Standard Matched Pairs:

Width\Length	0.16µm	0.18µm	0.3µm	0.6µm	2µm	5µm	10µm
0.6µm	1	1					
2µm		1					
5µm	1	1, 2				1, 20	
10µm		1, 2, 10	1, 10	1, 10			
20µm	1	1	1	1	1, 20	1, 20	1, 20

Note: The values in each box are the number of fingers per FET (total width is number of fingers x width).

Low Voltage Common Centroid Matched Pairs:

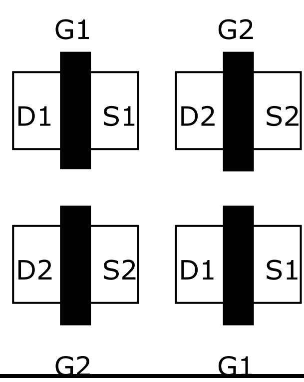
Width\Length	0.18µm	5µm
10µm	2	
20µm		20



Note: The device specification represents the size and configuration for each of the 4 FETs in the common centroid.

Low Voltage Matched Pairs with Various Spacings (140µm, 560µm, and 1260µm spacings):

Width\Length	0.14µm	0.18µm	0.6µm	5µm
10µm	10	10	10	
20µm				20



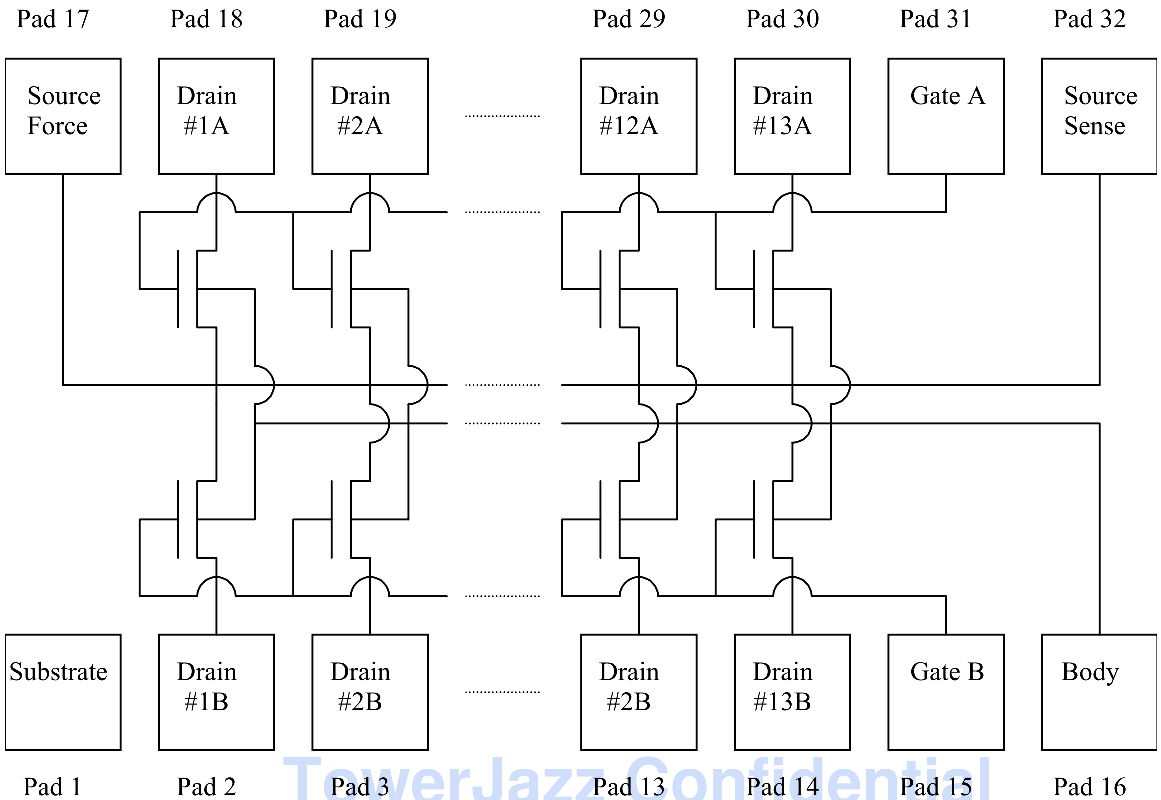


Figure 2: Schematic Diagram of FET Matching Module

The matched pairs are organized into modules as shown in figure 1. All of the transistors in the module share a common source bus, which has both force and sense pads to allow kelvin biasing of the source to maintain a known Vgs. It is important to use a common source pad for both transistors, as the variability in pad resistance will cause corresponding variablities in the effective Vgs for the two transistors if different pads are used. Since Id is a power function of Vgs in the saturation region, it is very sensitive to changes in Vgs. There are two gate buses which allow ΔVgs measurements (these have single pads each, since they should have essentially no current there should not be any concerns regarding pad resistance). There is also a single body tie for all of the transistors, as we want a consistent body voltage for both transistors in the matched pair and the current should be low enough to that pad resistance is not a concern. A single substrate tie is located between pads 1 and 17. Even though the non-kelvin drain pads can cause differences in Vds between the transistors, the transistors are usually biased in saturation for matching measurements, so the Id should be a weak function of Vds (certainly Id should be less sensitive to differences in Vds than in Vgs).

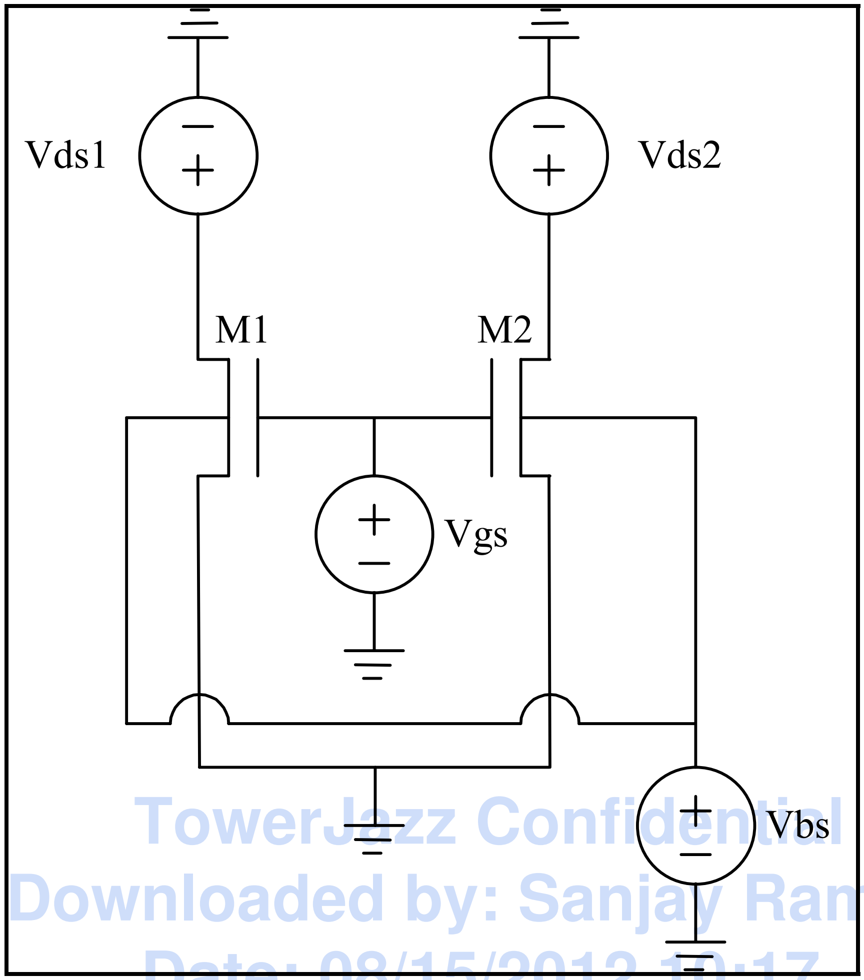


Figure 3: Circuit Configuration for Average Vt and DeltaIdVeff Tests

Test Description

The MOSFET matching test was performed on the "Analog Tester". The analog tester is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. All of the cabling between the HP4156, switch matrix, and probe card is guarded through the use of triaxial cable. The HP4156 is composed of 4 SMUs (Source Measure Units), 2 VSUs (Voltage Source Units), and 2 VMUs (Voltage Source Units). The SMUs are used to simultaneously force voltages and measure currents. They also support kelvin biasing, which allows voltages to be maintained at the DUT (Device Under Test) despite voltage offsets due to series resistance. The measurement resolution of the HP4156 SMUs is approximately 6 digits. All of the test equipment is controlled by a PC using a Visual Basic test program. The test program (WaferTest) is designed to provide a relatively open framework for implementing custom analog tests, and it places the measurement results directly into an Excel spreadsheet. Some of the tests use the term Veff, which stands for the effective gate voltage and is equal to Vgs - Vt (also called Vgst). The following tests were used in this characterization:

Contact - Measures the contact resistance of the probe tips. We have a module on the testchip which is designed specifically to check whether the probes are properly contacting the pads. This module has small metal 1 resistors between the adjacent pads in each row (e.g. pad 1 is connected to pad 17, pad 2 is

connected to pad 18, etc.). The contact test is usually the first test in the test program, and it verifies that the resistance of each pair of pads is less than a set value. If the probe resistance is greater than the set value, the tester stops to allow the probes to be checked.

AverageVt - Measures the Vt of both transistors in a matched pair simultaneously using the maximum transconductance method, and provides the average Vt value for use in subsequent tests. The test setup provides for connection inputs (Drain #1, Gate #1, Drain #2, Gate #2, Source Force, Source Sense, Body, Substrate), bias inputs (Start Vgs, Stop Vgs, Step Vgs, Vds, Vbs, Integration Time), and the ability to save the raw Id data. The setup for this test is described in figure 2. Both of the gate nodes and body nodes are connected to single voltage sources, thus there should not be any offsets between the two devices. The drains are connected to separate SMUs, which can result in Vds and Id offsets. The maximum transconductance method of calculating Vt is implemented in the following steps:

Perform the IdVg measurement on both transistors simultaneously.
Calculate the transconductance of each FET by taking the derivative of a 3 point second order polynomial fit of the IdVg curve.
Find the Vgs points which represent the maximum transconductances.
Perform linear least squares regressions (5 points centered at the point of maximum transconductance) to obtain the Vgs intercepts.
Subtract one-half of the Vds from the Vgs intercepts to obtain the Vts.
Calculate the average Vt.
Pass the average Vt to other tests.

This test also reports the individual Vts, delta Vt, and optionally the raw IdVg data.

DeltaVgsId - Measures both the delta Id and delta Vgs for a transistor pair for a range of Vds and Veff (Vgst or Vgs - Vt). The test setup provides for connection inputs (Drain #1, Gate #1, Drain #2, Gate #2, Source Force, Source Sense, Body, Substrate), bias inputs (Start Veff, Stop Veff, Step Veff, Start Vds, Stop Vds, Step Vds, Vbs), and the ability to save the raw Id data. Delta Id is defined as the percent difference in Id normalized by Id, and is taken from the first part of delta Vgs test.

$$\Delta Id = 100 * \frac{Id_2 - Id_1}{Id_1}$$

The delta Id results represent the error between the currents in a simple current mirror. Delta Vgs is determined by applying the same Veff and Vds to both transistors and then varying the Vgs of one of the transistors until the drain current is equal to the other transistor.

$$\Delta Vgs = Vgs_2 - Vgs_1$$

Delta Vgs represents the input offset voltage for a differential pair, and it is usually reported in milivolts (mV). The setup for this test is described in figure 3. Since the goal of this test is to look for small differences in Vgs between the two transistors, it would be difficult to obtain the required accuracy if the gates were biased independently through two voltage sources. The voltage offset and linearity differences between two voltage supplies would introduce errors, and the requirement of approximately 0.01mV precision cannot be met with our test system. In order to alleviate this problem, we have biased the gates of the transistors at ground level, and applied a -Vgs potential to the common source. The gate of the reference transistor (M1) is tied directly to ground, and the gate of the matched transistor (M2) is tied to a voltage source through a resistor divider. The resistor divider is used to increase the precision of the

voltage source by approximately 100 times. The voltage source is not ideal, and will have an offset voltage (~0.1mV), but the offset is divided down to a small value (~0.001mV) and should only cause a small fixed offset in the mean of the measurement results (we are interested in the 3 Sigma). The linearity of the voltage source is not very critical in this configuration, as we only have to supply the voltage offset magnified by ~100 about 0V rather than the absolute Vgs. The drains are connected to separate SMUs, which supply (Vds – Vgs) to bias the drains at the desired Vds. Since the drains are connected to separate SMUs, there will be offsets in both the Vds and Id between the devices.

The flow chart shown in figure 4 describes the algorithm used to perform the DeltaVgsId test. While the flow chart excludes several practical implementation details, it does represent the general flow which is followed for the test.
Test Conditions

The following test conditions were used for this characterization:

Average Vt

Device	Start Vgs	Stop Vgs	Step Vgs	Vds	Vbs	Integration	Delay	Hold	Save Id Data
NFET	0.4	1.5	0.05	0.1	0	M	0	0	1
PFET	-0.5	-1.6	-0.05	-0.1	0	M	0	0	1

DeltaVgsId

Device	Start Veff	Stop Veff	Step Veff	Start Vds	Stop Vds	Step Vds	Vbs	Save Id Data
NFET	0.1	0.5	0.2	0.2	1.4	0.4	0	1
PFET	-0.1	-0.5	-0.2	-0.2	-1.4	-0.4	0	1

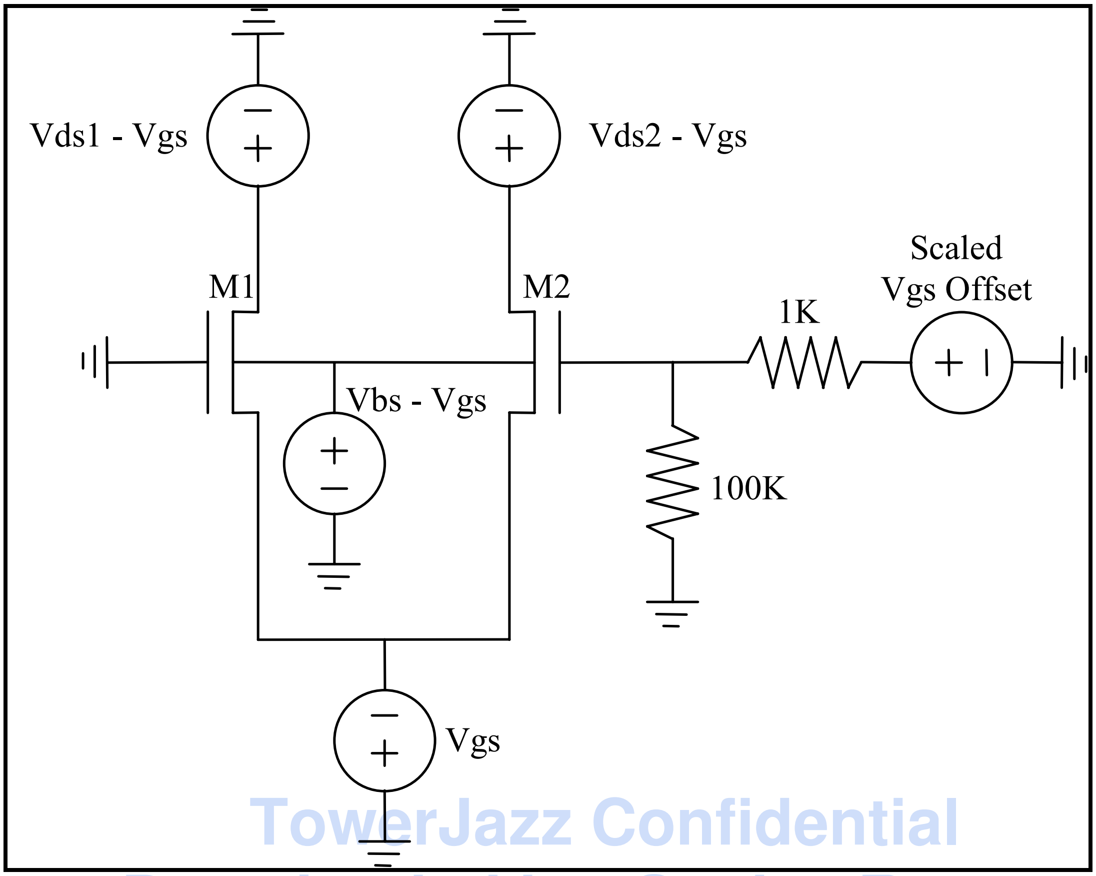


Figure 4: Circuit Configuration for DeltaVgsId Test

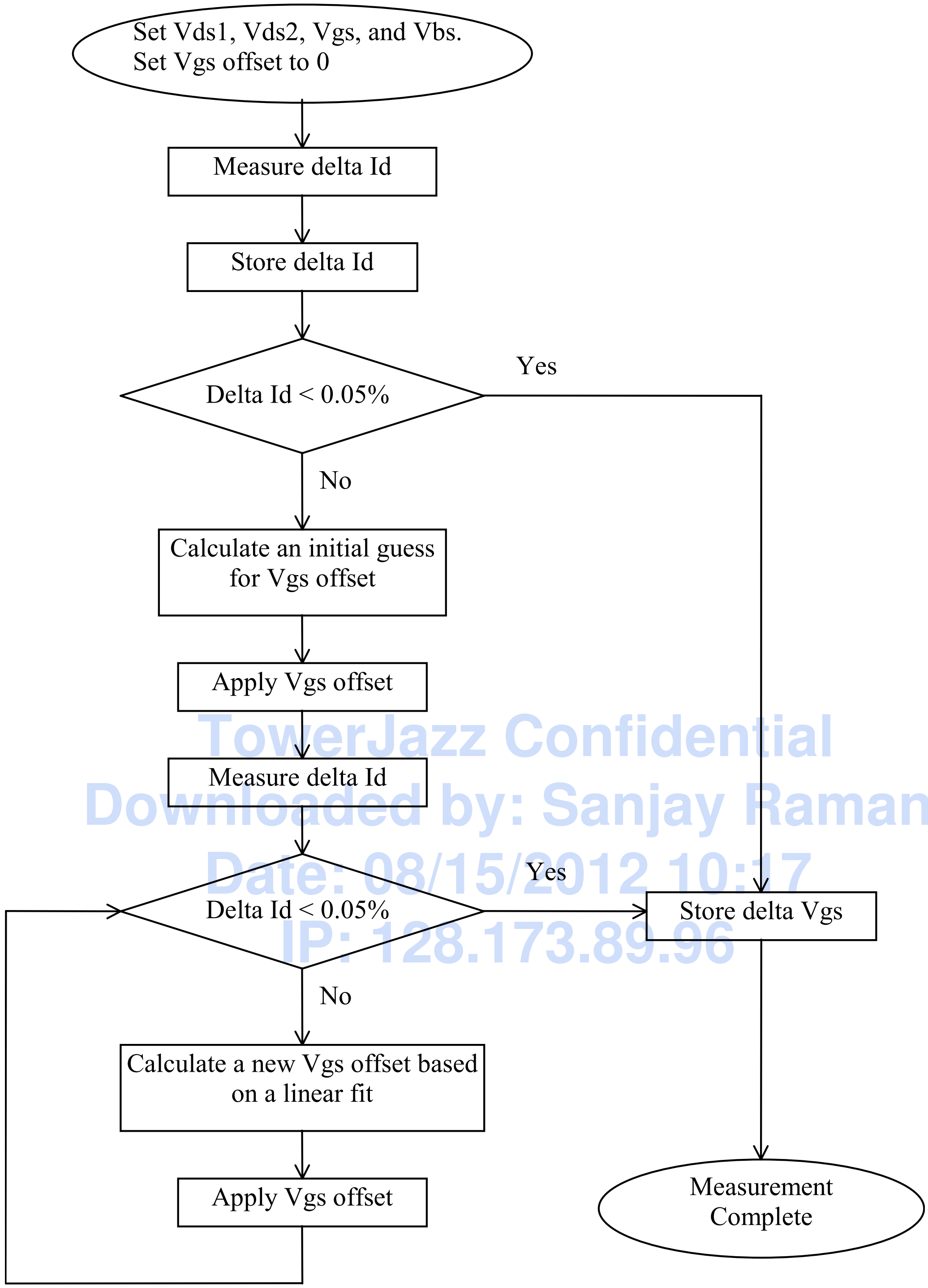


Figure 5: Delta Vgs Test Flowchart

5. NPN Mismatch Characterization

Table of Contents

1. Overview

NPN collector current mismatch and current gain mismatching characterization for SBC18 process has been performed.

SBC18 has six process variants. SBC18HX process offers three flavors of transistors, HS (high speed) NPN, STD (standard) NPN, and HV (high voltage) NPN, using deep trench isolation. SBC18PT, SBC18QTD and SBC18QTR processes offer two flavors of transistors, STD type and HV type, using deep trench isolation. Both SBC18QW and SBC18MW offer STD and HV type NPN, without deep trench isolation. Transistors with and without deep trench have same mismatch characteristics.

The data presented in this report are derived from measurements of four SBC18 lots, lot K19225.1-wafer#11, lot K19920.1-wafer#7 and lot K19863.1-wafer#8 & wafer#13, and lot K20655-wafer#6. All 48 dies of each wafer were tested, which resulted in a reasonable sample size of 240 devices.

For measurements involving a large number of samples, it is almost inevitable that there will be a few "bad points" which are significantly outside the distribution, which represents the rest of the data points. Since the standard deviation can be significantly affected by these "bad points," it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3 sigma limits. The standard deviation is then recalculated for the remaining points, and again, all points outside of the 3-Sigma limits are removed. This process continues until all data points are within the 3-Sigma limits of the distribution.

The three-sigma (3 times the standard deviation) mismatch results are reported in this report. Three types of NPN were characterized: high speed NPN (HS, breakdown voltage of 2.2V), standard NPN (STD, breakdown voltage of 3.5V), and high voltage NPN (HV, breakdown voltage of 6V). Delta Ic and delta Beta matching were both characterized over bias and geometry.

The bias range used for this report is as follows:

Vce	Je
0.6V, 1.0V, 1.4V	0.005mA/μm^2, 0.05mA/μm^2, 0.5mA/μm^2

2. Results:

2.1 Beta mismatching:

Beta mismatch is reported in the form of 3 sigma of Delta Beta, where Delta Beta is defined as the percent difference in Beta normalized by Beta.

2.1.1 Results of Beta mismatch of STD type devices:

Table 1 gives current gain mismatch between two standard type transistors in a pair over emitter size and bias. The two transistors in a pair are roughly 15um apart.

W (um)	L(um)	3 sigma (%diff)	Mean Beta	Vce (v)	Je (mA/um2)
0.2	0.76	52.3	106	0.6	0.005
0.2	2.64	29.5	143	0.6	0.005
0.6	2.64	14.3	201	0.6	0.005
0.2	10.16	20.2	140	0.6	0.005
0.9	10.16	9.7	190	0.6	0.005
0.2	0.76	52.4	107	1	0.005
0.2	2.64	28.4	143	1	0.005
0.6	2.64	13.8	202	1	0.005
0.2	10.16	20.2	139	1	0.005
0.9	10.16	9.6	191	1	0.005
0.2	0.76	52.3	107	1.4	0.005
0.2	2.64	28.5	143	1.4	0.005
0.6	2.64	13.8	202	1.4	0.005
0.2	10.16	20.3	140	1.4	0.005
0.9	10.16	9.5	191	1.4	0.005
0.2	0.76	31.5	102	0.6	0.05
0.2	2.64	15.9	137	0.6	0.05
0.6	2.64	7.6	191	0.6	0.05
0.2	10.16	7.8	135	0.6	0.05
0.9	10.16	3.2	181	0.6	0.05
0.2	0.76	31.5	102	1	0.05
0.2	2.64	16.0	137	1	0.05
0.6	2.64	7.5	192	1	0.05
0.2	10.16	7.8	135	1	0.05
0.9	10.16	3.2	181	1	0.05
0.2	0.76	31.6	102	1.4	0.05
0.2	2.64	15.8	137	1.4	0.05
0.6	2.64	7.5	192	1.4	0.05
0.2	10.16	7.8	135	1.4	0.05
0.9	10.16	3.2	181	1.4	0.05
0.2	0.76	23.6	89	0.6	0.5
0.2	2.64	12.3	121	0.6	0.5
0.6	2.64	6.1	167	0.6	0.5
0.2	10.16	6.3	118	0.6	0.5
0.9	10.16	2.4	155	0.6	0.5
0.2	0.76	23.6	89	1	0.5
0.2	2.64	12.3	121	1	0.5
0.6	2.64	6.1	167	1	0.5
0.2	10.16	6.3	118	1	0.5
0.9	10.16	2.4	154	1	0.5
0.2	0.76	23.6	89	1.4	0.5
0.2	2.64	12.3	121	1.4	0.5
0.6	2.64	6.0	166	1.4	0.5
0.2	10.16	6.3	118	1.4	0.5
0.9	10.16	2.4	153	1.4	0.5

Table 1. 3 sigma Beta mismatch results (in %) of STD type devices

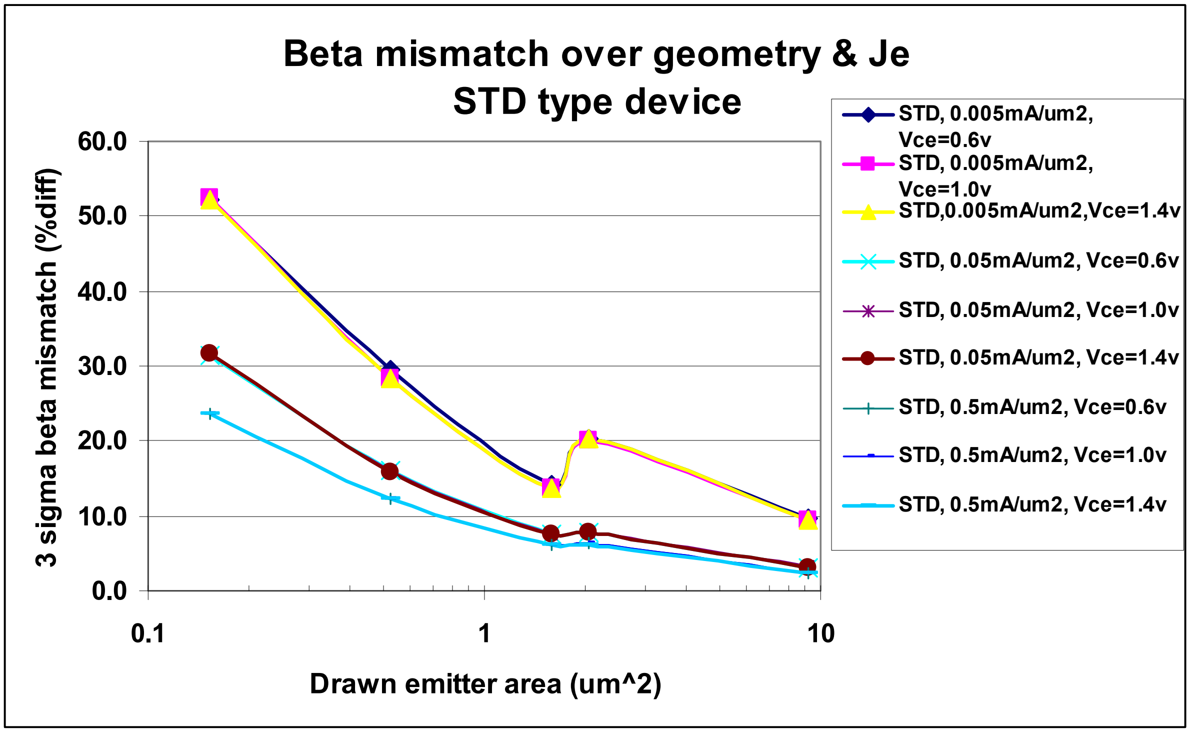


Figure 1. STD type device Beta mismatch over emitter size, Jc, and Vce bias

Beta mismatch is very sensitive to emitter size when drawn emitter area is less than 2um^2. Device operating at lower current density has higher Beta mismatch. The Delta Beta plot below shows the beta mismatch of STD type devices vs. drawn emitter area over Jc and Vce. Vce has no influence on beta mismatch.

2.1.2 Results of Beta mismatch of HV type devices:

Table 2 gives current gain mismatch between two high voltage type transistors in a pair over emitter size and bias. The two transistors in a pair are roughly 15um apart.

W (um)	L(um)	3 sigma (%diff)	Mean Beta	Vce (v)	Je (mA/um2)
0.2	0.76	40.9	105	0.6	0.005
0.2	2.64	27.6	140	0.6	0.005
0.6	2.64	15.4	198	0.6	0.005
0.2	10.16	19.2	139	0.6	0.005
0.9	10.16	9.4	189	0.6	0.005
0.2	0.76	40.9	105	1	0.005
0.2	2.64	27.7	140	1	0.005
0.6	2.64	15.4	199	1	0.005
0.2	10.16	19.2	139	1	0.005
0.9	10.16	9.4	190	1	0.005
0.2	0.76	40.9	105	1.4	0.005
0.2	2.64	27.7	140	1.4	0.005
0.6	2.64	15.3	199	1.4	0.005
0.2	10.16	19.2	139	1.4	0.005
0.9	10.16	9.3	190	1.4	0.005
0.2	0.76	26.2	100	0.6	0.05
0.2	2.64	14.5	138	0.6	0.05
0.6	2.64	6.8	190	0.6	0.05
0.2	10.16	8.6	135	0.6	0.05
0.9	10.16	3.4	180	0.6	0.05
0.2	0.76	26.2	100	1	0.05
0.2	2.64	14.6	138	1	0.05
0.6	2.64	7.1	191	1	0.05
0.2	10.16	8.6	135	1	0.05
0.9	10.16	3.4	180	1	0.05
0.2	0.76	26.2	100	1.4	0.05
0.2	2.64	14.6	139	1.4	0.05
0.6	2.64	6.8	191	1.4	0.05
0.2	10.16	8.6	136	1.4	0.05
0.9	10.16	3.3	180	1.4	0.05
0.2	0.76	23.4	84	0.6	0.5
0.2	2.64	11.8	115	0.6	0.5
0.6	2.64	5.7	140	0.6	0.5
0.2	10.16	7.1	112	0.6	0.5
0.9	10.16	3.0	120	0.6	0.5
0.2	0.76	24.2	87	1	0.5
0.2	2.64	12.4	120	1	0.5
0.6	2.64	5.8	157	1	0.5
0.2	10.16	6.9	116	1	0.5
0.9	10.16	2.9	139	1	0.5
0.2	0.76	24.3	88	1.4	0.5
0.2	2.64	12.5	121	1.4	0.5
0.6	2.64	5.7	163	1.4	0.5
0.2	10.16	6.9	117	1.4	0.5
0.9	10.16	2.9	148	1.4	0.5

Table 2. 3 sigma Beta mismatch results (in %) of HV type devices.

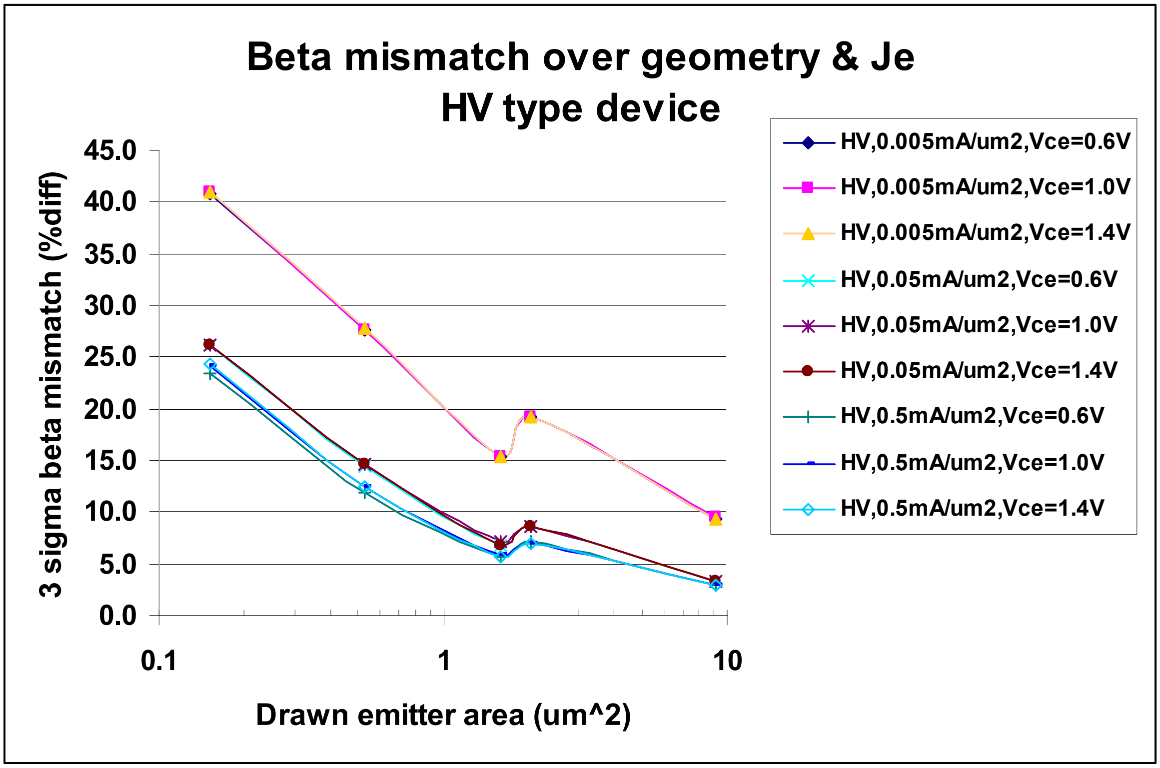


Figure 2. HV device Beta mismatch over emitter size, Jc , and Vce bias

Beta mismatch is very sensitive to emitter size when drawn emitter area is less than 2um^2. Device operating at lower current density has higher Beta mismatch. The Delta Beta plot below shows the beta mismatch of HV type devices vs. drawn emitter area over Jc and Vce. Vce has no influence on beta mismatch.

2.1.3 Results of Beta mismatch of HS type devices:

Table 3 gives current gain mismatch between two high-speed type transistors in a pair over emitter size and bias. The two transistors in a pair are roughly 15um apart.

W (um)	L(um)	3 sigma (%diff)	Mean Beta	Vce (v)	Je (mA/um2)
0.2	0.76	31.5	134	0.6	0.005
0.2	2.64	24.1	176	0.6	0.005
0.6	2.64	19.0	198	0.6	0.005
0.2	10.16	17.0	172	0.6	0.005
0.9	10.16	10.4	199	0.6	0.005
0.2	0.76	31.6	135	1	0.005
0.2	2.64	24.3	176	1	0.005
0.6	2.64	19.8	199	1	0.005
0.2	10.16	17.4	173	1	0.005
0.9	10.16	10.6	200	1	0.005
0.2	0.76	32.4	137	1.4	0.005
0.2	2.64	24.7	180	1.4	0.005
0.6	2.64	19.3	203	1.4	0.005
0.2	10.16	17.4	177	1.4	0.005
0.9	10.16	10.6	202	1.4	0.005
0.2	0.76	18.7	126	0.6	0.05
0.2	2.64	13.2	126	0.6	0.05
0.6	2.64	8.0	170	0.6	0.05
0.2	10.16	6.7	189	0.6	0.05
0.9	10.16	3.7	199	0.6	0.05
0.2	0.76	18.8	127	1	0.05
0.2	2.64	13.1	170	1	0.05
0.6	2.64	8.1	190	1	0.05
0.2	10.16	6.8	166	1	0.05
0.9	10.16	3.7	188	1	0.05
0.2	0.76	19.0	128	1.4	0.05
0.2	2.64	13.2	172	1.4	0.05
0.6	2.64	8.1	192	1.4	0.05
0.2	10.16	6.9	168	1.4	0.05
0.9	10.16	3.7	190	1.4	0.05
0.2	0.76	16.9	112	0.6	0.5
0.2	2.64	9.9	149	0.6	0.5
0.6	2.64	5.3	166	0.6	0.5
0.2	10.16	4.9	145	0.6	0.5
0.9	10.16	2.8	160	0.6	0.5
0.2	0.76	16.9	112	1	0.5
0.2	2.64	9.9	149	1	0.5
0.6	2.64	5.4	165	1	0.5
0.2	10.16	4.9	145	1	0.5
0.9	10.16	2.8	160	1	0.5
0.2	0.76	17.0	113	1.4	0.5
0.2	2.64	10.0	150	1.4	0.5
0.6	2.64	5.4	166	1.4	0.5
0.2	10.16	4.9	145	1.4	0.5
0.9	10.16	2.8	159	1.4	0.5

Table 3. 3 sigma Beta mismatch results (in %) of HS type devices.

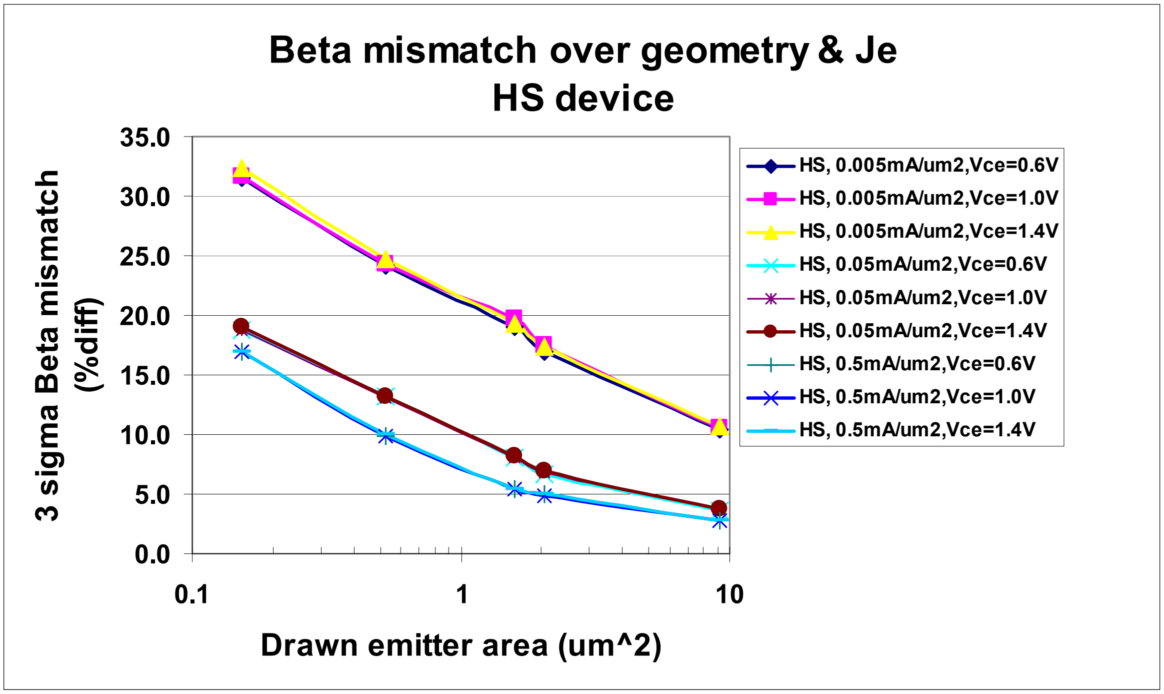


Figure 3. HS device Beta mismatch over emitter size, Jc , and Vce bias

Beta mismatch is very sensitive to emitter size when drawn emitter area. Device operating at lower current density has higher Beta mismatch. The Delta Beta plot below shows the beta mismatch of HS type devices vs. drawn emitter area over Jc and Vce. Vce has no influence on beta mismatch.

2.2 Results of Ic Mismatch:

Ic mismatch is reported in the form of 3 sigma of Delta Ic, where Delta Ic is defined as the percent difference in Ic normalized by Ic.

$$\Delta Ic = 100 * \frac{Ic_2 - Ic_1}{Ic_1}$$

<u>2.2.1 Ic mismatching result of STD type device:</u>
Table 4 gives Ic mismatch between two standard type transistors in a pair over emitter size and bias. The two transistors in a pair are roughly 15um apart.

W (um)	L(um)	3 sigma (%diff)	Vce (v)	Je (mA/um2)
0.2	0.76	13.2	0.6	0.005
0.2	2.64	7.1	0.6	0.005
0.6	2.64	5.2	0.6	0.005
0.2	10.16	4.2	0.6	0.005
0.6	10.16	3.0	0.6	0.005
0.2	0.76	13.3	1	0.005
0.2	2.64	7.1	1	0.005
0.6	2.64	5.3	1	0.005
0.2	10.16	4.2	1	0.005
0.6	10.16	3.1	1	0.005
0.2	0.76	13.4	1.4	0.005
0.2	2.64	7.2	1.4	0.005
0.6	2.64	5.3	1.4	0.005
0.2	10.16	4.2	1.4	0.005
0.6	10.16	3.1	1.4	0.005
0.2	0.76	12.5	0.6	0.05
0.2	2.64	6.7	0.6	0.05
0.6	2.64	4.8	0.6	0.05
0.2	10.16	4.0	0.6	0.05
0.6	10.16	2.9	0.6	0.05
0.2	0.76	12.5	1	0.05
0.2	2.64	6.8	1	0.05
0.6	2.64	4.9	1	0.05
0.2	10.16	4.0	1	0.05
0.6	10.16	2.9	1	0.05
0.2	0.76	12.6	1.4	0.05
0.2	2.64	6.8	1.4	0.05
0.6	2.64	4.9	1.4	0.05
0.2	10.16	4.0	1.4	0.05
0.6	10.16	2.9	1.4	0.05
0.2	0.76	11.7	0.6	0.5
0.2	2.64	6.0	0.6	0.5
0.6	2.64	4.4	0.6	0.5
0.2	10.16	3.7	0.6	0.5
0.6	10.16	2.6	0.6	0.5
0.2	0.76	11.8	1	0.5
0.2	2.64	6.1	1	0.5
0.6	2.64	4.6	1	0.5
0.2	10.16	3.8	1	0.5
0.6	10.16	2.8	1	0.5
0.2	0.76	11.9	1.4	0.5
0.2	2.64	6.2	1.4	0.5
0.6	2.64	4.8	1.4	0.5
0.2	10.16	3.9	1.4	0.5
0.6	10.16	2.9	1.4	0.5

Table 4. 3 sigma Ic mismatch results (in %) of STD type devices.

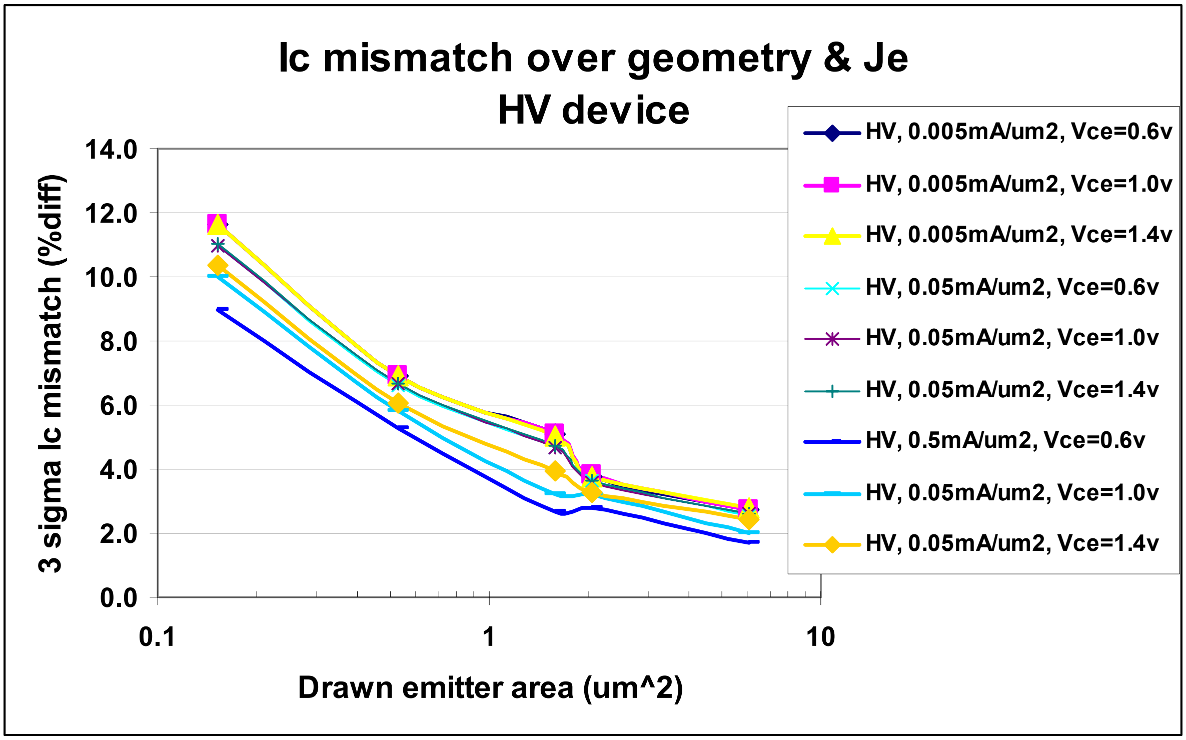


Figure 4. STD type device Ic mismatch over emitter size, Jc, and Vce bias

Ic mismatch is very sensitive to emitter size when drawn emitter area is less than 2um^2. Current density has small influence on Ic mismatch. The Delta Ic plot below shows the Ic mismatch of STD type devices vs. drawn emitter area over Jc and Vce. Vce has no influence on Ic mismatch.

2.2.2 Results of Ic mismatch of HV type devices:

Table 5 gives Ic mismatch between two high voltage type transistors in a pair over emitter size and bias. The two transistors in a pair are roughly 15um apart.

W (um)	L(um)	3 sigma (%diff)	Vce (v)	Je (mA/um2)
0.2	0.76	11.6	0.6	0.005
0.2	2.64	6.9	0.6	0.005
0.6	2.64	5.1	0.6	0.005
0.2	10.16	3.8	0.6	0.005
0.6	10.16	2.7	0.6	0.005
0.2	0.76	11.6	1	0.005
0.2	2.64	6.9	1	0.005
0.6	2.64	5.1	1	0.005
0.2	10.16	3.8	1	0.005
0.6	10.16	2.7	1	0.005
0.2	0.76	11.7	1.4	0.005
0.2	2.64	6.9	1.4	0.005
0.6	2.64	5.0	1.4	0.005
0.2	10.16	3.7	1.4	0.005
0.6	10.16	2.8	1.4	0.005
0.2	0.76	11.0	0.6	0.05
0.2	2.64	6.6	0.6	0.05
0.6	2.64	4.6	0.6	0.05
0.2	10.16	3.6	0.6	0.05
0.6	10.16	2.6	0.6	0.05
0.2	0.76	11.0	1	0.05
0.2	2.64	6.6	1	0.05
0.6	2.64	4.7	1	0.05
0.2	10.16	3.6	1	0.05
0.6	10.16	2.6	1	0.05
0.2	0.76	11.0	1.4	0.05
0.2	2.64	6.7	1.4	0.05
0.6	2.64	4.7	1.4	0.05
0.2	10.16	3.6	1.4	0.05
0.6	10.16	2.6	1.4	0.05
0.2	0.76	9.0	0.6	0.5
0.2	2.64	5.3	0.6	0.5
0.6	2.64	2.7	0.6	0.5
0.2	10.16	2.8	0.6	0.5
0.6	10.16	1.7	0.6	0.5
0.2	0.76	10.0	1	0.5
0.2	2.64	5.8	1	0.5
0.6	2.64	3.2	1	0.5
0.2	10.16	3.2	1	0.5
0.6	10.16	2.0	1	0.5
0.2	0.76	10.4	1.4	0.5
0.2	2.64	6.0	1.4	0.5
0.6	2.64	3.9	1.4	0.5
0.2	10.16	3.3	1.4	0.5
0.6	10.16	2.4	1.4	0.5

Table 5. 3 sigma Ic mismatch results (in %) of HV type devices.

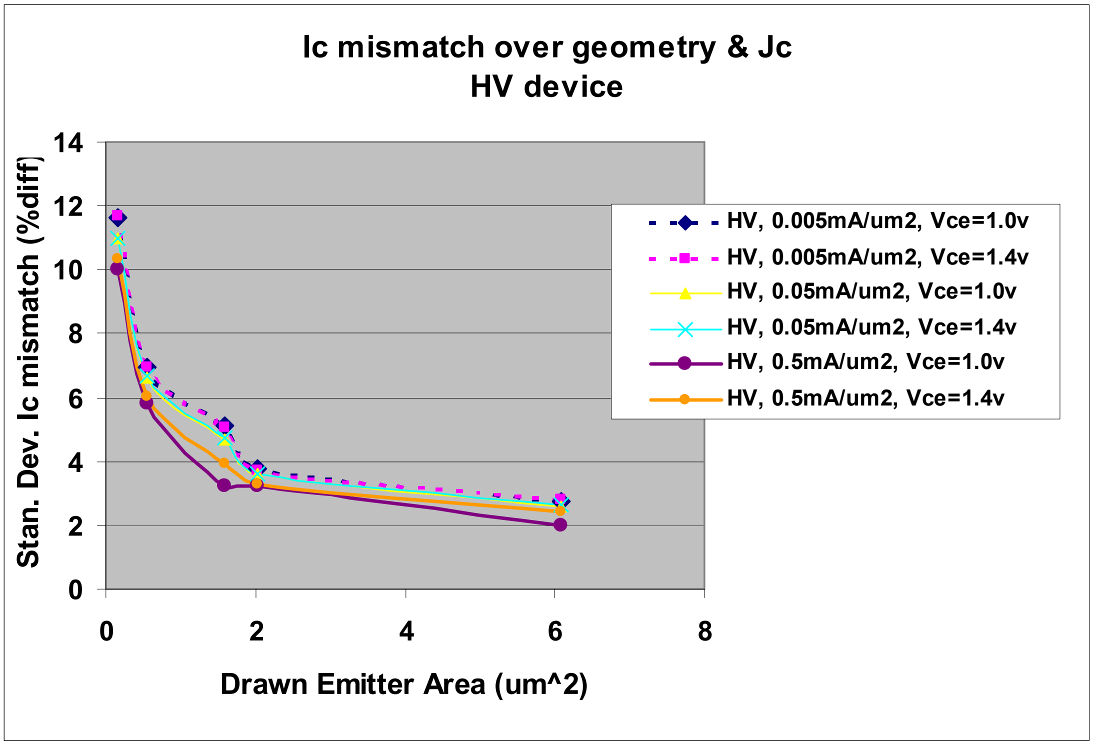


Figure 5. HV device Ic mismatch over emitter size, Jc , and Vce bias

Ic mismatch of HV type devices are very sensitive to emitter size when drawn emitter area is less than 2um^2. Device operating at lower current density has smaller Beta mismatch. The Delta Ic plot below shows the beta mismatch of HV type devices vs. drawn emitter area over Jc and Vce.

<u>2.2.3 Results of Ic mismatch of HS type devices:</u>

Table 6 gives Ic mismatch between two hig-speed type transistors in a pair over emitter size and bias. The two transistors in a pair are roughly 15um apart.

W (um)	L(um)	3 sigma (%diff)	Vce (v)	Je (mA/um2)
0.2	0.76	11.8	0.6	0.005
0.2	2.64	7.3	0.6	0.005
0.6	2.64	4.8	0.6	0.005
0.6	10.16	2.2	0.6	0.005
0.2	0.76	11.9	1	0.005
0.2	2.64	7.3	1	0.005
0.6	2.64	5.0	1	0.005
0.6	10.16	2.3	1	0.005
0.2	0.76	12.0	1.4	0.005
0.2	2.64	7.4	1.4	0.005
0.6	2.64	5.1	1.4	0.005
0.6	10.16	2.7	1.4	0.005
0.2	0.76	11.0	0.6	0.05
0.2	2.64	6.8	0.6	0.05
0.6	2.64	4.2	0.6	0.05
0.6	10.16	2.1	0.6	0.05
0.2	0.76	11.0	1	0.05
0.2	2.64	6.9	1	0.05
0.6	2.64	4.4	1	0.05
0.6	10.16	2.1	1	0.05
0.2	0.76	11.1	1.4	0.05
0.2	2.64	6.9	1.4	0.05
0.6	2.64	4.5	1.4	0.05
0.6	10.16	2.2	1.4	0.05
0.2	0.76	11.1	0.6	0.5
0.2	2.64	6.3	0.6	0.5
0.6	2.64	4.0	0.6	0.5
0.6	10.16	1.8	0.6	0.5
0.2	0.76	11.2	1	0.5
0.2	2.64	6.4	1	0.5
0.6	2.64	4.2	1	0.5
0.6	10.16	1.9	1	0.5
0.2	0.76	11.3	1.4	0.5
0.2	2.64	6.6	1.4	0.5
0.6	2.64	4.5	1.4	0.5
0.6	10.16	2.0	1.4	0.5

Table 6. 3 sigma Ic mismatch results (in %) of HS type devices.

Ic mismatch of HS type devices are very sensitive to emitter size when drawn emitter. Device operating at lower current density has smaller Beta mismatch. The Delta Ic plot below shows the beta mismatch of HS type devices vs. drawn emitter area over Jc and Vce.

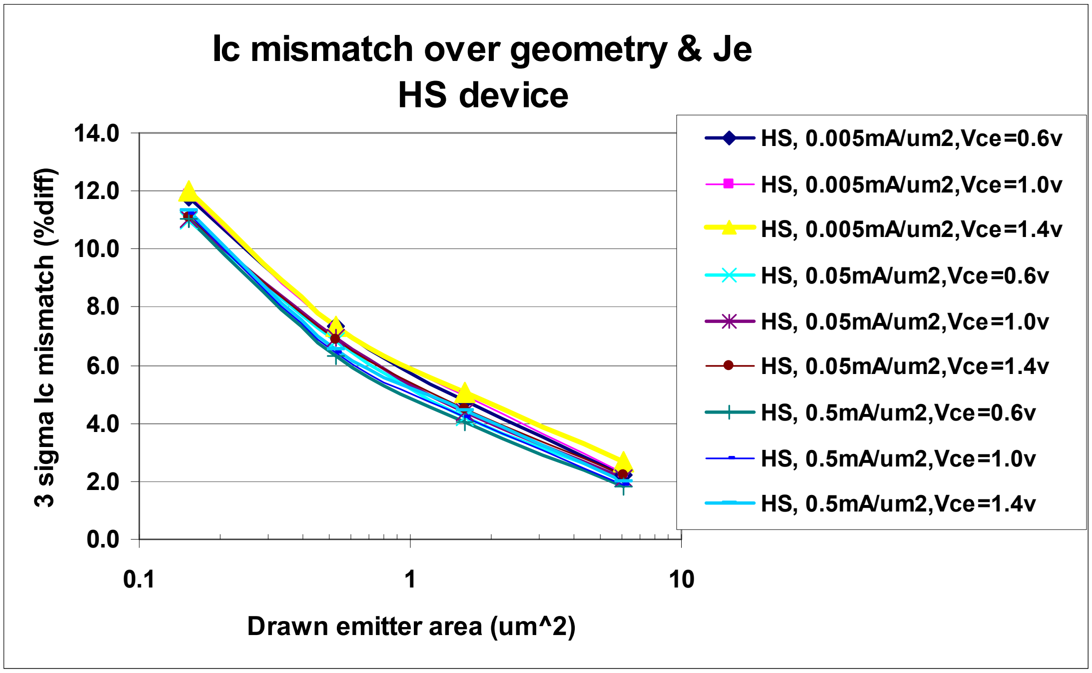


Figure 6. HS device Ic mismatch over emitter size, Jc , and Vce bias

NPN collector current matching and Beta matching results from SBC18 process lots have been reported. Both Ic and Beta mismatching decrease while emitter area increases for all three types of NPN and in the bias range characterized. Current density has some effect on Beta mismatch, with devices operating at lower current region having slightly higher mismatch. Current density does not have influence on Ic mismatch. Vce has no influence on mismatch.

6. Lateral PNP Mismatch Characterization

Table of Contents

1. Overview

Lateral PNP collector current mismatch and current gain mismatching characterization for SBC18 process have been performed for process qualification purpose. All sbc18 process variants offer the LPNP device.

Data presented in this report is derived from measurements of total of five wafers from three SBC18 lots, lot K20655- wafer#6 and wafer #10, lot K19863.1-wafer#8 and wafer # 13, and lot K19920.1-wafer#10. All 48 dies of each wafer were tested, which resulted in a reasonable sample size of 240 devices.

The three-sigma (3 times the standard deviation) mismatch results are reported in this report.

Two sizes of PNP device were available for characterization. One is a 2x32 array of unit PNPs, the other is a 2x4 array of unit PNPs. Delta_Ic and Delta_Beta matching were both characterized over Ie and Vce biase. Mismatch was characterized over three orders of Ie. For each Ie range, four different Vce biases were used. They are –0.5V, -1.0V, -1.5V, and –2.0V.

2. Results:

2.1 Beta mismatching:

For the Beta mismatch measurement, the goal is to measure the difference in Beta for the two devices in a pair with the same Ie and Vce.

Beta mismatch is reported in the form of 3 sigma of Delta Beta, where Delta Beta is defined as the percent difference in Beta normalized by Beta.

The delta Beta results represent the error between the Betas in simple current mirror.

Array size:	Vce=-.5	Vce=-1	Vce=-1.5	Vce=-2	Je (uA/ per unit)
2x32	0.74	0.70	0.72	0.75	Jc=-.1
2x4	1.49	1.48	1.52	1.53	Jc=-.1
2x32	0.60	0.63	0.65	0.68	Jc=-1.0
2x4	1.04	1.11	1.16	1.19	Jc=-1.0
2x32	0.95	1.12	1.23	1.38	Jc=-10.0
2x4	1.27	1.31	1.33	1.35	Jc=-10.0

Table 1 gives current gain mismatch between two identical PNPs in a pair.

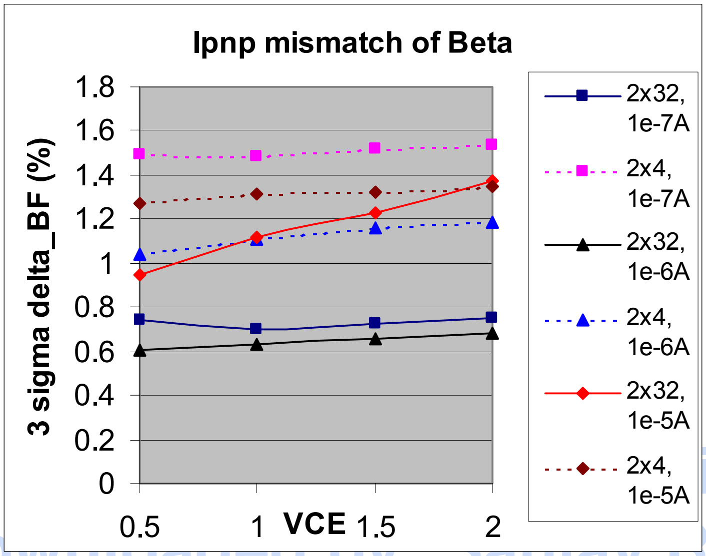


Figure 1. Beta mismatch over Vce. Device array size, and Je are also parameters.

Beta mismatch is sensitive to device size. It also depends on the current range. But Vce has little influence on Beta mismatch. Figure 1 and Figure 2 show the Beta mismatch over current and Vce bias.

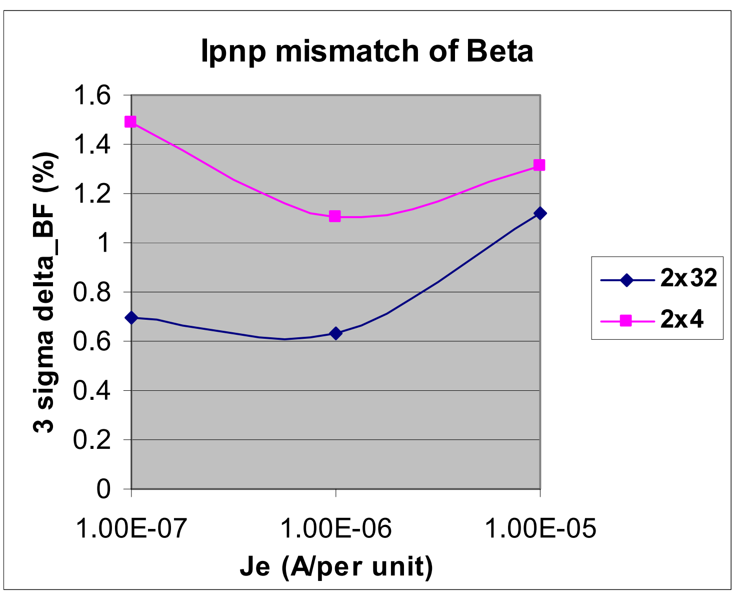


Figure 2. Beta mismatch over current (Vec=1.0V)

2.2 Results of Ic Mismatch:

Ic mismatch is reported in the form of 3 sigma of Delta Ic, where Delta Ic is defined as the percent difference in Ic normalized by Ic.

$$\Delta Ic = 100 * \frac{Ic_2 - Ic_1}{Ic_1}$$

Delta Ic result represents the error between the currents in a simple current mirror.

Array size:	Vce=-.5	Vce=-1	Vce=-1.5	Vce=-2	Je (uA/ per unit)
2x32	0.97	1.02	0.99	1.03	Jc=-.1
2x4	1.25	1.29	1.33	1.37	Jc=-.1
2x32	2.13	2.15	2.18	2.25	Jc=-1.0
2x4	4.36	4.38	4.39	4.40	Jc=-1.0
2x32	5.97	5.98	5.99	6.00	Jc=-10.0
2x4	11.58	11.58	11.59	11.58	Jc=-10.0

Table 2 gives Ic mismatch PNPs in a pair.

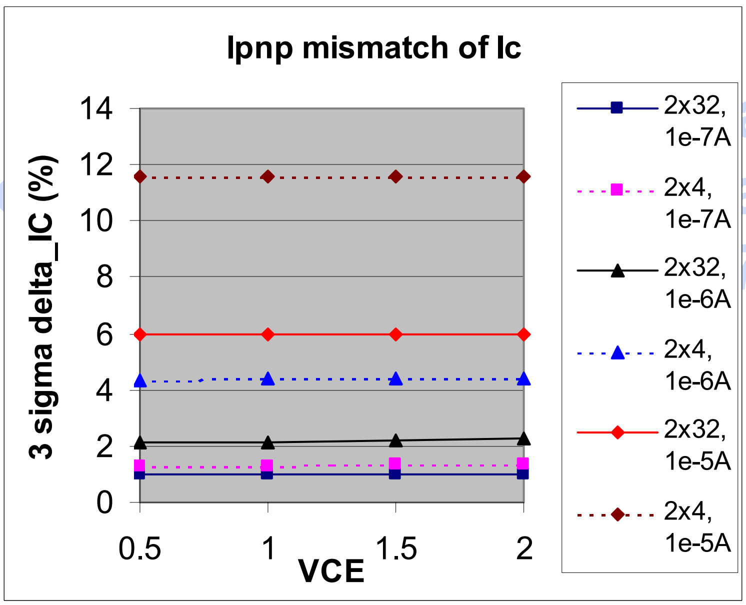


Figure 3. PNP mismatch over Vce bias. Current and device array size are also parameters.

Device of smaller size in general has larger Ic mismatch. Current also effects Ic mismatch, but Vce bias does not influence Ic mismath . Figure 3 and Figure 4 show the IS mismatch over devices sieze, current , and Vce bias.

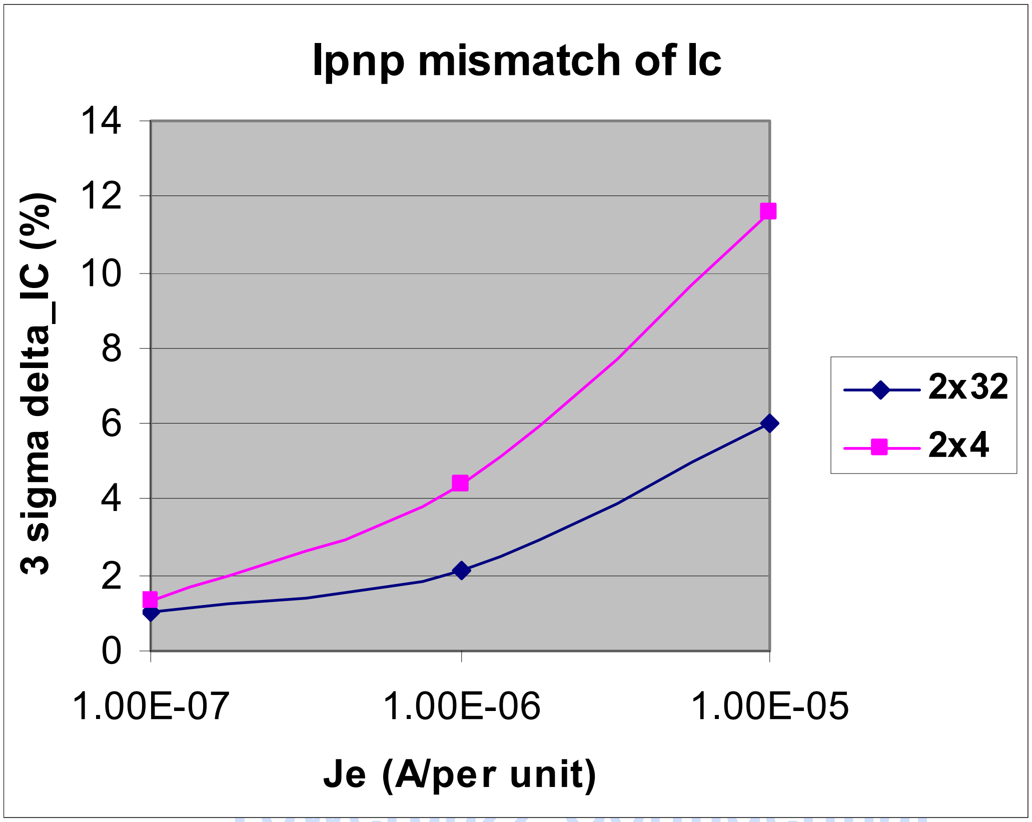


Figure 4. Ic mismatch over current (Vec=1.0V).

Lateral PNP current matching and Beta matching results from SBC18 process lots have been reported. Both Ic and Beta mismatching decrease while device size increases in the bias range characterized. Vec bias has no influence on both Ic mismatch and Beta mismatch. Ic mismatch increase with increased current, while beta mismatch is lowest when Je is around 1uA/per unit PNP.

7. High Value Unsilicided Poly Resistor Characterization

Table of Contents

Summary

A characterization of the high value resistors in the SBC18 process has been performed. The results for the following tests are presented: resistance, resistor matching, TCR (Temperature Coefficient of Resistance) and VCR (Voltage Coefficient of Resistance). The test structures, test procedures, and test conditions are described in the appendix. Although the characterization was carried out on SBC18QTD GA577 test chip, it is applicable to high value resistors for SBC18PT, QTD, QTR, QW, and MW process.

1. Measurement Results

The characterization was performed on wafers processed in the SBC18 process using the GA577 engineering test chip. For resistance, matching and TCR measurement, 24 dies from wafers from following five lots were tested: K17133 wf.16 to 22, K17157 wf20 to 25 K19225 wf.16 to 20, K19863 wf16 to 20 and K19220wf16,18,19,21,22. Since the goal of this characterization is to measure the standard deviation of the difference between two devices, a relatively large sample size is tested to obtain useful results.

For measurements involving a large number of samples, it is almost inevitable that there will be a few "bad points" which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these "bad points," it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3sigma limits.

1.1. HV Resistance and Resistor Matching

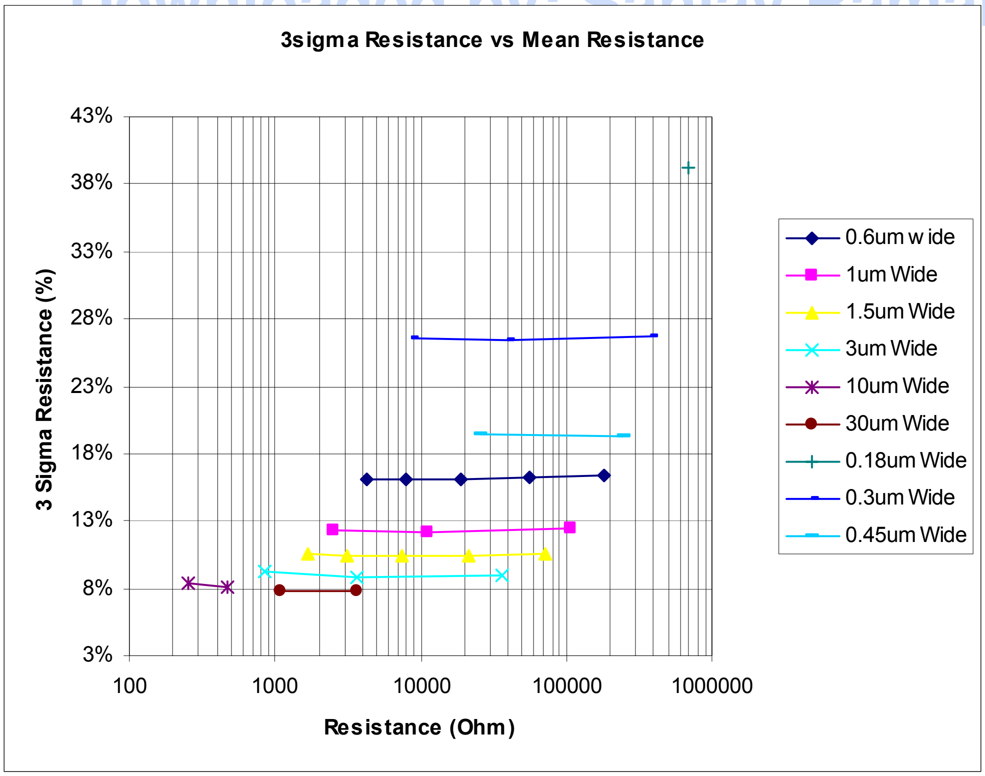
1.1.1. HV Resistor 3 Sigma Resistance

The following tables list both the mean and 3 sigma of the measured resistance for each test structure:

3 Sigma Resistance (%) = 100 * 3 Sigma Resistance / Mean Resistance

HV Resistors: 3 Sigma Resistance (%) / Mean Resistance (Ohms)

3 Sigma (%) / Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide					39.2% / 695,776
0.3um Wide	26.6% / 8,636		26.4% / 39,193		26.7% / 380,990
0.45um Wide			19.5% / 25,817		19.4% / 249,321
0.6um wide	16.1% / 4,244	16.0% / 7,885	16.1% / 18,782	16.2% / 55,318	16.5% / 184,135
1um Wide	12.3% / 2,502		12.2% / 11,070		12.4% / 108,355
1.5um Wide	10.6% / 1,668	10.5% / 3,088	10.4% / 7,355	10.4% / 21,579	10.6% / 71,758
3um Wide	9.3% / 841		8.9% / 3,682		8.9% / 35,764
10um Wide	8.4% / 257	8.1% / 473			
30um Wide				7.8% / 1,096	7.8% / 3,646

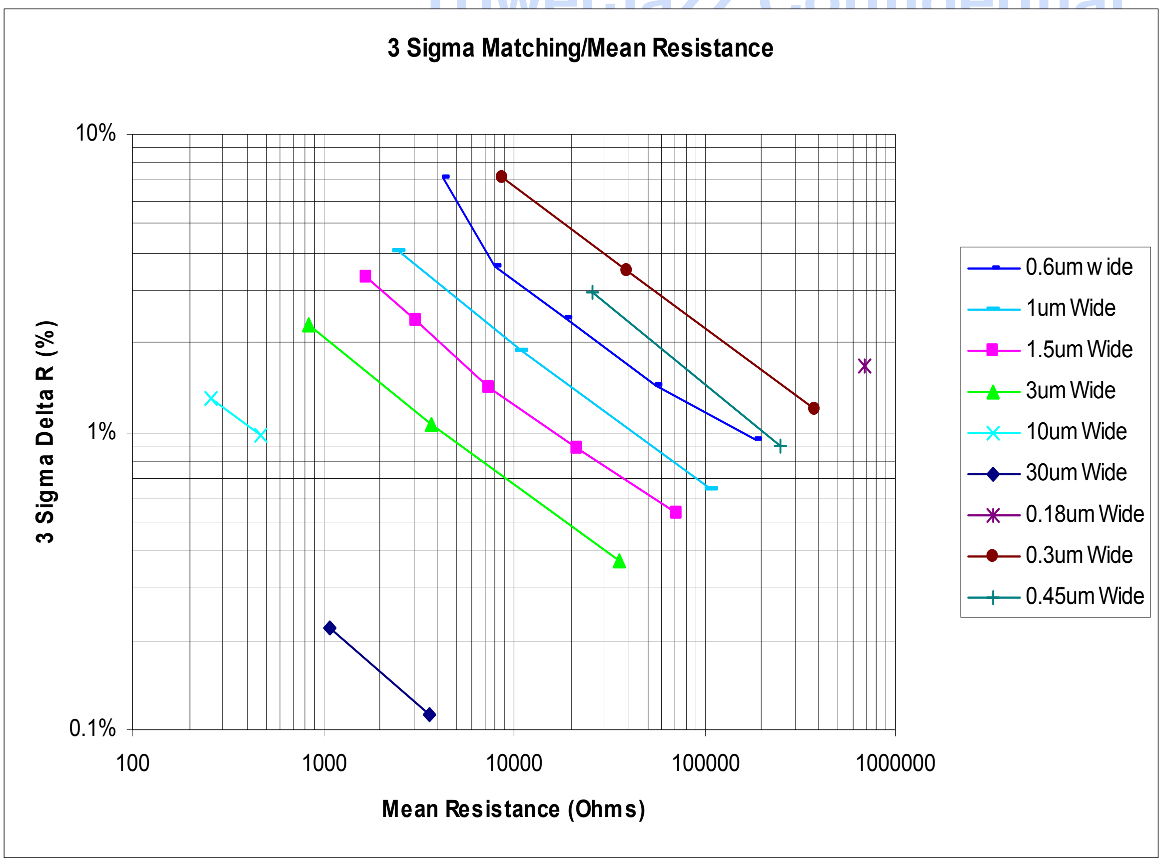


HV Resistor 3 Sigma Matching of Resistor Pairs

The following tables list the 3 sigma matching of resistance for each resistor pair:

HV Matched Resistors: 3 Sigma Matching (%) / Mean Resistance (Ohms)

Measured 3 Sigma Matching					
Width	2	4	10	30	100
0.18um Wide					1.7% / 695,776
0.3um Wide	7.2% / 8,636		3.5% / 39,193		1.2% / 380,990
0.45um Wide			2.9% / 25,817		0.9% / 249,321
0.6um wide	5.3% / 4,244	3.6% / 7,885	2.4% / 18,782	1.4% / 55,318	0.9% / 184,135
1um Wide	4.0% / 2,502		1.9% / 11,070		0.6% / 108,355
1.5um Wide	3.3% / 1,668	2.4% / 3,088	1.4% / 7,355	0.9% / 21,579	0.5% / 71,758
3um Wide	2.3% / 841		1.1% / 3,682		0.4% / 35,764
10um Wide	1.3% / 257	1.0% / 473			
30um Wide				0.2% / 1,096	0.1% / 3,646



1.2. HV Resistor Temperature Coefficient

The HV Resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 25°C and 125°C. The following table lists both the mean and 3 sigma of the measured TCR:

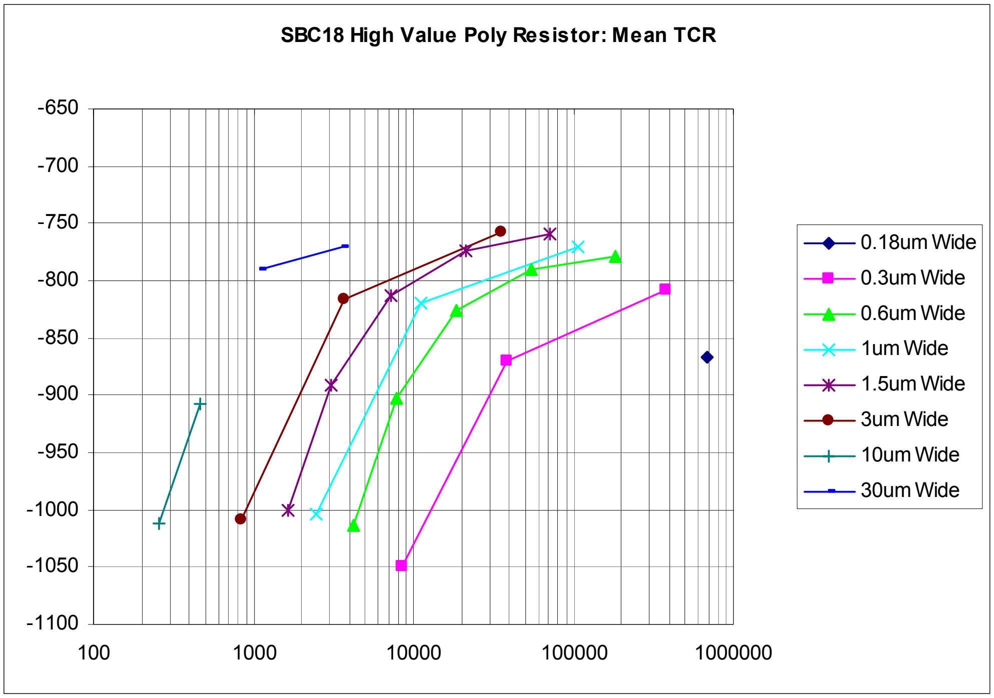
TCR= (R at 125C – R at 25C)/R at 25C x 100%

HV Resistors: Mean TCR (ppm/C) / Mean Resistance (Ohms)

Mean Tempco/Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide					-866 / 681,791
0.3um Wide	-1,049 / 8,514		-869 / 38,663		-808 / 375,852
0.45um Wide			-853 / 25,524		-786 / 246,585
0.6um Wide	-1,014 / 4,200	-903 / 7,799	-826 / 18,586	-790 / 54,784	-779 / 182,337
1um Wide	-1,003 / 2,482		-820 / 10,991		-770 / 107,483
1.5um Wide	-1,001 / 1,656	-892 / 3,067	-813 / 7,305	-773 / 21,432	-760 / 71,251
3um Wide	-1,008 / 836		-817 / 3,661		-758 / 35,559
10um Wide	-1,012 / 255	-908 / 470			
30um Wide				-790 / 1,091	-771 / 3,629

HV Resistors: 3 Sigma TCR (ppm/C) / Mean Resistance (Ohms)

3 Sigma Tempco/Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide					68 / 681,791
0.3um Wide	93 / 8,514		60 / 38,663		49 / 375,852
0.45um Wide			58 / 25,524		44 / 246,585
0.6um Wide	77 / 4,200	59 / 7,799	47 / 18,586	42 / 54,784	54 / 182,337
1um Wide	64 / 2,482		41 / 10,991		39 / 107,483
1.5um Wide	63 / 1,656	57 / 3,067	45 / 7,305	51 / 21,432	46 / 71,251
3um Wide	63 / 836		47 / 3,661		46 / 35,559
10um Wide	65 / 255	55 / 470			
30um Wide				54 / 1,091	49 / 3,629



1.3. HV Resistor Voltage Coefficient(VCR)

The voltage coefficient of resistance (VCR) has been measured for SBC18 high value resistors. The following three terminal resistor voltage coefficient model has been used to extract voltage coefficients:

$$R(VH, VL, Vbody) = Ro\left[VCRq(VH - VL)^2 + VCRld(VH - VL) + VCRlc\left(\frac{VH + VL}{2} - Vbody\right) + 1\right]$$

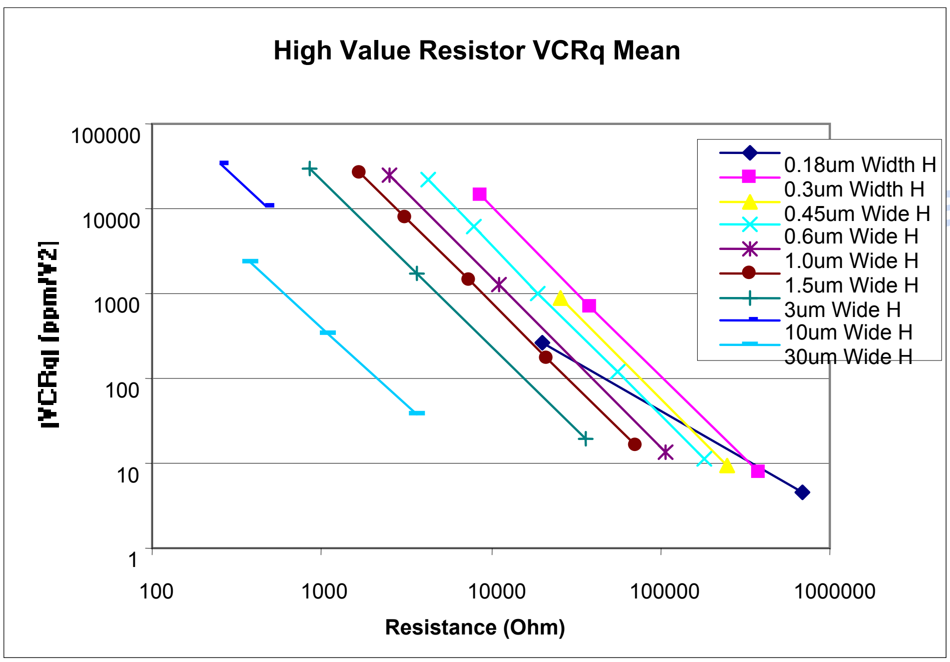
VCRq – quadratic differential mode voltage coefficient
VCRld – linear differential mode voltage coefficient
VCRlc – linear common mode voltage coefficient

Following wafers are used for VCR characterization: K17133/wf20/46sites, K17157/wf20/46sites, K19225/wf19&20/24sites and K19863/wf19&20/24sites. The number of total sites is 188 per resistor.

1.3.1. High value resistor VCRq

High Value Poly Matched Resistors Without Dummies: Mean VCRq (ppm/V^2) / Mean Resistance (Ohms)

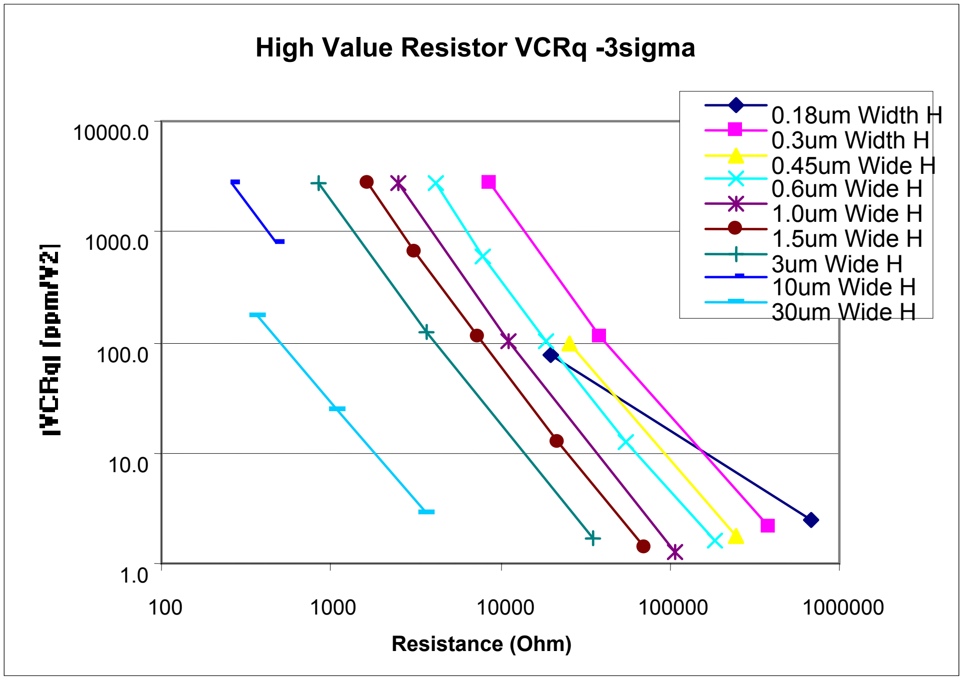
Width/Length	2	4	10	30	100
0.18um Width H			-271.1 / 19,888		-4.6 / 687,287
0.3um Width H	-14,730.9 / 8,567		-697.7 / 38,932		-7.6 / 378,436
0.45um Wide H			-870.0 / 25,709		-9.7 / 248,129
0.6um Wide H	-21,954.4 / 4,223	-5,987.6 / 7,843	-1,022.1 / 18,697	-116.6 / 55,095	-11.2 / 183,281
1.0um Wide H	-24,809.2 / 2,494		-1,268.3 / 11,044		-13.7 / 108,080
1.5um Wide H	-27,087.8 / 1,665	-7,950.4 / 3,080	-1,427.3 / 7,336	-170.7 / 21,550	-16.5 / 71,615
3um Wide H	-29,655.4 / 840		-1,728.9 / 3,679		-19.5 / 35,723
10um Wide H	-32,900.0 / 257	-10,629.6 / 473			
30um Wide H			-2,406.1 / 375	-334.9 / 1,097	-37.9 / 3,647



High Value Poly Matched Resistors Without Dummies: 3sigma VCRq (ppm/V^2) / Mean Resistance (Ohms)

Width/Length	2	4	10	30	100
0.18um Width H			77.5 / 19,888		2.5 / 687,287
0.3um Width H	2,747.5 / 8,567		110.2 / 38,932		2.2 / 378,436
0.45um Wide H			99.1 / 25,709		1.8 / 248,129
0.6um Wide H	2,797.6 / 4,223	613.0 / 7,843	101.7 / 18,697	12.4 / 55,095	1.6 / 183,281
1.0um Wide H	2,725.9 / 2,494		102.2 / 11,044		1.3 / 108,080
1.5um Wide H	2,818.9 / 1,665	661.9 / 3,080	110.4 / 7,336	12.4 / 21,550	1.4 / 71,615
3um Wide H	2,734.4 / 840		125.7 / 3,679		1.7 / 35,723

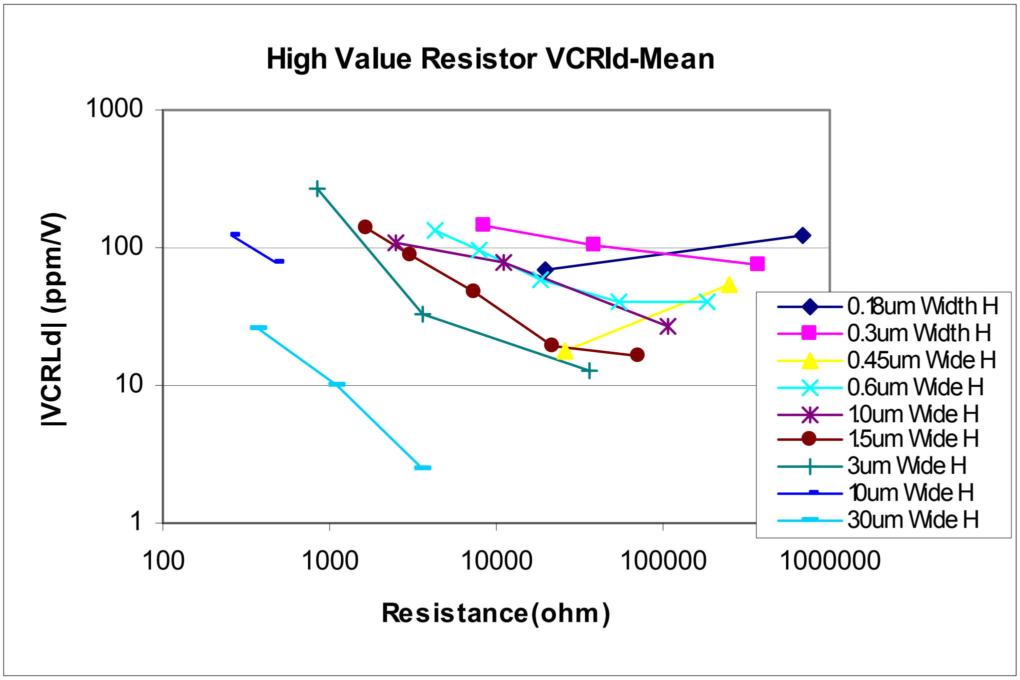
10um Wide H	2,822.3 / 257	787.8 / 473			
30um Wide H			171.5 / 375	25.0 / 1,097	2.8 / 3,647



1.3.2. High value resistor VCRld

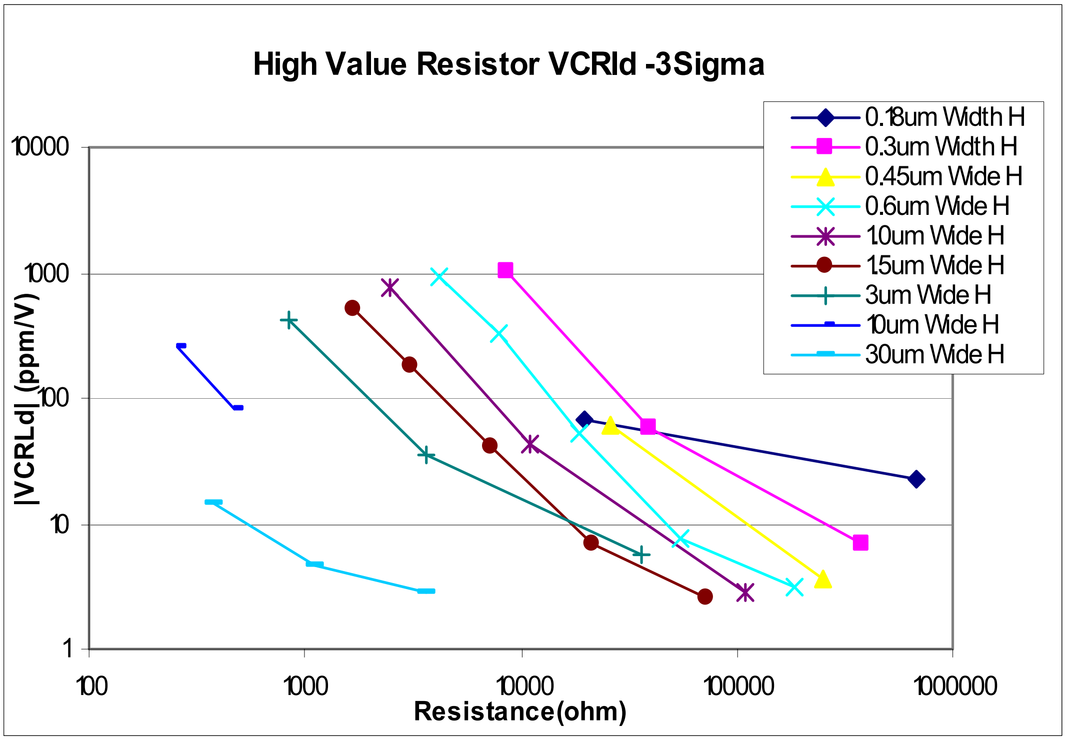
High Value Poly Matched Resistors Without Dummies: Mean VCRld (ppm/V) / Mean Resistance (Ohms)

Width/Length	2	4	10	30	100
0.18um Width H			-68.1 / 19,888		-122.1 / 687,287
0.3um Width H	-147.7 / 8,567		-102.9 / 38,932		-76.5 / 378,436
0.45um Wide H			-17.6 / 25,709		-54.9 / 248,129
0.6um Wide H	-136.0 / 4,223	-95.3 / 7,843	-59.7 / 18,697	-40.3 / 55,095	-40.5 / 183,281
1.0um Wide H	108.7 / 2,494		-77.8 / 11,044		-26.7 / 108,080
1.5um Wide H	-138.3 / 1,665	-89.9 / 3,080	-48.4 / 7,336	-19.3 / 21,550	-16.2 / 71,615
3um Wide H	-269.8 / 840		-33.0 / 3,679		-12.8 / 35,723
10um Wide H	-121.0 / 257	-79.5 / 473			
30um Wide H			-26.3 / 375	10.1 / 1,097	-2.5 / 3,647



High Value Poly Matched Resistors Without Dummies: 3sigma VCRld (ppm/V) / Mean Resistance (Ohms)

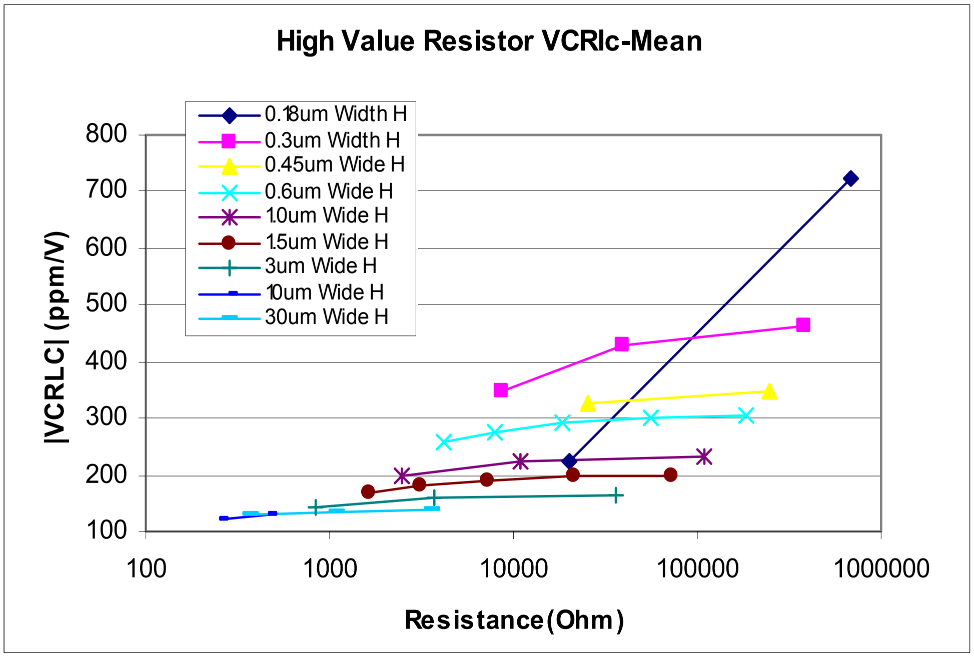
Width/Length	1	2	4	10	20
0.18um Width H			65.7 / 19,888		23.2 / 687,287
0.3um Width H	1,022.4 / 8,567		57.2 / 38,932		6.8 / 378,436
0.45um Wide H			60.6 / 25,709		3.7 / 248,129
0.6um Wide H	938.3 / 4,223	327.4 / 7,843	53.0 / 18,697	7.6 / 55,095	3.1 / 183,281
1.0um Wide H	775.3 / 2,494		42.1 / 11,044		2.8 / 108,080
1.5um Wide H	505.3 / 1,665	182.6 / 3,080	40.6 / 7,336	6.9 / 21,550	2.6 / 71,615
3um Wide H	411.3 / 840		34.8 / 3,679		5.7 / 35,723
10um Wide H	252.3 / 257	83.8 / 473			
30um Wide H			14.3 / 375	4.7 / 1,097	2.8 / 3,647



1.3.2. High value resistor VCRlc

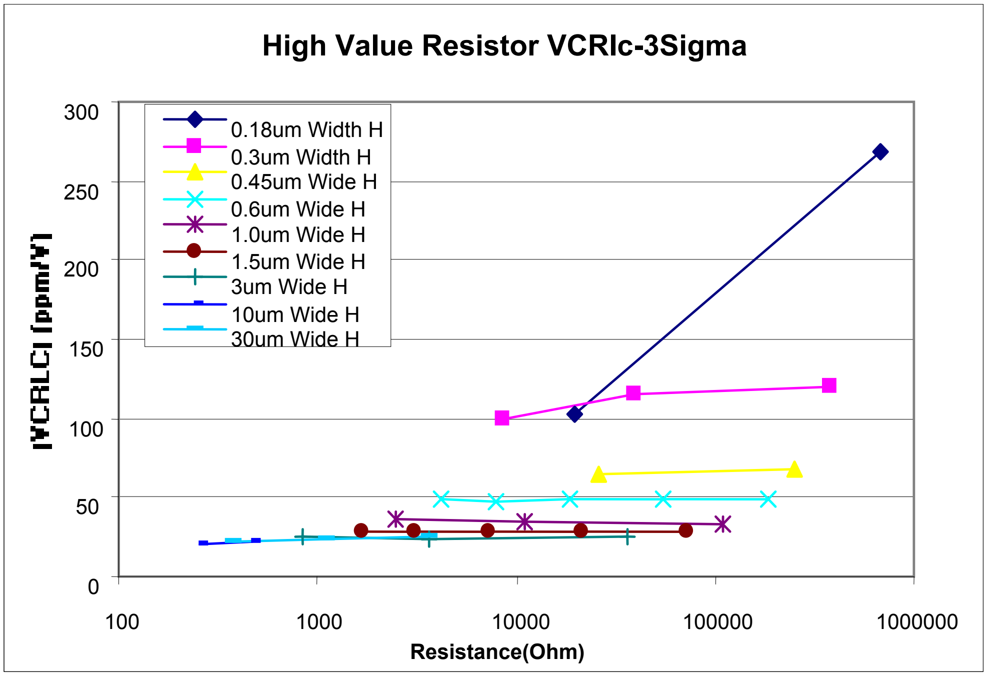
High Value Poly Matched Resistors Without Dummies: Mean VCRlc (ppm/V) / Mean Resistance (Ohms)

Width/Length	1	2	4	10	20
0.18um Width H			-224.2 / 19,888		-722.7 / 687,287
0.3um Width H	-348.9 / 8,567		-429.2 / 38,932		-460.7 / 378,436
0.45um Wide H			-327.5 / 25,709		-349.2 / 248,129
0.6um Wide H	-257.1 / 4,223	-275.0 / 7,843	-291.7 / 18,697	-299.9 / 55,095	-303.8 / 183,281
1.0um Wide H	-200.3 / 2,494		-224.6 / 11,044		-233.8 / 108,080
1.5um Wide H	-170.1 / 1,665	-181.8 / 3,080	-190.5 / 7,336	-198.1 / 21,550	-200.2 / 71,615
3um Wide H	-142.5 / 840		-157.9 / 3,679		-164.0 / 35,723
10um Wide H	-122.0 / 257	-127.9 / 473			
30um Wide H			-128.2 / 375	-133.6 / 1,097	-136.7 / 3,647



High Value Poly Matched Resistors Without Dummies: 3sigma VCRlc (ppm/V) / Mean Resistance (Ohms)

Width/Length	2	4	10	30	100
0.18um Width H			103.3 / 19,888		268.1 / 687,287
0.3um Width H	99.8 / 8,567		114.8 / 38,932		120.3 / 378,436
0.45um Wide H			65.5 / 25,709		68.3 / 248,129
0.6um Wide H	49.0 / 4,223	47.1 / 7,843	48.9 / 18,697	48.4 / 55,095	49.1 / 183,281
1.0um Wide H	36.2 / 2,494		34.0 / 11,044		33.4 / 108,080
1.5um Wide H	28.1 / 1,665	28.8 / 3,080	28.7 / 7,336	28.3 / 21,550	28.5 / 71,615
3um Wide H	24.9 / 840		24.1 / 3,679		24.6 / 35,723
10um Wide H	20.2 / 257	21.9 / 473			
30um Wide H			21.8 / 375	24.2 / 1,097	24.8 / 3,647

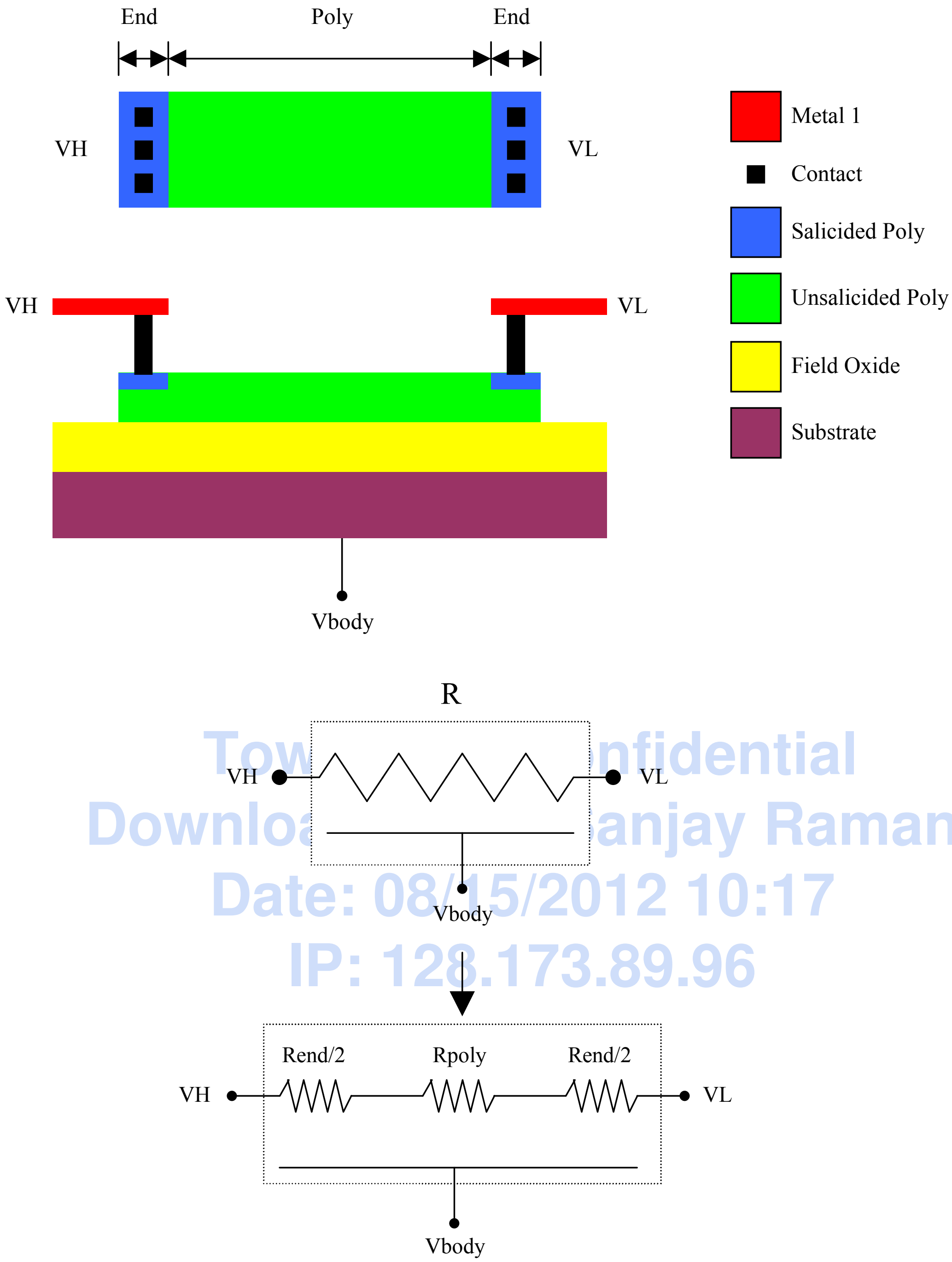


2. HV Resistor Models

2.1. HV Resistor Resistance Model

The model can be used for resistance, resistor tolerance, and resistor matching calculations.

The model describes the resistor with two components. The resistor is composed of a LV poly resistor in series with two end resistors.



The following equations are used to model the resistor:

$$R = Rpoly + Rend$$

$$Rpoly = Rs\frac{L}{W + \Delta W}$$

$$Rend = \frac{Re}{W + \Delta W}$$

$$R = Rs\frac{L}{W+\Delta W} + \frac{Re}{W+\Delta W}$$

We have used an optimizer to fit this model to the resistance data. The optimization was based on minimizing the RMS error in the fit for all resistors.

Parameter	Value	Unit
Mean Rs	1068	Ohm
Mean Re	339	Ohm - µm
Mean ΔW	-0.02	µm

2.1.1 HV Resistor Resistance Fit Error

The following table describes the ability of the model to fit the resistance data. The model fits all resistors to within 8.0% except 0.18um width resistors.

HV Matched Resistors: Mean Resistance Model Fit Error (%) / Mean Resistance (Ohms)

Delta Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide					-3.8% / 695,776
0.3um Wide			0.4% / 39,193		0.4% / 380,990
0.45um Wide			-0.7% / 25,817		-0.1% / 249,321
0.6um wide	0.6% / 4,244	0.8% / 7,885	1.2% / 18,782	0.9% / 55,318	0.3% / 184,135
1um Wide	1.0% / 2,502		1.6% / 11,070		0.9% / 108,355
1.5um Wide	0.3% / 1,668	0.9% / 3,088	1.3% / 7,355	1.4% / 21,579	0.9% / 71,758
3um Wide	-1.3% / 841		0.5% / 3,682		0.5% / 35,764
10um Wide	-3.4% / 257	-2.3% / 473			
30um Wide			-2.0% / 375	-1.5% / 1,096	-2.0% / 3,646

In order to determine the tolerances on Rs, Re, and ΔW; we have derived an equation which relates the standard deviations (σ) of the model parameters to the standard deviation of the resistance.

σ = standard deviation

σ^2 = variance

$$\sigma_R{}^2 = \sigma_{Rs}{}^2\left[\frac{\delta R}{\delta Rs}\right]^2 + \sigma_{Re}{}^2\left[\frac{\delta R}{\delta Re}\right]^2 + \sigma_{\Delta W}{}^2\left[\frac{\delta R}{\delta \Delta W}\right]^2$$

$$\sigma_R{}^2 = \sigma_{Rs}{}^2 \frac{L^2}{(W+\Delta W)^2} + \sigma_{Re}{}^2 \frac{1}{(W+\Delta W)^2} + \sigma_{\Delta W}{}^2 \left[\frac{L \cdot Rs}{(W+\Delta W)^2} + \frac{Rend}{(W+\Delta W)^2} \right]^2$$

We have used an optimizer to fit this model to the 3 sigma resistance data. The optimization was based on minimizing the RMS error in the fit for all resistors.

Parameter	Value	Unit
3 Sigma Rs	92.9	Ohm
3 Sigma Re	126.0	Ohm - μm
3 Sigma ΔW	0.073	μm

The error relative to the 3sigma resistance is below 10% for most resistors except 0.18um width
HV Matched Resistors: 3 Sigma **Fit Error** (%) / Mean Resistance (Ohms)

Delta 3Sigma Resistance					
Width\Length	2	4	10	30	100
0.18um Wide					14.3% / 695,776
0.3um Wide	6.5% / 8,636		4.5% / 39,193		3.7% / 380,990
0.45um Wide			-3.1% / 25,817		-1.4% / 249,321
0.6um wide	-3.1% / 4,244	-4.3% / 7,885	-4.4% / 18,782	-4.8% / 55,318	-6.7% / 184,135
1um Wide	-3.2% / 2,502		-5.9% / 11,070		-7.0% / 108,355
1.5um Wide	-2.5% / 1,668	-5.3% / 3,088	-4.6% / 7,355	-3.6% / 21,579	-4.6% / 71,758
3um Wide	0.0% / 841		0.2% / 3,682		1.6% / 35,764
10um Wide	4.8% / 257	3.1% / 473			
30um Wide			0.0% / 375	9.4% / 1,096	8.4% / 3,646

2.1.2. Repeatability of High value resistor Resistance

		High Value Resistor		
		Rs	Rend	Delta W
Spec	Nom.	1000	320	-0.09
	low	800		
	high	1200		
K17133	Mean	1040.7	335.2	0.007
	1sigma	12.2	29.5	0.004
K17157	Mean	1092.3	343.9	-0.041
	1sigma	14.7	29.6	0.002
K19225	Mean	1073.3	337.1	-0.027
	1sigma	14.4	29.7	0.005
K19863	Mean	1051.2	333.0	-0.003
	1sigma	18.5	31.1	0.003
K19920	Mean	1095.6	348.6	-0.03
	1sigma	12.6	20.1	0.004

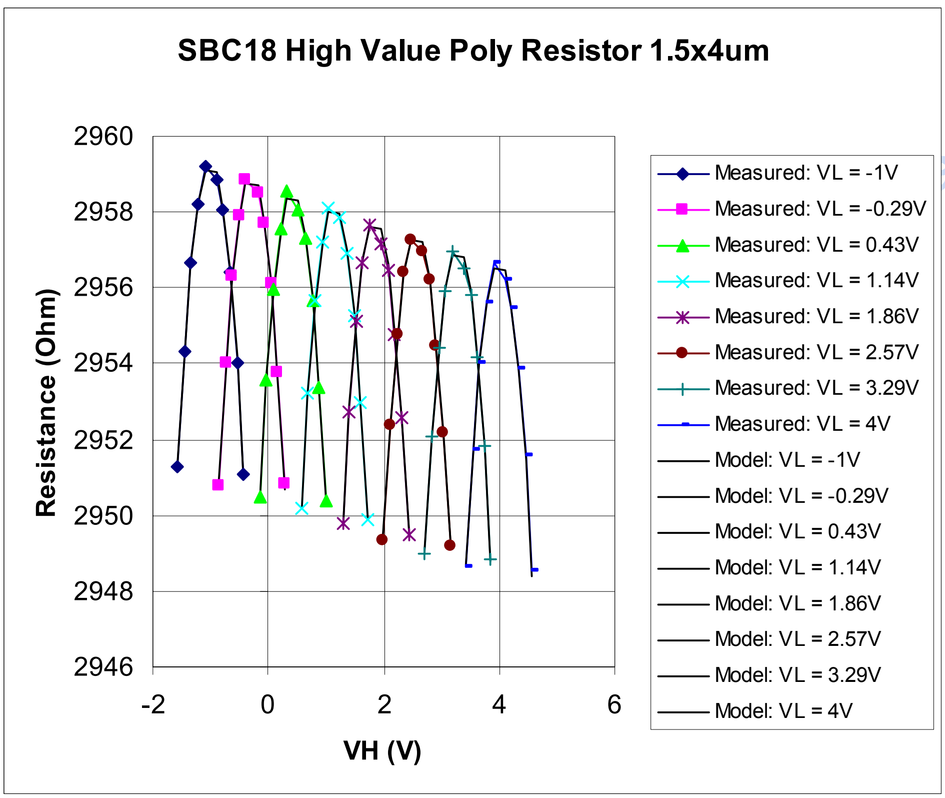
2.2. High value resistor VCR Model

The following model has been used to fit the voltage coefficient of resistance:

$$R(VH, VL, Vbody) = Ro\left[VCRq(VH - VL)^2 + VCRld(VH - VL) + VCRlc\left(\frac{VH + VL}{2} - Vbody\right) + 1\right]$$

VCRq – quadratic differential mode voltage coefficient
VCRld – linear differential mode voltage coefficient
VCRlc – linear common mode voltage coefficient

The VCRq term appears to be caused primarily by the change in temperature due to ohmic heating. The source of the asymmetric VCRld term is still unknown. The VCRlc term appears to be due to accumulation or depletion of the bottom surface of the resistor. For the differential case, the resistor has a linear gradient of depletion along the length of the resistor; whereas, for the common mode case, the depletion is constant along the length of the resistor. If the common mode voltage coefficient is completely linear, the average depletion in the differential case is one half of the common mode case.
The following chart gives an example of the VCR for a short resistor:



A characterization of the high value resistors in the SBC18 process has been completed. The measurement results for some parameters have been successfully modeled.

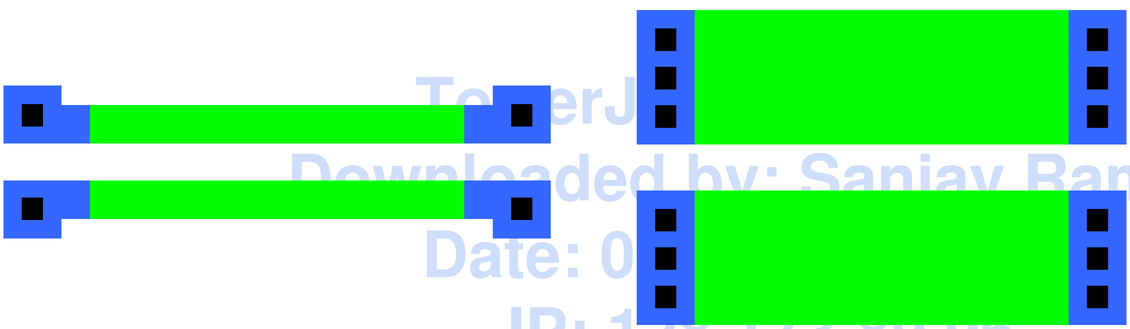
Appendix: Test Structure and Test Description

A. Test Structures

The GA577 SBC18 test chip was used for this characterization. This test chip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 4 modules devoted to HV Resistor characterization on the GA577. The following table describes the resistor types and sizes available for characterization:

Matched Resistors



Matched Pairs Without Dummies:

Width\Length	2μm	4μm	10μm	30μm	100μm
0.18μm					X
0.3μm			X		X
0.45um			X		X
0.6μm	X	X	X	X	X
1.0μm	X		X		X
1.5μm	X	X	X	X	X
3.0μm	X		X		X
10μm	X	X			
30μm			X	X	X

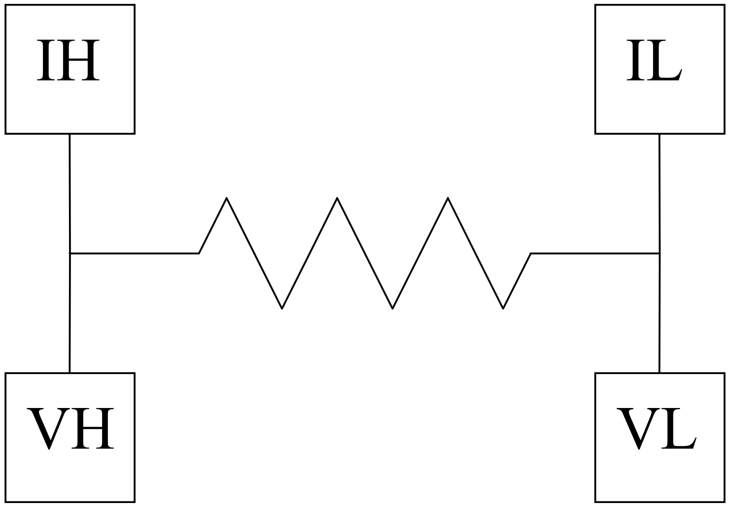


Figure 6: Resistor with Kelvin Pads

Since the resistance of the measurement system cables, probes, pads, and interconnect can degrade the accuracy of resistor measurements, all of the resistors are laid out with pads for Kelvin measurements (figure 1).

The Kelvin measurement method requires that two pads be connected to each end of the resistor. The IH pad is used to force a current into the resistor, and the IL pad is usually connected to a grounded ammeter in order to measure the current flow out of the resistor. The potentials at the IH current source and IL current meter will be different from the potentials at the resistor ends due to the effect of parasitic series resistance. By adding the VH and VL pads, we are able to accurately measure the potential at the resistor ends. Since no current flows through the VH and VL pads, the parasitic series resistances do not affect the measurement. The following equation is used to calculate the resistance:

$$R = -\frac{(VH - VL)}{IL}$$

In order to minimize the number of test modules, and thus the chip area, we have used the layout strategy shown in figure 2. This configuration allows kelvin measurements of all of the resistors, but it does not support simultaneous measurements for matching.

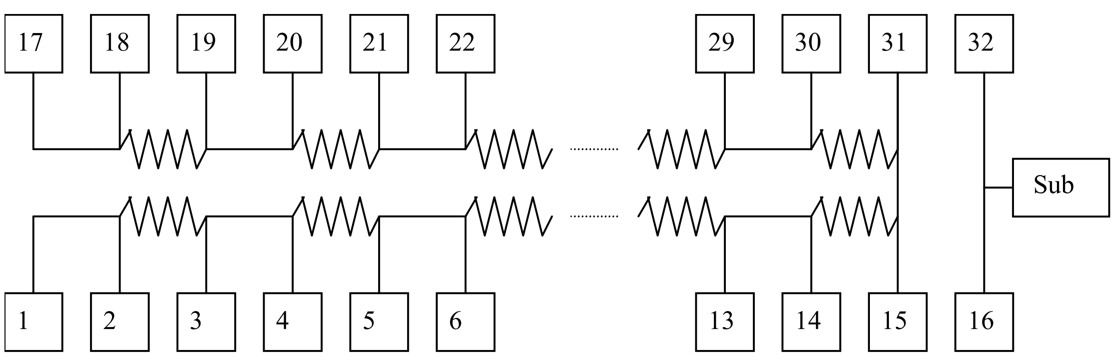


Figure 7: Resistor Matching Module Configuration

B. Test Description

B.1. Resistance and Resistor Matching

In order to simplify the data analysis, the resistance is reported only for the first resistor in the pair, and the test on the second resistor reports the resistance difference between the two resistors in percent.

$$\Delta R = 100 * \frac{R2 - R1}{R1}$$

B.2. Temperature Coefficient of Resistance

TCR testing is performed by changing the chuck temperature on the Reedholm tester, and then running the resistance and resistor matching test a second time.

$$TCR(\Delta T, Tref) = \frac{R(\Delta T) - R(Tref)}{R(Tref) \cdot \Delta T}$$

B.3. Voltage Coefficient of Resistance

The Analog Tester is a custom built tester intended for high resolution measurements which the Reedholm cannot support. The analog tester is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. All of the cabling between the HP4156, switch matrix, and probe card is guarded through the use of triaxial cable. The HP4156 is composed of 4 SMUs (Source Measure Units), 2 VSUs (Voltage Source Units), and 2 VMUs (Voltage Measurement Units). The SMUs are used to simultaneously force and measure voltages and currents. The measurement resolution of the HP4156 SMUs is approximately 6 digits. The Analog Tester is controlled by a PC using a Visual Basic test program. The test program (WaferTest) is designed to provide a relatively open framework for implementing custom analog tests, and it places the measurement results directly into an Excel spreadsheet.

The VCR test is performed on the Analog Tester, and measures the resistance of a single resistor in all bias regions. The test reports the measured resistance, and model extraction takes place in Excel during post processing. The setup for this test consists of the two resistor terminals (VH and VL) and the body terminal (Vbody), as shown in figure B1.1. In a circuit, the allowable bias range for resistors ranges from ground to VDD for both the VH and VL terminals with the substrate always grounded. This bias range is the region inside the box depicted in figure B.1.2a. The zero differential voltage line represents the region in which resistance cannot be measured. For shorter resistors, the maximum differential voltage is restricted by the maximum current density specification in order to prevent damage. The bias range for shorter resistors is depicted in figure B.1.2b.

We have chosen to use a bias scheme shown in figure B.1.3, in which the VL terminal is always held at ground. The VH terminal is used to provide a differential bias, and the Vbody terminal is used to provide a common mode bias. This configuration simplifies biasing, as the same differential bias range can be used for each sweep. In addition, the linearity requirements on the SMU measuring current are reduced, as the current is measured through the VL terminal which is always grounded. As no measurements can be made for small differential voltages, a minimum differential voltage is specified.

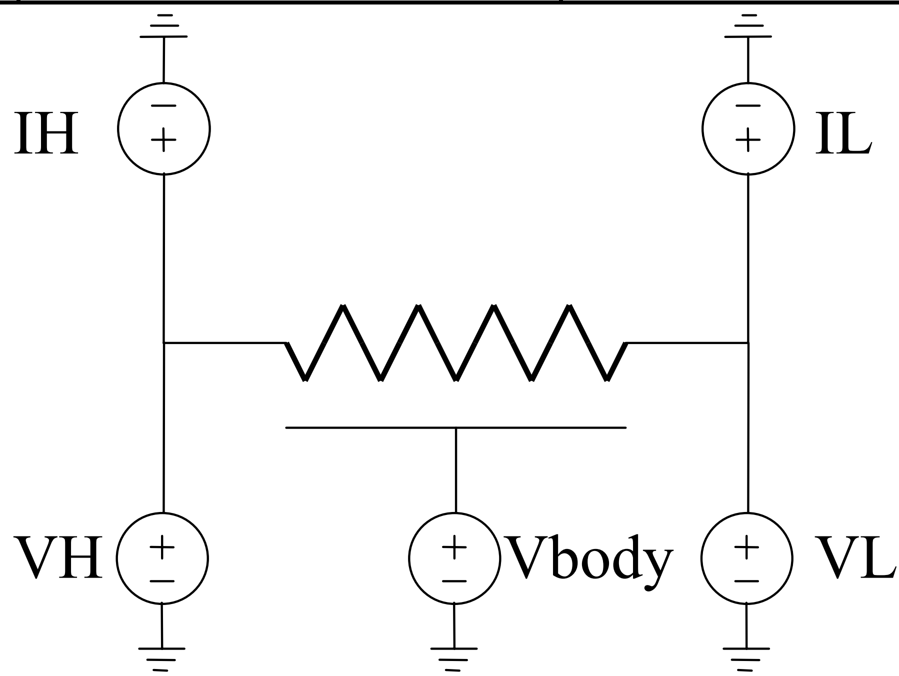


Figure B.1.1: VCR Measurement Configuration

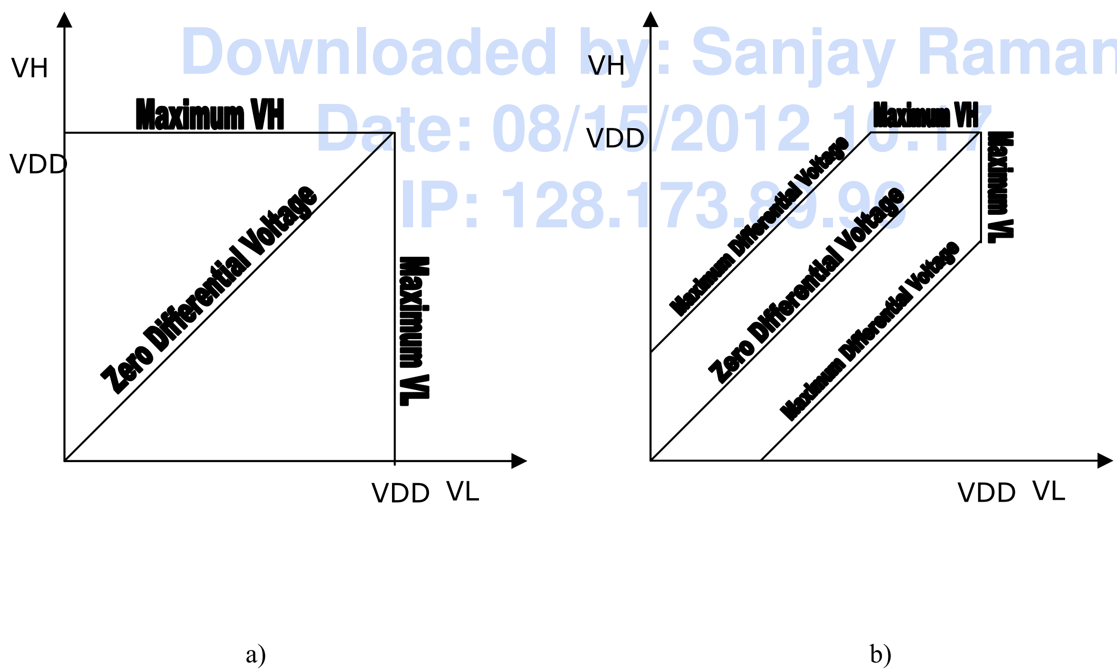
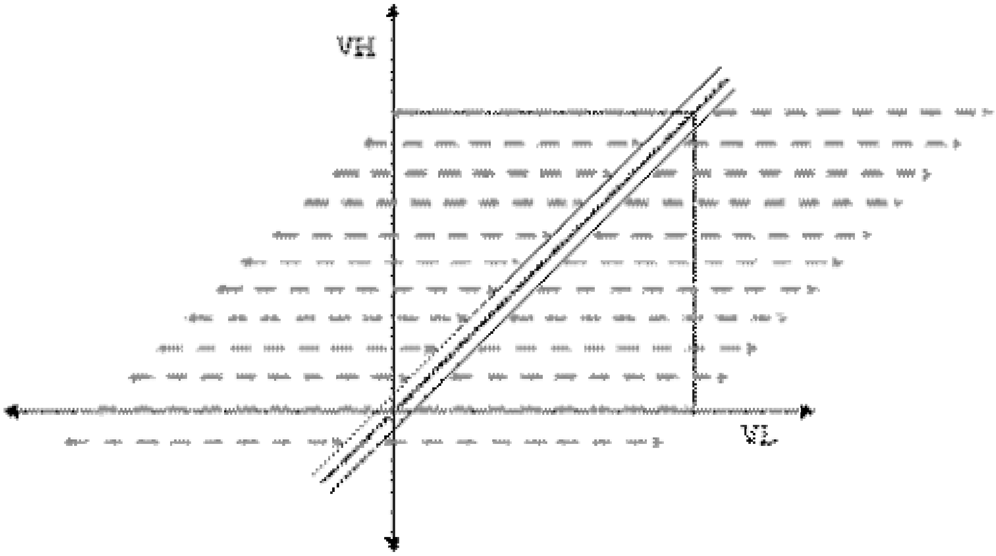


Fig B.1.2. a) Long Resistor VCR Bias Range, b) Short Resistor Bias Range



B.1.3. Long Resistor VCR Bias Sweep

C. Test Conditions

The following test conditions were used for this characterization:

<u>C.1. Resistance and Resistor Matching</u>

In order to maximize the accuracy of the resistance test, we have chosen the current so that the voltage drop over resistors is around 100mV in the four terminal set up.

<u>C.2. Temperature Coefficient of Resistance</u>

The HV Resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 30C and 130C.

C.3. Voltage Coefficient of Resistance

The measurement of VCR is complicated by the large ranges of resistances, voltages, and currents involved. The resistances to be measured, and the linear and quadratic voltage coefficients to be extracted, can vary by as much as 6 orders of magnitude over the space of available resistor widths and lengths. If the voltages or currents become too small, the HP4156 will not have sufficient precision to extract the VCR coefficients. There are problems measuring short resistors, as the voltage resolution of the HP4156 drops rapidly as the differential voltage drops below 0.3V. For short resistors, the maximum current density is often reached or exceeded at 0.5V. For very high value resistors, the current can be too low for the HP4156 to measure with high precision.

The test is implemented with node IH connected to a SMU, which is configured to force voltage. The VH and VL nodes are connected to VMUs (the VMUs cannot be used in differential mode, as this mode is limited to 2V). The IL node is connected to a SMU, which is set to force 0 volts, and measure the current. The Body node is connected to a VSU. The test setup provides for connection inputs (IH, VH, VL, IL, Body), resistor information inputs (Width, Length), and bias conditions (ConstDeltaV, SlopeDeltaV, NumDeltaV, MinDeltaV, MaxDeltaV, StartVb, StopVb, NumVb).

The following steps are performed in order to measure the VCR:
Determine the VH bias range based on the resistor length. The maximum VH is determined by the lesser of (MinDeltaV + SlopeDeltaV * Length) or MaxDeltaV.
Measure the resistance as a function of VH and Vbody.
Place the measured resistance, VH, and VL into Excel.

The VCR model parameters (Ro, VCRq, VCRld, and VCRlc) are extracted by optimization in Excel.

The following test conditions were used for VCR characterization:

Parameter	Value
ConstDeltaV	0.3
SlopeDeltaV	0.07
NumDeltaV	10
MinDeltaV	0.1
MaxDeltaV	5
StartVb	1
StopVb	-4
NumVb	8

8. Low Value Unsilicided Poly Resistor Characterization

Table of Contents

Summary

A characterization of the low value resistors in the SBC18 process has been performed. The results for the following tests are presented: resistance, resistor matching, TCR (Temperature Coefficient of Resistance) and VCR (Voltage Coefficient of Resistance). The test structures, test procedures, and test conditions are described in the appendix. Although the characterization was carried out on SBC18QTD GA577 test chip, it is applicable to low value resistors all sbc18 process variants.

1. Measurement Results

The characterization was performed on wafers processed in the SBC18 process using the GA577 engineering test chip. For resistance, matching and TCR measurement, 24 dies from wafers from following lots were tested: K17133 wf.16 to 22, K17157 wf20 to 25 K19225 wf.16 to 20, K19863 wf16 to 20, K19920wf16,18,19,21,22. Since the goal of this characterization is to measure the standard deviation of the difference between two devices, a relatively large sample size is tested to obtain useful results.

For measurements involving a large number of samples, it is almost inevitable that there will be a few "bad points" which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these "bad points," it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3sigma limits.

1.1. LV Resistance and Resistor Matching

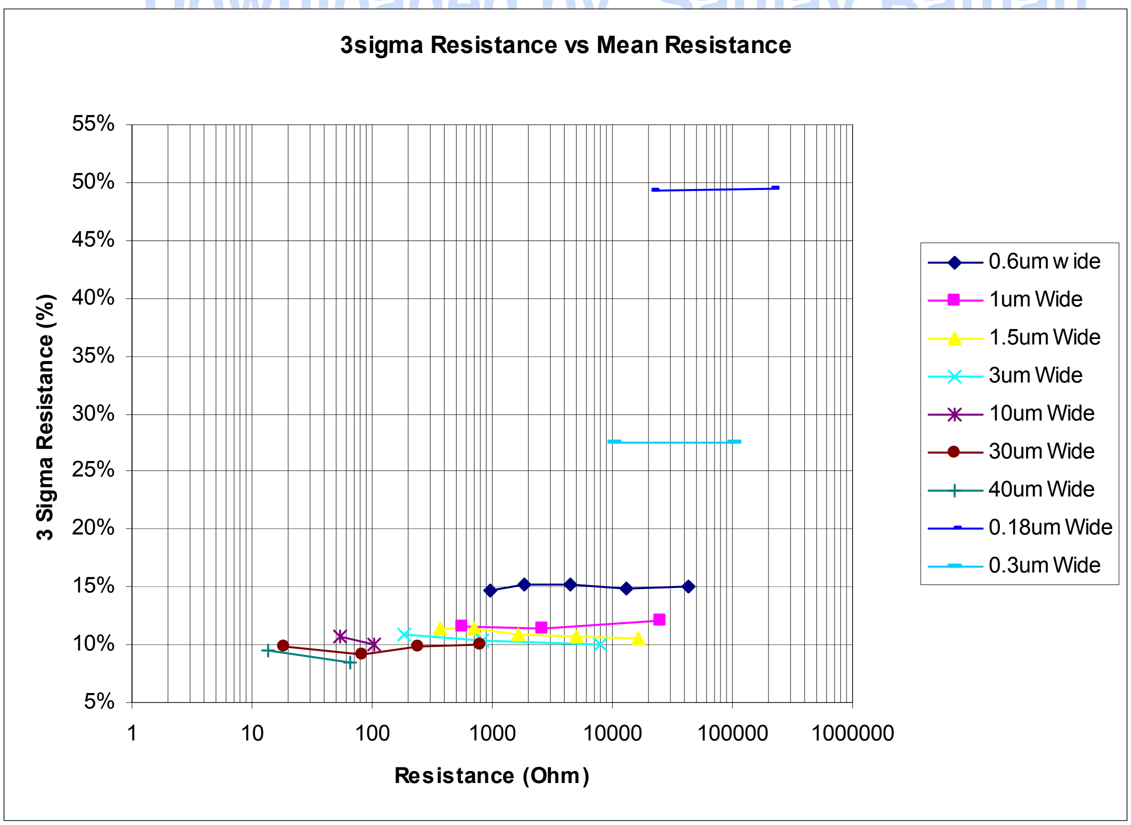
1.1.2. LV Resistor 3 Sigma Resistance

The following tables list both the mean and 3 sigma of the measured resistance for each test structure:

3 Sigma Resistance (%) = 100 * 3 Sigma Resistance / Mean Resistance

LV Resistors: 3 Sigma Resistance (%) / Mean Resistance (Ohms)

3 Sigma (%) / Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide			49.2% / 21,445		49.5% / 211,637
0.3um Wide			27.6% / 10,468		27.5% / 102,791
0.6um wide	14.7% / 976	15.2% / 1,851	15.2% / 4,474	14.9% / 13,189	15.1% / 43,626
1um Wide	11.6% / 562		11.4% / 2,566		12.0% / 25,057
1.5um Wide	11.5% / 369	11.4% / 696	11.0% / 1,674	10.7% / 4,934	10.6% / 16,314
3um Wide	10.9% / 182		10.3% / 822		10.0% / 7,991
10um Wide	10.6% / 55	10.0% / 102			
30um Wide	9.8% / 18		9.1% / 81	9.9% / 240	10.1% / 802
40um Wide	9.5% / 14		8.5% / 65		

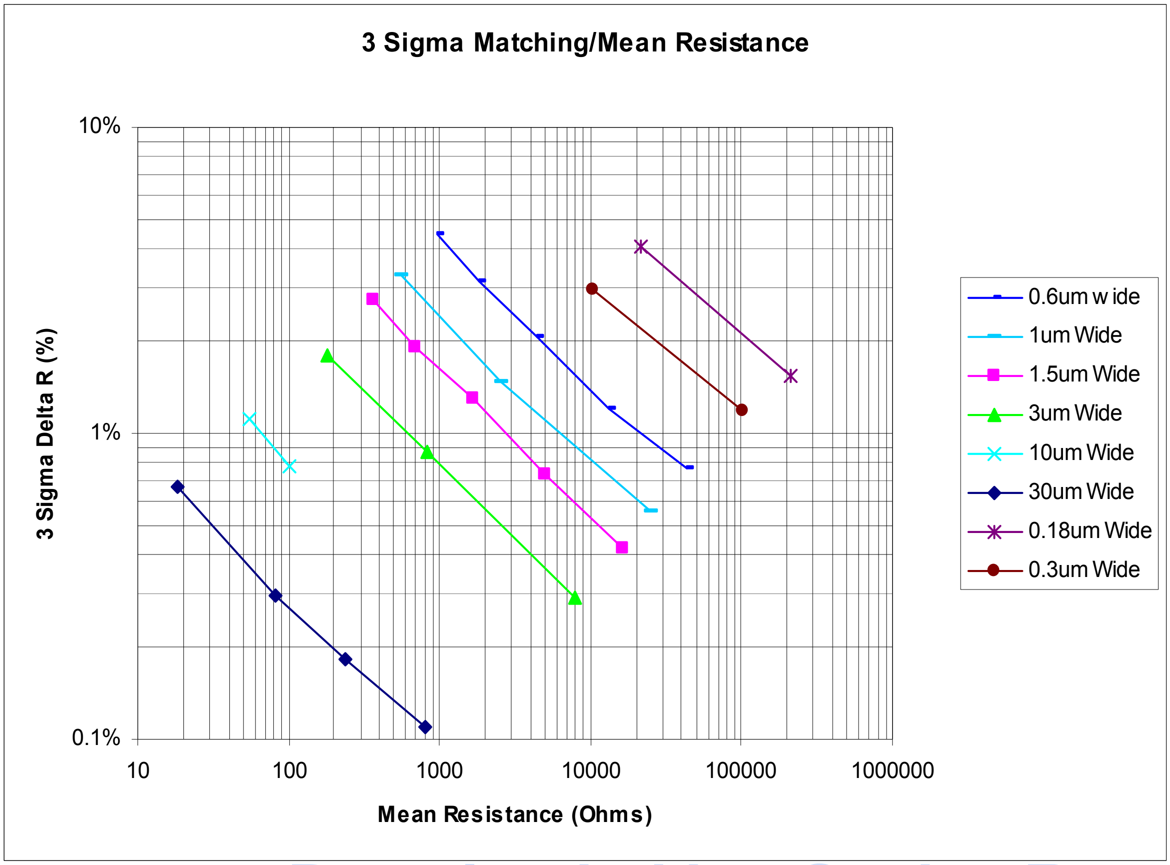


LV Resistor 3 Sigma Matching of Resistor Pairs

The following tables list the 3 sigma matching of resistance for each resistor pair:

LV Matched Resistors: 3 Sigma Matching (%) / Mean Resistance (Ohms)

Measured 3 Sigma Matching					
Width	2	4	10	30	100
0.18um Wide			4.1% / 21,445		1.5% / 211,637
0.3um Wide			2.9% / 10,468		1.2% / 102,791
0.6um wide	4.5% / 976	3.1% / 1,851	2.1% / 4,474	1.2% / 13,189	0.8% / 43,626
1um Wide	3.3% / 562		1.5% / 2,566		0.6% / 25,057
1.5um Wide	2.7% / 369	1.9% / 696	1.3% / 1,674	0.7% / 4,934	0.4% / 16,314
3um Wide	1.8% / 182		0.9% / 822		0.3% / 7,991
10um Wide	1.1% / 55	0.8% / 102			
30um Wide	0.7% / 18		0.3% / 81	0.2% / 240	0.1% / 802


3 Sigma Matching/Mean Resistance
10%
1%
0.1%
3 Sigma Delta R (%)
10
100
1000
10000
100000
1000000
Mean Resistance (Ohms)
0.6um w ide
1um Wide
1.5um Wide
3um Wide
10um Wide
30um Wide
0.18um Wide
0.3um Wide

1.2. LV Resistor Temperature Coefficient

The LV resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 25°C and 125°C. The following table lists both the mean and 3 sigma of the measured TCR:

TCR= (R at 125C – R at 25C)/R at 25C x 100%

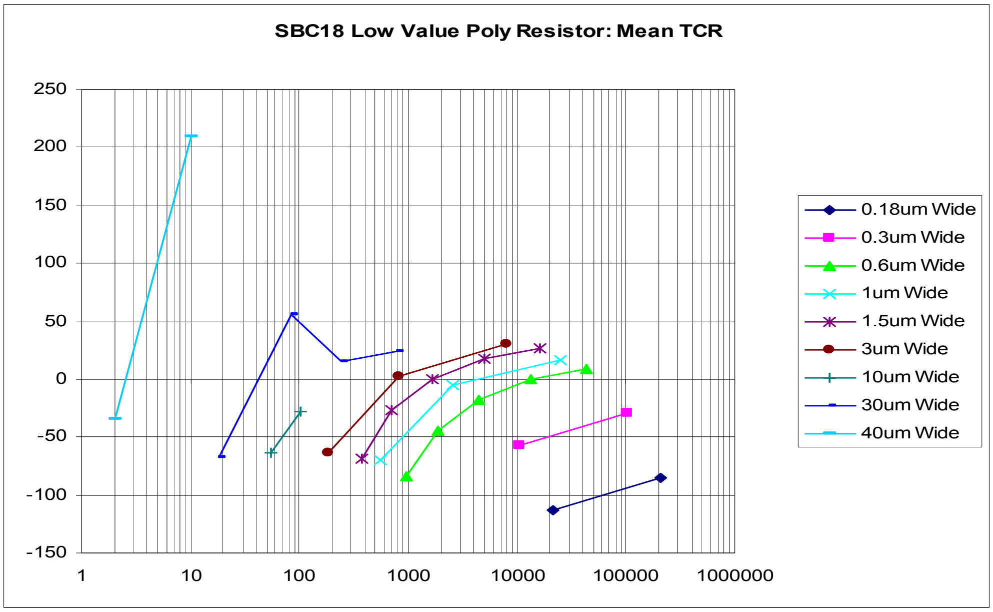
LV Resistors: Mean TCR (ppm/C) / Mean Resistance (Ohms)

Mean Tempco/Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide			-114 / 21,077		-85 / 207,476
0.3um Wide			-58 / 10,406		-29 / 102,147
0.6um wide	-84 / 978	-45 / 1,851	-17 / 4,474	-1 / 13,257	9 / 43,818
1um Wide	-71 / 564		-6 / 2,575		17 / 25,072
1.5um Wide	-68 / 369	-27 / 697	0 / 1,678	18 / 4,944	27 / 16,349
3um Wide	-64 / 183		2 / 822		31 / 7,986
10um Wide	-64 / 55	-29 / 102			
30um Wide	-67 / 18		55 / 84	15 / 240	24 / 804
40um Wide	-34 / 14		209 / 65		

LV Resistors: 3 Sigma TCR (ppm/C) / Mean Resistance (Ohms)

3 Sigma Tempco/Mean Resistance					
Width\Length	2	4	10	30	100
0.18um Wide			87 / 21,077		81 / 207,476
0.3um Wide			75 / 10,406		68 / 102,147
0.6um wide	94 / 978	104 / 1,851	84 / 4,474	81 / 13,257	82 / 43,818
1um Wide	107 / 564		84 / 2,575		91 / 25,072
1.5um Wide	125 / 369	99 / 697	87 / 1,678	72 / 4,944	82 / 16,349
3um Wide	99 / 183		83 / 822		96 / 7,986
10um Wide	118 / 55	115 / 102			
30um Wide	100 / 18		274 / 84	84 / 240	83 / 804

40um Wide	122 / 14		187 / 65		



1.3. LV Resistor Voltage Coefficient(VCR)

The voltage coefficient of resistance (VCR) has been measured for SBC18 low value resistors. The following three terminal resistor voltage coefficient model has been used to extract voltage coefficients:

$$R(VH, VL, Vbody) = Ro\left[VCRq(VH - VL)^2 + VCRld(VH - VL) + VCRlc\left(\frac{VH + VL}{2} - Vbody\right) + 1\right]$$

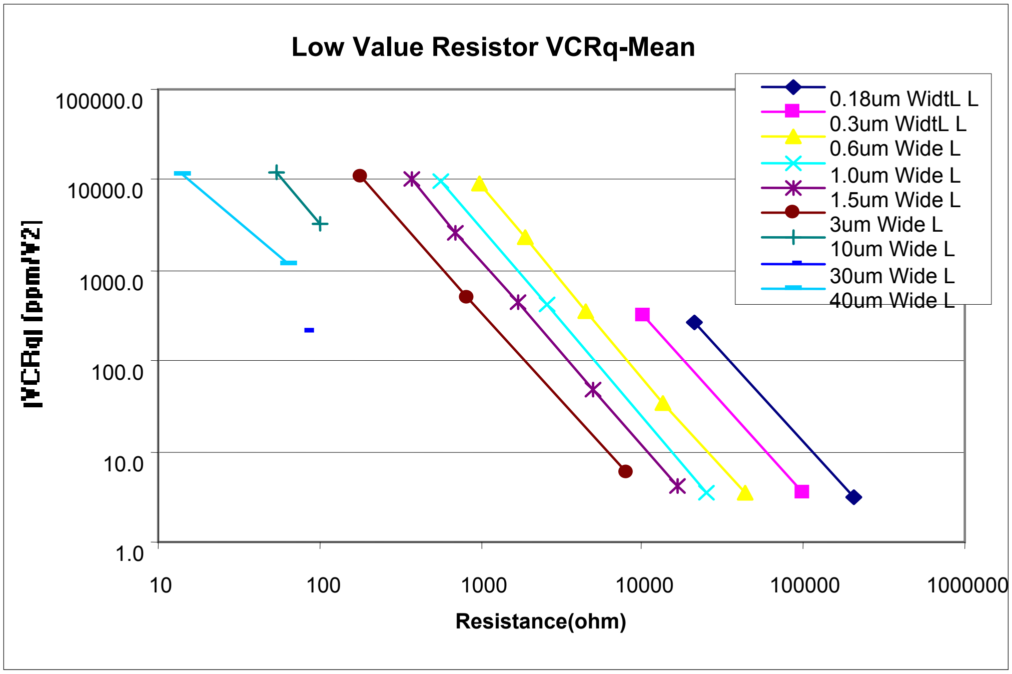
VCRq – quadratic differential mode voltage coefficient
VCRld – linear differential mode voltage coefficient
VCRlc – linear common mode voltage coefficient
Following wafers are used for VCR characterization: K17133/wf20/46sites, K17157/wf20/46sites, K19225/wf19&20/24sites and K19863/wf19&20/24sites. The number of total sites is 188 per resistor.

1.3.3. Low Value Resistor VCRq

Low Value Poly Matched Resistors Without Dummies: Mean VCRq (ppm/V^2) / Mean Resistance (Ohms)

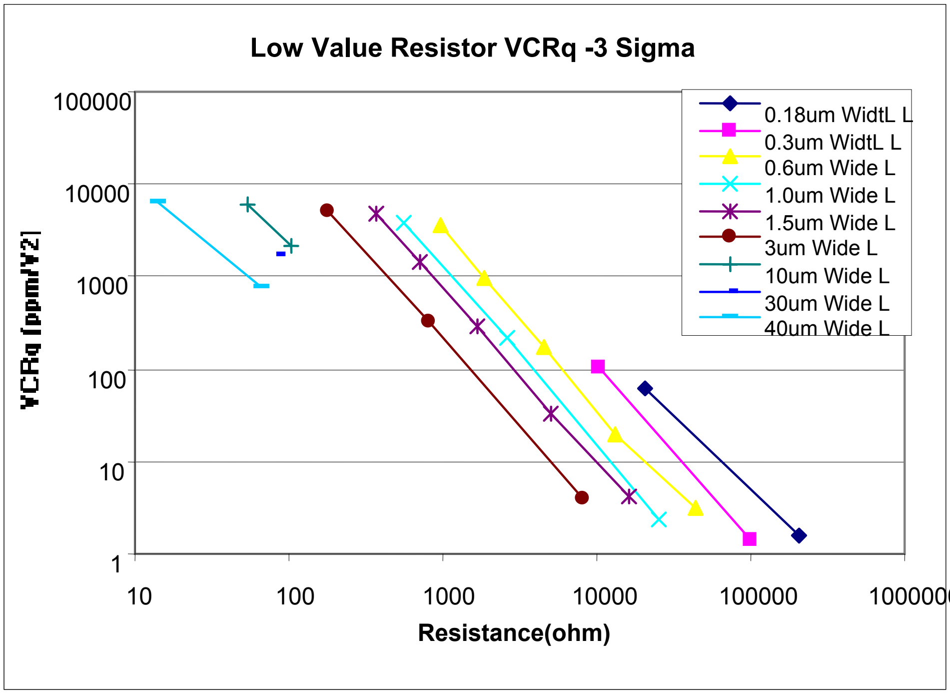
VCRq/R	2	4	10	30	100
0.18um WidtL L			-272.6 / 20,897		-3.2 / 206,810
0.3um WidtL L			-313.8 / 10,359		-3.4 / 99,556
0.6um Wide L	-9,239.6 / 983	-2,353.5 / 1,856	-359.4 / 4,491	-35.1 / 13,244	-3.5 / 43,848
1.0um Wide L	-9,772.8 / 565		-417.8 / 2,580		-3.5 / 25,165
1.5um Wide L	-10,297.3 / 370	-2,644.6 / 698	-454.1 / 1,678	-49.3 / 4,946	-4.2 / 16,369
3um Wide L	-10,727.8 / 182		-503.1 / 824		-5.8 / 8,022
10um Wide L	-12,028.5 / 54	-3,251.7 / 102			
30um Wide L			-215.7 / 83		

40um Wide L	-11,376.5 / 14		1,184.4 / 65		



Low Value Poly Matched Resistors Without Dummies: 3sigma VCRq (ppm/V^2) / Mean Resistance (Ohms)

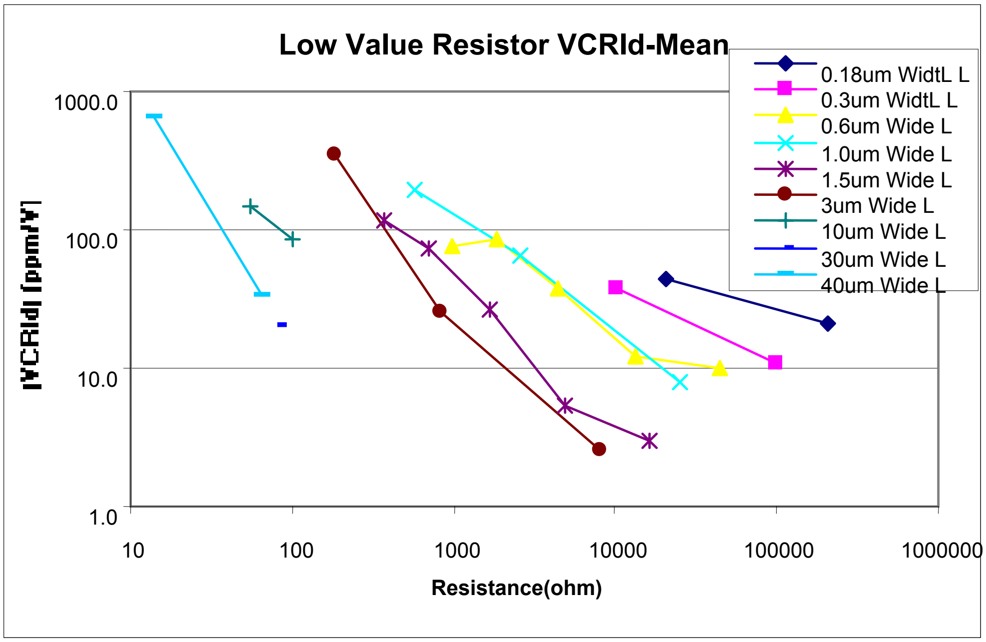
	2	4	10	30	100
0.18um WidtL L			62.4 / 20,897		1.5 / 206,810
0.3um WidtL L			103.5 / 10,359		1.4 / 99,556
0.6um Wide L	3,561.9 / 983	989.9 / 1,856	178.1 / 4,491	20.2 / 13,244	3.1 / 43,848
1.0um Wide L	3,865.0 / 565		220.7 / 2,580		2.4 / 25,165
1.5um Wide L	4,699.1 / 370	1,453.1 / 698	293.3 / 1,678	32.6 / 4,946	4.2 / 16,369
3um Wide L	5,117.9 / 182		331.2 / 824		3.9 / 8,022
10um Wide L	6,096.6 / 54	2,139.2 / 102			
30um Wide L			1,685.4 / 83		
40um Wide L	6,242.4 / 14		769.5 / 65		



1.3.2. Low Value Resistor VCRld

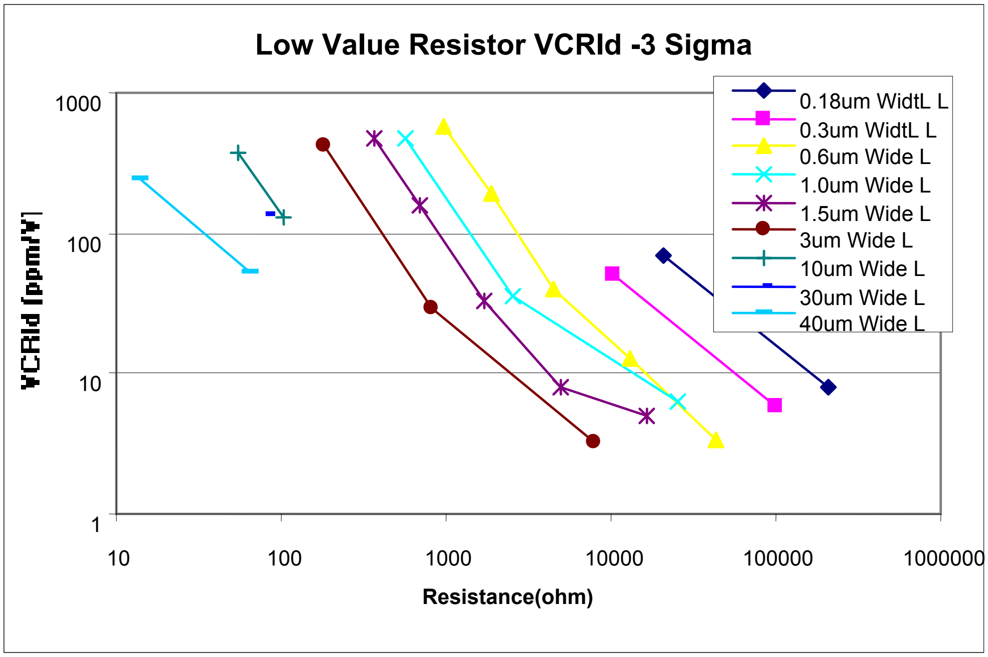
Low Value Poly Matched Resistors Without Dummies: Mean VCRld (ppm/V) / Mean Resistance (Ohms)

VCRld/R	2	4	10	30	100
0.18um WidtL L			-44.3 / 20,897		-21.3 / 206,810
0.3um WidtL L			-38.4 / 10,359		-10.6 / 99,556
0.6um Wide L	-75.2 / 983	-83.9 / 1,856	-37.5 / 4,491	-12.3 / 13,244	-10.2 / 43,848
1.0um Wide L	191.7 / 565		-65.9 / 2,580		-7.8 / 25,165
1.5um Wide L	-117.8 / 370	-72.3 / 698	-26.8 / 1,678	-5.4 / 4,946	-2.9 / 16,369
3um Wide L	-353.8 / 182		-25.9 / 824		-2.5 / 8,022
10um Wide L	-145.1 / 54	-85.0 / 102			
30um Wide L			20.3 / 83		
40um Wide L	-659.8 / 14		-33.4 / 65		



Low Value Poly Matched Resistors Without Dummies: 3sigma VCRld (ppm/V) / Mean Resistance (Ohms)

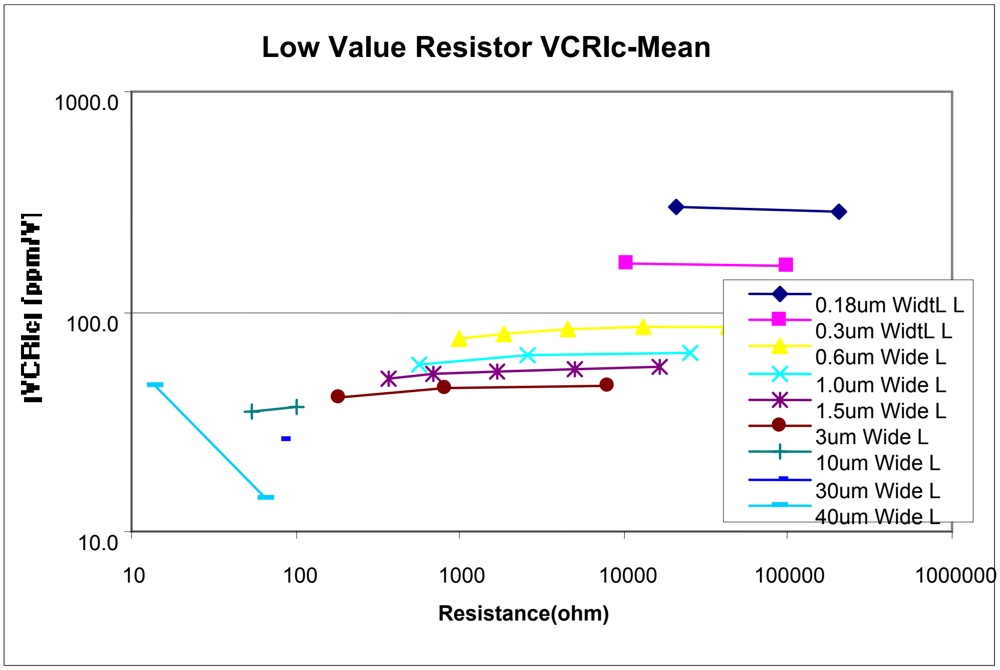
VCRld/R	2	4	10	30	100
0.18um WidtL L			69.6 / 20,897		8.1 / 206,810
0.3um WidtL L			50.2 / 10,359		5.9 / 99,556
0.6um Wide L	574.4 / 983	195.4 / 1,856	39.7 / 4,491	12.6 / 13,244	3.3 / 43,848
1.0um Wide L	481.3 / 565		35.9 / 2,580		6.2 / 25,165
1.5um Wide L	471.0 / 370	160.7 / 698	33.3 / 1,678	8.1 / 4,946	5.0 / 16,369
3um Wide L	427.2 / 182		28.9 / 824		3.3 / 8,022
10um Wide L	377.1 / 54	132.1 / 102			
30um Wide L			137.3 / 83		
40um Wide L	239.2 / 14		52.8 / 65		



1.3.4. Low Value Resistor VCRlc

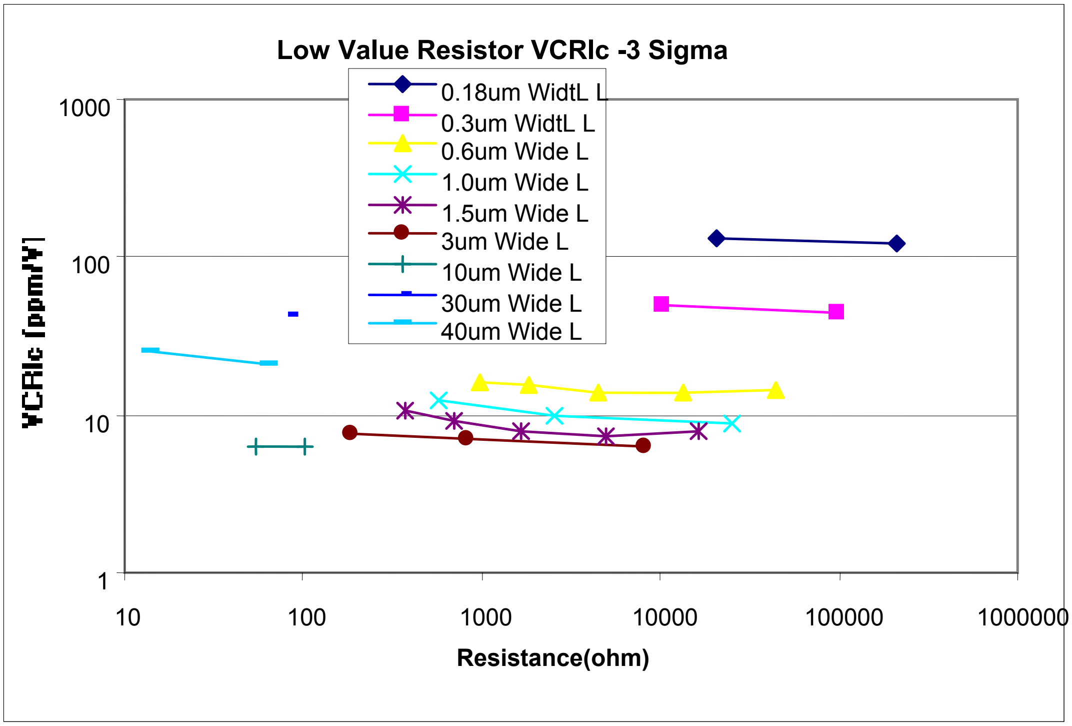
Low Value Poly Matched Resistors Without Dummies: Mean VCRlc (ppm/V) / Mean Resistance (Ohms)

VCRlc/R	2	4	10	30	100
0.18um WidtL L			-301.9 / 20,897		-283.6 / 206,810
0.3um WidtL L			-166.7 / 10,359		-160.4 / 99,556
0.6um Wide L	-75.4 / 983	-79.6 / 1,856	-83.4 / 4,491	-84.7 / 13,244	-85.4 / 43,848
1.0um Wide L	-58.0 / 565		-63.7 / 2,580		-65.2 / 25,165
1.5um Wide L	-49.3 / 370	-51.8 / 698	-53.9 / 1,678	-55.3 / 4,946	-55.7 / 16,369
3um Wide L	-41.2 / 182		-44.9 / 824		-45.9 / 8,022
10um Wide L	-34.7 / 54	-36.8 / 102			
30um Wide L			-25.9 / 83		
40um Wide L	-46.6 / 14		14.0 / 65		



Low Value Poly Matched Resistors Without Dummies: 3sigma VCRlc (ppm/V) / Mean Resistance (Ohms)

VCRlc/R	2	4	10	30	100
0.18um WidtL L			131.6 / 20,897		120.6 / 206,810
0.3um WidtL L			50.4 / 10,359		44.8 / 99,556
0.6um Wide L	16.3 / 983	15.2 / 1,856	14.0 / 4,491	14.1 / 13,244	14.2 / 43,848
1.0um Wide L	12.3 / 565		9.9 / 2,580		9.0 / 25,165
1.5um Wide L	10.5 / 370	9.2 / 698	7.8 / 1,678	7.2 / 4,946	8.0 / 16,369
3um Wide L	7.7 / 182		7.0 / 824		6.4 / 8,022
10um Wide L	6.2 / 54	6.2 / 102			
30um Wide L			41.9 / 83		
40um Wide L	25.1 / 14		21.3 / 65		

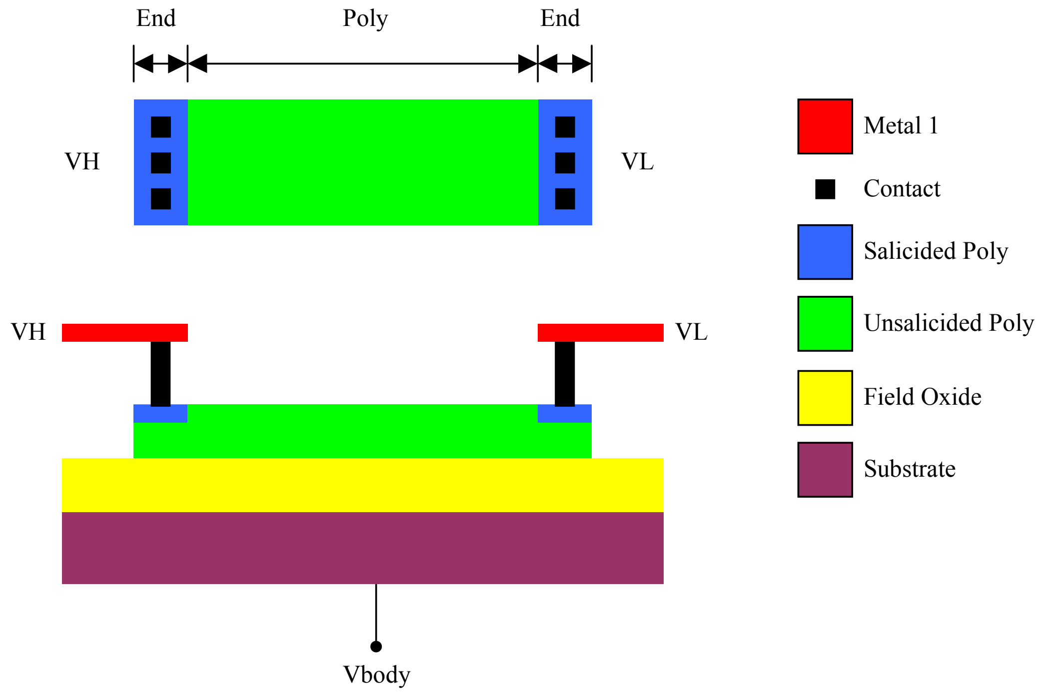


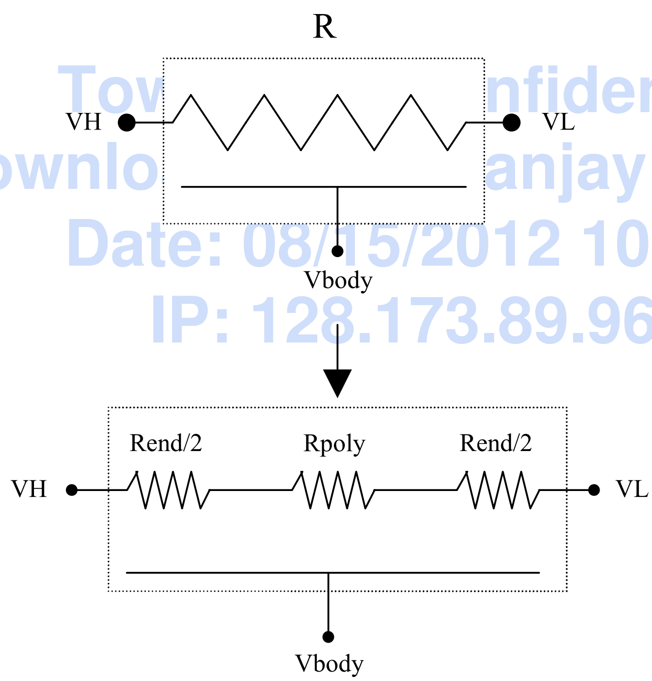
2. LV Resistor Models

2.1. LV Resistor Resistance Model

The model can be used for resistance, resistor tolerance, and resistor matching calculations.

The model describes the resistor with two components. The resistor is composed of a LV poly resistor in series with two end resistors.





The following equations are used to model the resistor:

$$R = Rpoly + Rend$$

$$Rpoly = Rs\frac{L}{W + \Delta W}$$

$$\mathrm{Rend} = \frac{\mathrm{Re}}{W + \Delta W}$$

$$R = Rs\frac{L}{W + \Delta W} + \frac{\mathrm{Re}}{W + \Delta W}$$

We have used an optimizer to fit this model to the resistance data. The optimization was based on minimizing the RMS error in the fit for all resistors.

Parameter	Value	Unit
Mean Rs	240	Ohm
Mean Re	63.8	Ohm - μm
Mean ΔW	-0.046	μm

2.1.1 LV Resistor Resistance Fit Error

The following table describes the ability of the model to fit the resistance data. The model fits all resistors to within 8.0% except 0.18um width resistors.

LV Matched Resistors: Mean Resistance Model Fit Error (%) / Mean Resistance (Ohms)

Delta Mean Resistance(Measured-Calculated)					
Width\Length	2	4	10	30	100
0.18um Wide			-14.5% / 21,445		-15.4% / 211,637
0.3um Wide			-7.7% / 10,468		-8.2% / 102,791
0.6um wide	0.2% / 976	-0.6% / 1,851	-1.0% / 4,474	-1.0% / 13,189	-0.8% / 43,626
1um Wide	1.0% / 562		0.3% / 2,566		0.3% / 25,057
1.5um Wide	1.0% / 369	0.8% / 696	0.8% / 1,674	0.8% / 4,934	1.0% / 16,314
3um Wide	0.7% / 182		1.0% / 822		1.5% / 7,991
10um Wide	-0.2% / 55	0.4% / 102			
30um Wide	-0.6% / 18		1.0% / 81	0.6% / 240	-0.3% / 802
40um Wide	-1.9% / 14		-5.5% / 65		

In order to determine the tolerances on Rs, Re, and ΔW; we have derived an equation which relates the standard deviations (σ) of the model parameters to the standard deviation of the resistance.

σ = standard deviation

σ^2 = variance

$$\sigma_R{}^2 = \sigma_{Rs}{}^2 \left[\frac{\delta R}{\delta Rs}\right]^2 + \sigma_{Re}{}^2 \left[\frac{\delta R}{\delta Re}\right]^2 + \sigma_{\Delta W}{}^2 \left[\frac{\delta R}{\delta \Delta W}\right]^2$$

$$\sigma_R{}^2 = \sigma_{Rs}{}^2 \frac{L^2}{(W+\Delta W)^2} + \sigma_{Re}{}^2 \frac{1}{(W+\Delta W)^2} + \sigma_{\Delta W}{}^2 \left[\frac{L \cdot Rs}{(W+\Delta W)^2} + \frac{Rend}{(W+\Delta W)^2}\right]^2$$

We have used an optimizer to fit this model to the 3 sigma resistance data. The optimization was based on minimizing the RMS error in the fit for all resistors.

Parameter	Value	Unit
3 Sigma Rs	23.3	Ohm
3 Sigma Re	28.7	Ohm - μm
3 Sigma ΔW	0.064	μm

The error relative to the 3sigma resistance is below 10% for most resistors
LV Matched Resistors: 3 Sigma **Fit Error** (%) / Mean Resistance (Ohms)

Delta 3Sigma (Measured-Calculated)					
Width\Length	2	4	10	30	100
0.18um Wide			-15.3% / 21,445		-16.6% / 211,637
0.3um Wide			-9.6% / 10,468		-9.6% / 102,791
0.6um wide	4.3% / 976	-1.9% / 1,851	-2.5% / 4,474	-0.1% / 13,189	-0.6% / 43,626
1um Wide	5.7% / 562		2.9% / 2,566		-1.6% / 25,057
1.5um Wide	-2.8% / 369	-6.5% / 696	-3.0% / 1,674	-0.1% / 4,934	2.3% / 16,314
3um Wide	-4.5% / 182		-3.6% / 822		1.5% / 7,991
10um Wide	-5.0% / 55	-3.3% / 102			
30um Wide	2.0% / 18		6.4% / 81	-1.4% / 240	-3.6% / 802
40um Wide	4.9% / 14		7.0% / 65		

2.1.2. Repeatability of Low Value Resistor Resistance

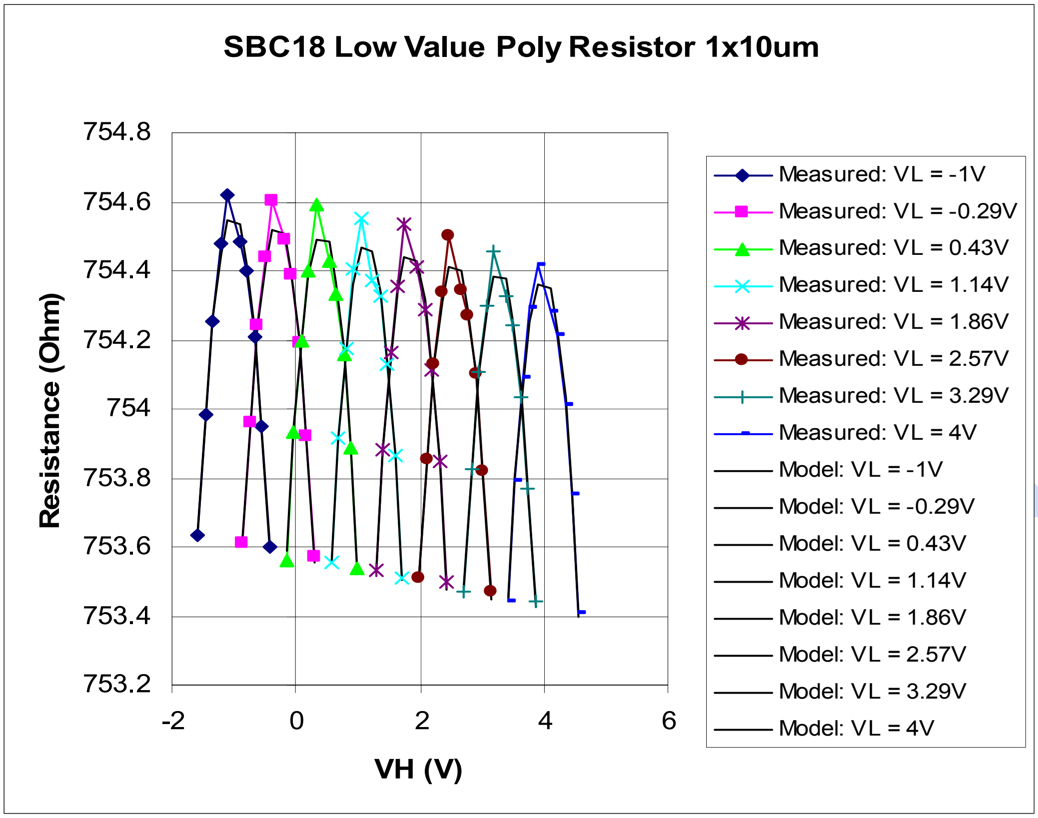
		Low Value Resistor		
		Rs	Rend	Delta W
Spec	Nom.	235	150	-0.03
	low	175		
	high	295		
K17133	Mean	240.8	66.0	-0.016
	1sigma	6.1	8.1	0.007
K17157	Mean	240.4	66.2	-0.063
	1sigma	5.7	10.1	0.004
K19225	Mean	243.7	66.7	-0.050
	1sigma	7.6	17.7	0.000
K19863	Mean	234.9	61.8	-0.030
	1sigma	3.5	6.2	0.006
K19225	Mean	232.8	63.0	-0.06
	1sigma	4.7	8.8	0.005

2.2. Low Value Resistor VCR Model

The following model has been used to fit the voltage coefficient of resistance:

$$R(VH, VL, Vbody) = Ro\left[VCRq(VH - VL)^2 + VCRld(VH - VL) + VCRlc\left(\frac{VH + VL}{2} - Vbody\right) + 1\right]$$

VCRq – quadratic differential mode voltage coefficient
VCRld – linear differential mode voltage coefficient
VCRlc – linear common mode voltage coefficient



The VCRq term appears to be caused primarily by the change in temperature due to ohmic heating. The source of the asymmetric VCRld term is still unknown. The VCRlc term appears to be due to accumulation or depletion of the bottom surface of the resistor. For the differential case, the resistor has a linear gradient of depletion along the length of the resistor; whereas, for the common mode case, the depletion is constant along the length of the resistor. If the common mode voltage coefficient is completely linear,the average depletion in the differential case is one half of the common mode case.
The chart gives an example of the VCR for a short resistor 1.5x4um measured and fitted resistance.
A characterization of the low value resistors in the SBC18 process has been completed. The measurement results for some parameters have been successfully modeled.

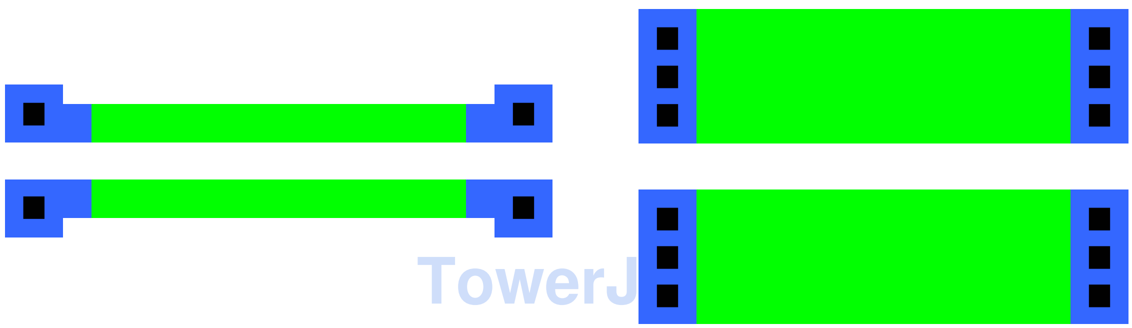
Appendix: Test Structure and Test Description

A. Test Structures

The GA577 SBC18 test chip was used for this characterization. This test chip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 4 modules devoted to LV resistor characterization on the GA577. The following table describes the resistor types and sizes available for characterization:

Matched Resistors



Matched Pairs Without Dummies:

Width\Length	2μm	4μm	10μm	30μm	100μm
0.18μm			X		X
0.3μm			X		X
0.6μm	X	X	X	X	X
1.0μm	X		X		X
1.5μm	X	X	X	X	X
3.0μm	X		X		X
10μm	X	X			
30μm	X		X	X	X
40μm	X		X		

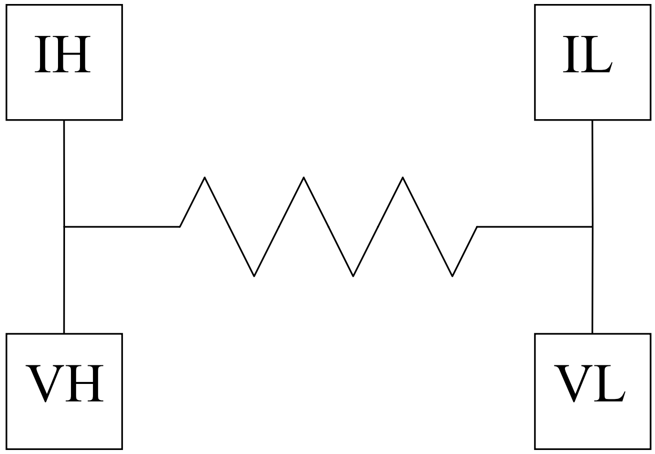


Figure 8: Resistor with Kelvin Pads

Since the resistance of the measurement system cables, probes, pads, and interconnect can degrade the accuracy of resistor measurements, all of the resistors are laid out with pads for kelvin measurements (figure 1).

The Kelvin measurement method requires that two pads be connected to each end of the resistor. The IH pad is used to force a current into the resistor, and the IL pad is usually connected to a grounded ammeter in order to measure the current flow out of the resistor. The potentials at the IH current source and IL current meter will be different from the potentials at the resistor ends due to the effect of parasitic series resistance. By adding the VH and VL pads, we are able to accurately measure the potential at the resistor ends. Since no current flows through the VH and VL pads, the parasitic series resistances do not affect the measurement. The following equation is used to calculate the resistance:

$$R = -\frac{(VH - VL)}{IL}$$

In order to minimize the number of test modules, and thus the chip area, we have used the layout strategy shown in figure 2. This configuration allows kelvin measurements of all of the resistors, but it does not support simultaneous measurements for matching.

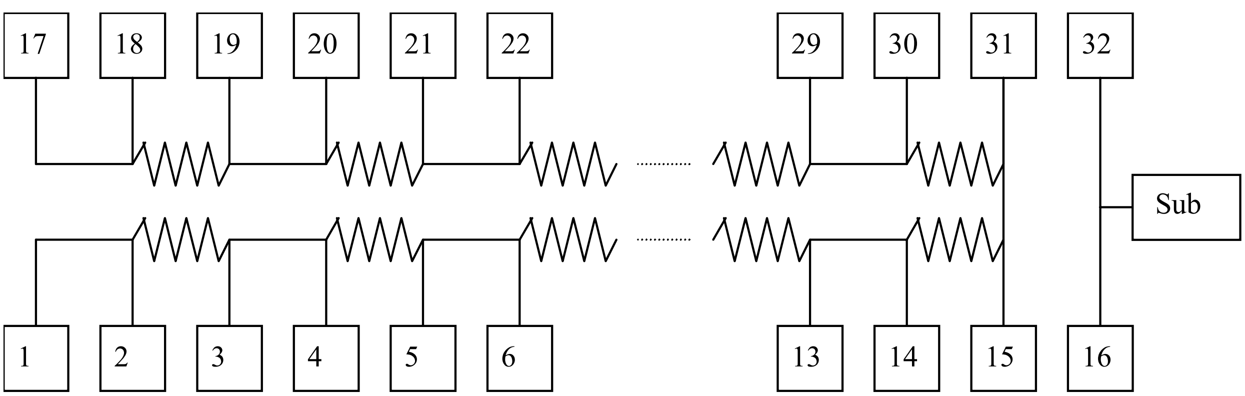


Figure 9: Resistor Matching Module Configuration

B. Test Description

B.1. Resistance and Resistor Matching

In order to simplify the data analysis, the resistance is reported only for the first resistor in the pair, and the test on the second resistor reports the resistance difference between the two resistors in percent.

$$\Delta R = 100 * \frac{R2 - R1}{R1}$$

B.2. Temperature Coefficient of Resistance

TCR testing is performed by changing the chuck temperature on the Reedholm tester, and then running the resistance and resistor matching test a second time.

$$TCR(\Delta T, Tref) = \frac{R(\Delta T) - R(Tref)}{R(Tref) \cdot \Delta T}$$

B.3. Voltage Coefficient of Resistance

The Analog Tester is a custom built tester intended for high resolution measurements which the Reedholm cannot support. The analog tester is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. All of the cabling between the HP4156, switch matrix, and probe card is guarded through the use of triaxial cable. The HP4156 is composed of 4 SMUs (Source Measure Units), 2 VSUs (Voltage Source Units), and 2 VMUs (Voltage Measurement Units). The SMUs are used to simultaneously force and measure voltages and currents. The measurement resolution of the HP4156 SMUs is approximately 6 digits. The Analog Tester is controlled by a PC using a Visual Basic test program. The test program (WaferTest) is designed to provide a relatively open framework for implementing custom analog tests, and it places the measurement results directly into an Excel spreadsheet.

The VCR test is performed on the Analog Tester, and measures the resistance of a single resistor in all bias regions. The test reports the measured resistance, and model extraction takes place in Excel during post processing. The setup for this test consists of the two resistor terminals (VH and VL) and the body terminal (Vbody), as shown in figure B1.1. In a circuit, the allowable bias range for resistors ranges from ground to VDD for both the VH and VL terminals with the substrate always grounded. This bias range is the region inside the box depicted in figure B.1.2a. The zero differential voltage line represents the region in which resistance cannot be measured. For shorter resistors, the maximum differential voltage is restricted by the maximum current density specification in order to prevent damage. The bias range for shorter resistors is depicted in figure B.1.2b.

We have chosen to use a bias scheme shown in figure B.1.3, in which the VL terminal is always held at ground. The VH terminal is used to provide a differential bias, and the Vbody terminal is used to provide a common mode bias. This configuration simplifies biasing, as the same differential bias range can be used for each sweep. In addition, the linearity requirements on the SMU measuring current are reduced, as the current is measured through the VL terminal which is always grounded. As no measurements can be made for small differential voltages, a minimum differential voltage is specified.

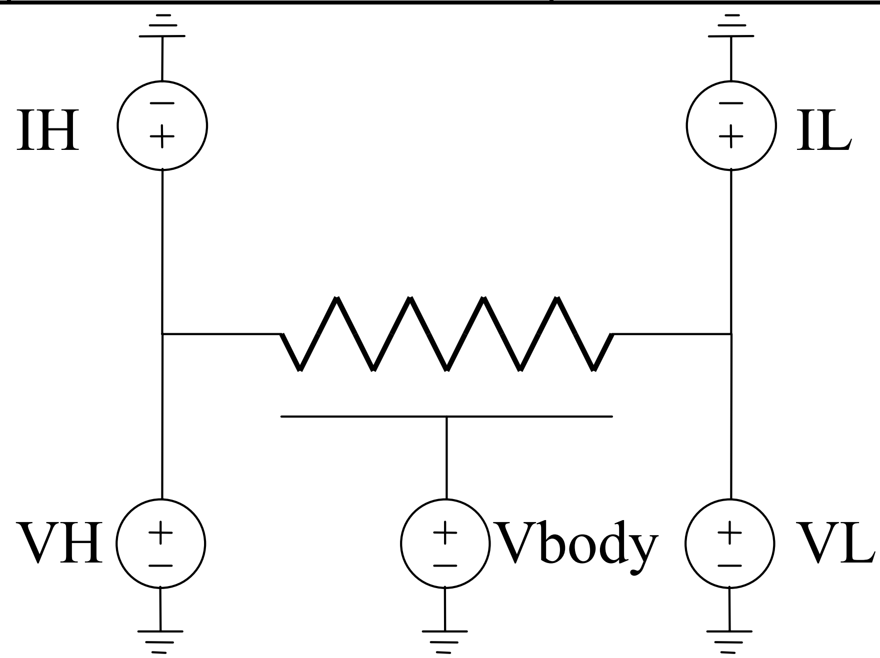


Figure B.1.1: VCR Measurement Configuration

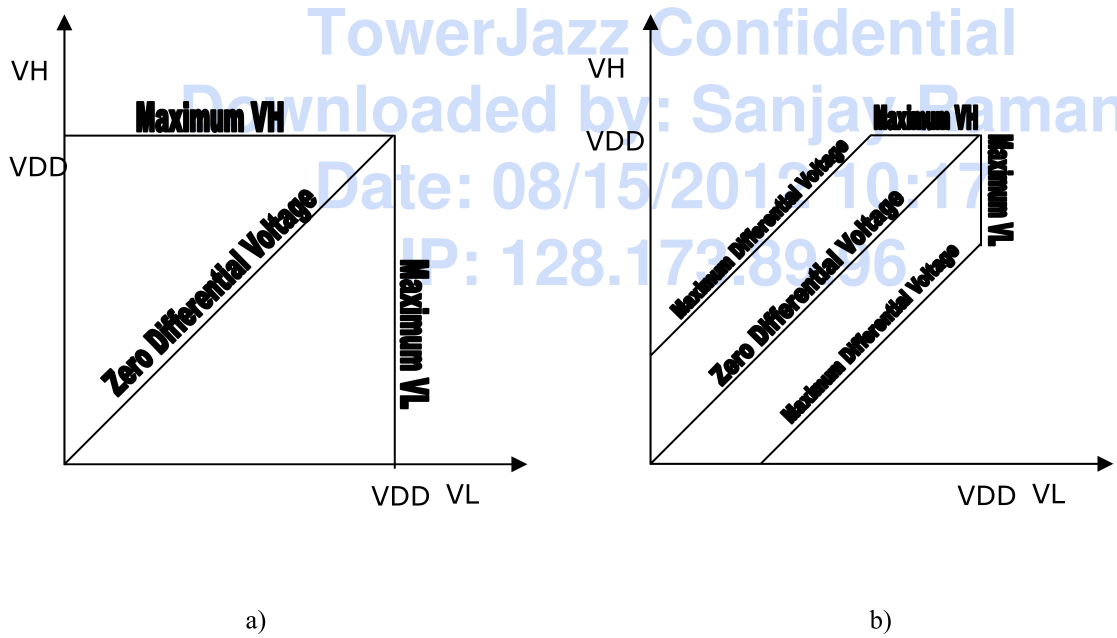
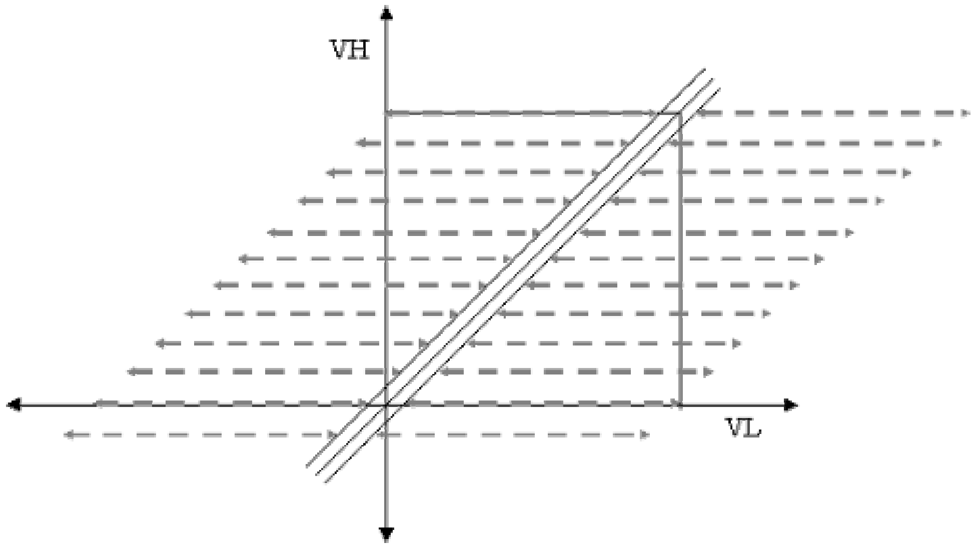


Fig B.1.2. a) Long Resistor VCR Bias Range, b) Short Resistor Bias Range



B.1.3. Long Resistor VCR Bias Sweep

C. Test Conditions

The following test conditions were used for this characterization:

C.1. Resistance and Resistor Matching

In order to maximize the accuracy of the resistance test, we have chosen the current so that the voltage drop over resistors is around 100mV in the four terminal set up.

C.2. Temperature Coefficient of Resistance

The LV resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 25C and 125C.

C.3. Voltage Coefficient of Resistance

The measurement of VCR is complicated by the large ranges of resistances, voltages, and currents involved. The resistances to be measured, and the linear and quadratic voltage coefficients to be extracted, can vary by as much as 6 orders of magnitude over the space of available resistor widths and lengths. If the voltages or currents become too small, the HP4156 will not have sufficient precision to extract the VCR coefficients. There are problems measuring short resistors, as the voltage resolution of the HP4156 drops rapidly as the differential voltage drops below 0.3V. For short resistors, the maximum current density is often reached or exceeded at 0.5V. For very high value resistors, the current can be too low for the HP4156 to measure with high precision.

The test is implemented with node IH connected to a SMU, which is configured to force voltage. The VH and VL nodes are connected to VMUs (the VMUs cannot be used in differential mode, as this mode is limited to 2V). The IL node is connected to a SMU, which is set to force 0 volts, and measure the current. The Body node is connected to a VSU. The test setup provides for connection inputs (IH, VH, VL, IL, Body), resistor information inputs (Width, Length), and bias conditions (ConstDeltaV, SlopeDeltaV, NumDeltaV, MinDeltaV, MaxDeltaV, StartVb, StopVb, NumVb).

The following steps are performed in order to measure the VCR:
Determine the VH bias range based on the resistor length. The maximum VH is determined by the lesser of (MinDeltaV + SlopeDeltaV * Length) or MaxDeltaV.
Measure the resistance as a function of VH and Vbody.
Place the measured resistance, VH, and VL into Excel.

The VCR model parameters (Ro, VCRq, VCRld, and VCRlc) are extracted by optimization in Excel.

The following test conditions were used for VCR characterization:

Parameter	Value
ConstDeltaV	0.3
SlopeDeltaV	0.07
NumDeltaV	10
MinDeltaV	0.1
MaxDeltaV	5
StartVb	1
StopVb	-4
NumVb	8

9. Silicided Poly Resistor Characterization

Table of Contents

Summary

A characterization of the salicided resistors in the SBC18 process has been performed. The results for the following tests are presented: resistance, resistor matching, TCR (Temperature Coefficient of Resistance) and VCR (Voltage Coefficient of Resistance). The test structures, test procedures, and test conditions are described in the appendix. Although the characterization was carried out on SBC18QTD GA577 test chip, it is applicable to salicided resistors available in all sbc18 process variants.

1. Measurement Results

The characterization was performed on wafers processed in the SBC18 process using the GA577 engineering test chip. For resistance, matching and TCR measurement, 24 dies from wafers from following five lots were tested: K17133 wf.16 to 22, K17157 wf20 to 25 K19225 wf.16 to 20, K19863 wf16 to 20 and K19920wf.16,18,19,21,22. Since the goal of this characterization is to measure the standard deviation of the difference between two devices, a relatively large sample size is tested to obtain useful results.

For measurements involving a large number of samples, it is almost inevitable that there will be a few “bad points” which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these “bad points,” it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3sigma limits.

1.1. Salicide Resistance and Resistor Matching

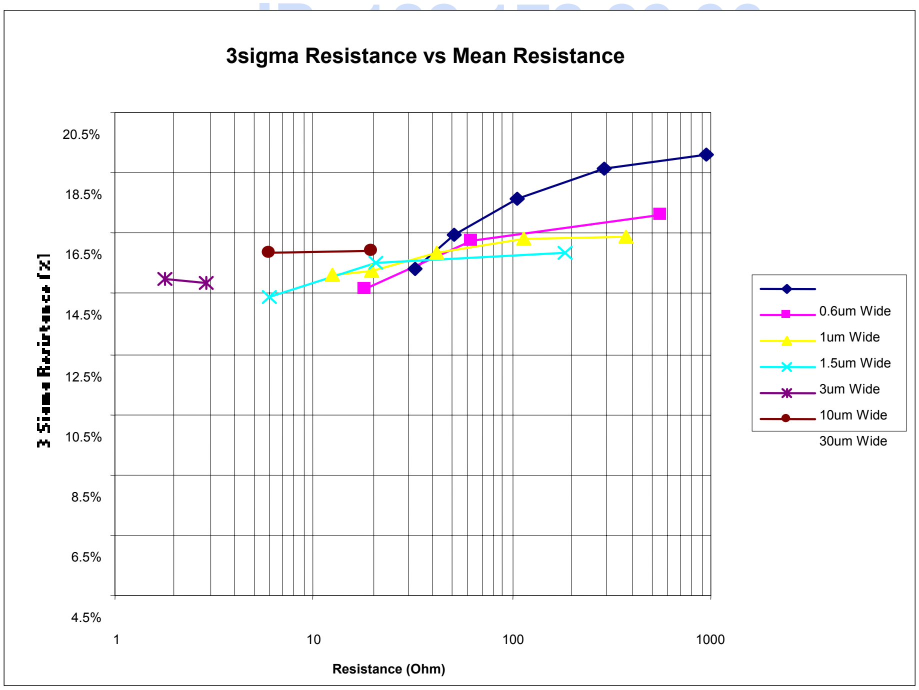
Salicide resistor 3 Sigma Resistance

The following tables list both the mean and 3 sigma of the measured resistance for each test structure:

3 Sigma Resistance (%) = 100 * 3 Sigma Resistance / Mean Resistance

Salicide resistors: 3 Sigma Resistance (%) / Mean Resistance (Ohms)

3 Sigma Resistance(%) / Mean Resistance(ohm)					
Width\Length	2	4	10	30	100
0.6um wide	15.4% / 32.51	16.4% / 51.36	17.6% / 106.75	18.6% / 292.29	19.1% / 942.28
1um Wide	14.7% / 18.06		16.2% / 62.12		17.1% / 559.04
1.5um Wide	15.1% / 12.43	15.2% / 19.69	15.9% / 41.59	16.3% / 114.47	16.4% / 370.13
3um Wide	14.4% / 6.01		15.5% / 20.70		15.8% / 184.01
10um Wide	15.0% / 1.77	14.8% / 2.86			
30um Wide				15.9% / 6.05	15.9% / 19.76

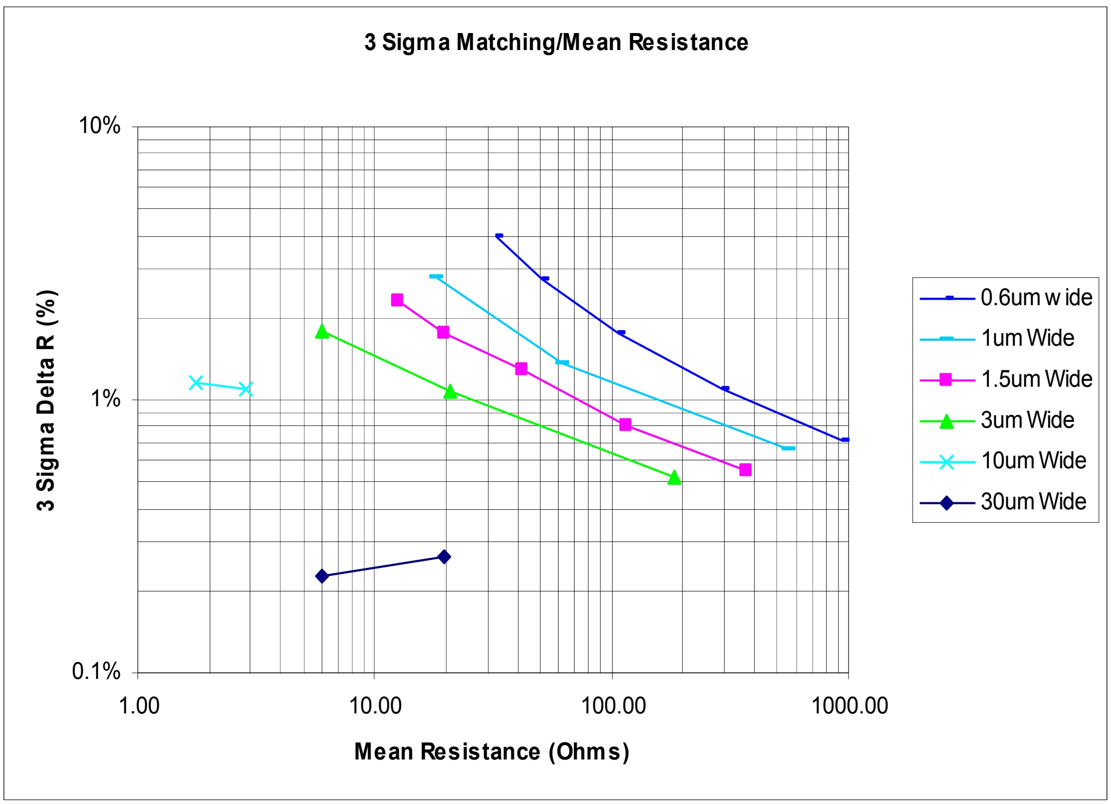


Salicide resistor 3 Sigma Matching of Resistor Pairs

The following tables list the 3 sigma matching of resistance for each resistor pair:

Salicide Matched Resistors: 3 Sigma Matching (%) / Mean Resistance (Ohms)

Measured 3 Sigma Matching					
Width	2	4	10	30	100
0.6um wide	4.0% / 33	2.8% / 51	1.8% / 107	1.1% / 292	0.7% / 942
1um Wide	2.8% / 18		1.4% / 62		0.7% / 559
1.5um Wide	2.3% / 12	1.8% / 20	1.3% / 42	0.8% / 114	0.5% / 370
3um Wide	1.8% / 6		1.1% / 21		0.5% / 184
10um Wide	1.2% / 2	1.1% / 3			
30um Wide				0.2% / 6	0.3% / 20



1.2. Salicide resistor Temperature Coefficient

The Salicide resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 25°C and 125°C. The following table lists both the mean and 3 sigma of the measured TCR:

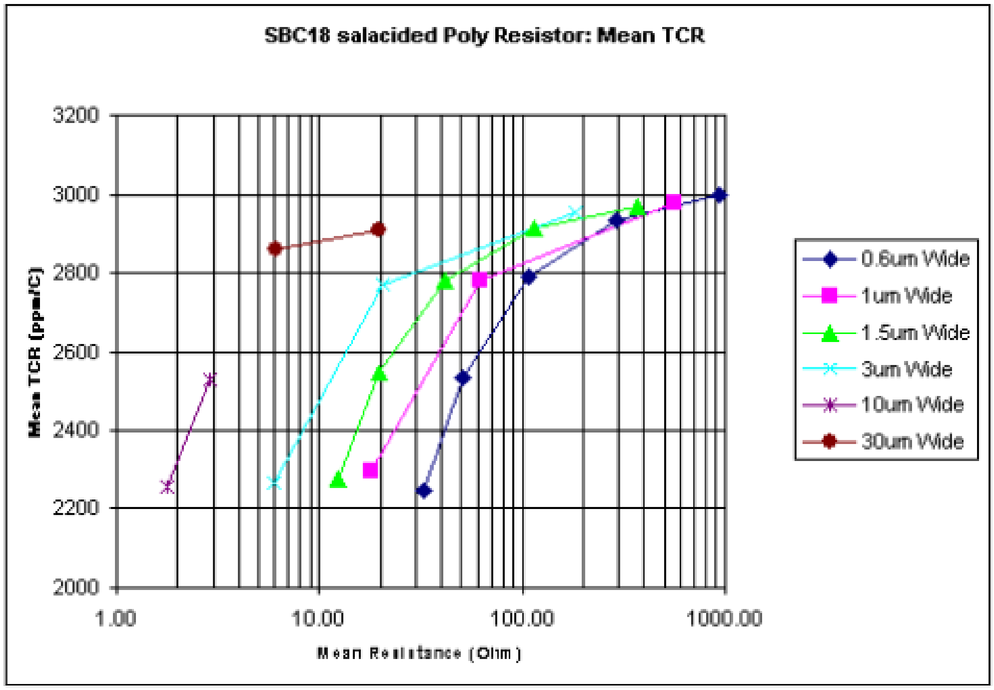
TCR= (R at 125C – R at 25C)/R at 25C x 100%

Salicide resistors: Mean TCR (ppm/C) / Mean Resistance (Ohms)

Mean Tempco/Mean Resistance					
Width\Length	2	4	10	30	100
0.6	2,244 / 33	2,529 / 51	2,792 / 107	2,934 / 292	2,996 / 942
1	2,296 / 18		2,783 / 62		2,979 / 559
1.5	2,274 / 12	2,546 / 20	2,781 / 42	2,916 / 114	2,971 / 370
3	2,264 / 6		2,773 / 21		2,955 / 184
10	2,254 / 2	2,528 / 3			
30				2,859 / 6	2,912 / 20

Salicide resistors: 3 Sigma TCR (ppm/C) / Mean Resistance (Ohms)

3 Sigma Tempco/Mean Resistance					
Width\Length	2	4	10	30	100
0.6	175 / 33	162 / 51	176 / 107	197 / 292	175 / 942
1	176 / 18		198 / 62		177 / 559
1.5	184 / 12	156 / 20	178 / 42	190 / 114	193 / 370
3	187 / 6		197 / 21		185 / 184
10	165 / 2	158 / 3			
30				197 / 6	201 / 20



1.3. Salicide resistor Voltage Coefficient(VCR)

The voltage coefficient of resistance (VCR) has been measured for SBC18 salicide resistors. The following three terminal resistor voltage coefficient model has been used to extract voltage coefficients:

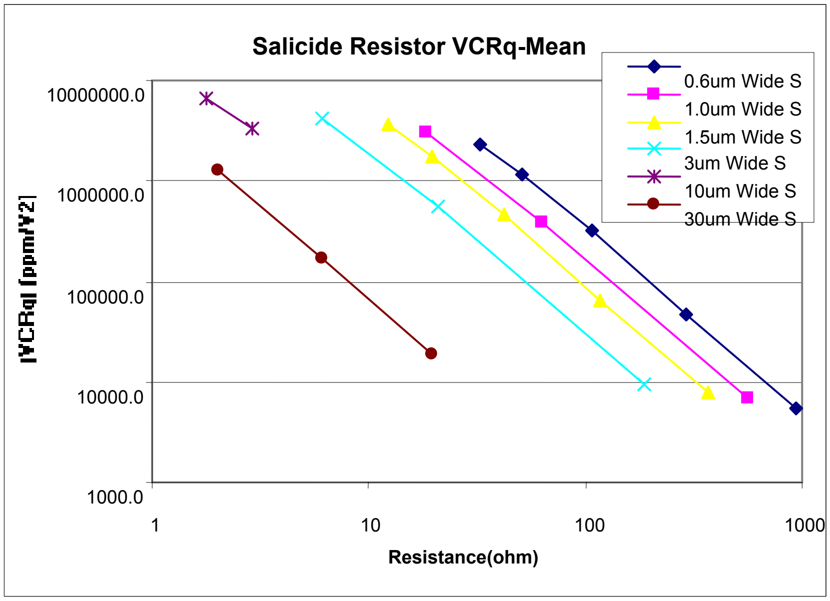
$$R(VH, VL, Vbody) = Ro\left[VCRq(VH - VL)^2 + VCRld(VH - VL) + VCRlc\left(\frac{VH + VL}{2} - Vbody\right) + 1\right]$$

VCRq – quadratic differential mode voltage coefficient
VCRld – linear differential mode voltage coefficient
VCRlc – linear common mode voltage coefficient
Following wafers are used for VCR characterization: K17133/wf20/46sites, K17157/wf20/46sites, K19225/wf19&20/24sites and K19863/wf19&20/24sites. The number of total sites is 188 per resistor.

Salicide resistor VCRq

Salicide Poly Matched Resistors Without Dummies: Mean VCRq (ppm/V^2) / Mean Resistance (Ohms)

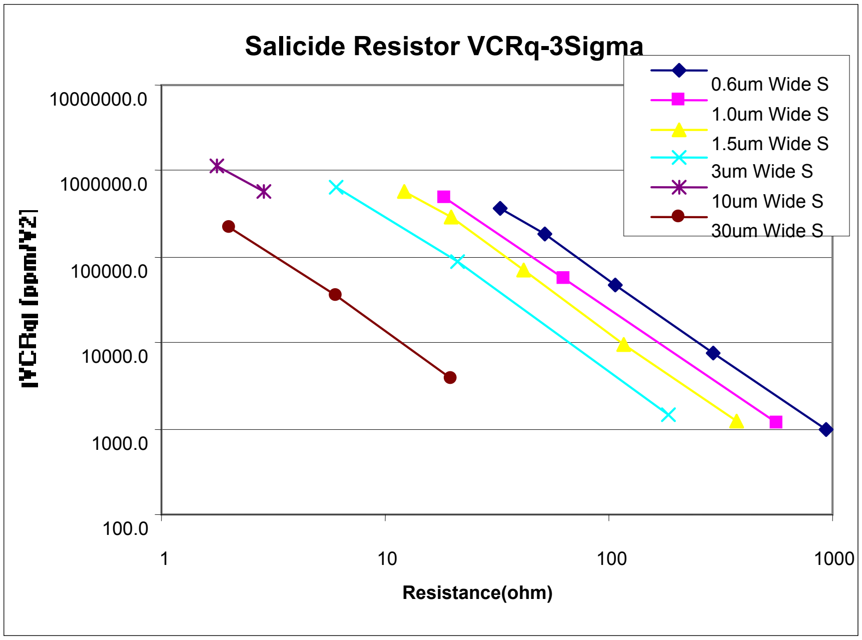
Width/Length	2	4	10	30	100
0.6um Wide S	2,277,884.4 / 32	1,162,895.4 / 51	317,361.4 / 107	47,213.0 / 294	5,433.5 / 941
1.0um Wide S	3,058,155.0 / 18		391,917.3 / 63		6,760.1 / 560
1.5um Wide S	3,573,378.1 / 12	1,778,659.2 / 20	466,074.6 / 42	66,155.2 / 116	7,772.0 / 371
3um Wide S	4,247,392.6 / 6		567,871.0 / 21		9,514.4 / 185
10um Wide S	6,477,879.0 / 2	3,323,241.4 / 3			
30um Wide S			1,286,560.4 / 2	171,418.8 / 6	18,818.8 / 20



Salicide Matched Resistors Without Dummies: 3sigma VCRq (ppm/V^2) / Mean Resistance (Ohms)

Width/Length	2	4	10	30	100
0.6um Wide S	376,823.0 / 32	181,009.1 / 51	48,270.1 / 107	7,439.2 / 294	964.8 / 941
1.0um Wide S	478,262.9 / 18		55,910.3 / 63		1,129.2 / 560
1.5um Wide S	590,673.4 / 12	286,389.4 / 20	71,981.0 / 42	9,760.5 / 116	1,254.6 / 371
3um Wide S	660,985.0 / 6		90,518.6 / 21		1,489.6 / 185
10um Wide S	1,126,207.2 / 2	582,416.3 / 3			
30um Wide S			220,601.5 / 2	35,896.4 / 6	3,940.2 / 20

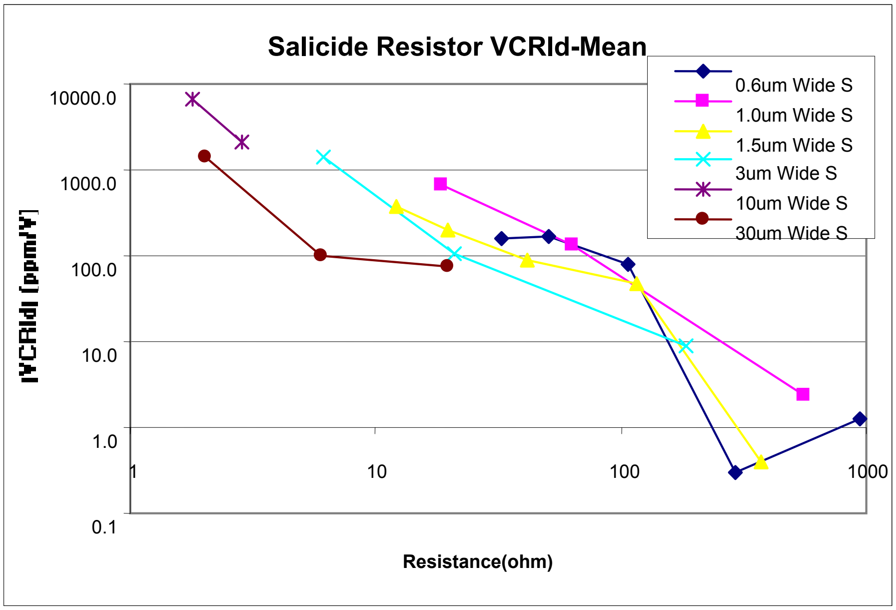
1.1.1.4



Salicide resistor VCRld

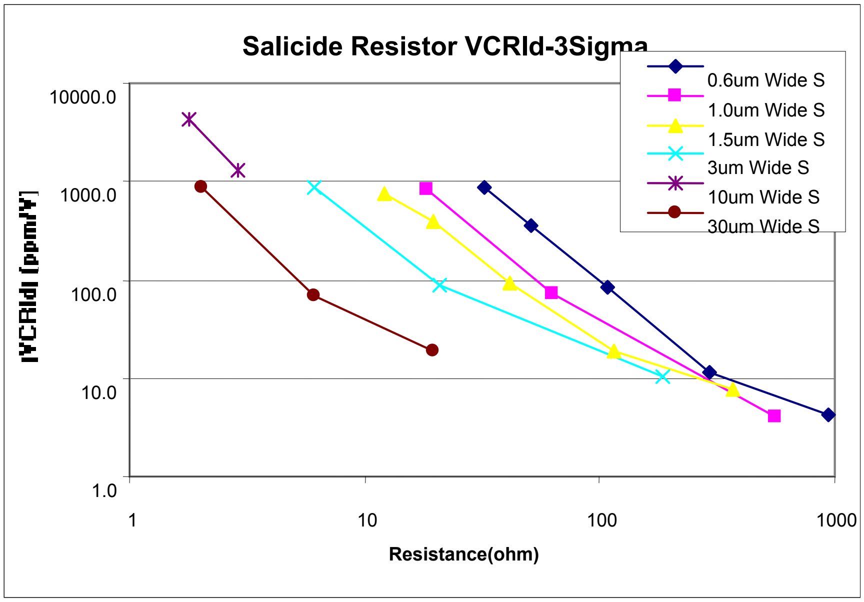
Salicide Matched Resistors Without Dummies: Mean VCRld (ppm/V) / Mean Resistance (Ohms)

WidtS/LengtS	2	4	10	30	100
0.6um Wide S	-158.7 / 32	-167.6 / 51	-80.7 / 107	-0.3 / 294	-1.2 / 941
1.0um Wide S	652.9 / 18		-131.7 / 63		-2.4 / 560
1.5um Wide S	-383.0 / 12	-195.3 / 20	-89.3 / 42	-46.6 / 116	-0.4 / 371
3um Wide S	-1,426.4 / 6		-107.3 / 21		-9.0 / 185
10um Wide S	-6,727.9 / 2	-2,074.6 / 3			
30um Wide S			-1,395.6 / 2	-101.9 / 6	-74.0 / 20



Salicide Matched Resistors Without Dummies: 3sigma VCRld (ppm/V) / Mean Resistance (Ohms)

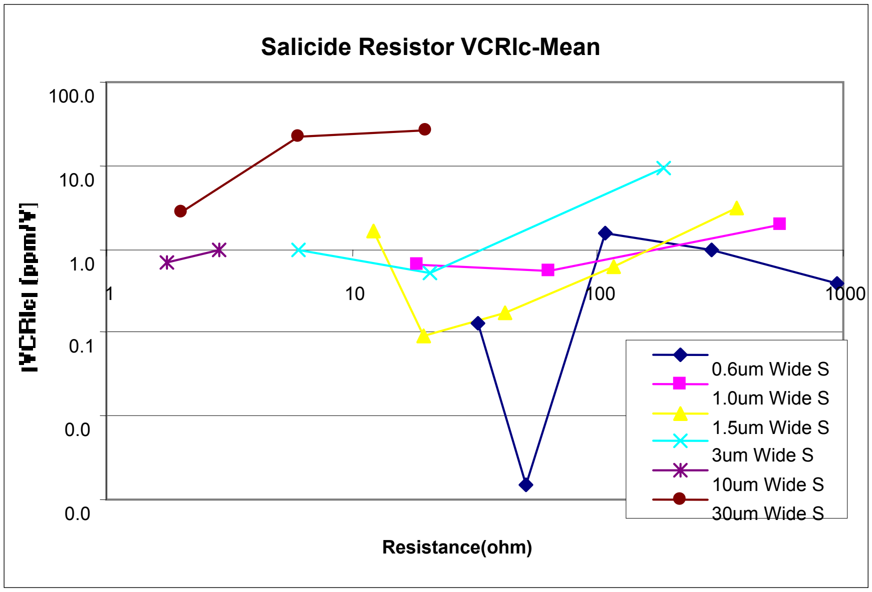
Width/Length	1	2	4	10	20
0.6um Wide S	877.6 / 32	347.5 / 51	85.4 / 107	11.4 / 294	4.2 / 941
1.0um Wide S	810.8 / 18		73.0 / 63		4.0 / 560
1.5um Wide S	762.8 / 12	395.0 / 20	91.1 / 42	18.8 / 116	7.8 / 371
3um Wide S	877.5 / 6		89.3 / 21		10.3 / 185
10um Wide S	4,240.9 / 2	1,302.4 / 3			
30um Wide S			866.1 / 2	69.6 / 6	18.7 / 20



Salicide resistor VCRlc

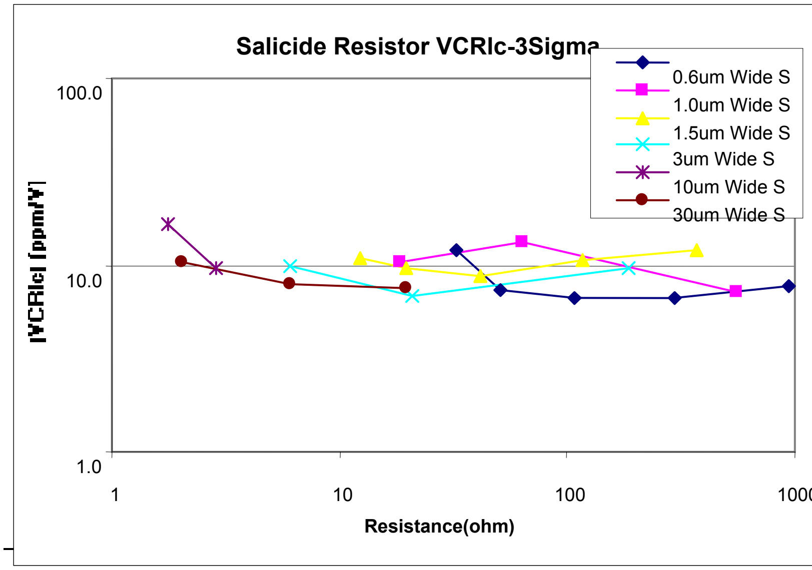
Salicide Matched Resistors Without Dummies: Mean VCRlc (ppm/V) / Mean Resistance (Ohms)

Width/Length	1	2	4	10	20
0.6um Wide S	0.1 / 32	0.0 / 51	-1.5 / 107	-1.0 / 294	-0.4 / 941
1.0um Wide S	-0.6 / 18		0.5 / 63		2.0 / 560
1.5um Wide S	1.7 / 12	-0.1 / 20	-0.2 / 42	0.6 / 116	3.2 / 371
3um Wide S	1.0 / 6		0.5 / 21		9.4 / 185
10um Wide S	0.7 / 2	1.0 / 3			
30um Wide S			2.7 / 2	22.1 / 6	25.8 / 20



Salicide Matched Resistors Without Dummies: 3sigma VCRlc (ppm/V) / Mean Resistance (Ohms)

Width/Length	2	4	10	30	100
0.6um Wide S	11.9 / 32	7.3 / 51	6.7 / 107	6.7 / 294	7.7 / 941
1.0um Wide S	10.4 / 18		13.2 / 63		7.2 / 560
1.5um Wide S	11.0 / 12	9.6 / 20	8.6 / 42	10.5 / 116	11.9 / 371
3um Wide S	10.0 / 6		6.7 / 21		9.7 / 185
10um Wide S	16.5 / 2	9.7 / 3			
30um Wide S			10.3 / 2	7.9 / 6	7.5 / 20



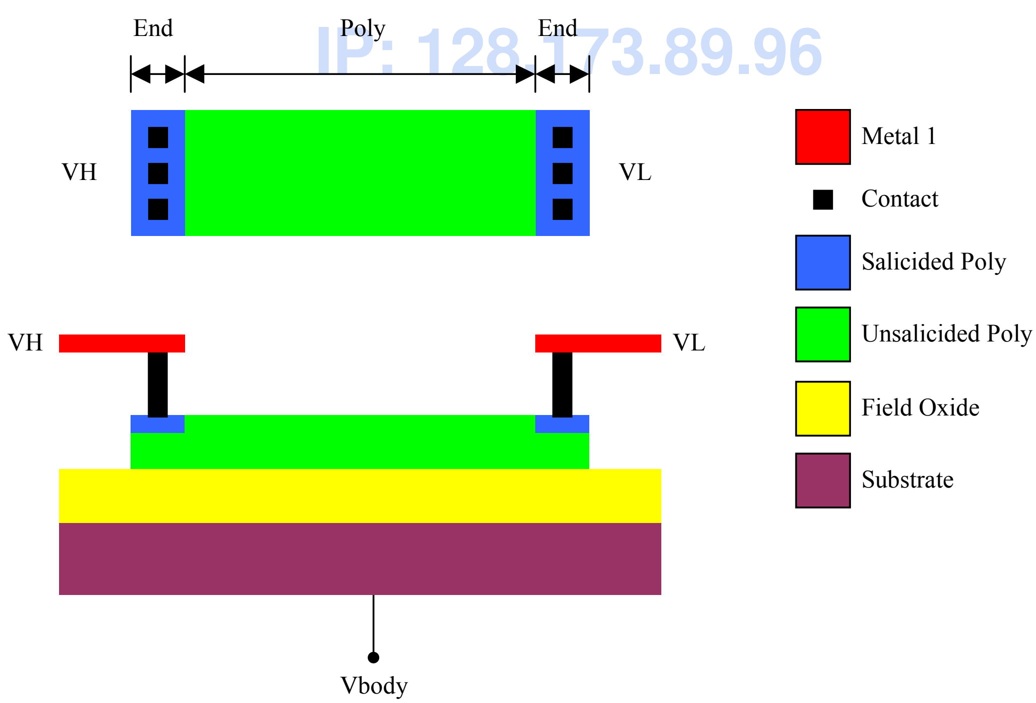
1.1.1.5

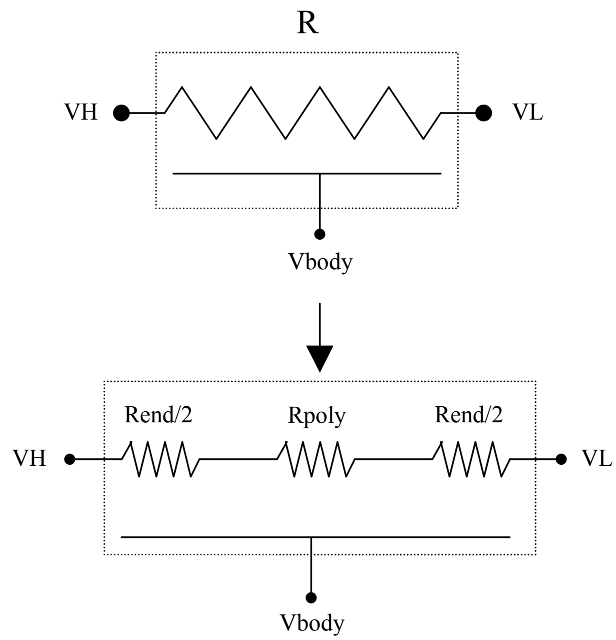
2. Salicide Resistor Models

2.1. Salicide resistor Resistance Model

The model can be used for resistance, resistor tolerance, and resistor matching calculations.

The model describes the resistor with two components. The resistor is composed of a salicide resistor in series with two end resistors.





The following equations are used to model the resistor:

$$R = Rpoly + Rend$$

$$Rpoly = Rs\frac{L}{W + \Delta W}$$

$$Rend = \frac{Re}{W + \Delta W}$$

$$R = Rs\frac{L}{W + \Delta W} + \frac{Re}{W + \Delta W}$$

We have used an optimizer to fit this model to the resistance data. The optimization was based on minimizing the RMS error in the fit for all resistors.

Parameter	Value	Unit
Mean Rs	5.50	Ohm
Mean Re	7.12	Ohm - μm
Mean ΔW	-0.017	μm

2.1.1 Salicide resistor Resistance Fit Error

The following table describes the ability of the model to fit the resistance data. The model fits all resistors to within 8.0% except 0.18um width resistors.

SalicideMatched Resistors: Mean Resistance Model Fit Error (%) / Mean Resistance (Ohms)

Delta Mean Resistance			

Width\Length	2	4	10	30	100
0.6um wide	-4.4% / 33	-2.7% / 51	-0.2% / 107	1.0% / 292	1.4% / 942
1um Wide	2.0% / 18		1.7% / 62		1.4% / 559
1.5um Wide	-1.7% / 12	-0.3% / 20	0.7% / 42	1.4% / 114	1.5% / 370
3um Wide	1.0% / 6		0.6% / 21		1.5% / 184
10um Wide	2.6% / 2	2.0% / 3			
30um Wide				-5.1% / 6	-6.0% / 20

In order to determine the tolerances on Rs, Re, and ΔW; we have derived an equation which relates the standard deviations (σ) of the model parameters to the standard deviation of the resistance.

σ = standard deviation

σ^2 = variance

$$\sigma_R^{\,2} = \sigma_{Rs}^{\,2}\left[\frac{\delta R}{\delta Rs}\right]^2 + \sigma_{Re}^{\,2}\left[\frac{\delta R}{\delta Re}\right]^2 + \sigma_{\Delta W}^{\,2}\left[\frac{\delta R}{\delta \Delta W}\right]^2$$

$$\sigma_R^{\,2} = \sigma_{Rs}^{\,2}\frac{L^2}{(W+\Delta W)^2} + \sigma_{Re}^{\,2}\frac{1}{(W+\Delta W)^2} + \sigma_{\Delta W}^{\,2}\left[\frac{L\cdot Rs}{(W+\Delta W)^2} + \frac{Rend}{(W+\Delta W)^2}\right]^2$$

We have used an optimizer to fit this model to the 3 sigma resistance data. The optimization was based on minimizing the RMS error in the fit for all resistors.

Parameter	Value	Unit
3 Sigma Rs	0.92	Ohm
3 Sigma Re	1.83	Ohm - μm
3 Sigma ΔW	0.049	μm

The error relative to the 3sigma resistance is below 10% for most resistors except 0.18um width
HV Matched Resistors: 3 Sigma **Fit Error** (%) / Mean Resistance (Ohms)

Delta 3 Sigma Resistance/Mean					
Width\Length	2	4	10	30	100
0.6um wide	3.5% / 33	-2.5% / 51	-1.9% / 107	-1.4% / 292	-1.2% / 942
1um Wide	5.5% / 18		-0.1% / 62		2.4% / 559
1.5um Wide	-4.3% /	-4.9% /	-1.6% / 42	2.4% / 114	4.7% / 370

	12	20			
3um Wide	1.4% / 6		-1.3% / 21		6.9% / 184
10um Wide	-1.7% / 2	-2.7% / 3			
30um Wide				-3.6% / 6	-2.1% / 20

2.1.2. Repeatability of Salicide Resistor Resistance

		Salicide Resistor		
		Rs	Rend	Delta W
Spec	Nom.	5.95	12.7	0.04
	low	4.46		
	high	7.44		
K17133	Mean	5.30	7.58	0.0052
	1sigma	0.09	0.30	0.004
K17157	Mean	5.62	7.11	-0.0466
	1sigma	0.17	0.38	0.0016
K19225	Mean	5.32	6.63	-0.0194
	1sigma	0.24	0.28	0.0000
K19863	Mean	5.96	7.56	-0.0018
	1sigma	0.15	0.52	0.000
K19920	Mean	5.36	6.59	-0.024
	1sigma	0.14	0.30	0.005

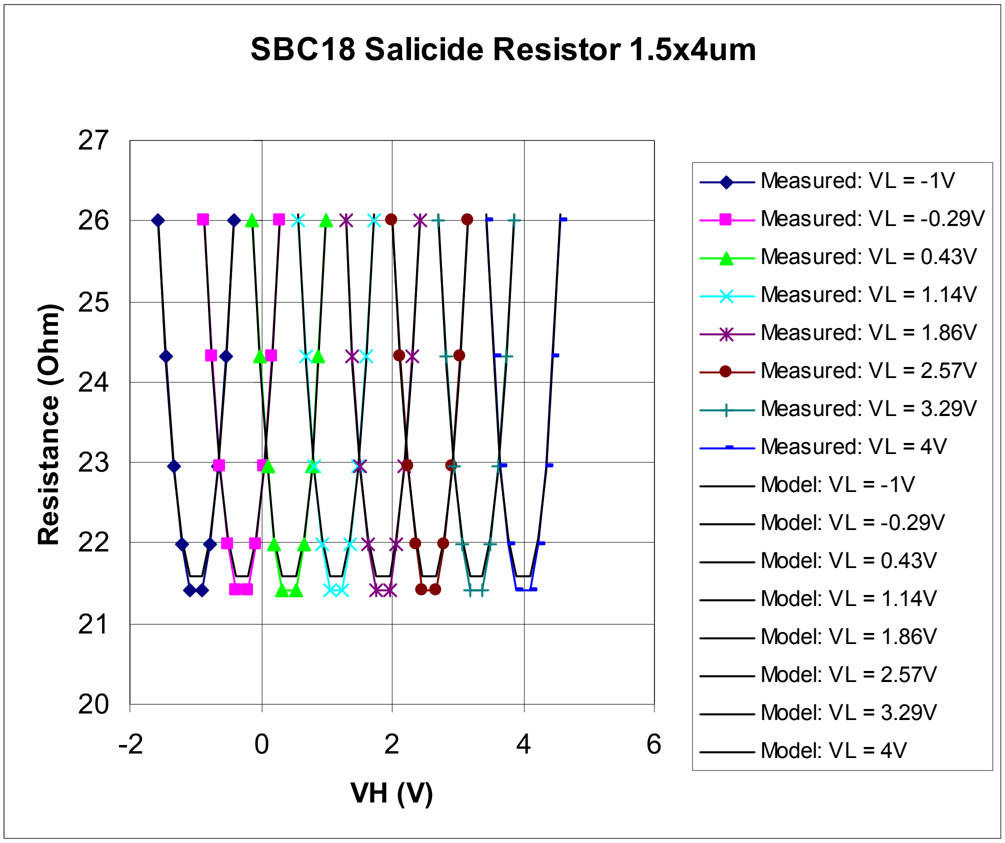
2.2. Salicide resistor VCR Model

The following model has been used to fit the voltage coefficient of resistance:

$$R(VH, VL, Vbody) = Ro\left[VCRq(VH - VL)^2 + VCRld(VH - VL) + VCRlc\left(\frac{VH + VL}{2} - Vbody\right) + 1\right]$$

VCRq – quadratic differential mode voltage coefficient
VCRld – linear differential mode voltage coefficient
VCRlc – linear common mode voltage coefficient

The VCRq term appears to be caused primarily by the change in temperature due to ohmic heating. The source of the asymmetric VCRld term is still unknown. The VCRlc term appears to be due to accumulation or depletion of the bottom surface of the resistor. For the differential case, the resistor has a linear gradient of depletion along the length of the resistor; whereas, for the common mode case, the depletion is constant along the length of the resistor. If the common mode voltage coefficient is completely linear, the average depletion in the differential case is one half of the common mode case.
The following chart gives an example of the VCR for a short resistor:



SBC18 Salicide Resistor 1.5x4um
Resistance (Ohm)
27
26
25
24
23
22
21
20
-2
0
2
4
6
VH (V)
Measured: VL = -1V
Measured: VL = -0.29V
Measured: VL = 0.43V
Measured: VL = 1.14V
Measured: VL = 1.86V
Measured: VL = 2.57V
Measured: VL = 3.29V
Measured: VL = 4V
Model: VL = -1V
Model: VL = -0.29V
Model: VL = 0.43V
Model: VL = 1.14V
Model: VL = 1.86V
Model: VL = 2.57V
Model: VL = 3.29V
Model: VL = 4V

A characterization of the salicide resistors in the SBC18 process has been completed. The measurement results for some parameters have been successfully modeled.

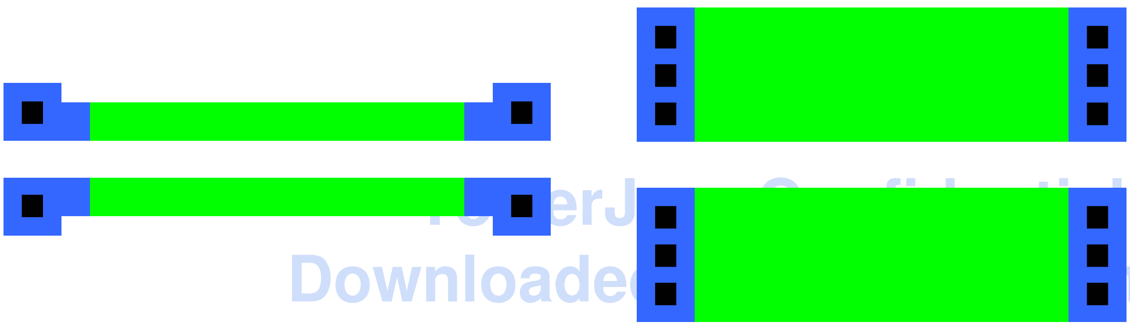
Appendix: Test Structure and Test Description

A. Test Structures

The GA577 SBC18 test chip was used for this characterization. This test chip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 4 modules devoted to Salicide resistor characterization on the GA577. The following table describes the resistor types and sizes available for characterization:

Matched Resistors



Matched Pairs Without Dummies:

Width\Length	2µm	4µm	10µm	30µm	100µm
0.6µm	X	X	X	X	X
1.0µm	X		X		X
1.5µm	X	X	X	X	X
3.0µm	X		X		X
10µm	X	X			
30µm				X	X

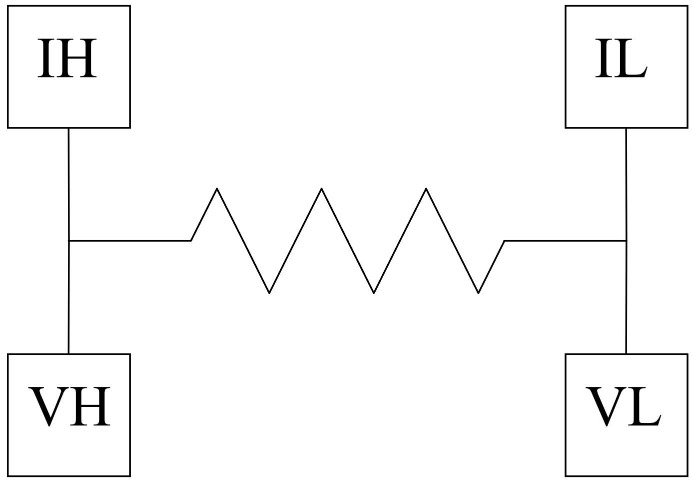


Figure 10: Resistor with Kelvin Pads

Since the resistance of the measurement system cables, probes, pads, and interconnect can degrade the accuracy of resistor measurements, all of the resistors are laid out with pads for Kelvin measurements (figure 1).

The Kelvin measurement method requires that two pads be connected to each end of the resistor. The IH pad is used to force a current into the resistor, and the IL pad is usually connected to a grounded ammeter in order to measure the current flow out of the resistor. The potentials at the IH current source and IL current meter will be different from the potentials at the resistor ends due to the effect of parasitic series resistance. By adding the VH and VL pads, we are able to accurately measure the potential at the resistor ends. Since no current flows through the VH and VL pads, the parasitic series resistances do not affect the measurement. The following equation is used to calculate the resistance:

$$R = -\frac{(VH - VL)}{IL}$$

In order to minimize the number of test modules, and thus the chip area, we have used the layout strategy shown in figure 2. This configuration allows kelvin measurements of all of the resistors, but it does not support simultaneous measurements for matching.

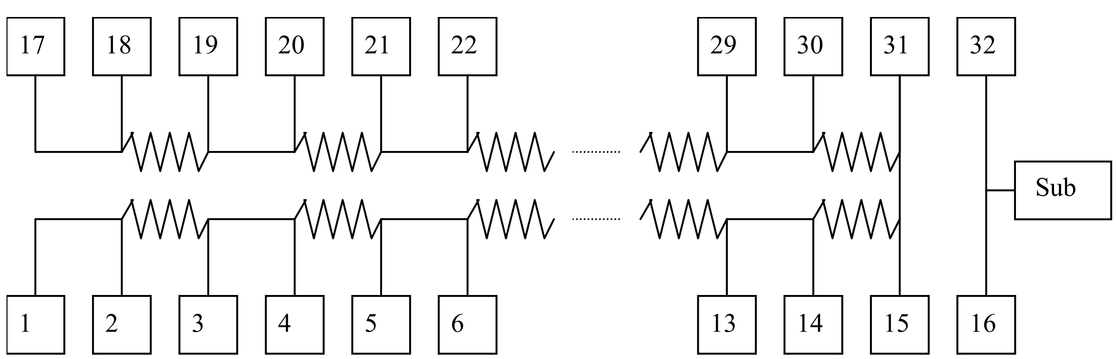


Figure 11: Resistor Matching Module Configuration

B. Test Description

B.1. Resistance and Resistor Matching

In order to simplify the data analysis, the resistance is reported only for the first resistor in the pair, and the test on the second resistor reports the resistance difference between the two resistors in percent.

$$\Delta R = 100 * \frac{R2 - R1}{R1}$$

B.2. Temperature Coefficient of Resistance

TCR testing is performed by changing the chuck temperature on the HP tester, and then running the resistance and resistor matching test a second time.

$$TCR(\Delta T, Tref) = \frac{R(\Delta T) - R(Tref)}{R(Tref) \cdot \Delta T}$$

B.3. Voltage Coefficient of Resistance

The Analog Tester is a custom built tester intended for high resolution measurements which the Reedholm cannot support. The analog tester is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. All of the cabling between the HP4156, switch matrix, and probe card is guarded through the use of triaxial cable. The HP4156 is composed of 4 SMUs (Source Measure Units), 2 VSUs (Voltage Source Units), and 2 VMUs (Voltage Measurement Units). The SMUs are used to simultaneously force and measure voltages and currents. The measurement resolution of the HP4156 SMUs is approximately 6 digits. The Analog Tester is controlled by a PC using a Visual Basic test program. The test program (WaferTest) is designed to provide a relatively open framework for implementing custom analog tests, and it places the measurement results directly into an Excel spreadsheet.

The VCR test is performed on the Analog Tester, and measures the resistance of a single resistor in all bias regions. The test reports the measured resistance, and model extraction takes place in Excel during post processing. The setup for this test consists of the two resistor terminals (VH and VL) and the body terminal (Vbody), as shown in figure B1.1. In a circuit, the allowable bias range for resistors ranges from ground to VDD for both the VH and VL terminals with the substrate always grounded. This bias range is the region inside the box depicted in figure B.1.2a. The zero differential voltage line represents the region in which resistance cannot be measured. For shorter resistors, the maximum differential voltage is restricted by the maximum current density specification in order to prevent damage. The bias range for shorter resistors is depicted in figure B.1.2b.

We have chosen to use a bias scheme shown in figure B.1.3, in which the VL terminal is always held at ground. The VH terminal is used to provide a differential bias, and the Vbody terminal is used to provide a common mode bias. This configuration simplifies biasing, as the same differential bias range can be used for each sweep. In addition, the linearity requirements on the SMU measuring current are reduced, as the current is measured through the VL terminal which is always grounded. As no measurements can be made for small differential voltages, a minimum differential voltage is specified.

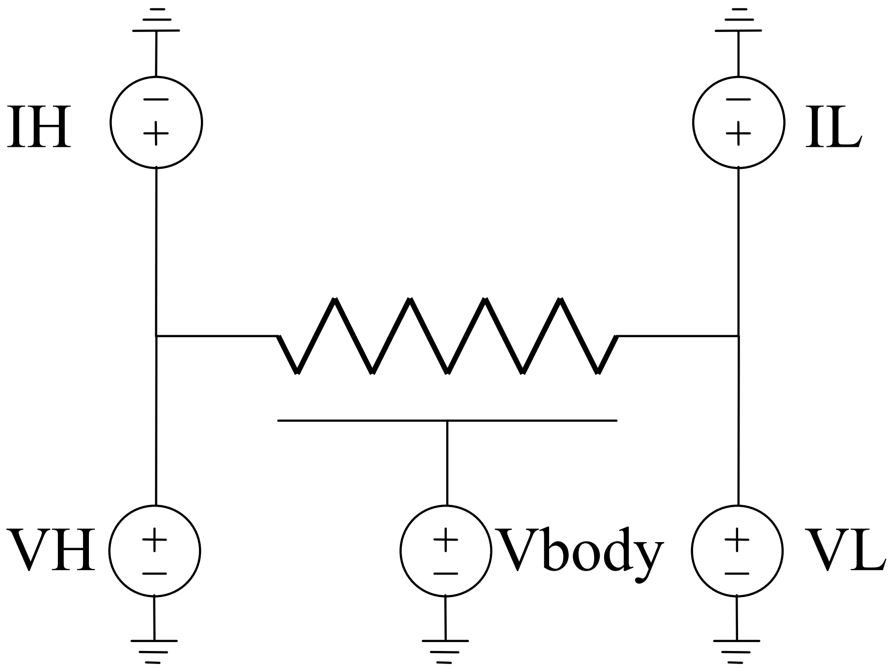
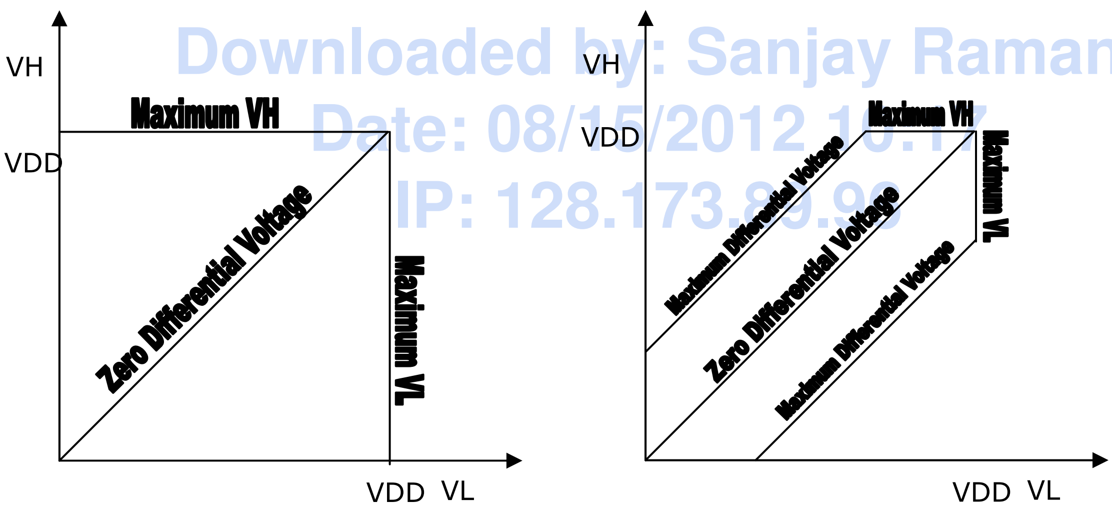
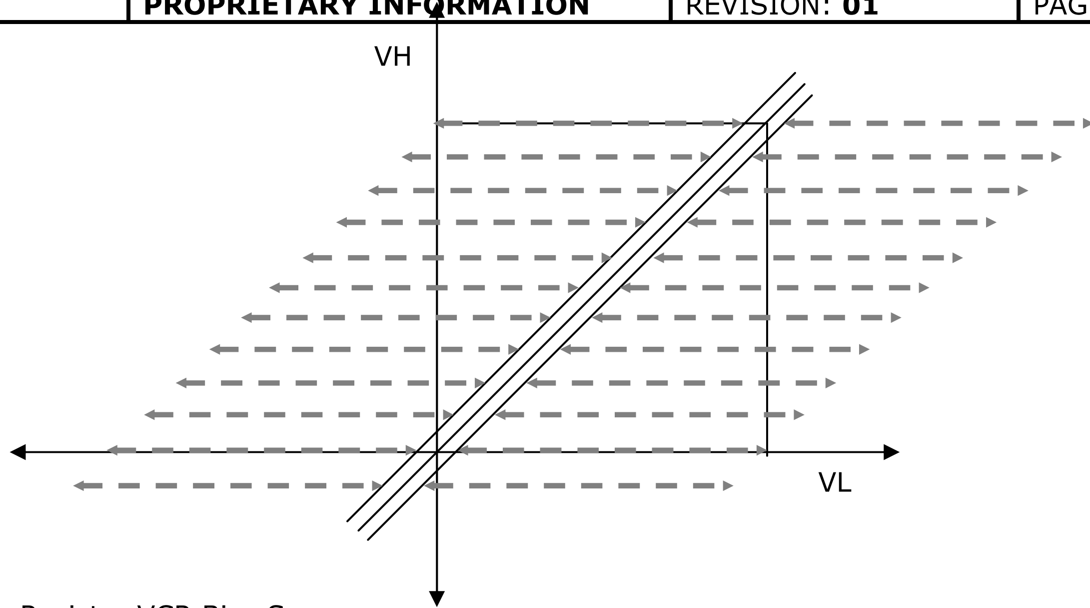


Figure B.1.1: VCR Measurement Configuration



a) b)

Fig B.1.2. a) Long Resistor VCR Bias Range, b) Short Resistor Bias Range



B.1.3. Long Resistor VCR Bias Sweep

C. Test Conditions

The following test conditions were used for this characterization:

C.1. Resistance and Resistor Matching

In order to maximize the accuracy of the resistance test, we have chosen to bias the resistors near the maximum current density. The following bias conditions were used:

Salicide resistors (Resistance and Matching)

Length	Current Density
L <= 100µm	0.2mA/µm
L > 100µm	0.1mA/µm

C.2. Temperature Coefficient of Resistance

The Salicide resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 30C and 130C.

C.3. Voltage Coefficient of Resistance

The measurement of VCR is complicated by the large ranges of resistances, voltages, and currents involved. The resistances to be measured, and the linear and quadratic voltage coefficients to be extracted, can vary by as much as 6 orders of magnitude over the space of available resistor widths and lengths. If the voltages or currents become too small, the HP4156 will not have sufficient precision to extract the VCR coefficients. There are problems measuring short resistors, as the voltage resolution of the HP4156 drops rapidly as the differential voltage drops below 0.3V. For short resistors, the maximum current density is often reached or exceeded at 0.5V. For very salicide resistors, the current can be too low for the HP4156 to measure with high precision.

The test is implemented with node IH connected to a SMU, which is configured to force voltage. The VH and VL nodes are connected to VMUs (the VMUs cannot be used in differential mode, as this mode is limited to 2V). The IL node is connected to a SMU, which is set to force 0 volts, and measure the current. The Body node is connected to a VSU. The test setup provides for connection inputs (IH, VH, VL, IL, Body), resistor information inputs (Width, Length), and bias conditions (ConstDeltaV, SlopeDeltaV, NumDeltaV, MinDeltaV, MaxDeltaV, StartVb, StopVb, NumVb).

The following steps are performed in order to measure the VCR:
Determine the VH bias range based on the resistor length. The maximum VH is determined by the lesser of (MinDeltaV + SlopeDeltaV * Length) or MaxDeltaV.
Measure the resistance as a function of VH and Vbody.
Place the measured resistance, VH, and VL into Excel.

The VCR model parameters (Ro, VCRq, VCRld, and VCRlc) are extracted by optimization in Excel.

The following test conditions were used for VCR characterization:

Parameter	Value
ConstDeltaV	0.3
SlopeDeltaV	0.07
NumDeltaV	10
MinDeltaV	0.1
MaxDeltaV	5
StartVb	1
StopVb	-4
NumVb	8

10. NWell Resistor Over Field Characterization

Table of Contents

Summary

A characterization of the N Well resistors over field in the SBC18 process has been performed. The results for the following tests are presented: resistance, resistor matching and TCR (Temperature Coefficient of Resistance). The test structures, test procedures, and test conditions are described in the appendix. Although the characterization was carried out on SBC18QTD GA577 test chip, it is applicable to N Well resistors for available in all sbc18 process variants.

1. Measurement Results

The characterization was performed on wafers processed in the SBC18 process using the GA577 engineering test chip. For resistance, matching and TCR measurement, 24 dies from wafers from following lots were tested: K17133 wf.16 to 22, K17157 wf20 to 25 K19225 wf.16 to 20, K19863 wf16 to 20, and K19920wf16,18,19,21,22. Since the goal of this characterization is to measure the standard deviation of the difference between two devices, a relatively large sample size is tested to obtain useful results.

For measurements involving a large number of samples, it is almost inevitable that there will be a few "bad points" which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these "bad points," it is important to remove them before calculating statistics. To efficiently perform this operation, a three sigma screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3sigma limits.

1.1. N Well Resistance and Resistor Matching

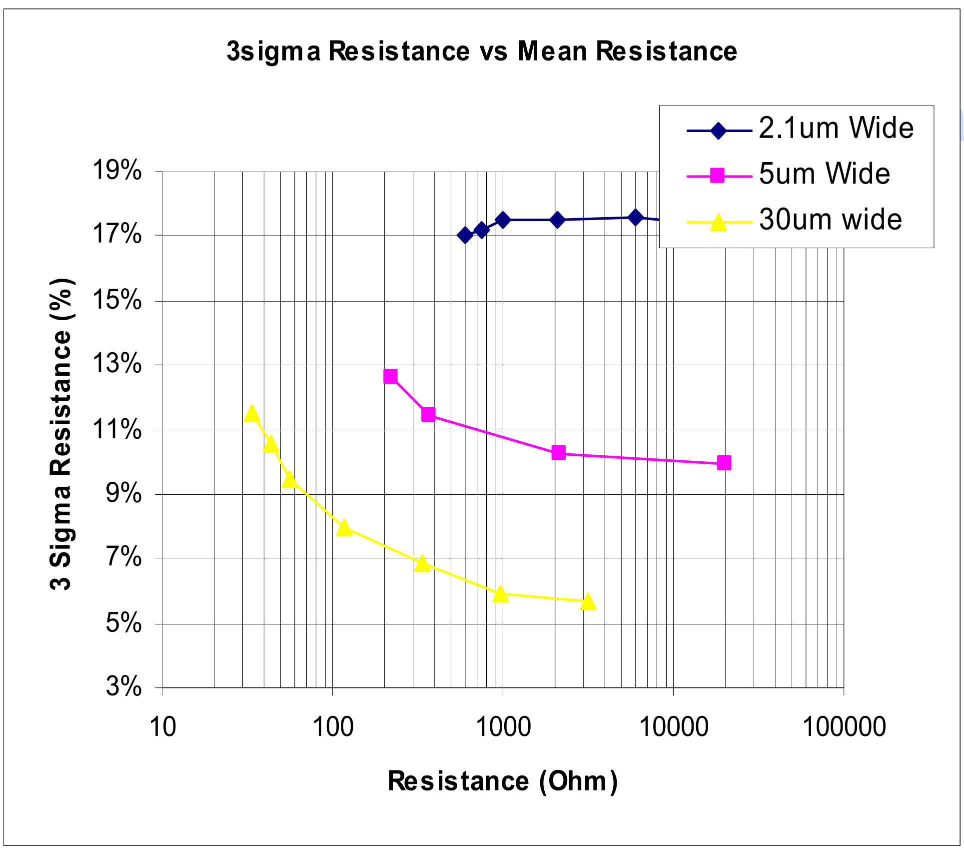
1.1.1. N Well Resistor 3 Sigma Resistance

The following tables list both the mean and 3 sigma of the measured resistance for each test structure:

3 Sigma Resistance (%) = 100 * 3 Sigma Resistance / Mean Resistance

N Well Resistors: 3 Sigma Resistance (%) / Mean Resistance (Ohms)

3 Sigma (%) / Mean Resistance(ohm)							
Width\Length	0.28	0.5	1	3	10	30	100
2.1um Wide	17.0% / 595	17.2% / 742	17.5% / 995	17.5% / 2,084	17.6% / 5,989	17.4% / 17,155	17.7% / 56,333
5um Wide	12.6% / 219		11.4% / 366		10.3% / 2,180		9.9% / 20,485
30um wide	11.5% / 34	10.6% / 43	9.5% / 57	8.0% / 117	6.8% / 335	5.9% / 958	5.7% / 3,138

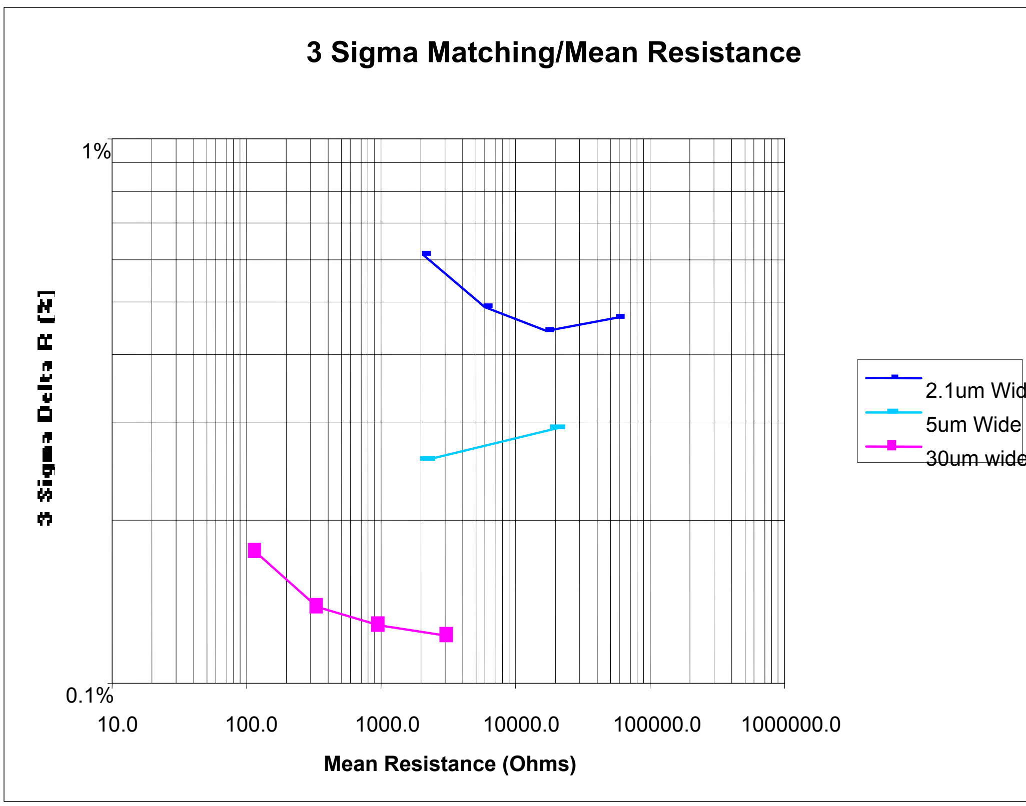


1.1.2 N Well Resistor 3 Sigma Matching of Resistor Pairs

The following tables list 3 sigma matching of resistance for each resistor pair:

N Well Matched Resistors: 3 Sigma Matching (%) / Mean Resistance (Ohms)

Measured 3sigma matching /Mean Resistance				
Width	3	10	30	100
2.1um Wide	0.6% / 2,084	0.5% / 5,989	0.4% / 17,155	0.5% / 56,333
5um Wide		0.3% / 2,180		0.3% / 20,485
30um wide	0.2% / 117	0.1% / 335	0.1% / 958	0.1% / 3,138



1.2. N Well Resistor Temperature Coefficient

The N Well Resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 25°C and 125°C. The following table lists both the mean and 3 sigma of the measured TCR:

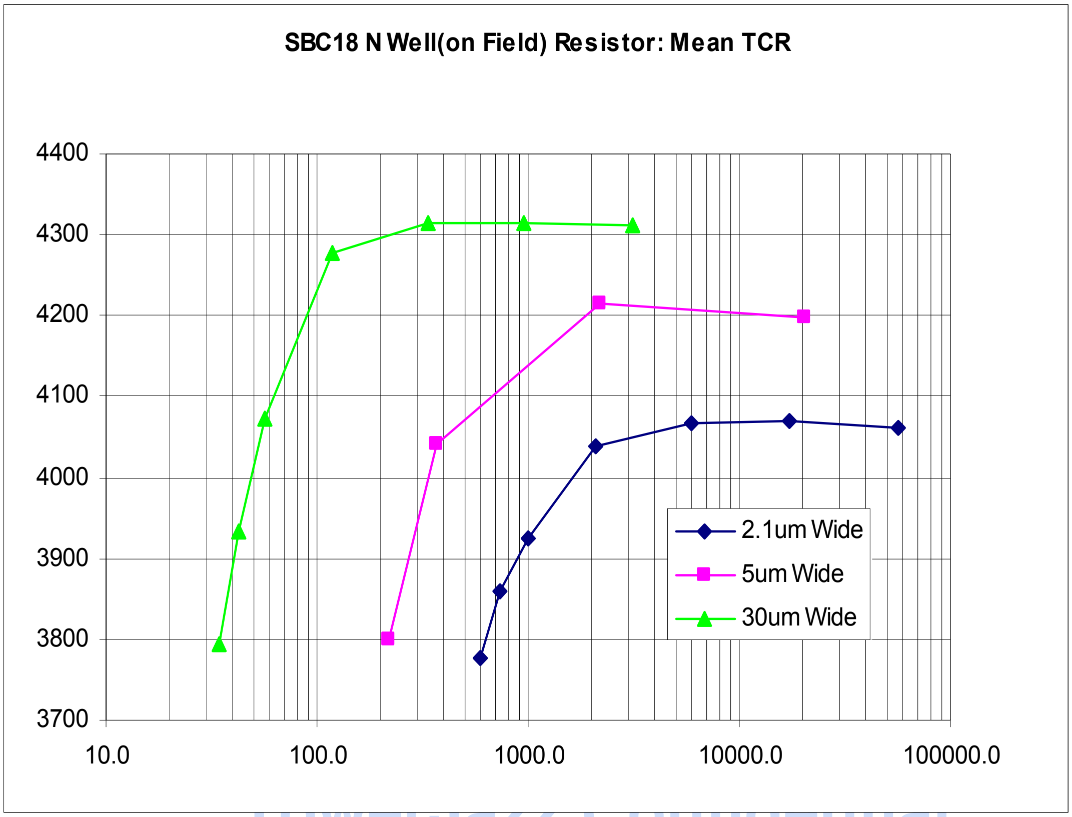
TCR= (R at 125C – R at 25C)/R at 25C x 100%

N Well Resistors: Mean TCR (ppm/C) / Mean Resistance (Ohms)

Mean Tempco/Mean Resistance							
Width\Length	0.28	0.5	1	3	10	30	100
2.1um Wide	3,775 / 595	3,859 / 742	3,926 / 995	4,039 / 2,084	4,066 / 5,989	4,070 / 17,155	4,061 / 56,333
5um Wide	3,799 / 219		4,041 / 366		4,215 / 2,180		4,199 / 20,485
30um Wide	3,794 / 34	3,932 / 43	4,071 / 57	4,279 / 117	4,314 / 335	4,316 / 958	4,312 / 3,138

N Well Resistors: 3 Sigma TCR (ppm/C) / Mean Resistance (Ohms)

3 Sigma Tempco/Mean Resistance							
Width\Length	0.28	0.5	1	3	10	30	100
2.1um Wide	243 / 595	248 / 742	272 / 995	275 / 2,084	270 / 5,989	280 / 17,155	279 / 56,333
5um Wide	260 / 219		264 / 366		270 / 2,180		286 / 20,485
30um Wide	252 / 34	252 / 43	268 / 57	280 / 117	280 / 335	286 / 958	279 / 3,138

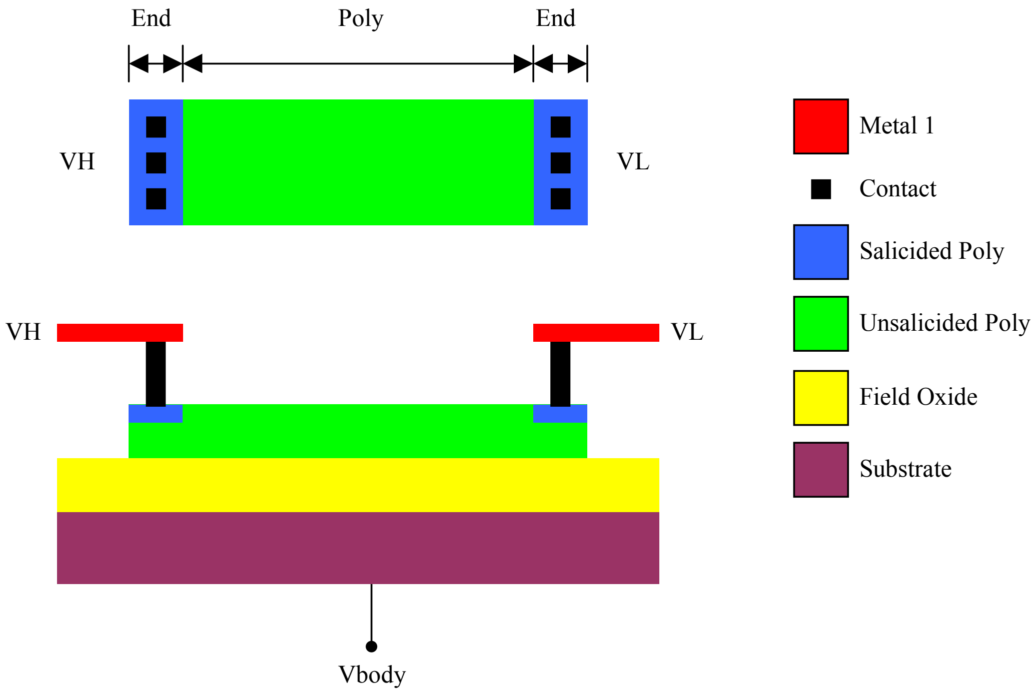


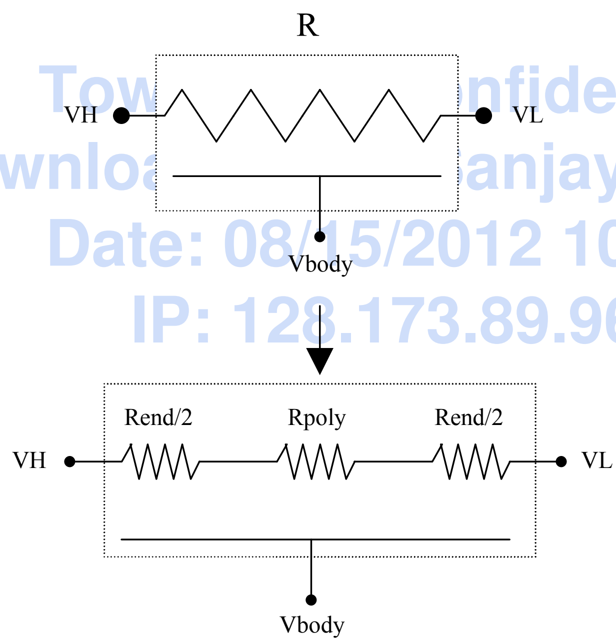
2. N Well Resistor Models

2.1. N Well Resistor Resistance Model

The model can be used for resistance, resistor tolerance, and resistor matching calculations.

The model describes the resistor with two components. The resistor is composed of a N well resistor in series with two end resistors.





The following equations are used to model the resistor:

$$R = Rpoly + Rend$$

$$Rpoly = Rs\frac{L}{W + \Delta W}$$

$$Rend = \frac{Re}{W + \Delta W}$$

$$R = Rs\frac{L}{W+\Delta W} + \frac{Re}{W+\Delta W}$$

We have used an optimizer to fit this model to the resistance data. The optimization was based on minimizing the RMS error in the fit for resistors with length ≥3um.

Parameter	Value	Unit
Mean Rs	922.8	Ohm
Mean Re	679	Ohm - μm
Mean ΔW	-0.448	μm

2.2 N Well Resistor Resistance Fit Error

The following table describes the ability of the model to fit the resistance data. The model fits all resistors ≥3um length to less than 1.0% error.

HV Matched Resistors: Mean Resistance Model Fit Error (%) / Mean Resistance (Ohms)

Delta Mean Resistance							
Width\Length	0.28	0.5	1	3	10	30	100
2.1um Wide	-4.7% / 595	-7.0% / 742	-2.6% / 995	0.1% / 2,084	0.1% / 5,989	0.1% / 17,155	-0.1% / 56,333
5um Wide	-6.2% / 219		-3.8% / 366		-0.2% / 2,180		-0.3% / 20,485
30um wide	-7.1% / 34	-10.1% / 43	-4.8% / 57	-0.1% / 117	0.0% / 335	0.2% / 958	0.3% / 3,138

In order to determine the tolerances on Rs, Re, and ΔW; we have derived an equation which relates the standard deviations (σ) of the model parameters to the standard deviation of the resistance.

σ = standard deviation

σ^2 = variance

$$\sigma_R^{\ 2} = \sigma_{Rs}^{\ 2}\left[\frac{\delta R}{\delta Rs}\right]^2 + \sigma_{Re}^{\ 2}\left[\frac{\delta R}{\delta Re}\right]^2 + \sigma_{\Delta W}^{\ 2}\left[\frac{\delta R}{\delta \Delta W}\right]^2$$

$$\sigma_R^{\ 2} = \sigma_{Rs}^{\ 2}\frac{L^2}{(W+\Delta W)^2} + \sigma_{Re}^{\ 2}\frac{1}{(W+\Delta W)^2} + \sigma_{\Delta W}^{\ 2}\left[\frac{L\cdot Rs}{(W+\Delta W)^2} + \frac{Rend}{(W+\Delta W)^2}\right]^2$$

We have used an optimizer to fit this model to the 3 sigma resistance data. The optimization was based on minimizing the RMS error in the fit for resistors ≥3um in length.

Parameter	Value	Unit

3 Sigma Rs	57.7	Ohm
3 Sigma Re	216.8	Ohm - μm
3 Sigma ΔW	0.278	μm

N Well Matched Resistors: 3 Sigma **Fit Error** (%) / Mean Resistance (Ohms)

Delta Mean Resistance							
Width\Length	0.28	0.5	1	3	10	30	100
2.1um Wide	60.2% / 595	38.2% / 742	21.9% / 995	6.7% / 2,084	2.0% / 5,989	3.3% / 17,155	1.0% / 56,333
5um Wide	78.8% / 219		28.3% / 366		-15.4% / 2,180		-12.4% / 20,485
30um wide	87.9% / 34	63.5% / 43	41.4% / 57	1.3% / 117	-8.1% / 335	4.8% / 958	10.3% / 3,138

2.3. Repeatability of N Well resistor Resistance

		Rs	Rend	Delta W
Spec	Nom	890	875	-0.28
	low	710	700	-0.38
	high	1070	1050	-0.18
K17133	Mean	925	674	-0.520
	1sigma	13	57	0.014
K17157	Mean	934	717	-0.517
	1sigma	10	51	0.021
K19225	Mean	903	662	-0.379
	1sigma	27	79	0.025
K19863	Mean	937	650	-0.419
	1sigma	8	32	0.018
K19920	Mean	910	689	-0.34
	1sigma	6.7	46	0.011

A characterization of the N Well resistors over the field in the SBC18 process has been completed. The measurement results for some parameters have been successfully modeled.

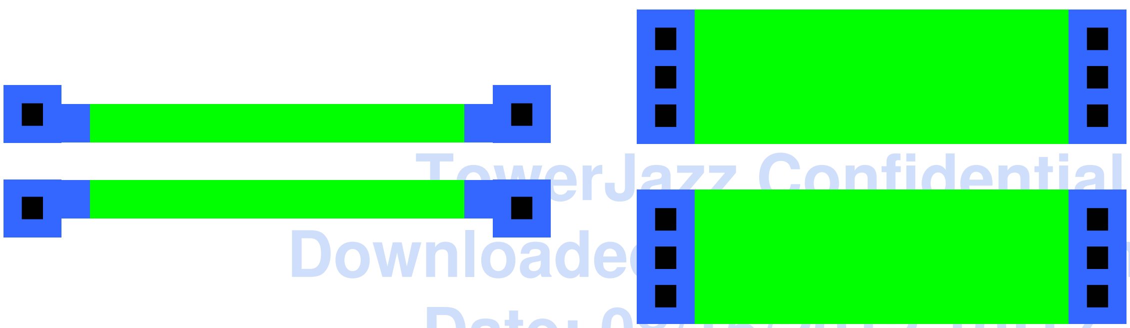
Appendix: Test Structure and Test Description

A. Test Structures

The GA577 SBC18 test chip was used for this characterization. This test chip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 2 modules devoted to N Well over the field resistor characterization on the GA577. The following table describes the resistor types and sizes available for characterization:

Matched Resistors



Single Resistors and Matched Pairs Without Dummies:

	Single Resistors			Matched Resistor Pairs			
Width\Length	0.28μm	0.5μm	1μm	3μm	10μm	30μm	100μm
2.1μm	X	X	X	X	X	X	X
5μm	X		X		X		X
30μm	X	X	X	X	X	X	X

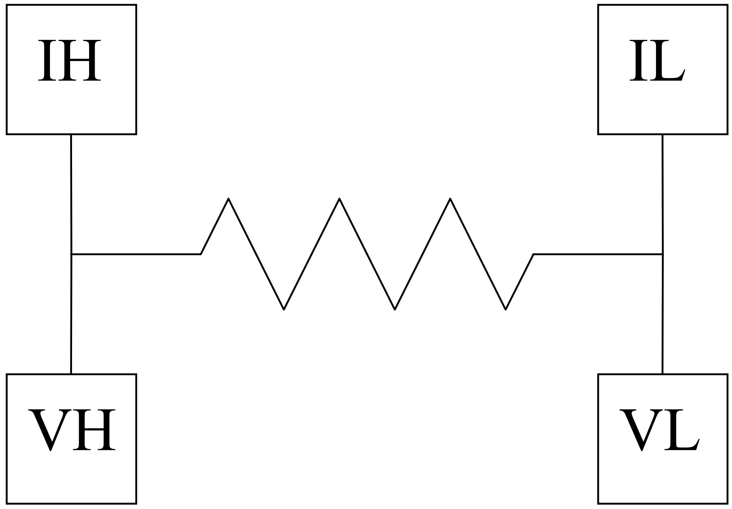


Figure A.12: Resistor with Kelvin Pads

Since the resistance of the measurement system cables, probes, pads, and interconnect can degrade the accuracy of resistor measurements, all of the resistors are laid out with pads for Kelvin measurements (figure A1).

The Kelvin measurement method requires that two pads be connected to each end of the resistor. The IH pad is used to force a current into the resistor, and the IL pad is usually connected to a grounded ammeter in order to measure the current flow out of the resistor. The potentials at the IH current source and IL current meter will be different from the potentials at the resistor ends due to the effect of parasitic series resistance. By adding the VH and VL pads, we are able to accurately measure the potential at the resistor ends. Since no current flows through the VH and VL pads, the parasitic series resistances do not affect the measurement. The following equation is used to calculate the resistance:

$$R = -\frac{(VH - VL)}{IL}$$

In order to minimize the number of test modules, and thus the chip area, we have used the layout strategy shown in figure A2. This configuration allows kelvin measurements of all of the resistors, but it does not support simultaneous measurements for matching.

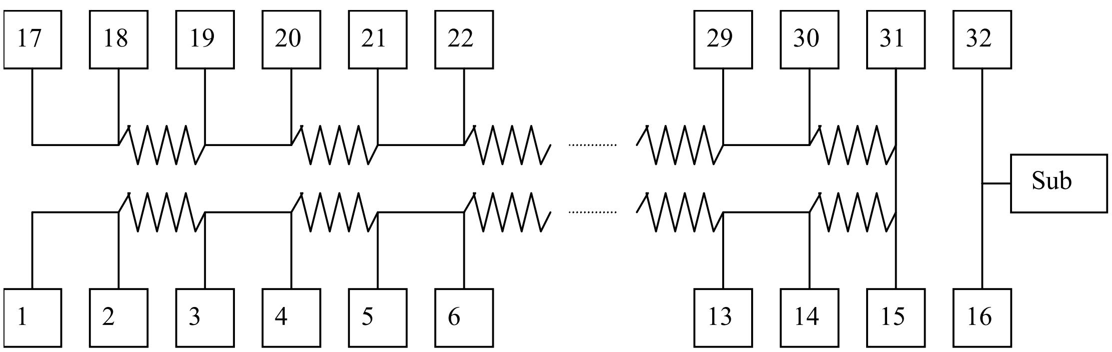


Figure A13: Resistor Matching Module Configuration

B. Test Description

B.1. Resistance and Resistor Matching

In order to simplify the data analysis, the resistance is reported only for the first resistor in the pair, and the test on the second resistor reports the resistance difference between the two resistors in percent.

$$\Delta R = 100 * \frac{R2 - R1}{R1}$$

B.2. Temperature Coefficient of Resistance

TCR testing is performed by changing the chuck temperature on the Reedholm tester, and then running the resistance and resistor matching test a second time.

$$TCR(\Delta T, Tref) = \frac{R(\Delta T) - R(Tref)}{R(Tref) \cdot \Delta T}$$

C. Test Conditions

The following test conditions were used for this characterization:

C.1. Resistance and Resistor Matching

In order to maximize the accuracy of the resistance test, we have chosen the current so that the voltage drop over resistors is around 100mV in the four terminal set up.

C.2. Temperature Coefficient of Resistance

The N Well Resistor TCR was measured on the same resistors as the resistance and resistance matching. The temperatures used were 25C and 125C.

11. 2fF/μm² MIM Capacitor Characterization Report

Summary

SBC18 MIM capacitors with a dielectric of nitride, targeted for 2fF/μm^2, have been characterized on five GA577 SBC18 lots for 5wafers from each lot: K17133.1 wf.16 to 20, K17157,.1 wf21 to 25, K19225 wf.16 to 20, K19863 wf.16 to 20 and K19920 wf.16,18,19,21,22. The following characterization results are presented in this report: the breakdown voltage of the MIM capacitors, the leakage current of MIM capacitors at 10V stress voltage, the area and perimeter components of the capacitance, the voltage coefficient of capacitance (VCC), and the temperature coefficient of the capacitance (TCC). Although the characterization was carried out on SBC18QTD GA577 test chip, it is applicable to 2fF MIM capacitors for SBC18PT, QTD, QR, QW, and MW process.

Test Structures

The test structures used in this characterization are Metal-Insulator-Metal (MIM) capacitors on GA577 test chip. The capacitors have a dielectric of nitride film. The capacitor is built on metal 2, which serves as the bottom plate of the capacitor. After metal 2 deposition, a capacitor dielectric film (PECVD nitride) is then deposited, followed by the deposition of a TM layer. The top plate is patterned first and etched, stopping on the capacitor dielectric. The bottom plate (metal 2) is subsequently patterned, and remaining dielectric and metal stack are etched in sequence to complete the MIM capacitor formation. Fig. 1 shows a schematic drawing of the cross section of an MIM capacitor.

Capacitors with various areas and perimeter lengths were designed for extracting the area and perimeter components of the capacitance. The area intensive capacitors are laid out in squares with area (defined by TM plate) varying from 100μm^2 to 40000μm^2. The perimeter intensive capacitors are multi-finger structures sitting on either common or separate metal 2 bottom plates. Fig. 2 shows the schematic of the MIM capacitor layout. Bottom (M2) connection to metal 3 was made through pads. There is no via contacts present on either side of the capacitor. Table 1 lists the dimension of the capacitors used for this characterization.

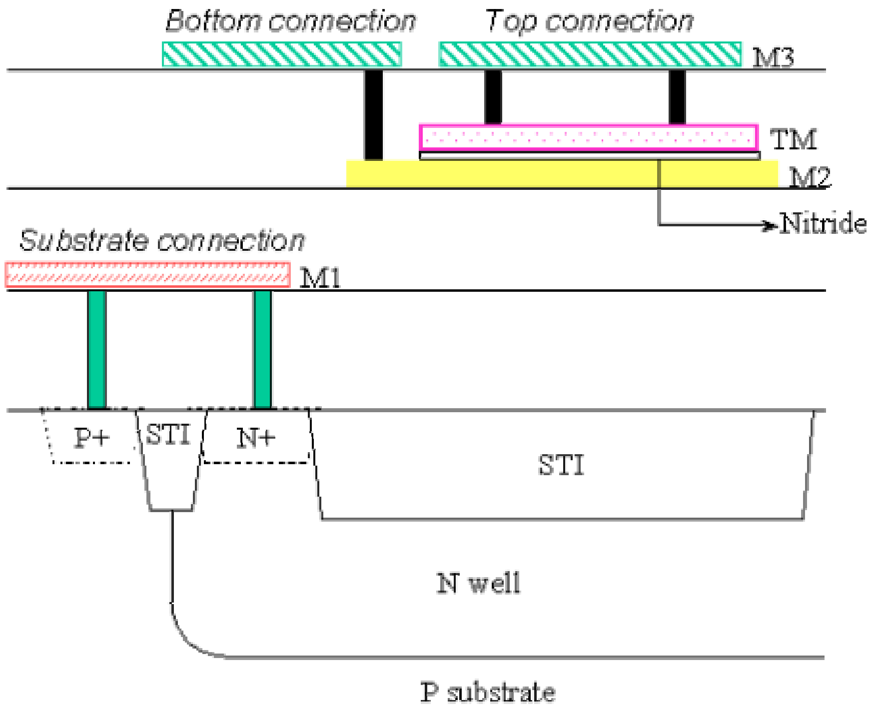


Fig. 1 Cross section of an MIM capacitor

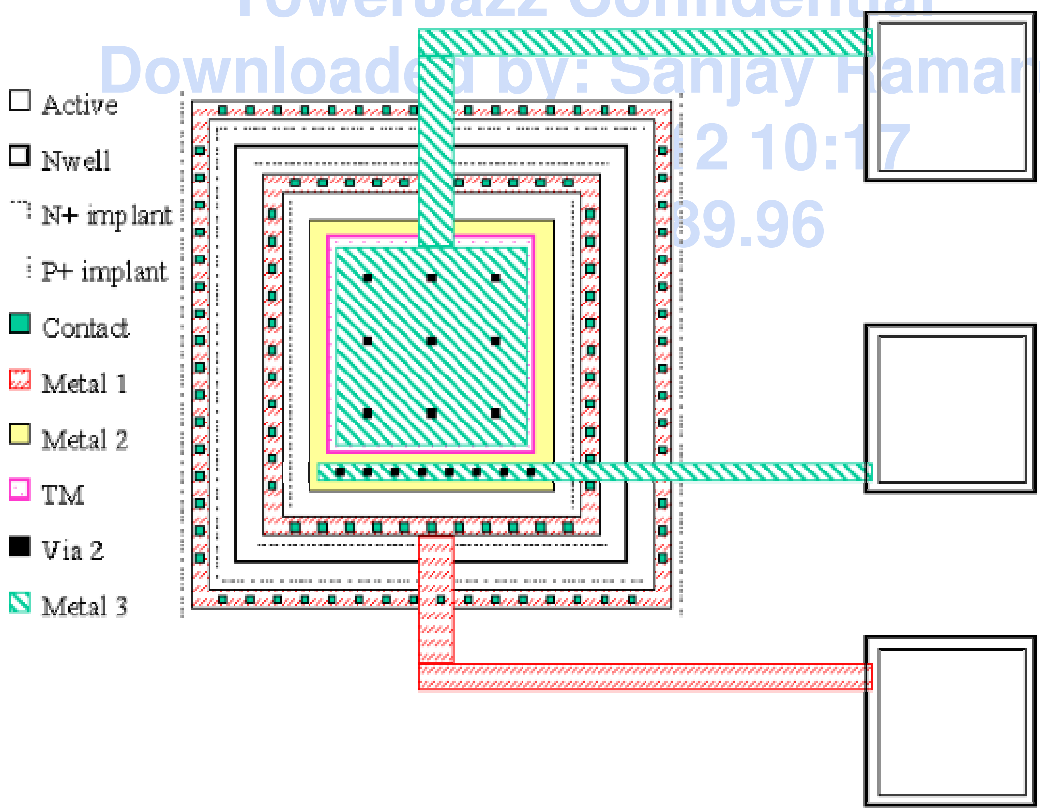


Fig. 2. Schematic drawing of MIM capacitor layout. The structure is not drawn to scale.

Table 1. Capacitor area and perimeter length

W(μm)	L(μm)	No. of fingers	Area (μm2)	Perimeter (μm)	Approx. Cap(pF)
600	300	1	180000	1800	360
10	10	1800	180000	72000	360
2.5	300	240	180000	145200	360
10	10	1	100	40	0.2
20	20	1	400	80	0.8
50	50	1	2500	200	5
100	100	1	10000	400	20
200	200	1	40000	800	80
10	200	20	40000	8400	80
10	10	400	40000	16000	80

The first three devices are large capacitors with the same total area (180000um2). The capacitance calculated from Carea only is 360pF. They varied in length of capacitor sides and are used for characterization of capacitor breakdown voltage, leakage current and defectivity. The other devices are used for area/perimeter capacitance extraction, temperature coefficient calculation. Voltage coefficient (VCC) was measured on 100x100um device only.

Measurement Schemes and Parameter Extraction

Capacitance measurement:

An HP4284A LCR meter was used to measure the capacitance. The capacitance was measured between top TM plate and bottom metal 2 plate by applying ac signal on top plate, while the substrate tie was grounded. The measurement was taken at the frequency of 1MHz, ac bias of 100mV, and DC bias of 0 volt, averaged15 times with long integration time. In order to compensate for the parasitic capacitance from pads, an open calibration measurement was done on a set of open pads prior to capacitance measurement.

Breakdown Voltage and Leakage Current

Breakdown voltage was measured on HP test by voltage sweeping at 0.1V/step. The breakdown point was defined when the leakage current reach 1uA.
The leakage current was measured by biasing the capacitor at 10V.

Area and perimeter capacitance extraction

The area and perimeter capacitances were extracted from capacitances of various sizes capactors. The capacitance can be expressed as:

$$C = Carea \cdot A + Cperimeter \cdot L \qquad (1)$$

where *Carea* is area capacitance, *A* is capacitor area, *Cperimeter* is perimeter capacitance, and *L* is perimeter lengths. At least three different sizes capacitors are needed in order to extract *Carea*, and *Cperimeter*. In this study, seven capacitors were used (see table 1), and *Carea* and *Cperimeter* were extracted using least square regression.

Temperature coefficient of capacitance

The temperature coefficient of capacitance (TCC) of MIM capacitors is extracted from capacitances measured at two temperatures: 25°C and 125°C. The TCC is then calculated using the following equation:

$$TCC(ppm/^{\circ}C) = \frac{C(125^{\circ}C) - C(25^{\circ}C)}{C(25^{\circ}C)\cdot(125-25)}\cdot 1000000 \qquad (2$$

Voltage coefficients of capacitance

The voltage coefficients of capacitance (VCC) are extracted from 100μm×100μm capacitors. The capacitance as a function of bias voltage can be expressed as:

$$C = C_0\,(1 + C_1 \times V + C_2 \times V^2) \qquad (3)$$

where C_0 is the capacitance at 0 volt, V the voltage across the capacitor, C_1 the linear voltage coefficient, and C_2 the quadratic voltage coefficient. In order to extract the voltage coefficients, the capacitances at different DC biasing voltages are measured. In this characterization, the biasing voltage varies from −5V to 5V. The bias is applied on the top plate. By fitting the measured capacitances at different voltages into the above equation by least square method, the linear and quadratic voltage coefficients can be extracted.

Results

Twenty wafers/24sites per wafer from four SBC18 lots (Part No. GA577) were characterized. K17133.1 wf.16 to 20, K17157.1 wf21 to 25, K19225 wf.16 to 20, K19863 wf.16 to 20 and K19920 wf18,18,20,22,23. All measurements were done at 25°C, except for TCC, which was extracted from capacitances measured at two temperatures: 25°C and 125°C.

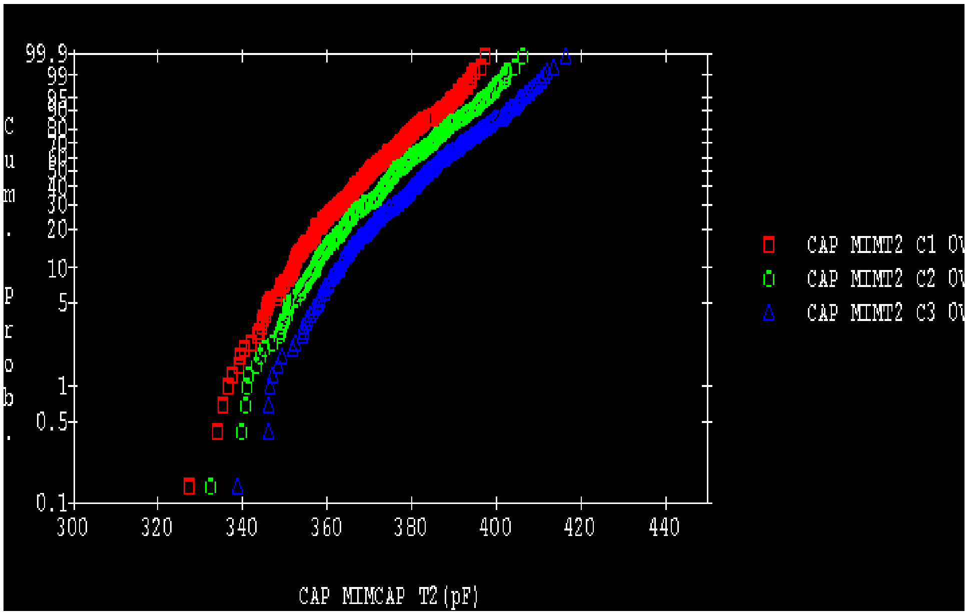
1) **Large Capacitor Statistics and Defectivity**

Table 2 is the statistic summary table for three large capacitors. The specs for capacitor is not used here for the big range of the edge length.

Table 2: Statistic Summary Table for Three Large Capacitors

Test Name	Cell	Unit	Spec	Mean	Med	Max	Min	Stdev	Yield
	Description								
CAPC1	600x300 Large Plate	fF/um2	N.A.	2.053	2.057	2.208	1.819	0.074	100
BVGOC1	600x300 Large Plate	V	>15V	20.4	20.4	23.6	18.4	1.0	100
CAPC2	10x10x60x30 array	fF/um2	N.A.	2.085	2.088	2.222	1.848	0.075	100
BVGOC2	10x10x60x30 array	V	>15V	20.4	20.3	23.6	18.4	1.0	100
CAPC3	2.5x300x240 Finger	fF/um2	N.A.	2.109	2.119	2.220	1.882	0.071	100
BVGOC3	2.5x300x240 Finger	V	>15V	20.4	20.3	23.6	17.0	1.0	100

The Weibull probability plots below showed that same distributions for capacitance and breakdown voltage. There is no failure sites for capacitance and breakdown voltage. The defectivity of SBC18 2fF MIM capacitor process is shown in Table 3.



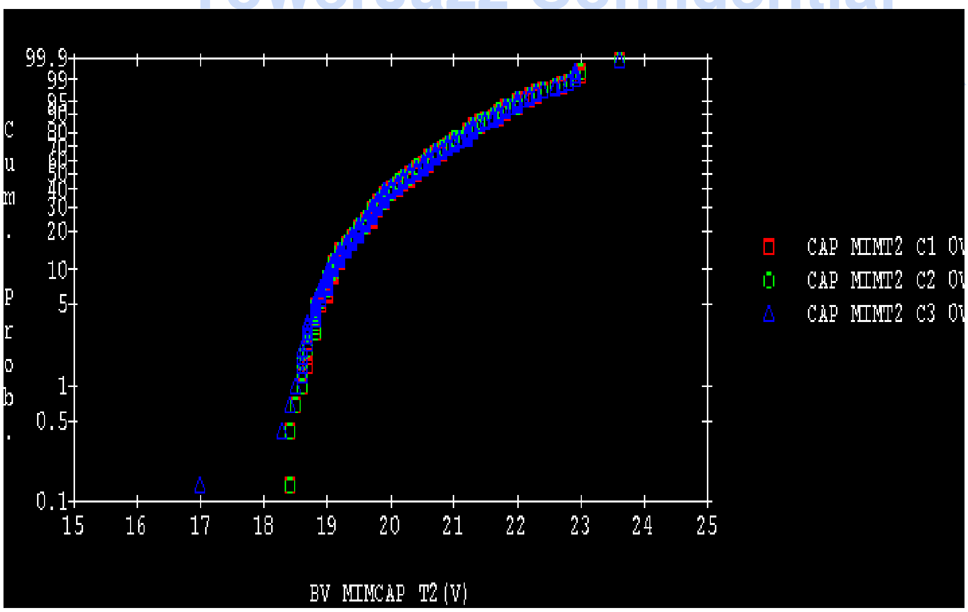


Fig. 3 Weibull plots of 360pF MIM Capacitor (a) Capacitance, (b) Breakdown Voltage.

Table 3 The Defectivity of 360pF MIM Capacitors

Test Name	Cell	Area	Defectivity	Edge	Defectivity
	Description	cm2	per cm2 area	cm	per cm edge
CAPC1	600x300 Large Plate	0.0018	less than 1.56	0.18	
BVGOC1	600x300 Large Plate	0.0018		0.18	less than 0.0156
LKC1 @10V	600x300 Large Plate	0.0018		0.18	
CAPC2	10x10x60x30 array	0.0018	less than 1.56	7.2	
BVGOC2	10x10x60x30 array	0.0018		7.2	less than 0.0004
LKC2 @10V	10x10x60x30 array	0.0018		7.2	
CAPC3	2.5x300x240 Finger	0.0018	less than 1.56	14.52	
BVGOC3	2.5x300x240 Finger	0.0018		14.52	equals 0.0386
LKC3 @10V	2.5x300x240 Finger	0.0018		14.52	

The breakdown failure is area dependent and the leakage failure is considered edge dependent. The area defectivity is less than 1.56 per cm2 for three different capacitors. The edge defectivity for 600x300 large cap and 10x10x60x30 arrays is less than 0.0156 per cm and 0.0004 per cm respectively and for 2.5x300x240 finger capacitor 0.0386 per cm edge.

2) Area and perimeter capacitance of MIM capacitors

The area capacitance and perimeter capacitance of MIM capacitors were extracted by using the above mentioned methodology. Table 4 summarizes the extracted Carea and Cperimeter for the four lots. Figure 4 shows the lot to lot variation of the extracted area and perimeter capacitances.

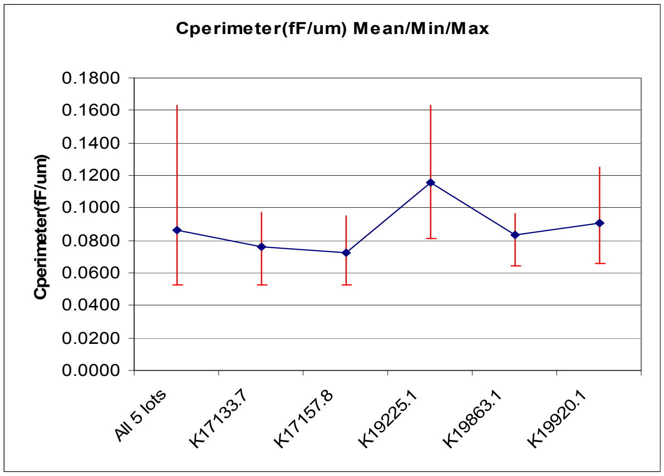
Table 4. Area and perimeter capacitance of SBC18 MIM capacitors.

2fF/um2 MIM capacitor

Area Cap	Unit	Mean	Median	Maximum	Minimum	StdDev	3sigma%
All 5 lots	fF/um2	**2.0560**	**2.0477**	**2.2924**	**1.8069**	**0.0996**	**14.53%**
K17133.7	fF/um2	**2.0005**	**1.9958**	**2.0976**	**1.8781**	**0.0475**	**7.13%**
K17157.8	fF/um2	**1.9428**	**1.9473**	**2.0520**	**1.8069**	**0.0475**	**7.34%**
K19225.1	fF/um2	**2.0796**	**2.0800**	**2.1991**	**1.9377**	**0.0608**	**8.77%**
K19863.1	fF/um2	**2.0767**	**2.0737**	**2.1904**	**1.9747**	**0.0509**	**7.36%**
K19920.1	fF/um2	**2.1975**	**2.2062**	**2.2924**	**2.0858**	**0.0543**	**7.41%**
Perimeter Cap	**Unit**	**Mean**	**Median**	**Maximum**	**Minimum**	**StdDev**	**3sigma%**
All 5 lots	fF/um	**0.0867**	**0.0814**	**0.1630**	**0.0526**	**0.0197**	**68.26%**
K17133.7	fF/um	**0.0759**	**0.0753**	**0.0972**	**0.0526**	**0.0095**	**37.43%**
K17157.8	fF/um	**0.0726**	**0.0721**	**0.0951**	**0.0530**	**0.0097**	**40.11%**
K19225.1	fF/um	**0.1155**	**0.1105**	**0.1630**	**0.0815**	**0.0200**	**51.96%**
K19863.1	fF/um	**0.0833**	**0.0822**	**0.0969**	**0.0641**	**0.0068**	**24.36%**
K19920.1	fF/um	**0.0904**	**0.0844**	**0.1248**	**0.0660**	**0.0155**	**51.41%**

The area capacitance within a lot is around 7% for all 5 lots. However, there is a large lot-to-lot variation in area capacitance. The 3 sigma variation of area capacitance over 5lots is almost 15%, as the film deposition thickness varied.

The correct action is to tighten the in-line film deposition spec so the film thickness can be centered at the targeted thickness.



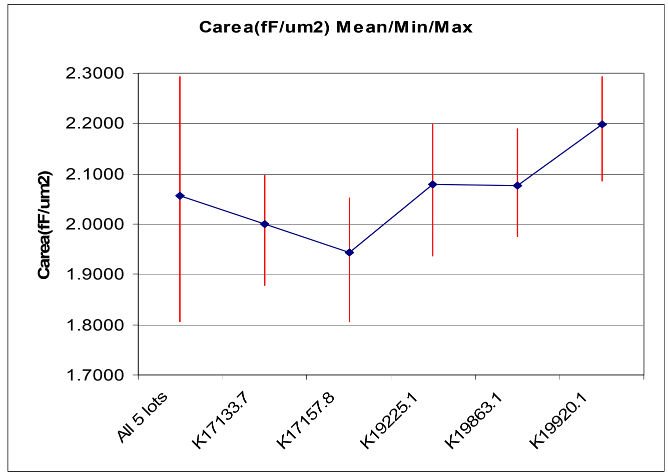


Fig. 4. Lot to lot variation of extracted area and perimeter capacitances.

The correctness of the area and perimeter capacitance extraction is examined by comparing the measured and the calculated capacitances for different dimension devices. Table 5 shows the nominal capacitance and the fitting error for all device sizes. The nominal capacitance is calculated from the overall averaged area and perimeter capacitances. The fitting error is calcultated for all sites that measured. The 3 sigma fitting error is about 15% for all dimension capacitors, which is comparable to the dielectric thickness variation caused capacitance spread, indicating the accuracy of the extracted area and perimeter capacitances.

Table 5. Nominal capacitance and averaged fitting error.

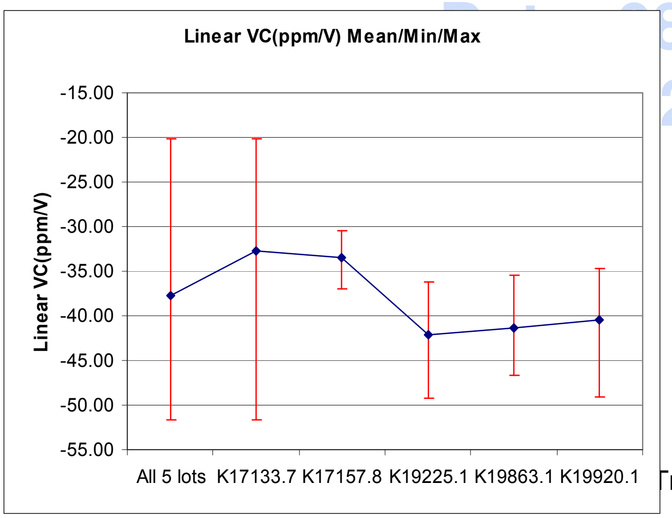
Fitting Error for AC all 4 lots	Area (um2)	L (no cnt)	Mominal cap(pF)	Ave. Error %	Stdev	3σ Error
CAP 10X10	100	40	0.21	0.02%	5.02%	15.06%
CAP 20X20	400	80	0.83	0.16%	4.88%	14.64%
CAP 50X50	2500	200	5.16	0.20%	4.79%	14.37%
CAP 100X100	10000	400	20.60	0.03%	4.86%	14.58%
CAP 200X200	40000	800	82.31	-0.03%	4.87%	14.61%
CAP 10X200X20	40000	8400	82.97	-0.03%	4.91%	14.72%
CAP 10X10X20x20	40000	16000	83.63	0.04%	4.93%	14.80%

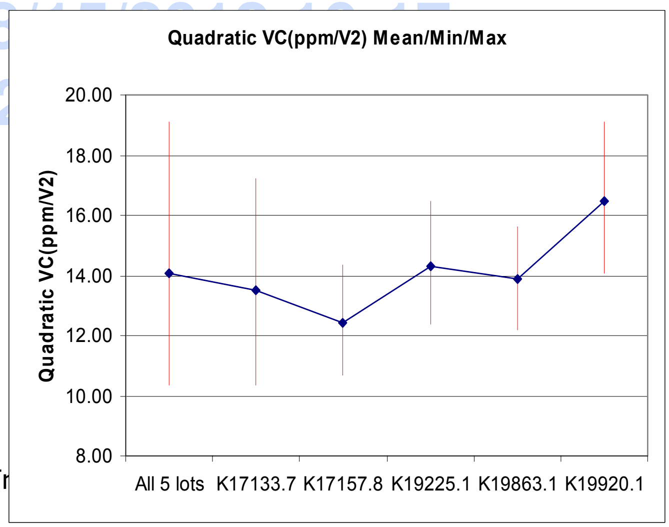
3) Voltage coefficients of capacitance

The voltage coefficients of capacitance (VCC's) of SBC18 MIM capacitors were characterized across five GA577 lots. The extracted 0V capacitance, linear VCC, and quadratic VCC for each lot and overall mean and standard deviations are summerized in table 6. Due to the symmetry of its electrodes, the MIM capacitor has very low voltage coefficients compare to older technologies. A linear VCC of −37.7± 5.74ppm/V, and a quadratic VCC of 14.1± 1.72ppm/V^2 are obtained. The distribution of linear VCC and quadratic VCC of MIM capacitors are shown in Fig. 5(a) and (b).

Table 6. Voltage coefficients of SBC18 MIM capacitors

Co VC_VCC	**Unit**	**Mean**	**Median**	**Maximum**	**Minimum**	**StdDev**	**3sigma%**
All 5 lots	pF	**20.61**	**20.50**	**22.96**	**18.15**	**0.99**	**14.35%**
K17133.7	pF	20.05	20.50	21.02	18.81	0.48	7.18%
K17157.8	pF	19.52	19.60	20.53	18.15	0.53	8.13%
K19225.1	pF	20.84	20.90	22.05	19.51	0.60	8.69%
K19863.1	pF	20.80	20.78	21.94	19.77	0.51	7.41%
K19920.1	pF	22.02	22.11	22.96	20.89	0.55	7.43%
Linear VCC	**Unit**	**Mean**	**Median**	**Maximum**	**Minimum**	**StdDev**	**3sigma%**
All 5 lots	ppm/V	**-37.72**	**-38.68**	**-20.12**	**-51.70**	**5.74**	**-45.66%**
K17133.7	ppm/V	-32.70	-38.69	-20.12	-51.70	6.57	-60.31%
K17157.8	ppm/V	-33.47	-33.36	-30.41	-36.90	1.22	-10.93%
K19225.1	ppm/V	-42.15	-42.82	-36.27	-49.18	3.14	-22.34%
K19863.1	ppm/V	-41.35	-41.56	-35.43	-46.67	2.61	-18.94%
K19920.1	ppm/V	-40.39	-40.47	-34.67	-49.16	2.97	-22.05%
Quadratic VCC	**Unit**	**Mean**	**Median**	**Maximum**	**Minimum**	**StdDev**	**3sigma%**
All 5 lots	ppm/V2	**14.09**	**13.84**	**19.11**	**10.37**	**1.72**	**36.63%**
K17133.7	ppm/V2	13.51	13.86	17.22	10.37	1.59	35.23%
K17157.8	ppm/V2	12.42	12.37	14.34	10.67	0.74	17.86%
K19225.1	ppm/V2	14.30	14.32	16.47	12.37	1.03	21.69%
K19863.1	ppm/V2	13.90	13.86	15.62	12.19	0.87	18.73%
K19920.1	ppm/V3	16.45	16.52	19.11	14.06	1.11	20.23%





The fitting error for voltage coefficient is small as indicated by close to 1 Rsquare of the data fitting, as shown in table 7.

Table 7: Rsq of the VCC fitting

Rsqr	Unit	Mean	Median	Maximum	Minimum	StdDev	3sigma%
All 5 lots	ppm/V2	**0.999**	**0.999**	**1.000**	**0.998**	**0.000**	**0.13%**
K17133.7	ppm/V2	1.000	0.999	1.000	0.999	0.000	0.07%
K17157.8	ppm/V2	0.999	0.999	1.000	0.999	0.000	0.08%
K19225.1	ppm/V2	0.999	0.999	0.999	0.998	0.000	0.10%
K19863.1	ppm/V2	0.999	0.999	1.000	0.998	0.000	0.10%
K19920.1	ppm/V3	1.000	1.000	1.000	0.999	0.000	0.05%

3) Temperature coefficient of capacitance

The SBC18 MIM capacitor TCC was extracted from capacitance measurement done at 25°C and 125°C for 20 wafers across 5 lots. 24 sites per wafer were tested. Table 8 shows the mean, standard deviation, and 3σ variation of the TCC of MIM capacitors for different size capacitors that were measured. The results on capacitors with area of 50μm per side or less seem not meaningful because of the large TCC variation. The overall TCC of the capacitors is calculated by averaging TCC of capacitors of areas larger than 50μm per side. The average TCC's for four lots are listed in table 7. The lot to lot variation of TCC is small, as shown in Fig. 5. The average TCC for SBC MIM capacitor is about 20.6ppm/°C.

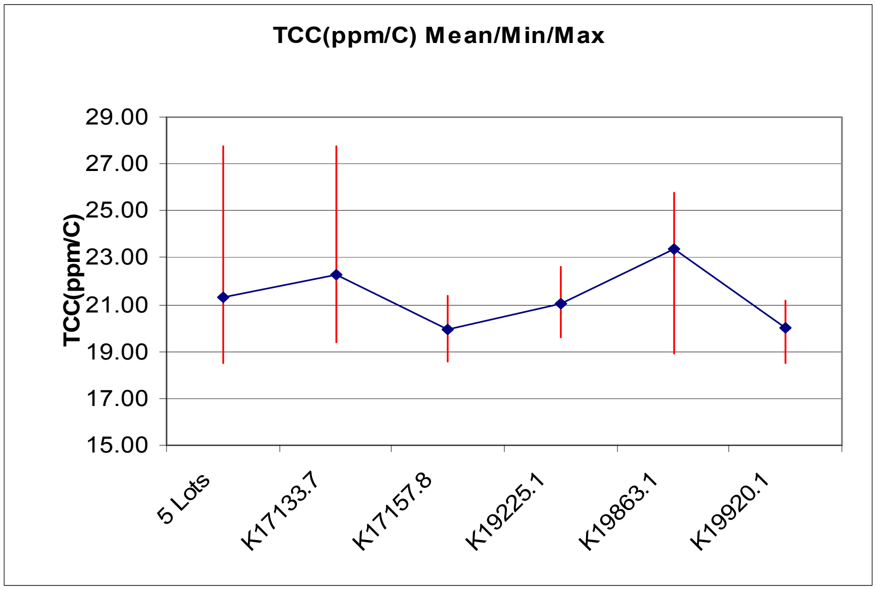
Table 8. Temperature coefficient for different sizes MIM capacitors

TCC of MIM	Unit	Mean	Median	Max	Min	Stdev	3s/M
TC10x10	ppm/C	94.16	31.71	463.31	0.77	143.32	457%
TC20x20	ppm/C	38.64	23.23	415.11	11.96	38.13	296%
TC50X50	ppm/C	29.44	21.47	44.89	18.50	10.49	107%
TC100X100	ppm/C	21.34	20.63	27.79	18.51	1.93	27%
TC200X200	ppm/C	20.62	20.22	22.63	18.20	0.84	12%
TC10X200X20	ppm/C	20.62	20.57	22.89	18.45	0.81	12%
TC10X10X20X20	ppm/C	19.59	19.54	21.84	17.40	0.82	13%
TCC(average)	ppm/C	**20.55**	**20.24**	**23.79**	**18.14**	**1.10**	**16%**

Table 9. Temperature coefficient of capacitance of SBC18 MIM capacitors 100x100um cell.

TCC on 100x100um	Unit	Mean	Median	Max	Min	Stdev	3s/M
5 Lots	**ppm/C**	**21.34**	**20.63**	**27.79**	**18.51**	**1.93**	**27.1%**
K17133.7	ppm/C	22.30	21.24	27.79	19.42	2.37	31.9%
K17157.8	ppm/C	19.96	19.98	21.38	18.59	0.55	8.3%
K19225.1	ppm/C	21.04	21.00	22.59	19.59	0.66	9.4%
K19863.1	ppm/C	23.40	24.03	25.78	18.90	1.73	22.1%
K19920.1	ppm/C	20.00	20.01	21.17	18.51	0.53	8.0%

Fig. 5. Lot to lot variation of SBC18 MIM capacitor temperature coefficient (on 100x100um cell)



One wafer(wf#5) from K19225 was measured on analog tester at several different temperatures from –40C to 125C to check the linearity of the temperature coefficient. Fig 6 showed that the capacitance is linear over temperature in the measurement range. The TCC extracted from different temperature range is almost the same ~20ppm/C, as showed in table 10.

Fig. 6 Capacitance of 100x100um capacitor at different temperatures

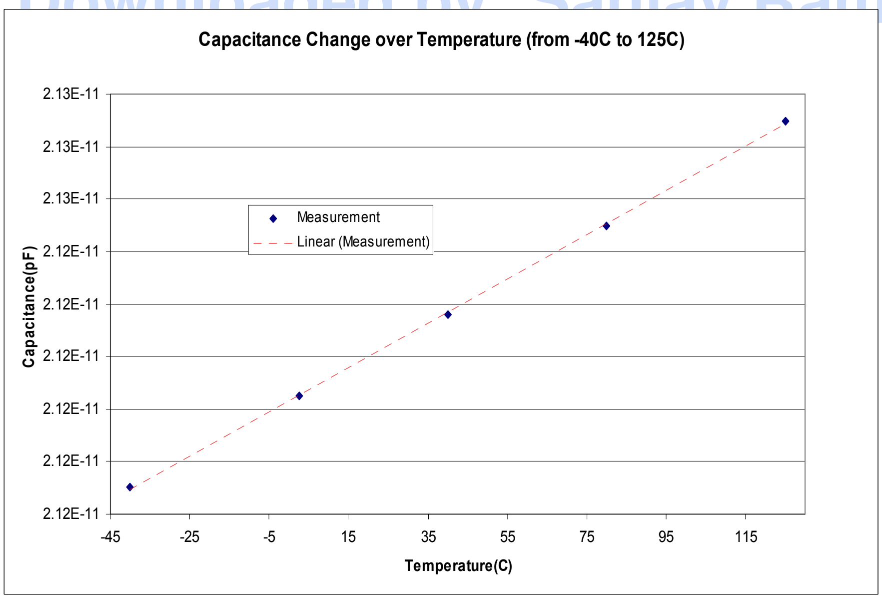


Table 10: TCC of 100x100um Capacitor Over Different Temperature Ranges

TCC in ppm/C	Mean	Median	Stdev	Min	Max	3 Sigma %
from -40C to 2.5C	19.28	19.27	0.64	17.93	20.26	10%
from 2.5C to 40C	19.55	19.49	0.58	18.54	20.55	9%
from 40C to 80C	19.95	19.95	0.58	19.09	20.97	9%
from 80C to 125C	20.86	20.81	0.56	19.92	22.09	8%
all range -40C to 125C	**19.96**	**20.05**	**0.39**	**19.28**	**20.55**	**6%**

Table 10: TCC of 100x100um Capacitor Over Different Temperature Ranges

12. 2fF/μm² MIM Capacitor Matching Characterization

Table of Contents

Summary

A matching characterization of 2fF/um2 MIM capacitors in the SBC18 process has been performed. The test structures, test procedures, and test conditions are described in the appendix. Although the characterization was carried out on SBC18QTD GA577 test chip, it is applicable to 2fF MIM capacitors for SBC18PT, QTD, QR, QW, and MW process.

Measurement Results

The characterization was performed on wafers processed in the SBC18 process using the GA577 engineering testchip. 24 dies on the following four lots were tested: K17157 wafers 20-25; and K19225 wafers 16 to 20, K19863 wafers 16 to 20, K19920 wf.17, 18, 20, 21, 22. Since the goal of this characterization is to measure the standard deviation of the difference between two devices, a relatively large sample size is required to obtain useful results. In this characterization the sample size is reasonable, as we have measured 100 pairs per lot for each parameter.

Two types of screening have been performed on the data. The first is based on the Rsquared values provided by the linear least squares regression and the second is based on removing data points outside of three sigma limits. We have observed that the relationship between Vin and Vout for correctly functioning test structures is extremely linear, as evidenced by Rsquared values which are normally better than 0.99999. We have used this property to provide a very useful screening mechanism. The second screening method is 3 sigma screening.

For matching measurements involving a large number of samples, it is almost inevitable that there will be a few “bad points” which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these “bad points,” it is important to remove them before calculating statistics. To efficiently perform this operation, a second screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3 sigma limits. The standard deviation is then recalculated for the remaining points, and again, all points outside of the 3 sigma limits are removed. This process continues until all data points are within the 3 sigma limits of the distribution. The 3 sigma limits should only cause problems for very large sample sizes.

The following tables present the matching results first for each lot separately and then for all of the lots analyzed together. The tables contain the mean matching, 3 sigma matching, and the yield after completing all of the screening operations.

MIM Capacitor Matching Data

MIM Capacitor Pairs Without Dummy

MIM Capacitor pairs without dummy					
Size	Nom. Cap. (pF)	Mean Delta C %	3 Sigma Delta C %	Mean/3 Sigma Delta C	Yield(%)
5x5um	0.05	0.2109	0.6148	34.31%	100%
20x20um	0.8	-0.0189	0.0300	-62.89%	99%
30x30um	1.8	0.0005	0.0209	2.63%	99%
45x45um	4.05	-0.0020	0.0162	-12.24%	99%
70x70um	9.8	-0.0011	0.0185	-5.97%	99%
100x100um	20	-0.0007	0.0241	-3.01%	100%
200x200um	80	-0.0026	0.0469	-5.54%	98%

Note: The nominal capacitance was calculated using 2fF/μm^2 area capacitance.

MIM Capacitor Common Centroid With Separate Bottom Plate

MIM Capacitor Common Centroid with Separate Bottom Plate					
Size	Nominal Capacitance	Mean Delta C %	3 Sigma Delta C %	Mean/3 Sigma Delta C	Yield(%)
10x10um	0.2	-0.0241	0.1035	-23.30%	97%
20x20um	0.8	0.0080	0.0270	29.61%	100%
45x45um	4.05	0.0038	0.0107	35.35%	99%
70x70um	9.8	0.0011	0.0058	18.50%	99%
100x100um	20	0.0013	0.0040	32.45%	99%
200x200um	80	-0.0002	0.0030	-7.89%	98%

MIM Capacitor Pairs with 20um Space

MIM Capacitor Pairs with 20um Space					
Size	Nominal Capacitance	Mean Delta C %	3 Sigma Delta C %	Mean/3 Sigma Delta C	Yield(%)
10x10um	0.2	-0.1884	0.4464	-42.22%	100%
20x20um	0.8	0.0016	0.0384	4.09%	99%
45x45um	4.05	0.0009	0.0174	4.95%	100%
100x100um	20	-0.0011	0.0285	-3.78%	99%

MIM Capacitor Pairs with 50um Space

MIM Capacitor Pairs with 50um Space					
Size	Nominal Capacitance	Mean Delta C %	3 Sigma Delta C %	Mean/3 Sigma Delta C	Yield(%)
10x10um	0.2	-0.1610	0.2559	-62.91%	100%
20x20um	0.8	0.1463	0.2465	59.35%	100%
100x100um	20	0.0051	0.0358	14.21%	99%

MIM Capacitor Pairs with 100um Space

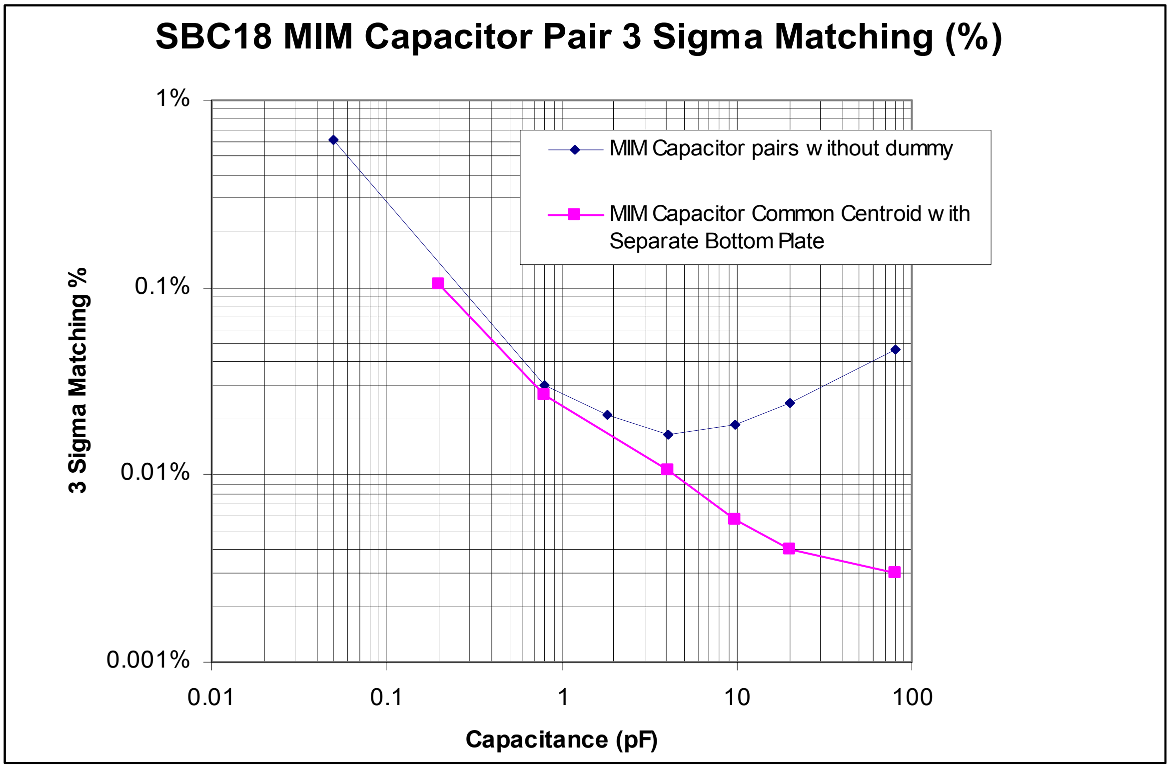
MIM Capacitor Pairs with 100um Space					
Size	Nominal Capacitance	Mean Delta C %	3 Sigma Delta C %	Mean/3 Sigma Delta C	Yield(%)
100x100um	20	0.0015	0.0464	3.21%	98%

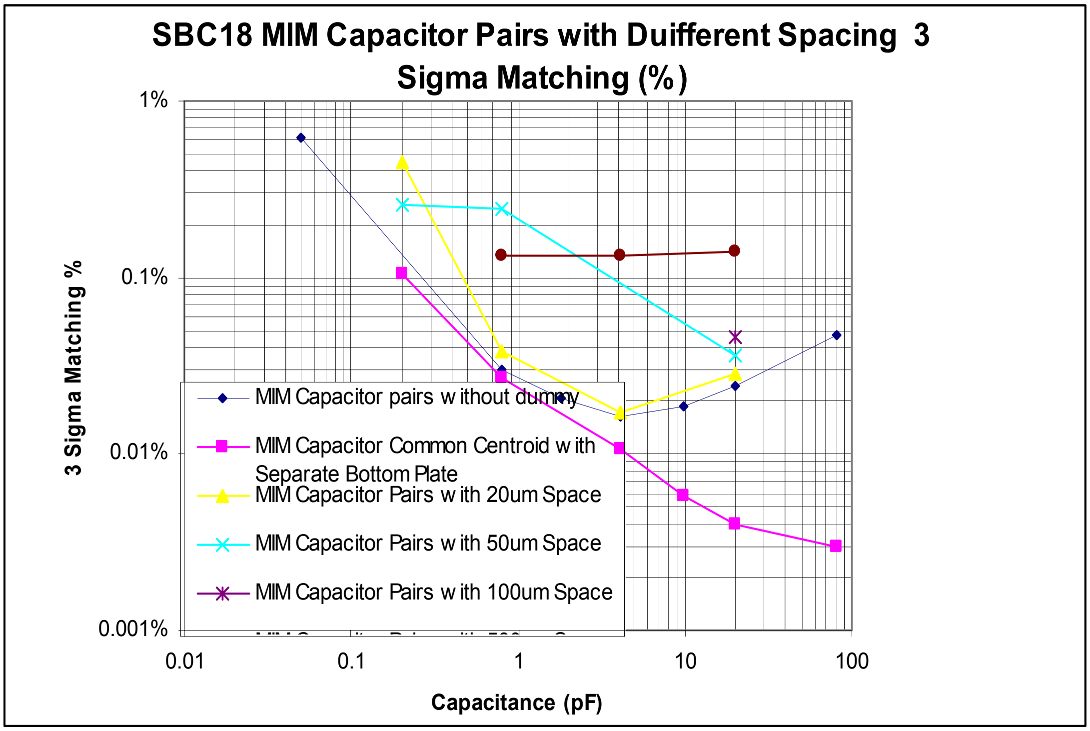
MIM Capacitor Pairs with 500um Space

MIM Capacitor Pairs with 500um Space					
Size	Nominal Capacitance	Mean Delta C %	3 Sigma Delta C %	Mean/3 Sigma Delta C	Yield(%)
20x20um	0.8	-0.0174	0.1344	-12.93%	99%
45x45um	4.05	0.0309	0.1318	23.44%	100%
100x100um	20	-0.0014	0.1392	-1.01%	99%

MIM Capacitor Plots

The following plot summarizes the matching data for all of the MIM capacitors:




SBC18 MIM Capacitor Pairs with Duifferent Spacing 3 Sigma Matching (%)
3 Sigma Matching %
1%
0.1%
0.01%
0.001%
0.01
0.1
1
10
100
Capacitance (pF)
MIM Capacitor pairs w ithout dummy
MIM Capacitor Common Centroid w ith Separate Bottom Plate
MIM Capacitor Pairs w ith 20um Space
MIM Capacitor Pairs w ith 50um Space
MIM Capacitor Pairs w ith 100um Space

Appendix: Test Structure and Test Description

Test Structures

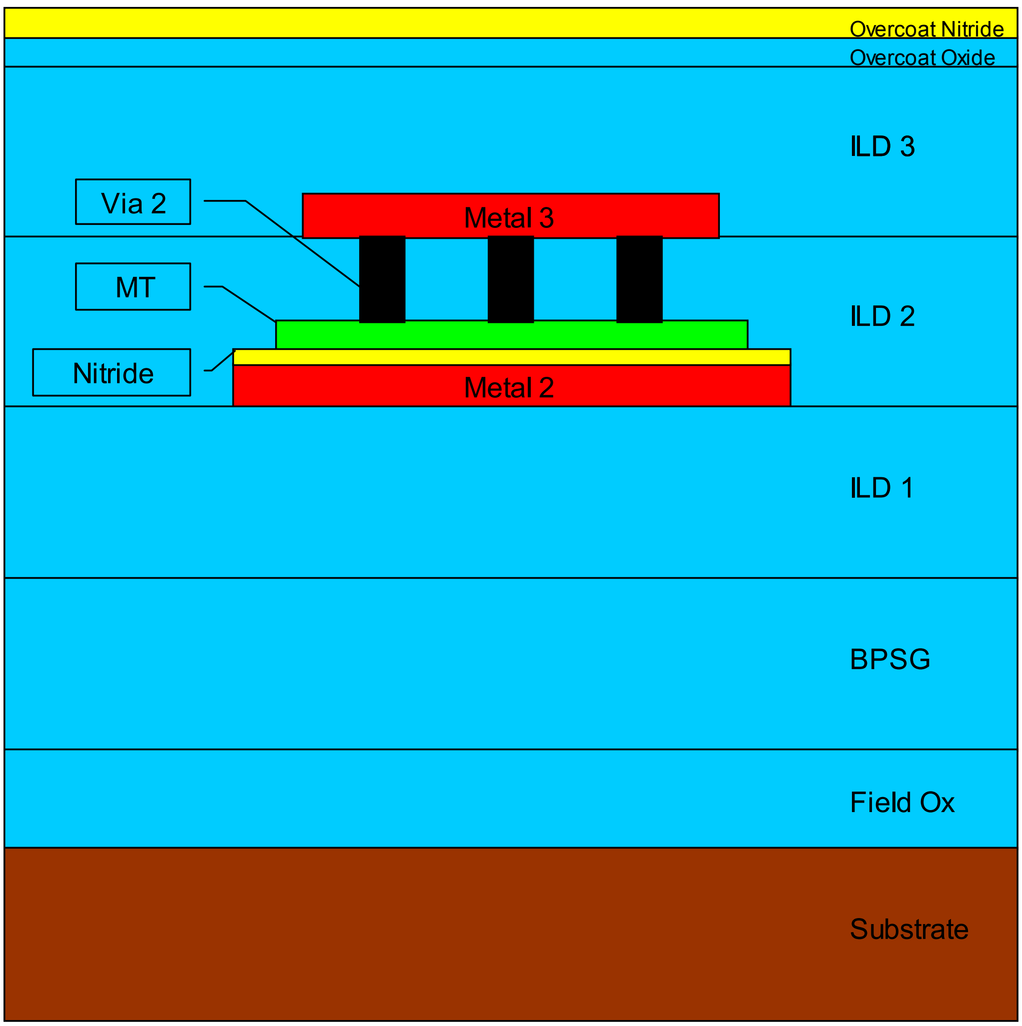
The GA577 SBC18 process test chip was used for this characterization. This testchip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There is 1 module devoted to capacitor matching on the GA577. The capacitor matching modules each contain 28 capacitor pairs. The types of layouts are as follows: pairs without dummy, pairs with dummy, common centroid pairs with dummy, and various spaced pairs.

MIM Capacitor Test Structures

MIM Capacitor Cross Section

The following picture shows a cross section of a single MIM capacitor over field without dummy:



Note: This cross section is not drawn to scale.

MIM Capacitor Pairs without Dummy

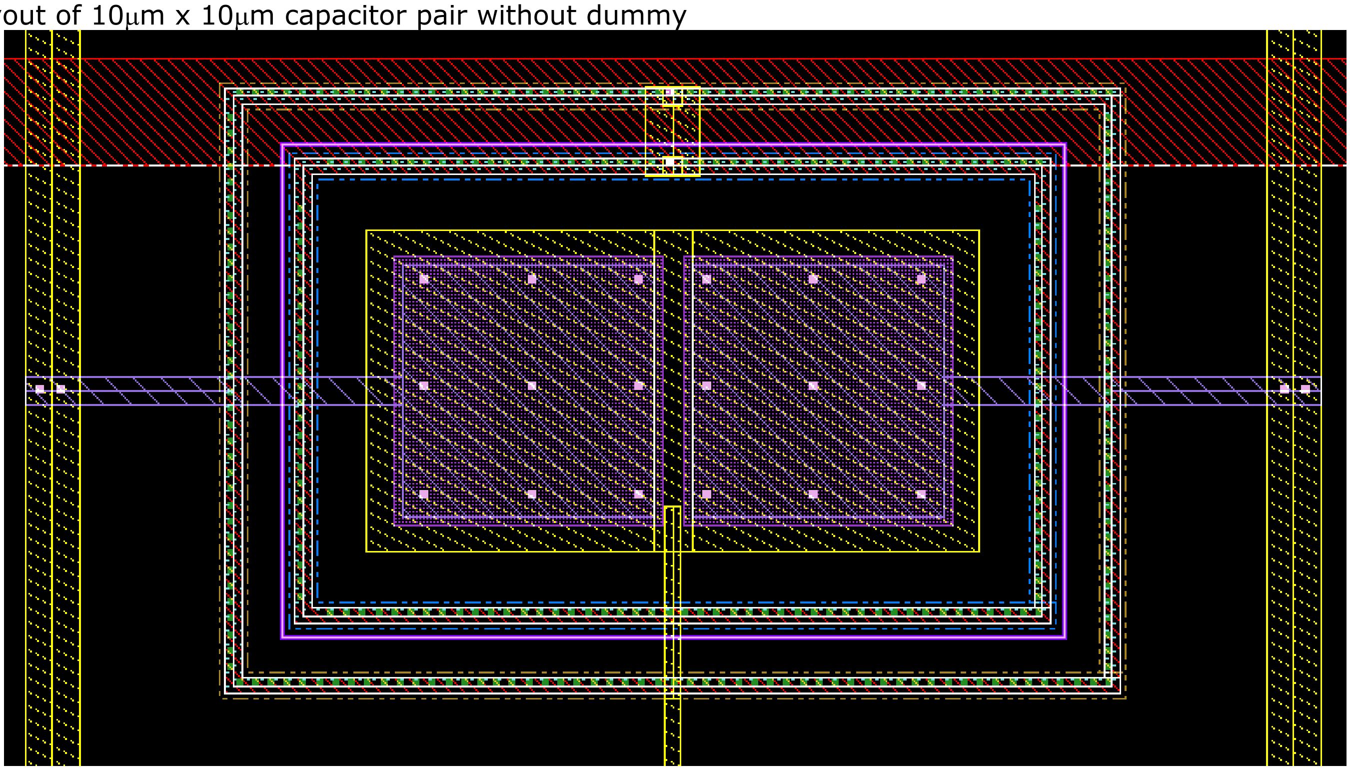
These pairs are composed of a single bottom plate with two capacitor top plates at minimum spacing. The metal 2 bottom plate has minimum overlap of the TM top plate, and the bottom plate is connected directly through metal 2. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Cell Size	Area	Perimeter	Nominal Capacitance
5µm x 5µm	100µm^2	40µm	0.104 pF
20µm x 20µm	400µm^2	80µm	0.408 pF
30µm x 30µm	900µm^2	120µm	0.912 pF
45µm x 45µm	2025µm^2	180µm	2.043 pF
70µm x 70µm	4900µm^2	280µm	4.928 pF
100µm x 100µm	10000µm^2	400µm	10.04 pF
200µm x 200µm	40000µm^2	800µm	40.08 pF

Note: The nominal capacitance is calculated for 1.0fF/µm^2 and 0.1fF/µm.

Layout of 10µm x 10µm capacitor pair without dummy



MIM Capacitor Pairs with Various Spacing (20μm, 50μm, 100μm, and 500μm)

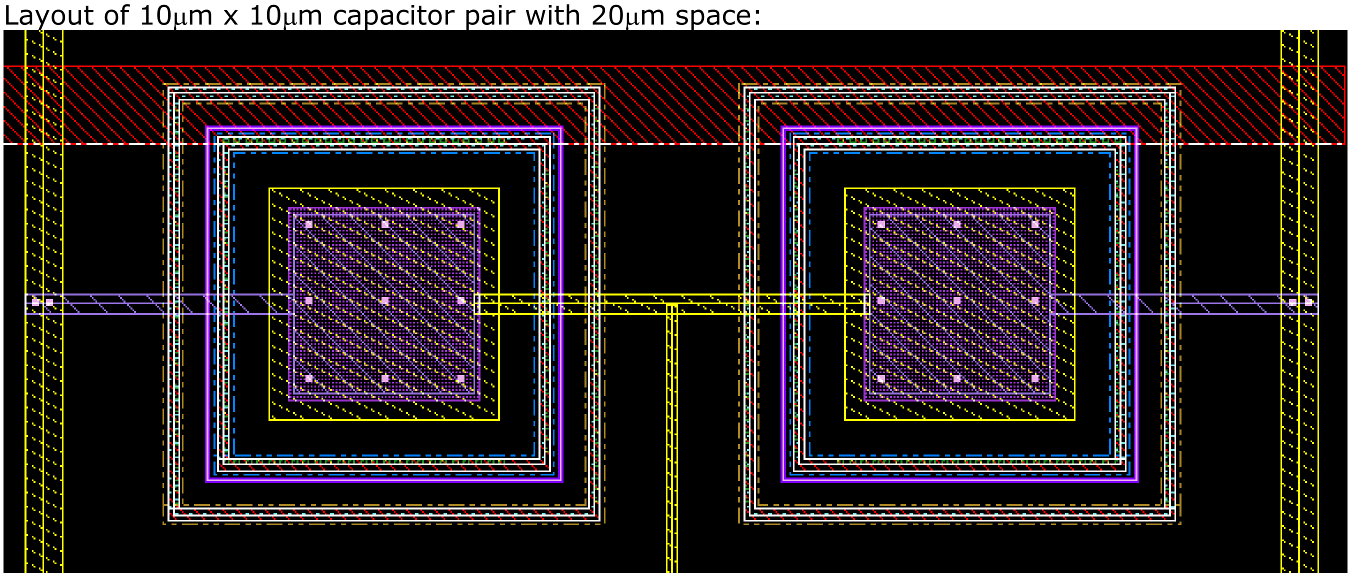
These pairs are composed of separate top and bottom plates separated by various distances (20μm, 50μm, 100μm, and 500μm). The separation distance is defined as the distance between the TM edges. The metal 2 bottom plates have minimum overlap of the TM top plates, and the bottom plats are connected together through a small metal 2 interconnect. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Cell Size	Area	Perimeter	Nominal Capacitance
10μm x 10μm	100μm^2	40μm	0.104 pF
20μm x 20μm	400μm^2	80μm	0.408 pF
45μm x 45μm	2025μm^2	180μm	2.043 pF
100μm x 100μm	10000μm^2	400μm	10.04 pF

Note: The nominal capacitance is calculated for 1.0fF/μm^2 and 0.1fF/μm.

Layout of 10μm x 10μm capacitor pair with 20μm space:



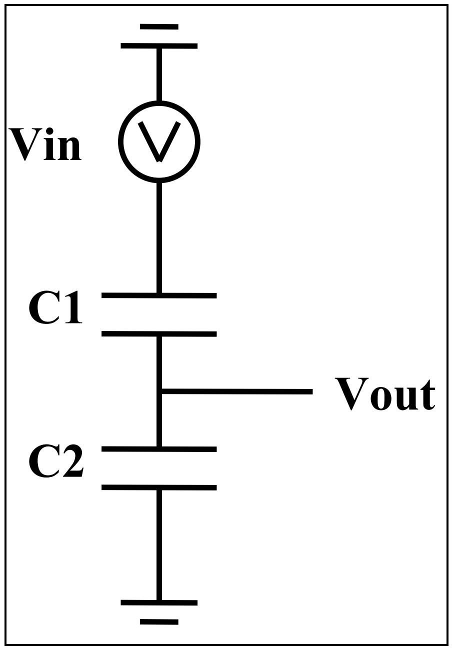


Figure 14: Capacitor Voltage Divider

<u>Test Circuit Description</u>

From our experience, it is impractical to measure capacitor matching by simply measuring the capacitance of adjacent capacitors with a capacitance meter. From our characterization of the C06TA process, we found that our current measurement system can reliably measure the mismatch only if it is greater than approximately 0.5%. Due to circuit designs which require 10 bit matching, we need to be able to measure the matching with an accuracy better than 0.1%. While some groups have been able to obtain reasonable measurements by simply measuring capacitance, they have been required to make significant modifications to their test systems. Due to the difficulty in setting up and maintaining such a test setup, we have chosen to use a different approach based upon a capacitor voltage divider.

The basic circuit used to measure the matching of capacitor pairs is a simple capacitor voltage divider as shown in figure 1. From basic circuit theory, the ratio of the applied voltage to the voltage between the two capacitors is:

$$Vout = Vin * \frac{C1}{C1 + C2}$$

Unfortunately, it is impractical to connect a voltmeter directly to the Vout node of the divider. As shown in figure 2, any practical voltmeter (including the probes, cabling, and switch matrix) will have parasitic capacitances and leakages which will be too large to allow a direct measurement to be performed. Several approaches have been proposed to overcome this problem, but the one we have chosen to use is probably the simplest one, yet it obtains the highest accuracy[1]. The basic concept of this circuit is to use an on chip buffer amplifier to allow the voltage ratio of the capacitor divider to be measured off chip with a standard voltmeter. The fundamental properties of a buffer amplifier are high input impedance, low output impedance, and a voltage gain of one.

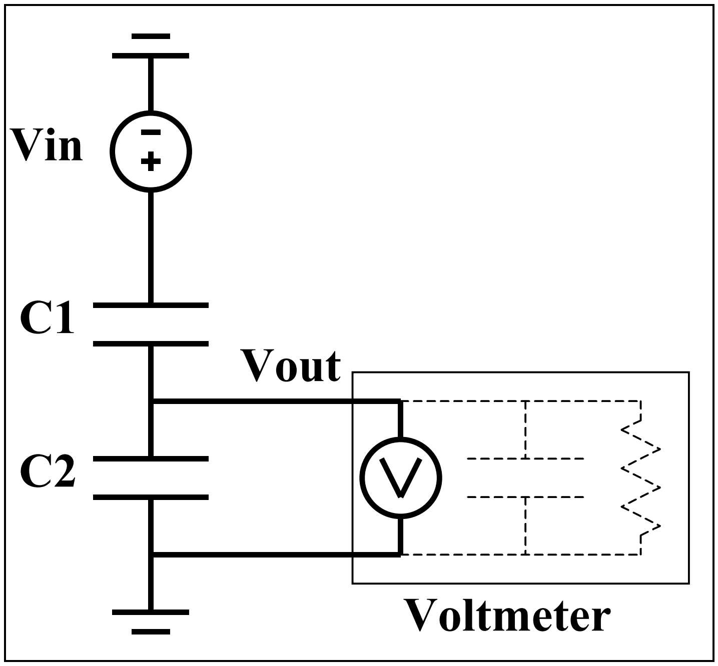


Figure 15: Capacitor Voltage Divider with a Simple Voltmeter Model

The circuit is shown in figure 3, and it uses a single PFET in common drain configuration as the buffer amplifier. Since the input to the amplifier is the PFET gate, the input impedance is determined by the gate leakage, which should be negligible. The output impedance of this circuit is also negligible. The voltage gain is determined by the biasing and IV characteristics the PFET. An external current source is used to bias the amplifier, so the current source should be nearly ideal, and it should have high output impedance. A relatively long and narrow (2μm x 10μm) PFET has been used with a 1μA bias current to ensure that the amplifier is very linear.

There are two properties of this amplifier which prevent us from making direct measurements of the capacitor voltage ratio. The first is the DC shift in the output voltage between the input and output, and the second is the parasitic capacitance caused by interconnect and the PFET. While common drain amplifier configuration provides a voltage gain of one, there is a DC voltage offset between the input node (Vfloat) and the output node (Vout) equal to Vgs. The exact value of this offset voltage is unknown, as each transistor will have a slightly different Vgs at the bias current of 1μa. In order to circumvent this problem, we can simply apply a range of input voltages and measure the slope of the output voltages. The slope (S) of Vout relative to Vin is equal to

$$S = \frac{C1}{C1 + C2}$$

as shown in figure 4. It can be shown that the capacitor matching can be determined from the slope by the following equation:

$$\frac{\Delta C}{C} = 4S - 2$$

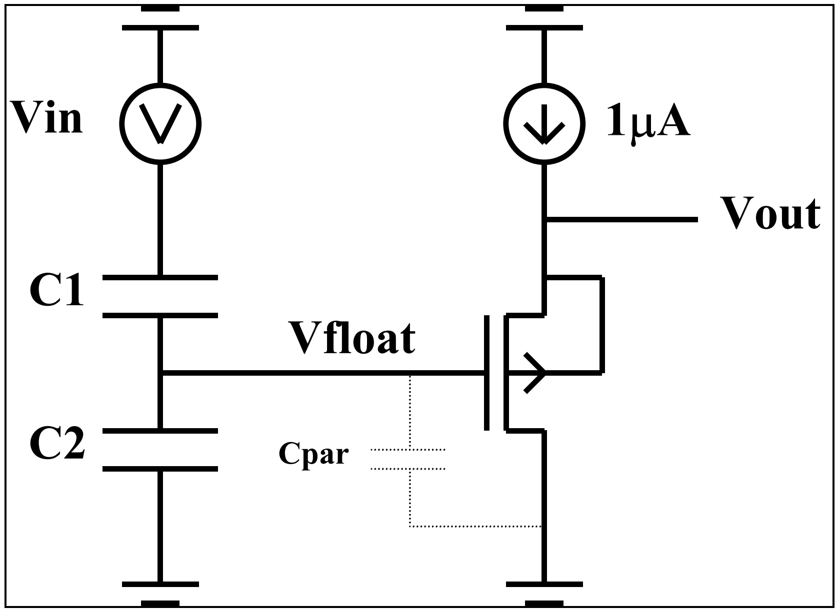


Figure 16: Schematic Diagram of Capacitor Matching Circuit

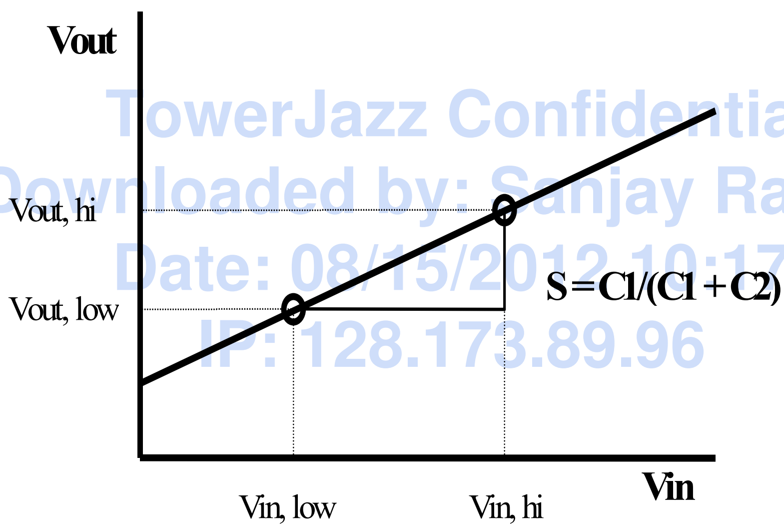


Figure 17: Input/Output Voltage of Capacitor Matching Circuit

The parasitic capacitance is also unknown, and since it is in parallel with C2, it will cause an offset equal to its value to the mismatch. If the parasitic capacitance is included, the equation for the slope is

$$S = \frac{C1}{C1 + C2 + Cpar}$$

This problem can be solved to first order by measuring the slope in the standard (forward) configuration, reversing the connections between C1 and C2, and then remeasuring the slope in the in the reverse configuration. With both the forward and reverse slopes, we can calculate the capacitor matching using the following equations

Forward Slope: $S1 = \frac{C1}{C1 + C2 + Cpar}$

Reverse Slope: $S2 = \frac{C2}{C1 + C2 + Cpar}$

$$\frac{\Delta C}{C} = 2\frac{S1 - S2}{S1 + S2} = 2\frac{C1 - C2}{C1 + C2}$$

By measuring the slope in both directions, the parasitic capacitance can be canceled out of the equation. Since the only physical change to the circuit is the connections to the two capacitors, we can to first order assume that the parasitic capacitance is the same for both configurations, and cancels out exactly.

Figure 5 shows the layout methodology of the capacitor pair matching test structure. Since the matching of capacitor pairs is very sensitive to layout, we have tried to maintain perfect symmetry wherever possible. The capacitors are mirror images of each other, and the interconnect also has mirror symmetry.

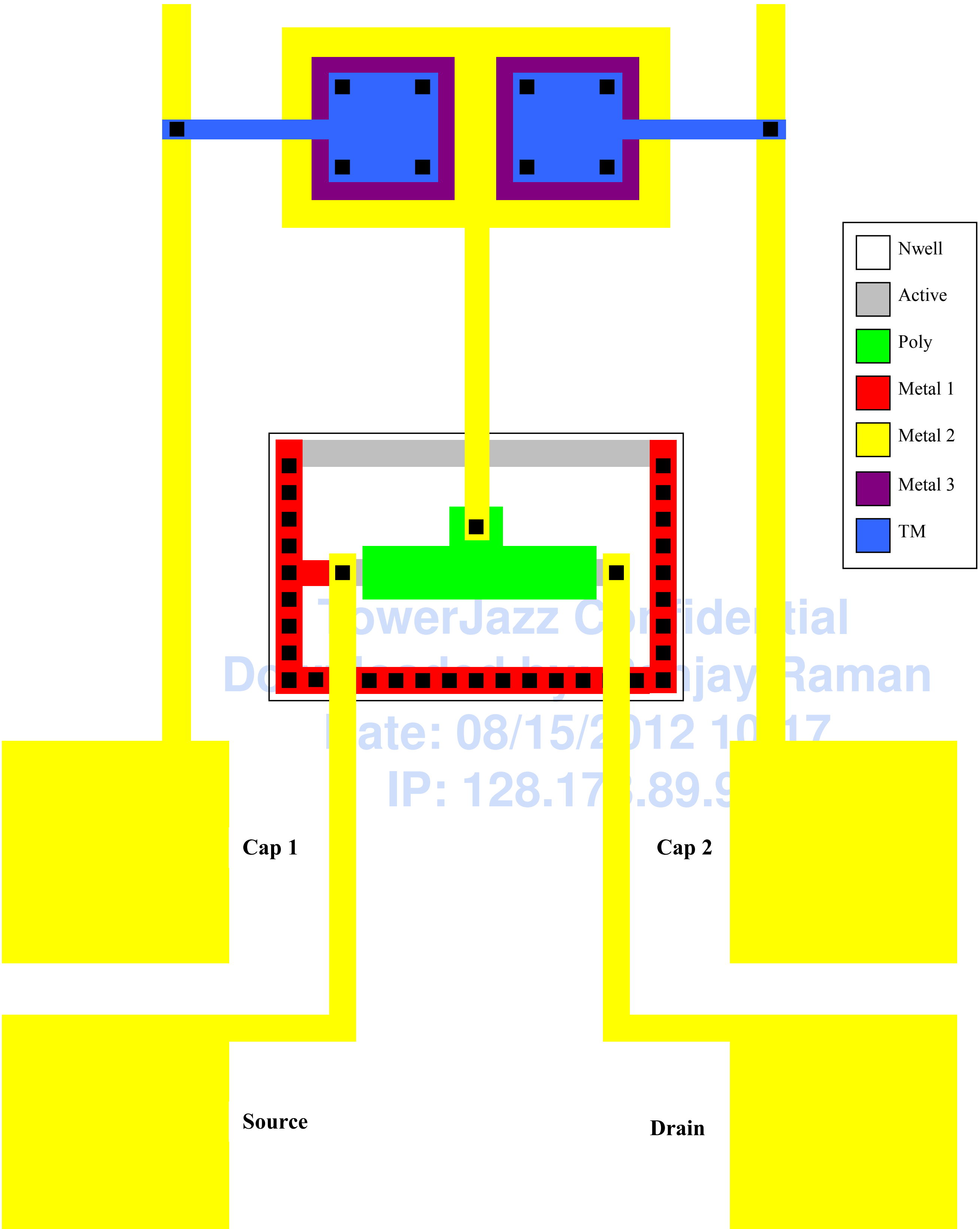


Figure 18: Layout of Capacitor Pair Matching Test Structure (Not to Scale)

Test Description

The capacitor matching test was performed on the Reedholm tester, which is a commercial high speed parametric tester. This tester is based on a single non-integrating 16 bit DMM, but by averaging hundreds of samples over one power line cycle, it is able to produce good results. The following tests were used in this characterization:

Contact - Measures the contact resistance of the probe tips. We have a module on the testchip which is designed specifically to check whether the probes are properly contacting the pads. This module has small metal 1 resistors between the adjacent pads in each row (e.g. pad 1 is connected to pad 17, pad 2 is connected to pad 18, etc.). The contact test is the first test performed on each die, and it verifies that the resistance of each pair of pads is less than a set value. If the probe resistance is greater than 30 Ohms, the tester stops to allow the probes to be checked.

Cmatch - Measures the matching of capacitor pairs. The test setup provides for connection inputs (C1, C2, Drain, Source, Body), bias inputs (Start Vin, Stop Vin, Step Vin, I Source, V Source Compliance), and the ability to save the raw Vout data. The following tables describe the measurement connections for this test:

Forward Measurement	
Pad	SMU
Cap #1	3
Cap #2	4
Drain	1
Source	2
Substrate	4

Reverse Measurement	
Pad	SMU
Cap #1	4
Cap #2	3
Drain	1
Source	2
Substrate	4

The following steps describe the measurement:
Connect the terminals as shown for the forward measurement. Ground the Cap #2, Drain, and Substrate node. Force a 1μA current into the Source node. Sweep the Cap #1 node (Vin) from 0V to 3V using 0.3V steps while measuring the voltage at the Source node (Vout).
Calculate the forward slope, intercept, and Rsquared between Vout and Vin through a linear least squares regression. Since the Rsquared values are so close to 1, the value reported is actually 1 – Rsquared.
Connect the terminals as shown for the reverse measurement. Ground the Cap #1, Drain, and Substrate node. Force a 1μA current into the Source node. Sweep the Cap #2 node (Vin) from 0V to 4V using 0.4V steps while measuring the voltage at the Source node (Vout).
Calculate the reverse slope, intercept, and Rsquared between Vout and Vin through a linear least squares regression. Since the Rsquared values are so close to 1, the value reported is actually 1 – Rsquared.
Calculate the percent matching from the following formula:

$$\frac{\Delta C}{C} = 2\frac{S1 - S2}{S1 + S2} = 2\frac{C1 - C2}{C1 + C2}$$

This test reports the percent matching, forward slope, forward intercept, forward Rsquared, reverse slope, reverse intercept, and reverse Rsquared.

13. 1fF/μm^2 MIM Capacitor Matching Characterization

Table of Contents

Summary

The matching properties of the capacitors from the SBC18 process have been characterized. These devices are available in the sbc18hx process variant. The test structures, test procedures, and test conditions are described. The measurement results are presented, but no attempt has been made to provide a model to describe the results.

Measurement Results

Since the goal of this characterization is to measure the standard deviation of the difference between two devices, a relatively large sample size is required to obtain useful results. In this characterization the sample size is reasonable, as we have measured 100 pairs per lot for each parameter.

Two types of screening have been performed on the data. The first is based on the Rsquared values provided by the linear least squares regression and the second is based on removing data points outside of three sigma limits. We have observed that the relationship between Vin and Vout for correctly functioning test structures is extremely linear, as evidenced by Rsquared values which are normally better than 0.99999. Since it is difficult to read values so close to 1, for this characterization we will report the quantity (1 - Rsquared). Thus, we have based our initial screening on both the forward and reverse Rsquareds being less than 1e-5.

For matching measurements involving a large number of samples, it is almost inevitable that there will be a few “bad points” which are significantly outside the distribution which represents the rest of the data points. Since the standard deviation can be significantly affected by these “bad points,” it is important to remove them before calculating statistics. To efficiently perform this operation, a second screening operation is performed. This screening calculates the standard deviation of the distribution, and then removes all points outside of the 3 sigma limits. The standard deviation is then recalculated for the remaining points, and again, all points outside of the 3 sigma limits are removed. This process continues until all data points are within the 3 sigma limits of the distribution. Although it would be more appropriate to determine the limits as a function of sigma for the specific sample size, even for an ideal distribution, only 0.3 out of the 100 data points per lot in this characterization would be screened out. The 3 sigma limits should only cause problems for very large sample sizes.

The following tables present the matching results first for each lot separately and then for all of the lots analyzed together. The tables contain the mean matching, 3 sigma matching, and the yield after completing all of the screening operations.

Capacitor Matching Data

Lot B71077.1

Old Pairs

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.017%	0.270%	6.34%	100%
15µm x 15µm	0.23pF	0.000%	0.145%	1.14%	100%
20µm x 20µm	0.4pF	0.002%	0.095%	2.06%	100%
30µm x 30µm	0.9pF	0.002%	0.029%	32.71%	98%
45µm x 45µm	2.03pF	0.009%	0.014%	41.11%	96%
70µm x 70µm	4.9pF	0.006%	0.015%	27.68%	97%
100µm x 100µm	10pF	0.004%	0.016%	25.61%	94%

Pairs Without Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
20µm x 20µm	0.1pF	-0.020%	0.031%	-64.17%	100%
45µm x 45µm	0.23pF	-0.004%	0.012%	-34.65%	98%

Pairs With Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.010%	0.052%	-19.19%	99%
15µm x 15µm	0.23pF	-0.010%	0.032%	-32.68%	99%
20µm x 20µm	0.4pF	-0.002%	0.023%	-10.10%	99%
30µm x 30µm	0.9pF	-0.002%	0.019%	-8.62%	98%
45µm x 45µm	2.03pF	0.002%	0.013%	14.49%	98%
70µm x 70µm	4.9pF	0.000%	0.014%	0.29%	98%
100µm x 100µm	10pF	-0.003%	0.018%	-14.16%	96%

Two Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.004%	0.058%	-7.35%	99%
20µm x 20µm	0.23pF	0.003%	0.020%	12.91%	98%
45µm x 45µm	0.1pF	-0.002%	0.008%	-22.24%	98%
70µm x 70µm	0.23pF	-0.002%	0.012%	-19.81%	100%

Four Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.003%	0.057%	-6.13%	100%
20µm x 20µm	0.23pF	-0.002%	0.024%	-9.01%	99%
45µm x 45µm	0.1pF	0.001%	0.009%	5.89%	100%
70µm x 70µm	0.23pF	0.002%	0.012%	19.97%	99%

Eight Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.000%	0.060%	-0.17%	100%
20µm x 20µm	0.23pF	0.002%	0.029%	8.61%	99%
45µm x 45µm	0.1pF	0.003%	0.012%	20.93%	100%
70µm x 70µm	0.23pF	0.002%	0.006%	39.27%	100%

Lot B71078.1

Old Pairs

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.004%	0.154%	2.28%	99%
15µm x 15µm	0.23pF	-0.007%	0.076%	4.68%	97%
20µm x 20µm	0.4pF	0.004%	0.050%	-0.75%	99%
30µm x 30µm	0.9pF	0.000%	0.031%	25.09%	98%
45µm x 45µm	2.03pF	0.008%	0.015%	42.96%	97%
70µm x 70µm	4.9pF	0.006%	0.015%	23.45%	97%
100µm x 100µm	10pF	0.004%	0.017%	20.93%	96%

Pairs Without Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
20µm x 20µm	0.1pF	0.023%	0.024%	95.50%	100%
45µm x 45µm	0.23pF	0.015%	0.015%	97.40%	100%

Pairs With Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.014%	0.059%	23.30%	100%
15µm x 15µm	0.23pF	0.003%	0.039%	7.99%	100%
20µm x 20µm	0.4pF	0.006%	0.029%	19.96%	100%
30µm x 30µm	0.9pF	0.003%	0.021%	15.48%	98%
45µm x 45µm	2.03pF	0.003%	0.018%	18.63%	100%
70µm x 70µm	4.9pF	0.001%	0.022%	4.04%	100%
100µm x 100µm	10pF	-0.001%	0.023%	-2.81%	98%

Two Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.001%	0.063%	1.32%	100%
20µm x 20µm	0.23pF	0.005%	0.029%	18.29%	100%
45µm x 45µm	0.1pF	-0.001%	0.010%	-12.99%	100%
70µm x 70µm	0.23pF	-0.001%	0.013%	-8.03%	100%

Four Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.003%	0.078%	-4.23%	99%
20µm x 20µm	0.23pF	0.001%	0.031%	2.36%	100%
45µm x 45µm	0.1pF	0.001%	0.010%	13.36%	100%
70µm x 70µm	0.23pF	0.003%	0.012%	21.35%	100%

Eight Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.005%	0.085%	-5.52%	100%
20µm x 20µm	0.23pF	0.006%	0.036%	15.42%	100%
45µm x 45µm	0.1pF	0.003%	0.015%	19.30%	100%
70µm x 70µm	0.23pF	0.003%	0.006%	44.33%	100%

Lot B71446.1

Old Pairs

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.002%	0.192%	1.23%	99%
15µm x 15µm	0.23pF	-0.010%	0.089%	2.15%	99%
20µm x 20µm	0.4pF	0.002%	0.062%	-0.32%	96%
30µm x 30µm	0.9pF	0.000%	0.033%	26.27%	98%
45µm x 45µm	2.03pF	0.009%	0.015%	41.41%	96%
70µm x 70µm	4.9pF	0.006%	0.017%	29.96%	98%
100µm x 100µm	10pF	0.005%	0.021%	24.39%	98%

Pairs Without Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
20µm x 20µm	0.1pF	-0.020%	0.035%	-57.19%	100%
45µm x 45µm	0.23pF	-0.004%	0.013%	-29.94%	99%

Pairs With Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.008%	0.063%	-12.29%	100%
15µm x 15µm	0.23pF	-0.013%	0.042%	-30.39%	100%
20µm x 20µm	0.4pF	-0.003%	0.028%	-9.96%	95%
30µm x 30µm	0.9pF	-0.002%	0.022%	-8.44%	100%
45µm x 45µm	2.03pF	0.002%	0.015%	14.62%	96%
70µm x 70µm	4.9pF	0.001%	0.016%	3.54%	98%
100µm x 100µm	10pF	-0.001%	0.021%	-6.55%	97%

Two Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.001%	0.069%	1.93%	99%
20µm x 20µm	0.23pF	0.004%	0.025%	16.84%	100%
45µm x 45µm	0.1pF	-0.002%	0.010%	-17.16%	100%
70µm x 70µm	0.23pF	-0.001%	0.011%	-9.56%	100%

Four Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.007%	0.081%	-8.36%	99%
20µm x 20µm	0.23pF	0.000%	0.031%	-0.94%	99%
45µm x 45µm	0.1pF	0.001%	0.011%	8.28%	100%
70µm x 70µm	0.23pF	-0.001%	0.013%	-7.47%	98%

Eight Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.005%	0.077%	-7.03%	100%
20µm x 20µm	0.23pF	0.003%	0.033%	7.71%	100%
45µm x 45µm	0.1pF	0.002%	0.015%	13.13%	100%
70µm x 70µm	0.23pF	0.002%	0.006%	30.93%	99%

Lot B72069.1

Old Pairs

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.005%	0.181%	2.61%	93%
15µm x 15µm	0.23pF	-0.009%	0.093%	-0.81%	95%
20µm x 20µm	0.4pF	-0.001%	0.052%	3.65%	90%
30µm x 30µm	0.9pF	0.002%	0.033%	19.20%	89%
45µm x 45µm	2.03pF	0.006%	0.024%	23.24%	92%
70µm x 70µm	4.9pF	0.006%	0.025%	24.15%	97%
100µm x 100µm	10pF	0.006%	0.032%	19.00%	98%

Pairs Without Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
20µm x 20µm	0.1pF	0.002%	0.036%	5.78%	99%
45µm x 45µm	0.23pF	0.005%	0.013%	38.56%	97%

Pairs With Dummy

Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	-0.015%	0.070%	-21.78%	100%
15µm x 15µm	0.23pF	-0.009%	0.036%	-26.04%	100%
20µm x 20µm	0.4pF	-0.004%	0.026%	-15.41%	100%
30µm x 30µm	0.9pF	-0.003%	0.018%	-18.99%	98%
45µm x 45µm	2.03pF	0.000%	0.018%	-2.59%	100%
70µm x 70µm	4.9pF	0.000%	0.019%	-1.45%	98%
100µm x 100µm	10pF	-0.001%	0.026%	-3.89%	95%

Two Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.004%	0.065%	6.37%	98%
20µm x 20µm	0.23pF	0.006%	0.024%	25.82%	97%
45µm x 45µm	0.1pF	0.000%	0.010%	3.27%	99%
70µm x 70µm	0.23pF	0.003%	0.005%	52.24%	95%

Four Cell Pairs With Dummy

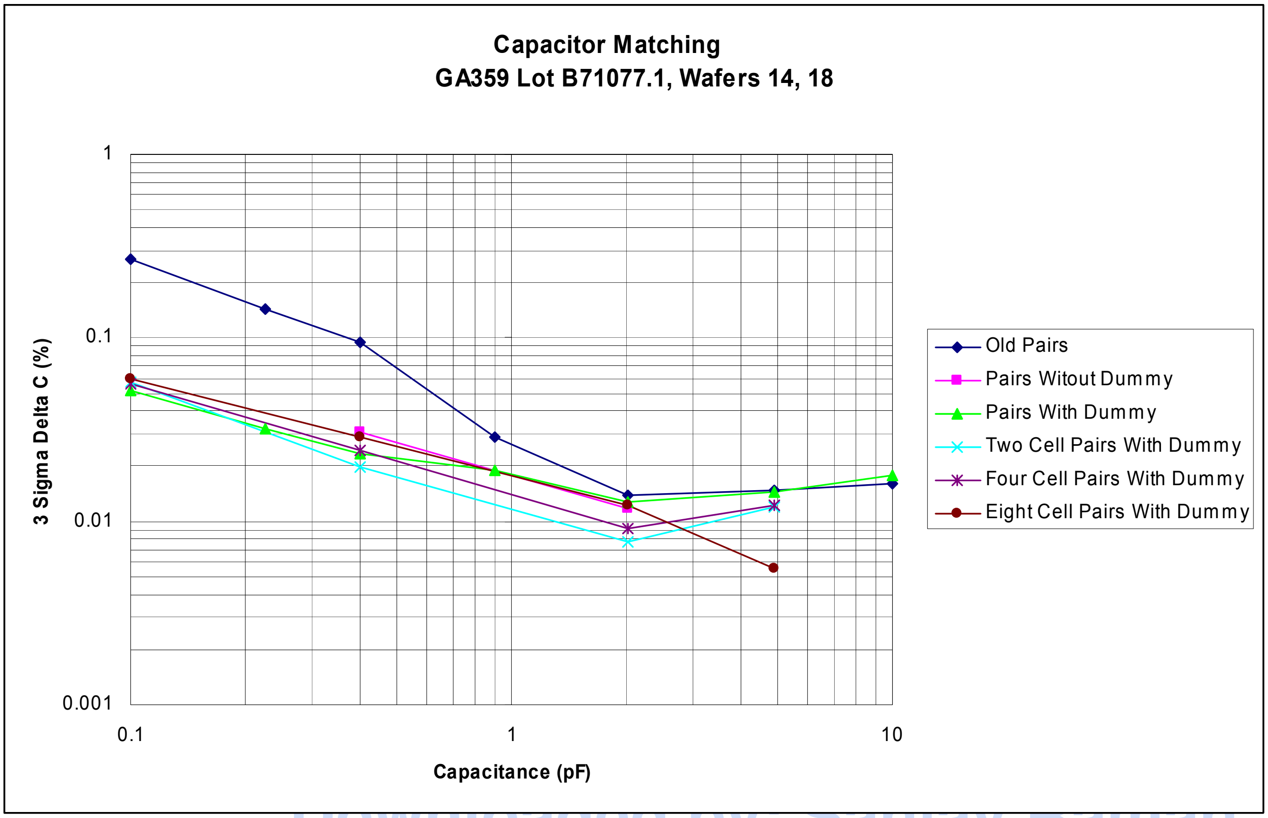
Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.001%	0.081%	0.70%	98%
20µm x 20µm	0.23pF	0.001%	0.029%	4.18%	100%
45µm x 45µm	0.1pF	0.004%	0.011%	37.19%	98%
70µm x 70µm	0.23pF	0.003%	0.009%	34.81%	98%

Eight Cell Pairs With Dummy

Equivalent Capacitor Size	Nominal Capacitance	Mean Delta C	3 Sigma Delta C	Mean/3 Sigma Delta C	Yield
10µm x 10µm	0.1pF	0.007%	0.083%	8.57%	98%
20µm x 20µm	0.23pF	0.007%	0.030%	23.93%	98%
45µm x 45µm	0.1pF	0.006%	0.011%	50.62%	93%
70µm x 70µm	0.23pF	0.003%	0.006%	48.50%	96%

Matching Plots by Lot

Lot B71077.1



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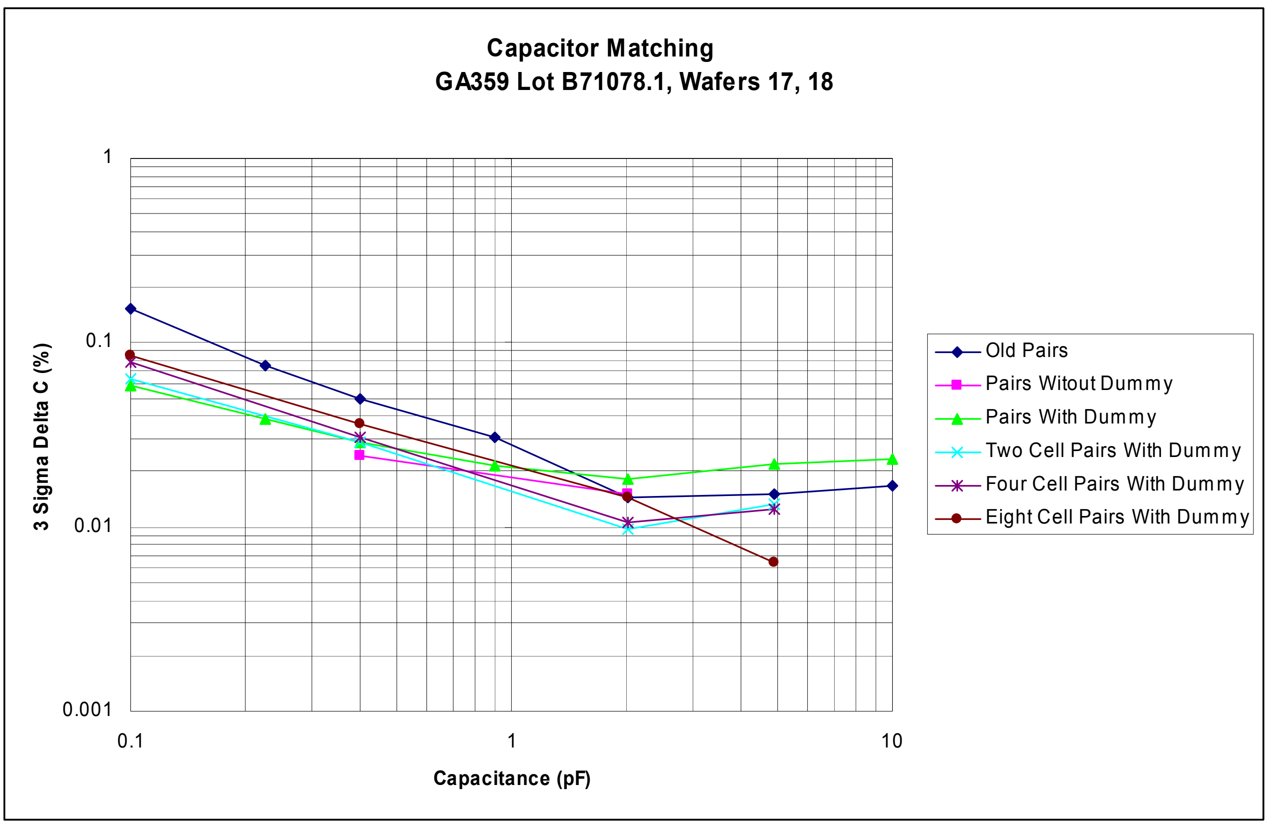

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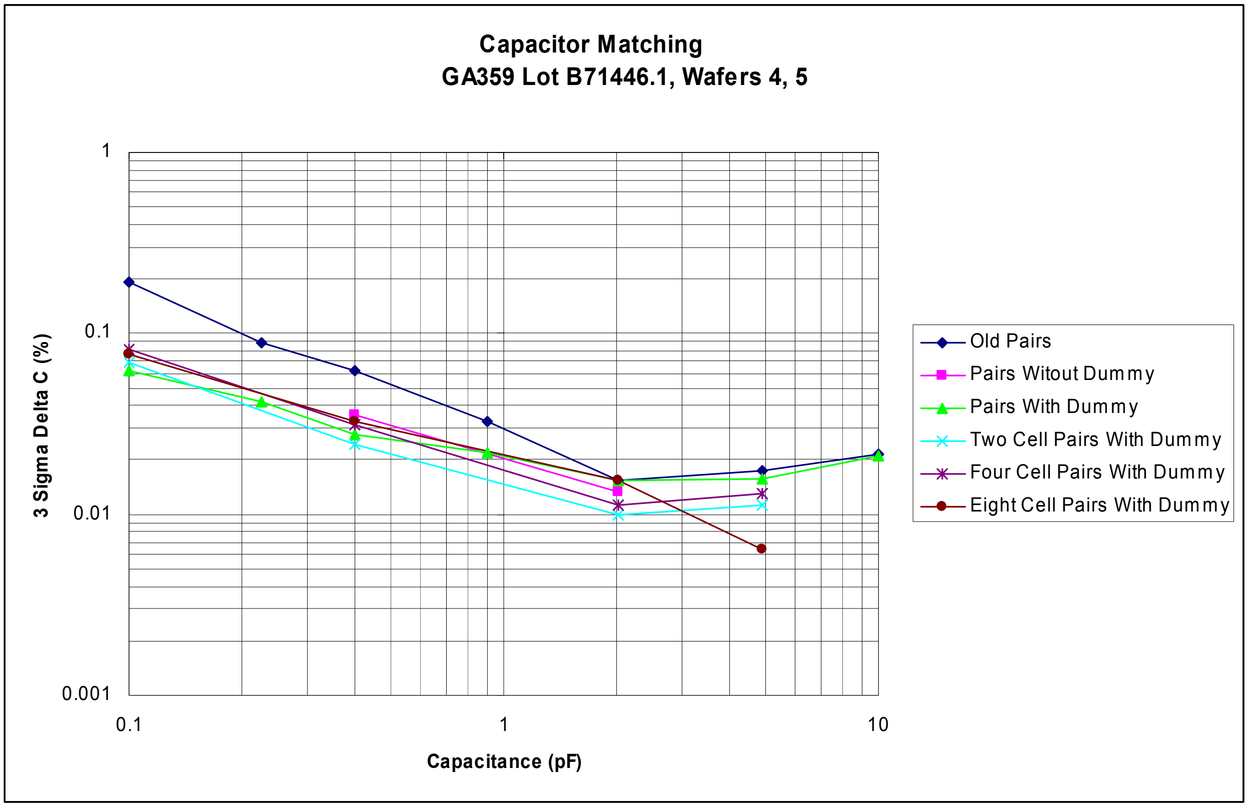
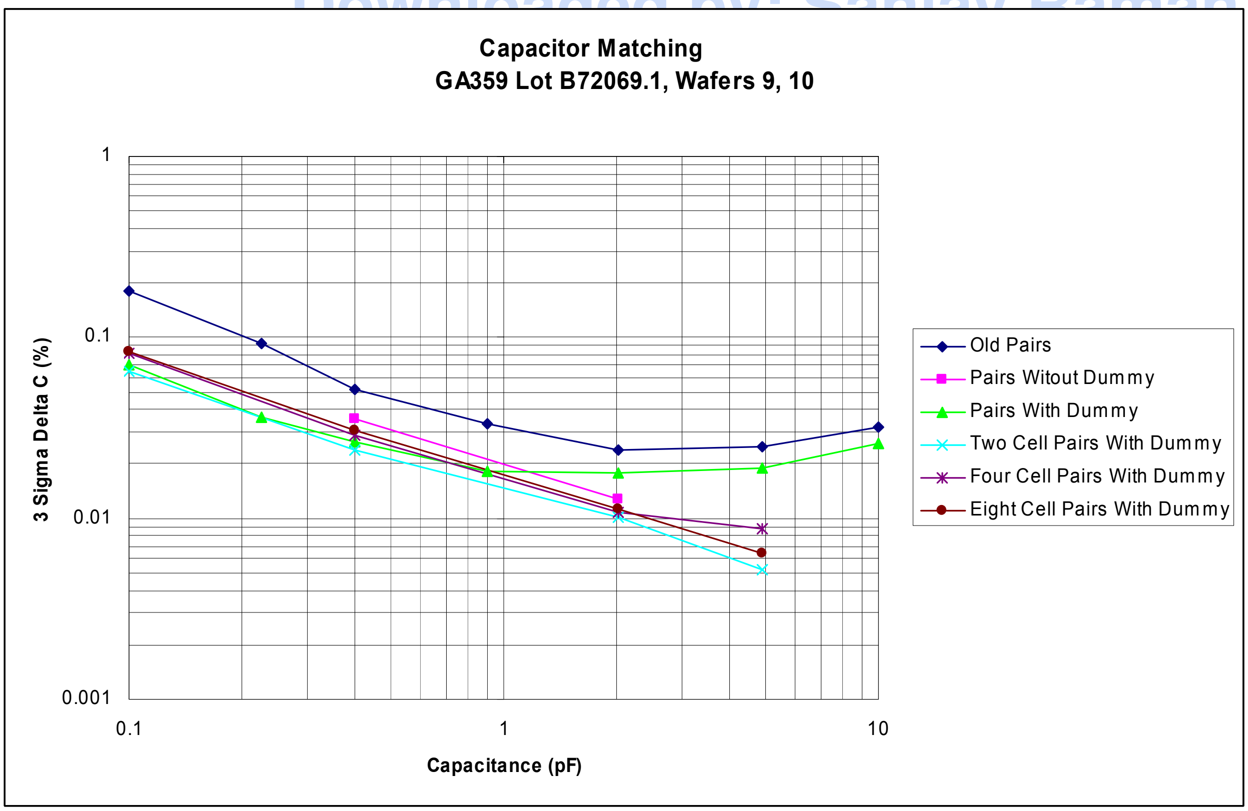
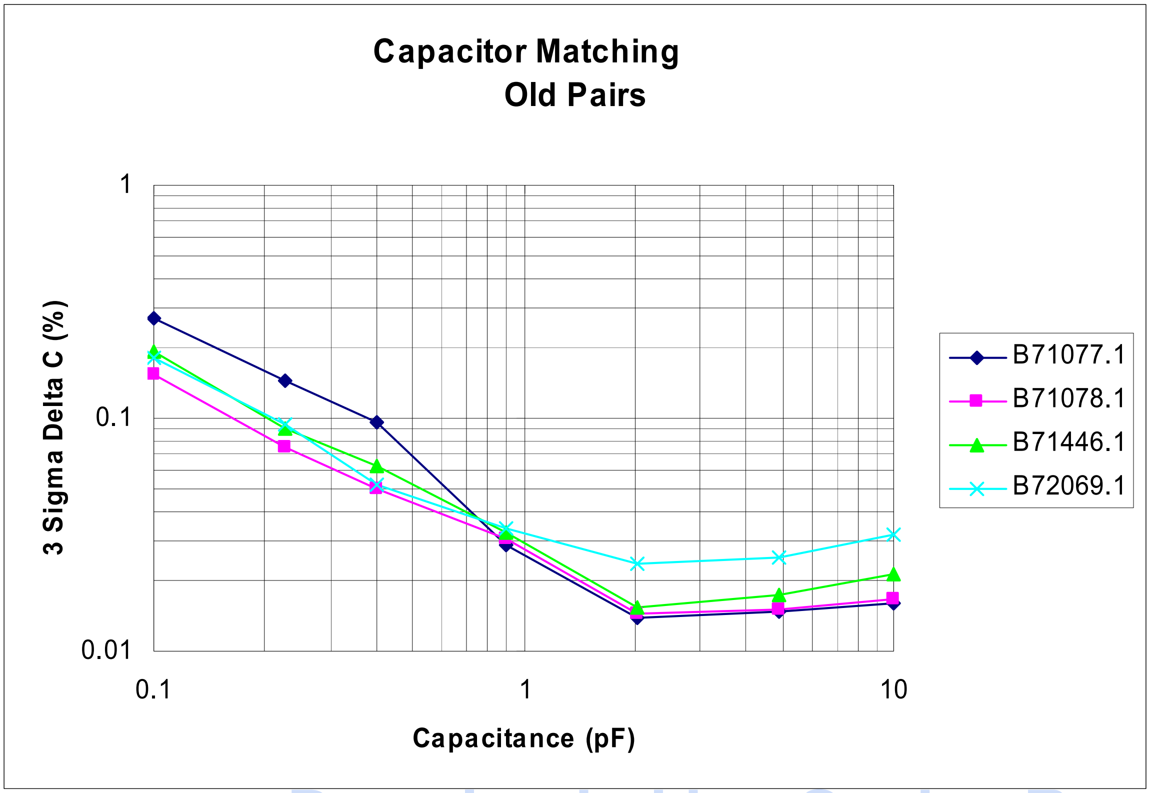


Lot B72069.1

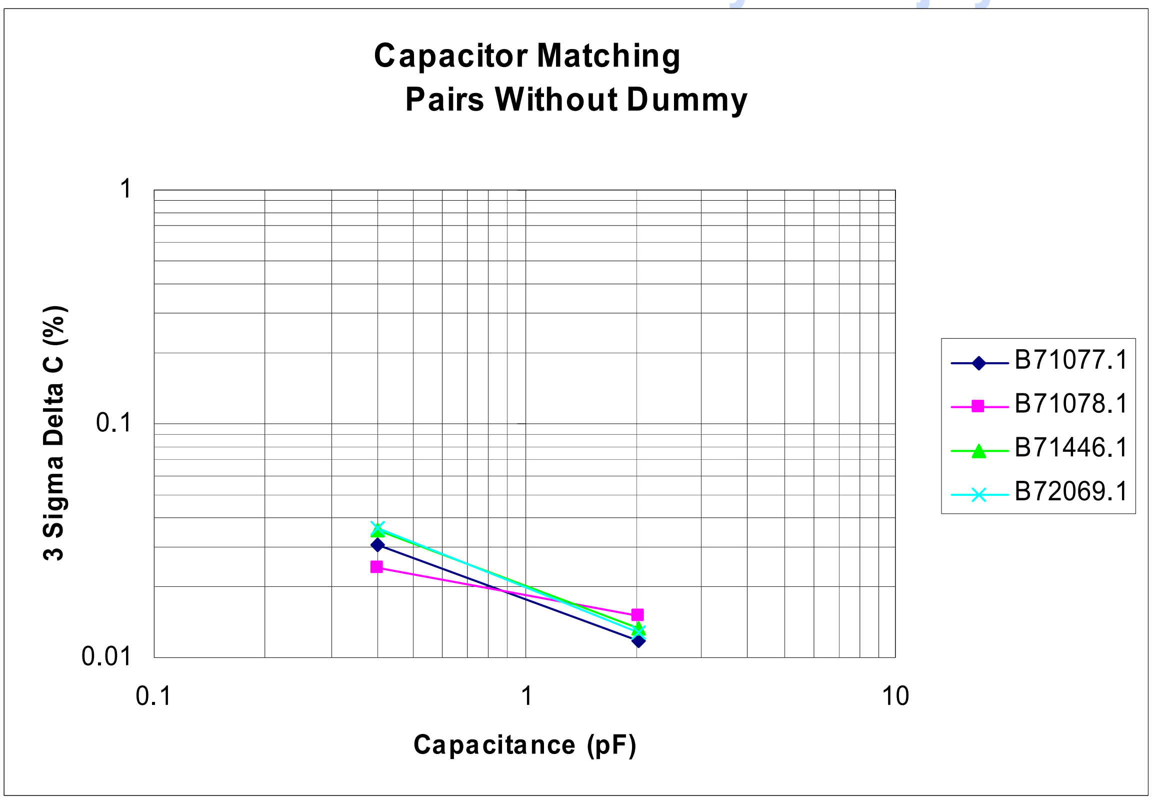


Matching Plots by Device Type

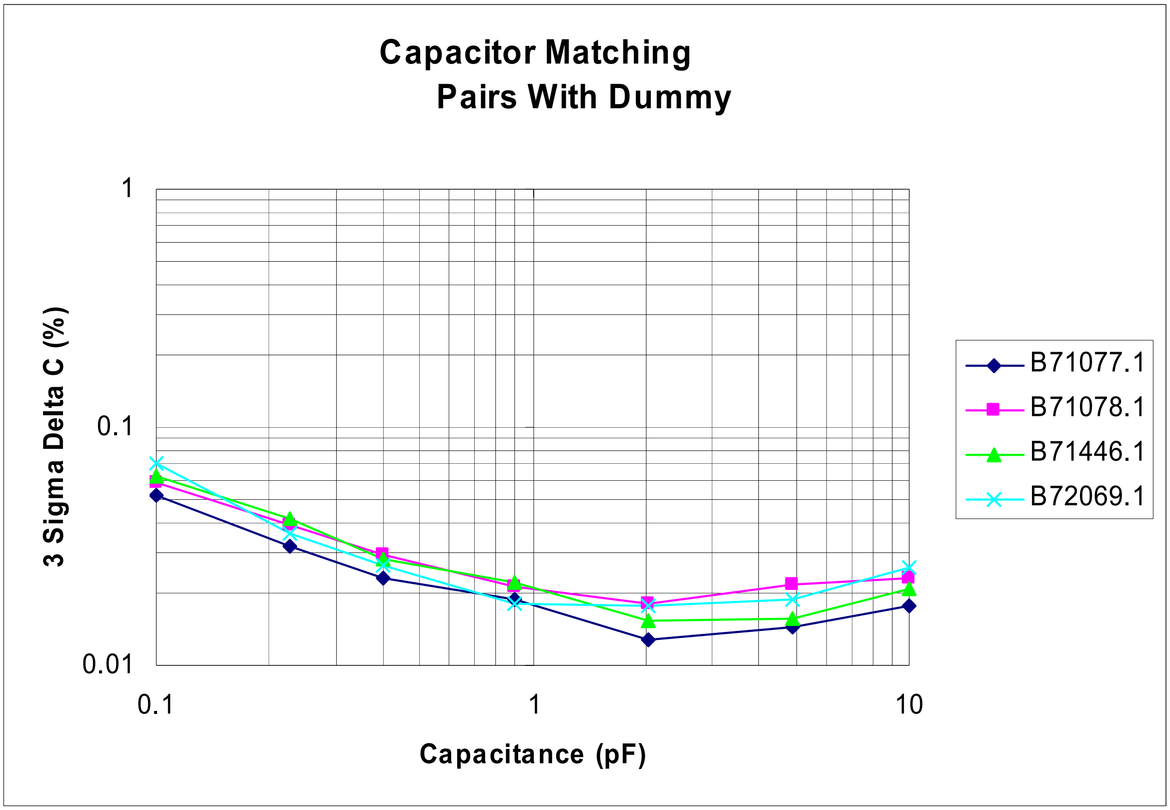
Old Pairs



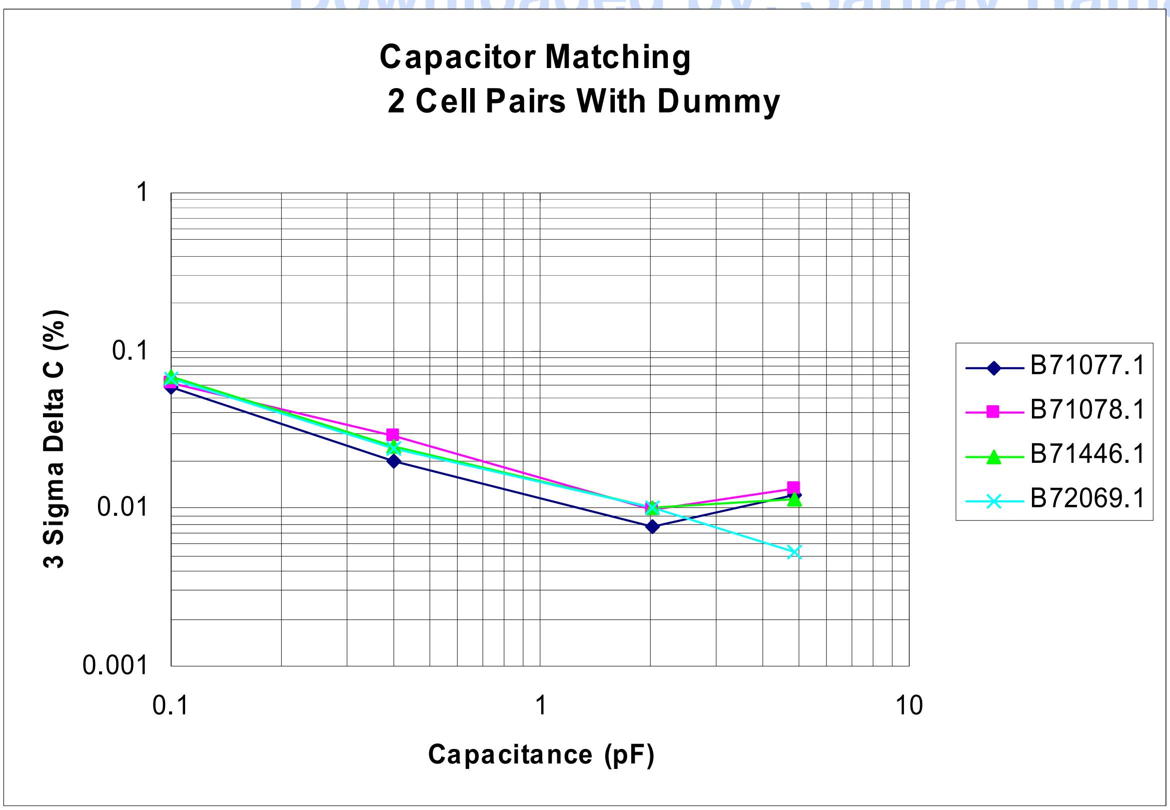
Pairs Without Dummy



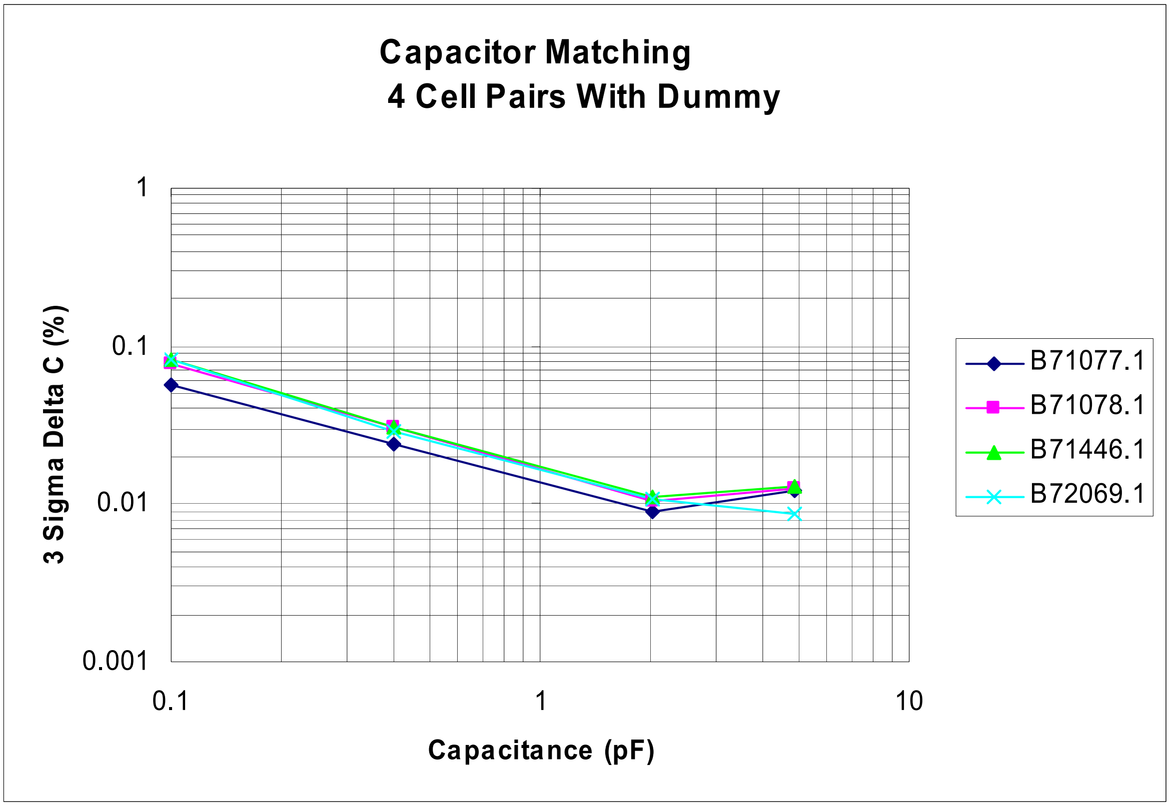
Pairs With Dummy



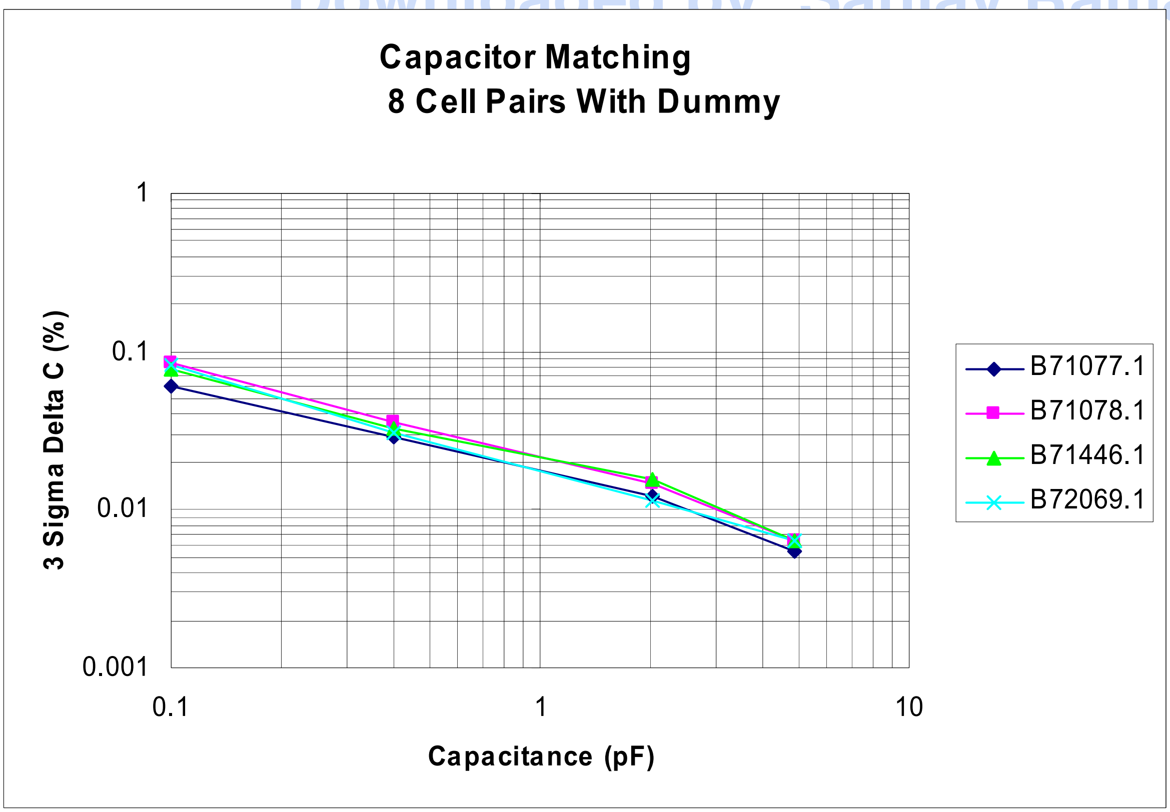
Two Cell Pairs With Dummy



Four Cell Pairs With Dummy



Eight Cell Pairs With Dummy



Capacitor Matching Model

A simple capacitor matching model has been developed which takes account of three of the most important sources of capacitance variation. The model is described by the following equations:

$$\sigma_{\frac{\Delta C}{C}}{}^2 = \sigma_{edge}{}^2 + \sigma_{area}{}^2 + \sigma_{dis\tan ce}{}^2$$

$$\sigma_{edge} = \frac{A_{edge}}{C^{3/4}}$$

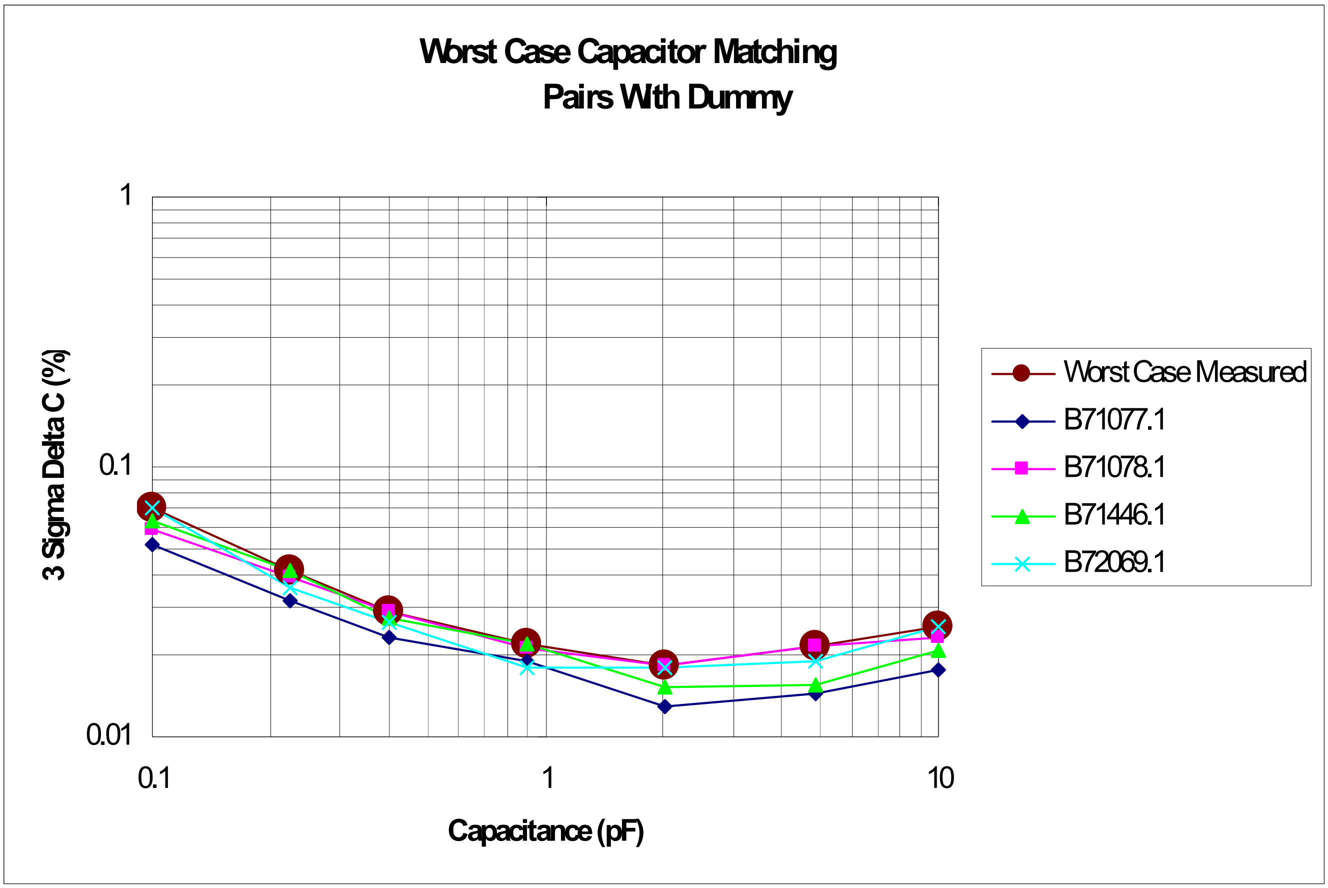
$$\sigma_{area} = \frac{A_{area}}{C^{1/2}}$$

$$\sigma_{dis\tan ce} = A_{dis\tan ce} \cdot dis\tan ce$$

The edge component models the effect of edge roughness, and it is most significant for small capacitors which have relatively large amount of edge capacitance. The area component models the effect of short range dielectric thickness variations, and it is most significant for moderate size capacitors. The distance component models the effect of global dielectric thickness variations across the wafer, and it becomes significant for large capacitors or widely spaced capacitors. The distance is defined from the center of one capacitor to the center of the other capacitor.

Pairs with Dummy Model

We have first fit the model to the results of the pairs with dummy, as these structures have fairly reproducible results which are easily described by the model. As circuits must be designed to work for the worst case matching, we have used the worst case mismatch for each size based on all of the lots we have characterized. The following plot shows the curve we have used:



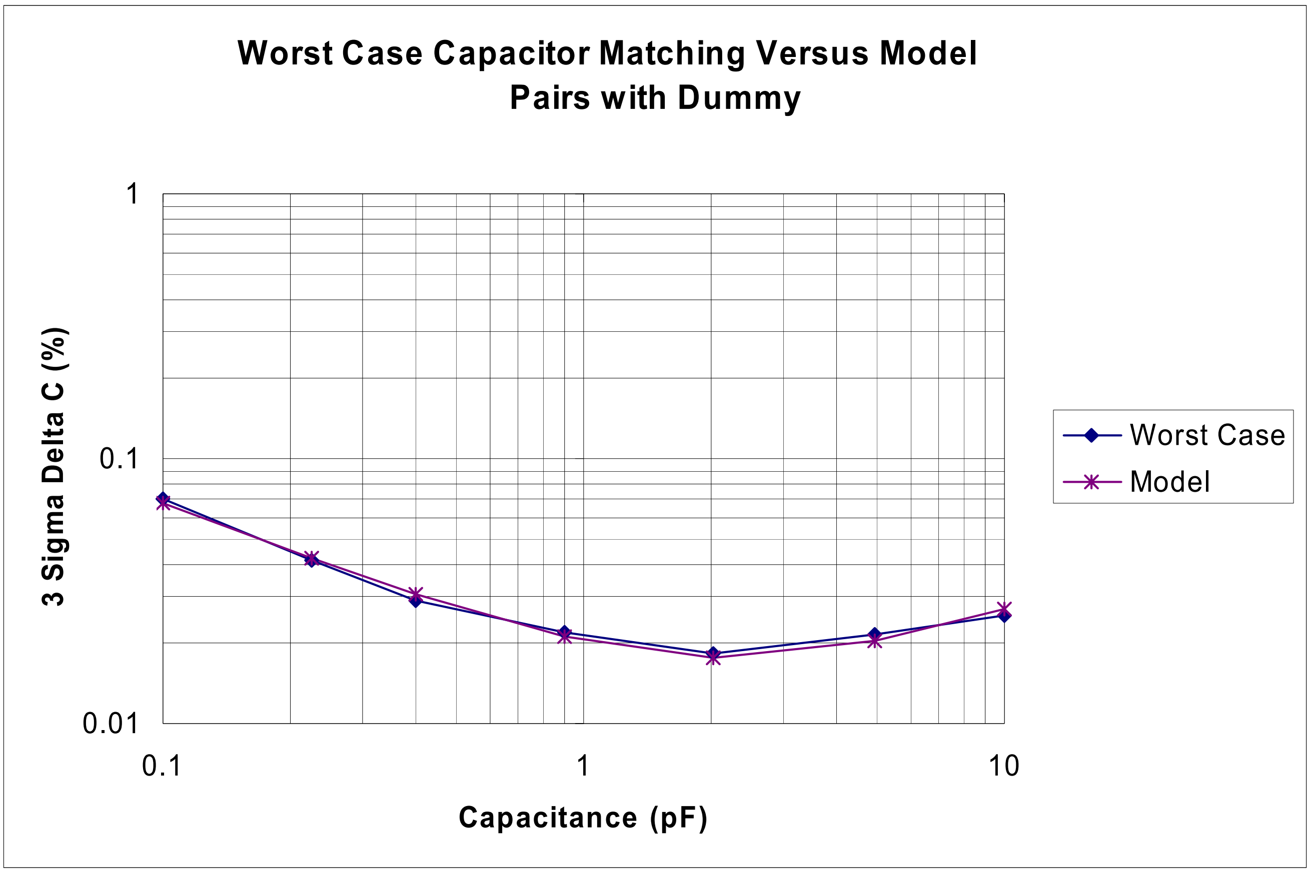
We have used an optimizer to fit the model to the worst case matching data. The optimization was based on minimizing the RMS error in the fit for all capacitor sizes.

Parameter	Value
A_{edge}	2.42E-03
A_{area}	5.64E-03
$A_{distance}$	8.62E-05

The model fits the worst case matching quite well, as can be seen in the following table and chart:

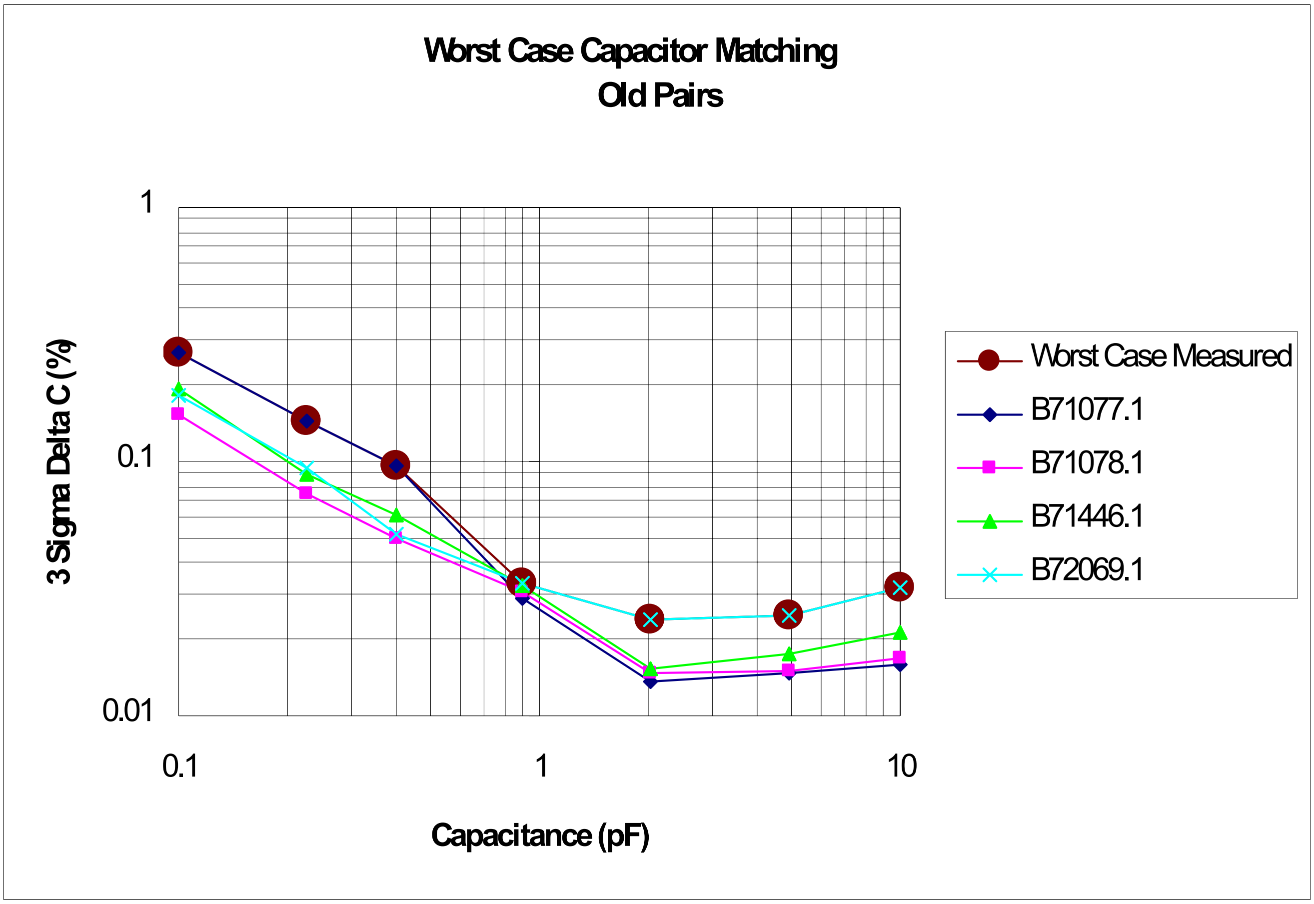
Cell Size	Model Relative Fit Error
10μm x 10μm	-3.66%
15μm x 15μm	1.54%
20μm x 20μm	6.63%
30μm x 30μm	-3.67%
45μm x 45μm	-2.75%
70μm x 70μm	-5.69%
100μm x 100μm	5.98%

Note: Model relative fit error is calculated as 100*(Model – Measured)/Measured.



Old Pairs Model

We have also fit the model to the results of the old pairs, as these structures have significantly worse mismatch for the smaller capacitors. We have again used the worst case mismatch for each size based on all of the lots we have characterized. The following plot shows the curve we have used:



Since the matching for the old pairs is similar to the pairs with dummy for the larger sized capacitors, we have used the same values for the area and distance parameters. An optimizer was used to fit the edge component of the model to the worst case matching data. The optimization was based on minimizing the RMS error in the fit for all capacitor sizes other than the 30µm x 30µm and 45µm x 45µm sizes.

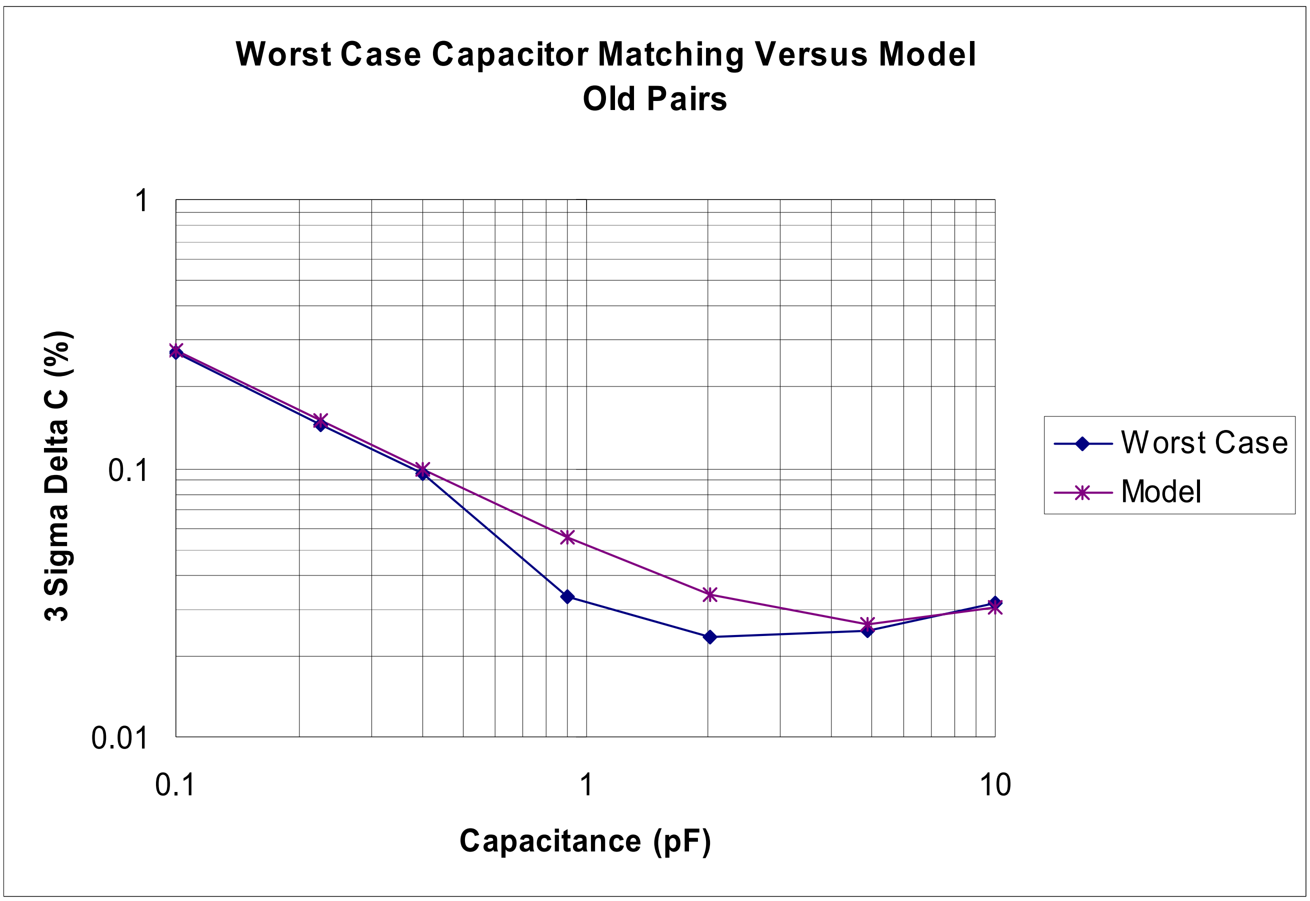
Parameter	Value
A_{edge}	1.59E-02
A_{area}	5.64E-03
$A_{distance}$	8.62E-05

The edge parameter for the old pairs is about 6.6 times greater than that of the pairs with dummy.

The model fits the worst case matching fairly well for the small and large cases, but overestimates the mismatch for the medium sized capacitors. Since we currently do not know the source of the degraded matching, we must assume that the mismatch of the 30µm x 30µm and 45µm x 45µm sizes could increase on some lots. The fit error can be seen in the following table and chart:

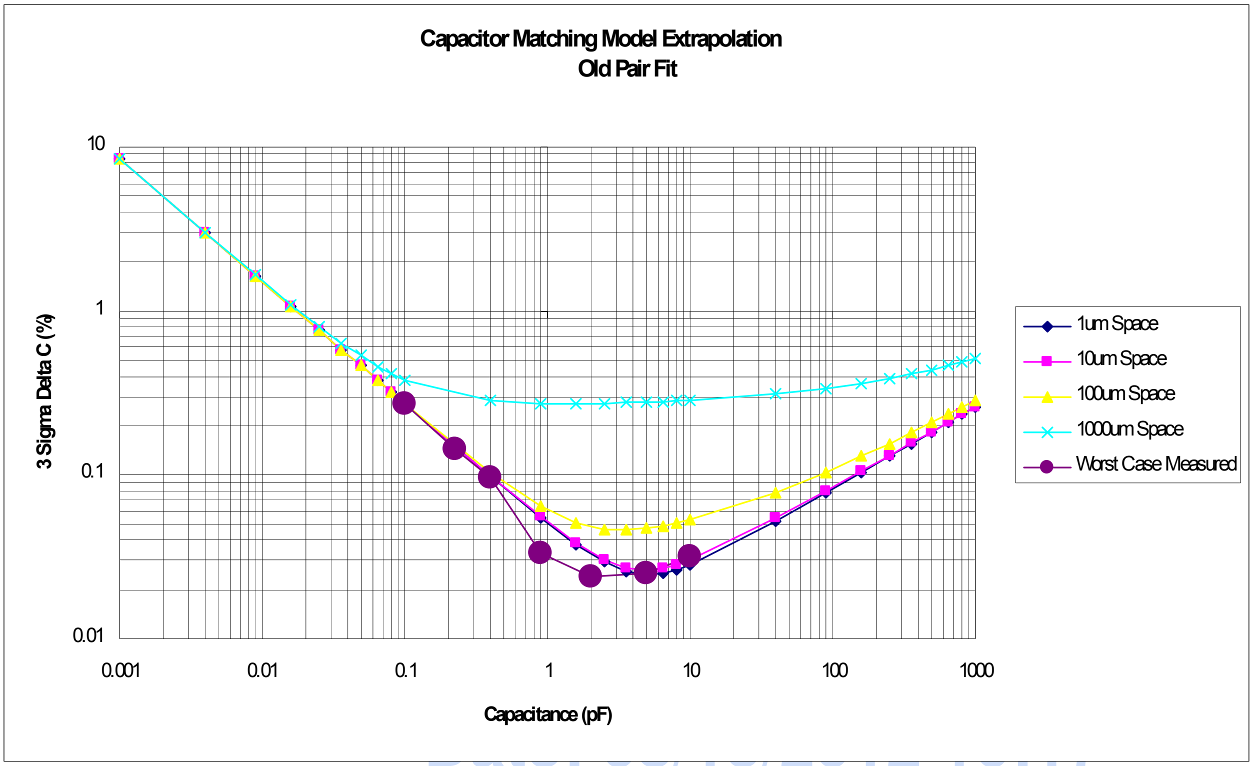
Cell Size	Model Relative Fit Error
10µm x 10µm	1.00%
15µm x 15µm	3.44%
20µm x 20µm	3.34%
30µm x 30µm	66.29%
45µm x 45µm	41.77%
70µm x 70µm	5.37%
100µm x 100µm	-5.14%

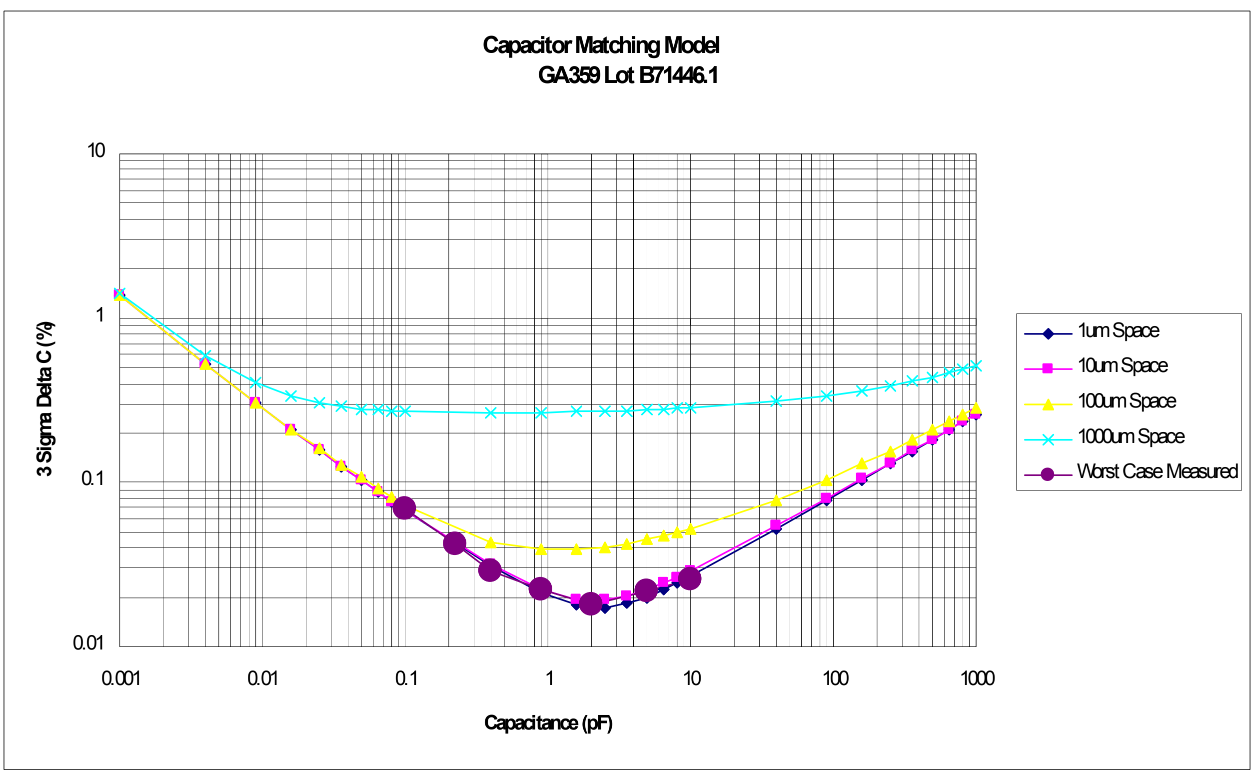
Note: Model relative fit error is calculated as 100*(Model – Measured)/Measured.



Model Extrapolation

We have used the capacitor matching model to provide an estimate of the matching performance for capacitor pairs with sizes other than those measured or with larger spacing between capacitors. The following plots are only an estimate of the matching performance that can be expected, as the model has only been validated for a small subset of the region shown.





Appendix: Test Structure and Test Description

Test Structures:
This test chip is composed of various process and device characterization structures, and it is organized into modules each with 32 pads (except for the RF test structures). This standard pad configuration allows automated measurements to be performed on almost all of the test structures.

There are 3 modules devoted to capacitor matching. The first module was laid out before the design rules were complete, so it violates design rules for metal 2. This module uses the top plate as the floating node, and separate bottom plates. The second module contains the same size capacitors as the first, but the capacitors have been revised to use a single bottom plate for the floating node, and the capacitors are surrounded by a grounded dummy capacitor. The final module contains two single cell capacitors without dummy, and common centroid arrays of 2, 4, and 8 cells with dummy.

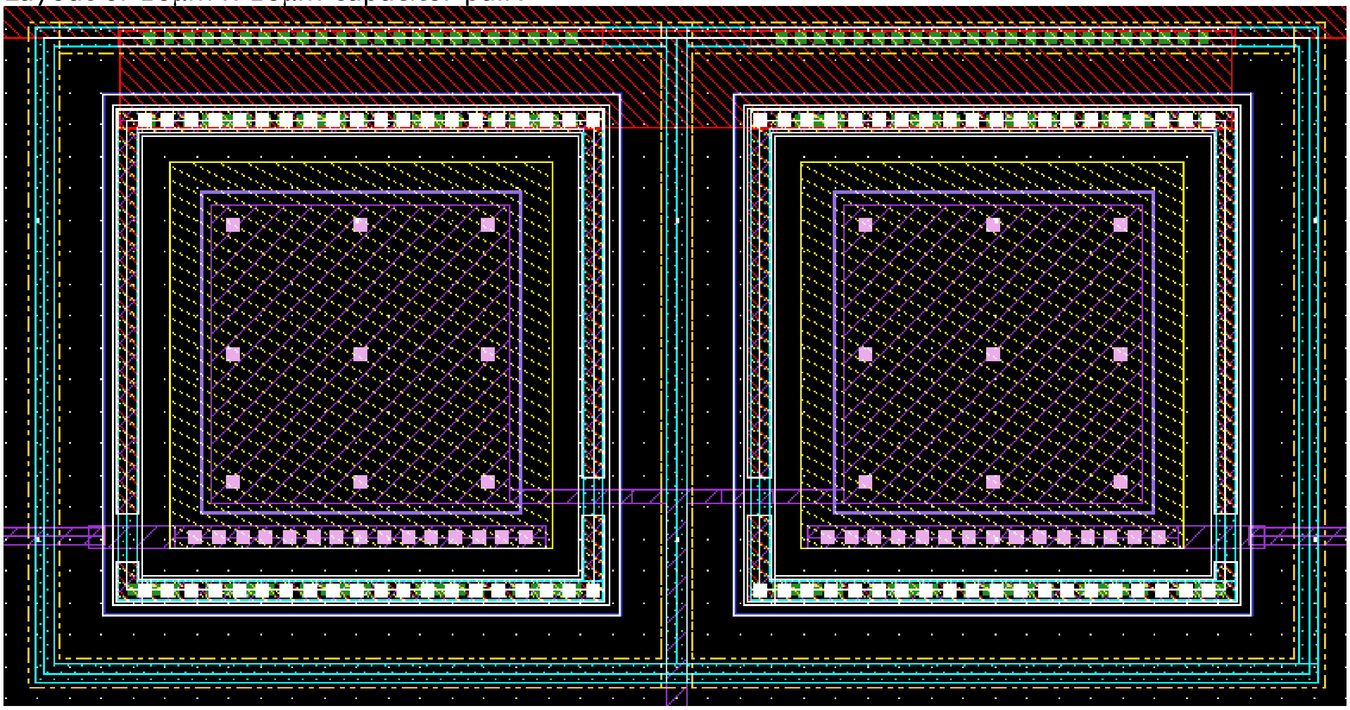
Old 1 Cell Pairs

There are two separate bottom plates which are over separate grounded Nwells with shields on metals 1, 2, and 3. The floating node is composed of the two separate top plates. Note that the metal shields on these structures violate the metal 2 spacing rules.

Capacitor Sizes:

Cell Size	Area	Perimeter	Nominal Capacitance
10µm x 10µm	100µm^2	40µm	0.1pF
15µm x 15µm	225µm^2	60µm	0.225pF
20µm x 20µm	400µm^2	80µm	0.4pF
30µm x 30µm	900µm^2	120µm	0.9pF
45µm x 45µm	2025µm^2	180µm	2.025pF
70µm x 70µm	4900µm^2	280µm	4.9pF
100µm x 100µm	10000µm^2	400µm	10pF

Layout of 10µm x 10µm capacitor pair:



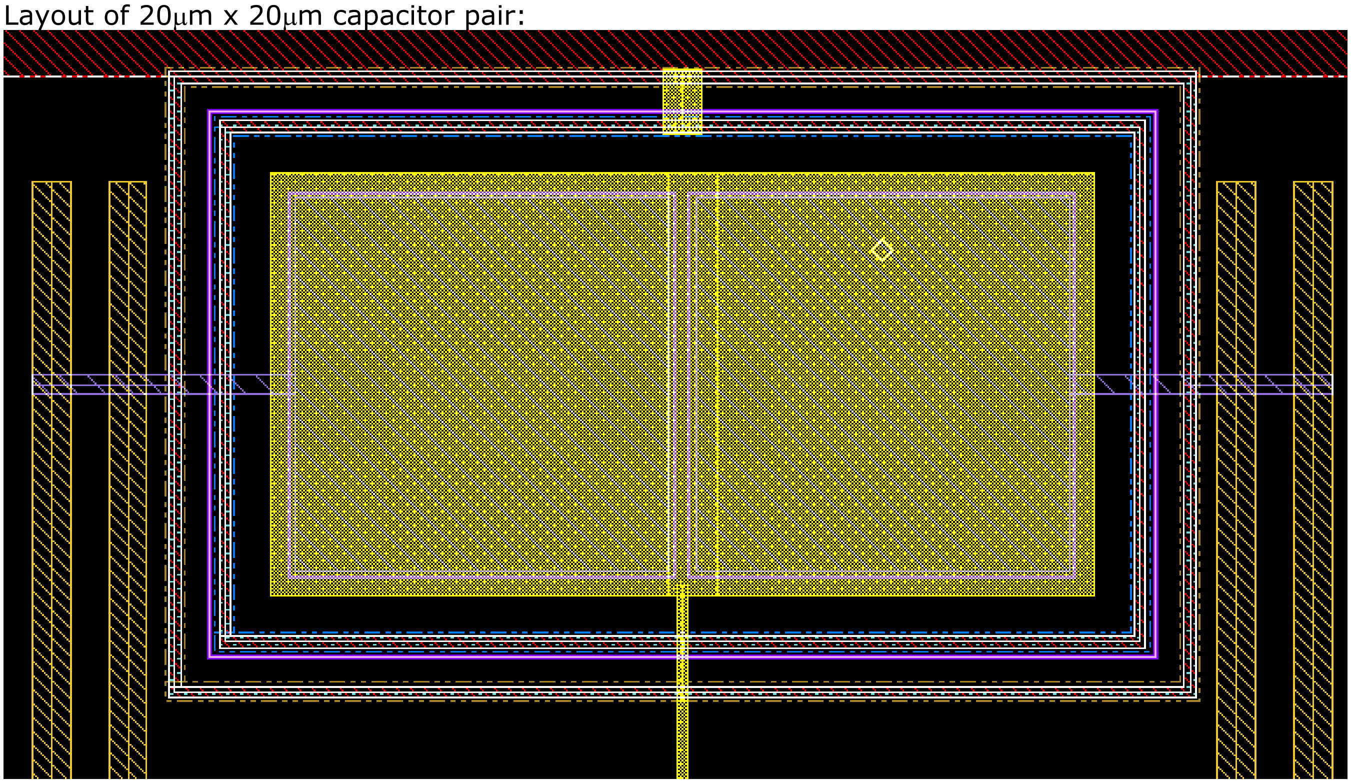
One Cell Pairs without Dummy

These pairs are composed of a single bottom plate with two capacitor top plates at minimum spacing. The metal 2 bottom plate has minimum overlap of the TM top plate, and the bottom plate is connected directly through metal 2. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Cell Size	Area	Perimeter	Nominal Capacitance
20μm x 20μm	400μm^2	80μm	0.4pF
45μm x 45μm	2025μm^2	180μm	2.025pF

Layout of 20μm x 20μm capacitor pair:



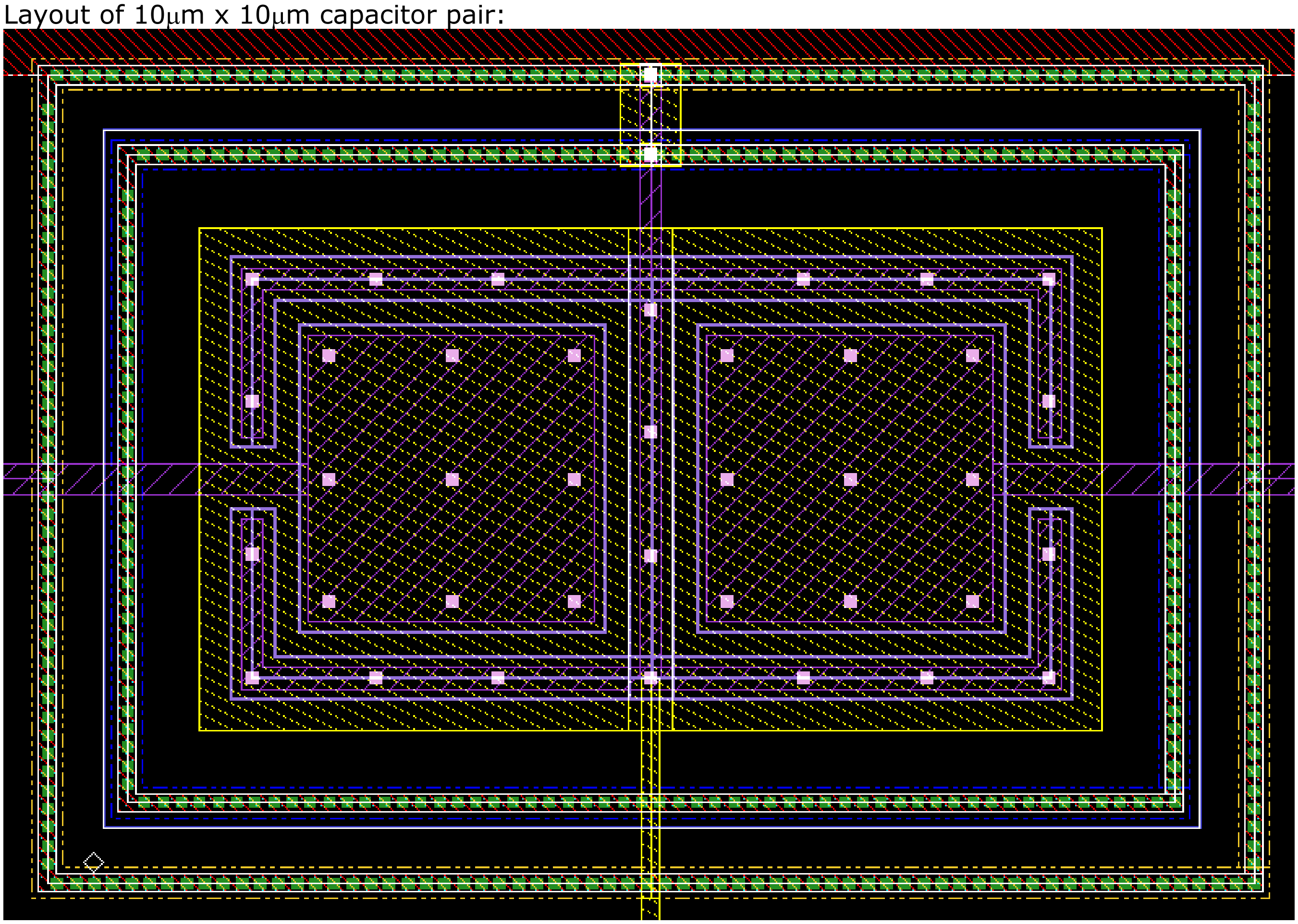
One Cell Pairs with Dummy

These pairs are composed of a single bottom plate with two capacitor top plates. The bottom plate is connected directly through metal 2. There is a minimum width grounded dummy capacitor which surrounds each cell with minimum TM space. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Cell Size	Area	Perimeter	Nominal Capacitance
10μm x 10μm	100μm^2	40μm	0.1pF
15μm x 15μm	225μm^2	60μm	0.225pF
20μm x 20μm	400μm^2	80μm	0.4pF
30μm x 30μm	900μm^2	120μm	0.9pF
45μm x 45μm	2025μm^2	180μm	2.025pF
70μm x 70μm	4900μm^2	280μm	4.9pF
100μm x 100μm	10000μm^2	400μm	10pF

Layout of 10μm x 10μm capacitor pair:



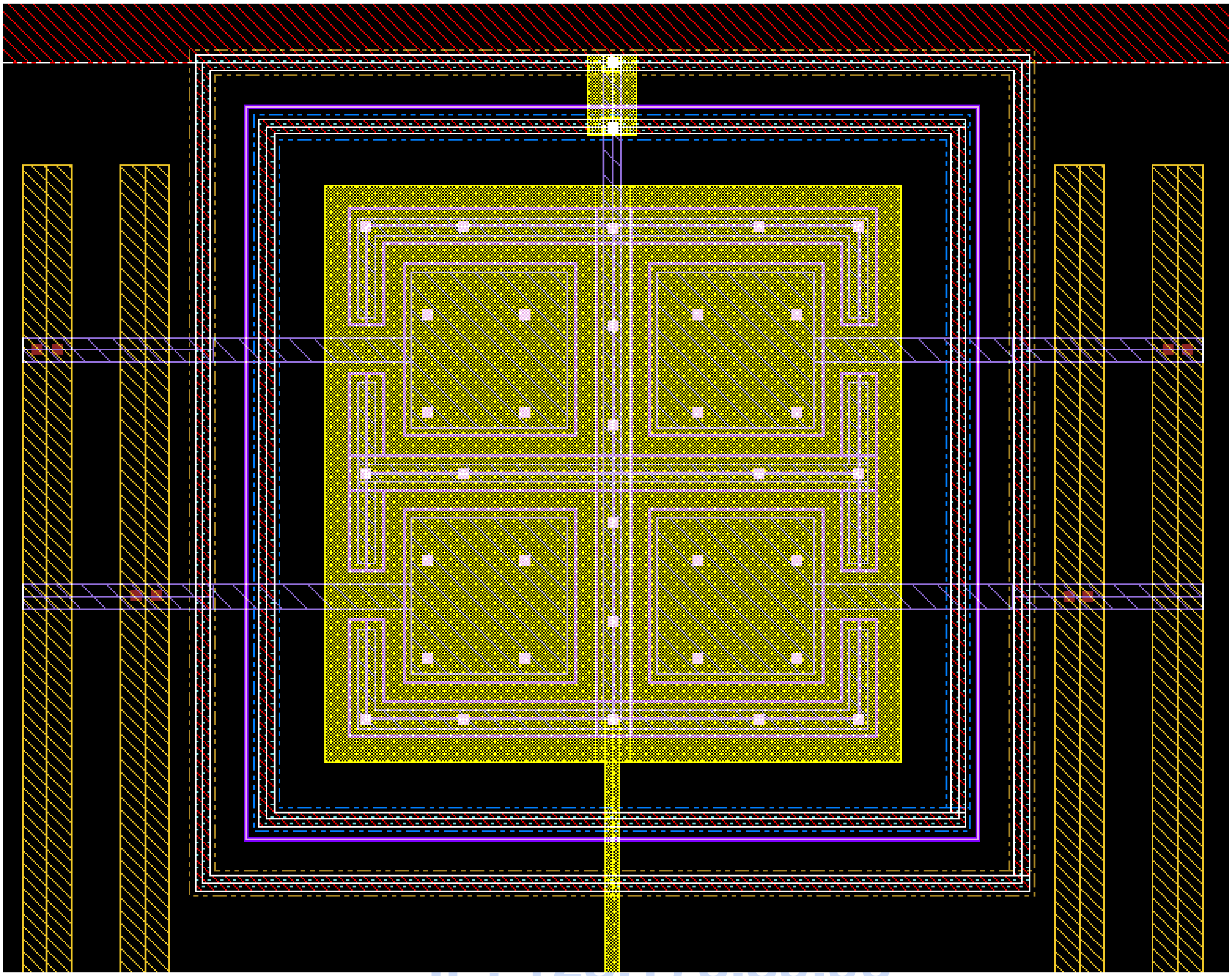
Two Cell Pairs with Dummy

These pairs are composed of a single bottom plate with four capacitor top plates in a common centroid configuration. The bottom plate is connected directly through metal 2. There is a minimum width grounded dummy capacitor which surrounds each cell with minimum TM space. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Equivalent Capacitor Size	Cell Size	Area	Perimeter	Nominal Capacitance
10μm x 10μm	7.01μm x 7.01μm	49.19μm^2	28.06μm	0.1pF
20μm x 20μm	14.08μm x 14.08μm	198.37μm^2	56.34μm	0.225pF
45μm x 45μm	31.76μm x 31.76μm	1008.80μm^2	127.05μm	2.025pF
70μm x 70μm	49.44μm x 49.44μm	2444.22μm^2	197.76μm	4.9pF

Layout of 10μm x 10μm equivalent capacitor pair:



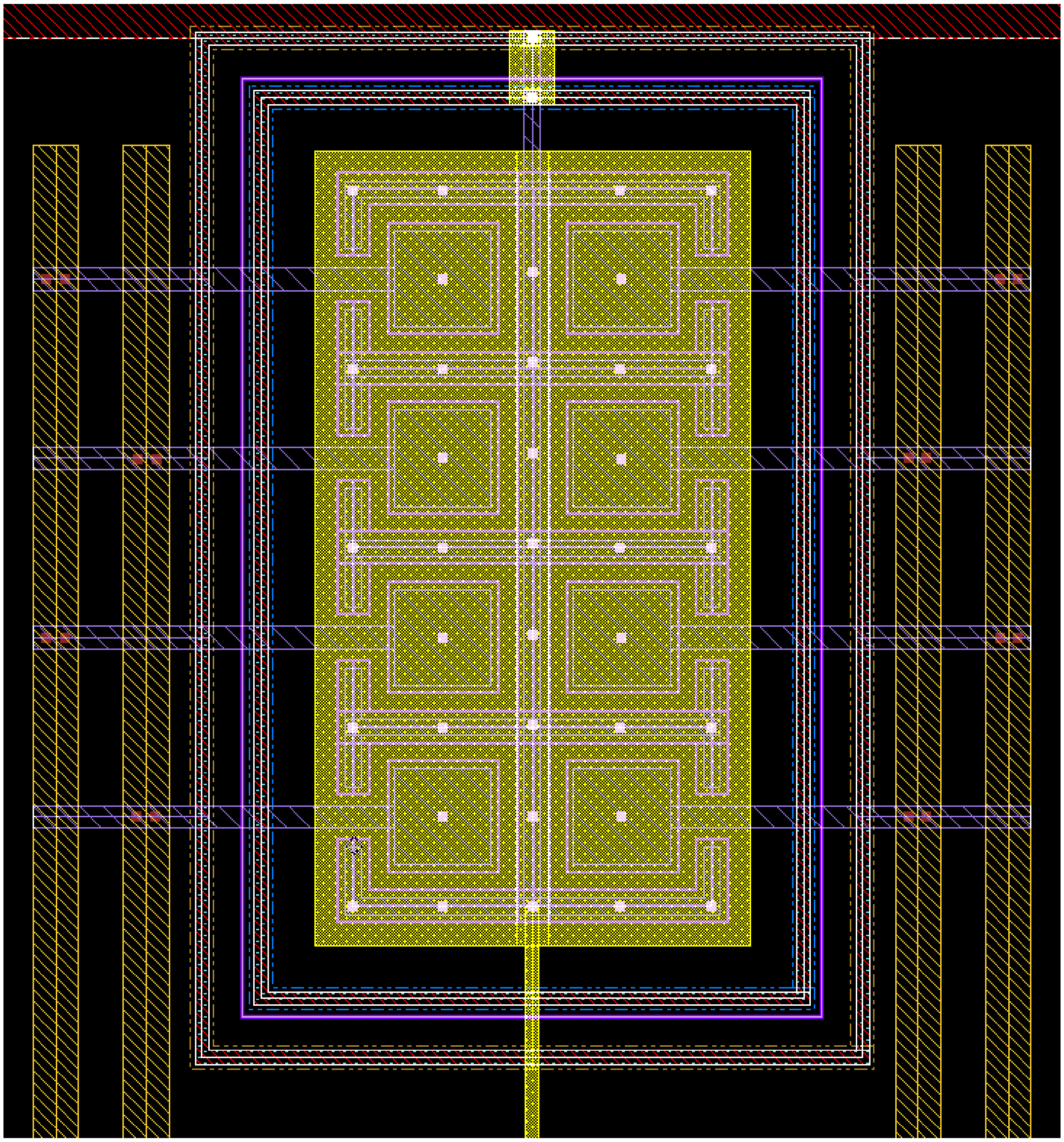
Four Cell Pairs with Dummy

These pairs are composed of a single bottom plate with eight capacitor top plates in a common centroid configuration. The bottom plate is connected directly through metal 2. There is a minimum width grounded dummy capacitor which surrounds each cell with minimum TM space. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Equivalent Capacitor Size	Cell Size	Area	Perimeter	Nominal Capacitance
10μm x 10μm	4.90μm x 4.90μm	24.04μm^2	19.61μm	0.1pF
20μm x 20μm	9.90μm x 9.90μm	98.04μm^2	39.61μm	0.225pF
45μm x 45μm	22.40μm x 22.40μm	501.79μm^2	89.60μm	2.025pF
70μm x 70μm	34.90μm x 34.90μm	1218.04μm^2	139.60μm	4.9pF

Layout of 10μm x 10μm equivalent capacitor pair:



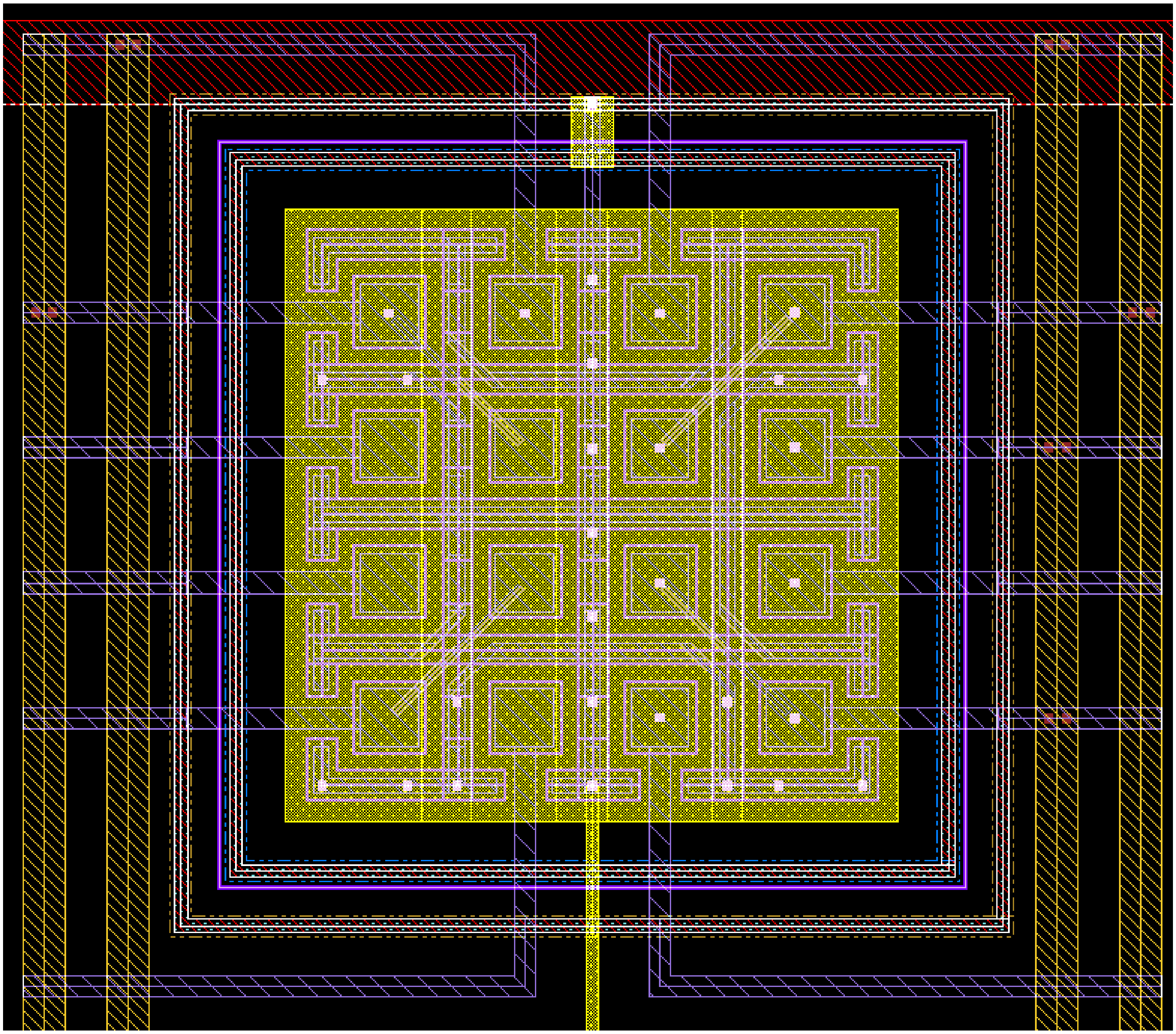
Eight Cell Pairs with Dummy

These pairs are composed of a single bottom plate with sixteen capacitor top plates in a common centroid configuration. The bottom plate is connected directly through metal 2. There is a minimum width grounded dummy capacitor which surrounds each cell with minimum TM space. The capacitor pair is placed over a grounded Nwell which is tied to the substrate.

Capacitor Sizes:

Equivalent Capacitor Size	Cell Size	Area	Perimeter	Nominal Capacitance
10μm x 10μm	3.41μm x 3.41μm	11.64μm^2	13.64μm	0.1pF
20μm x 20μm	6.94μm x 6.94μm	48.22μm^2	27.78μm	0.225pF
45μm x 45μm	15.78μm x 15.78μm	249.06μm^2	63.13μm	2.025pF
70μm x 70μm	24.62μm x 24.62μm	606.15μm^2	98.48μm	4.9pF

Layout of 10μm x 10μm equivalent capacitor pair:



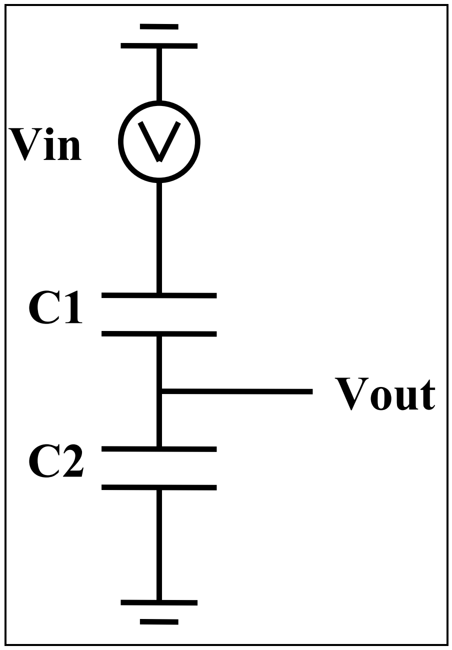


Figure 19: Capacitor Voltage Divider

Test Circuit Description
From our experience, it is impractical to measure capacitor matching by simply measuring the capacitance of adjacent capacitors with a capacitance meter. From past process characterizations, we found that our current measurement system can reliably measure the mismatch only if it is greater than approximately 0.5%. Due to circuit designs which require 10 bit matching, we need to be able to measure the matching with an accuracy better than 0.1%. While some groups have been able to obtain reasonable measurements by simply measuring capacitance, they have been required to make significant modifications to their test systems. Due to the difficulty in setting up and maintaining such a test setup, we have chosen to use a different approach based upon a capacitor voltage divider.

The basic circuit used to measure the matching of capacitor pairs is a simple capacitor voltage divider as shown in figure 1. From basic circuit theory, the ratio of the applied voltage to the voltage between the two capacitors is:

$$Vout = Vin * \frac{C1}{C1 + C2}$$

Unfortunately, it is impractical to connect a voltmeter directly to the Vout node of the divider. As shown in figure 2, any practical voltmeter (including the probes, cabling, and switch matrix) will have parasitic capacitances and leakages which will be too large to allow a direct measurement to be performed. Several approaches have been proposed to overcome this problem, but the one we have chosen to use is probably the simplest one, yet it obtains the highest accuracy[1]. The basic concept of this circuit is to use an on chip buffer amplifier to allow the voltage ratio of the capacitor divider to be measured off chip with a standard voltmeter. The fundamental properties of a buffer amplifier are high input impedance, low output impedance, and a voltage gain of one.

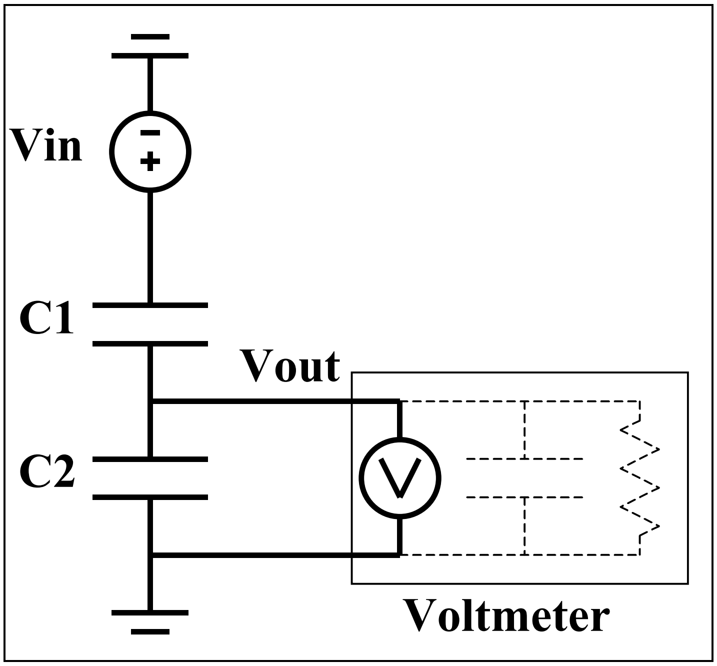


Figure 20: Capacitor Voltage Divider with a Simple Voltmeter Model

The circuit is shown in figure 3, and it uses a single PFET in common drain configuration as the buffer amplifier. Since the input to the amplifier is the PFET gate, the input impedance is determined by the gate leakage, which should be negligible. The output impedance of this circuit is also negligible. The voltage gain is determined by the biasing and IV characteristics the PFET. An external current source is used to bias the amplifier, so the current source should be nearly ideal, and it should have a high output impedance. A relatively long and narrow (2μm x 10μm) PFET has been used with a 1μA bias current to ensure that the amplifier is very linear.

There are two properties of this amplifier which prevent us from making direct measurements of the capacitor voltage ratio. The first is the DC shift in the output voltage between the input and output, and the second is the parasitic capacitance caused by interconnect and the PFET. While common drain amplifier configuration provides a voltage gain of one, there is a DC voltage offset between the input node (Vfloat) and the output node (Vout) equal to Vgs. The exact value of this offset voltage is unknown, as each transistor will have a slightly different Vgs at the bias current of 1μa. In order to circumvent this problem, we can simply apply a range of input voltages and measure the slope of the output voltages. The slope (S) of Vout relative to Vin is equal to

$$S = \frac{C1}{C1 + C2}$$

as shown in figure 4. It can be shown that the capacitor matching can be determined from the slope by the following equation:

$$\frac{\Delta C}{C} = 4S - 2$$

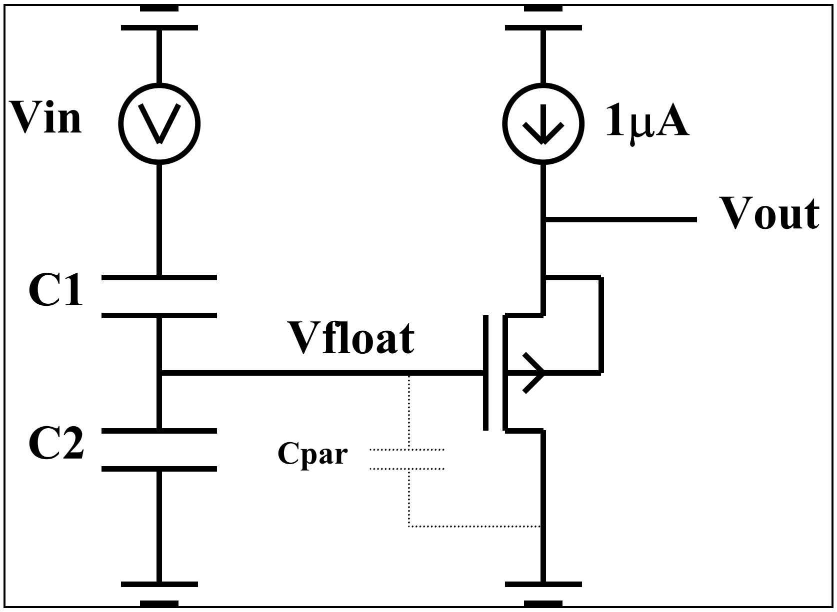


Figure 21: Schematic Diagram of Capacitor Matching Circuit

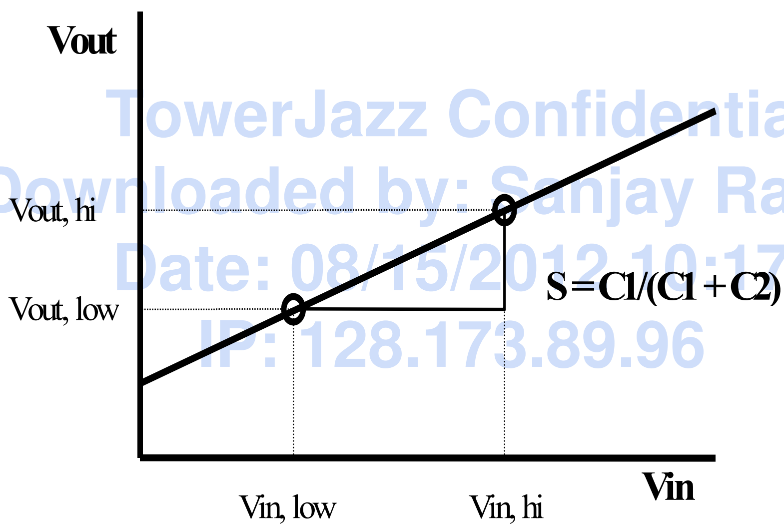


Figure 22: Input/Output Voltage of Capacitor Matching Circuit

The parasitic capacitance is also unknown, and since it is in parallel with C2, it will cause an offset equal to its value to the mismatch. If the parasitic capacitance is included, the equation for the slope is

$$S = \frac{C1}{C1 + C2 + Cpar}$$

This problem can be solved to first order by measuring the slope in the standard (forward) configuration, reversing the connections between C1 and C2, and then remeasuring the slope in the in the reverse configuration. With both the forward and reverse slopes, we can calculate the capacitor matching using the following equations

Forward Slope: $S1 = \frac{C1}{C1 + C2 + Cpar}$

Reverse Slope: $S2 = \frac{C2}{C1 + C2 + Cpar}$

$$\frac{\Delta C}{C} = 2\frac{S1 - S2}{S1 + S2} = 2\frac{C1 - C2}{C1 + C2}$$

By measuring the slope in both directions, the parasitic capacitance can be canceled out of the equation. Since the only physical change to the circuit is the connections to the two capacitors, we can to first order assume that the parasitic capacitance is the same for both configurations, and cancels out exactly.

Figure 5 shows the layout methodology of the capacitor pair matching test structure. Since the matching of capacitor pairs is very sensitive to layout, we have tried to maintain perfect symmetry wherever possible. The capacitors are mirror images of each other, and the interconnect also has mirror symmetry.

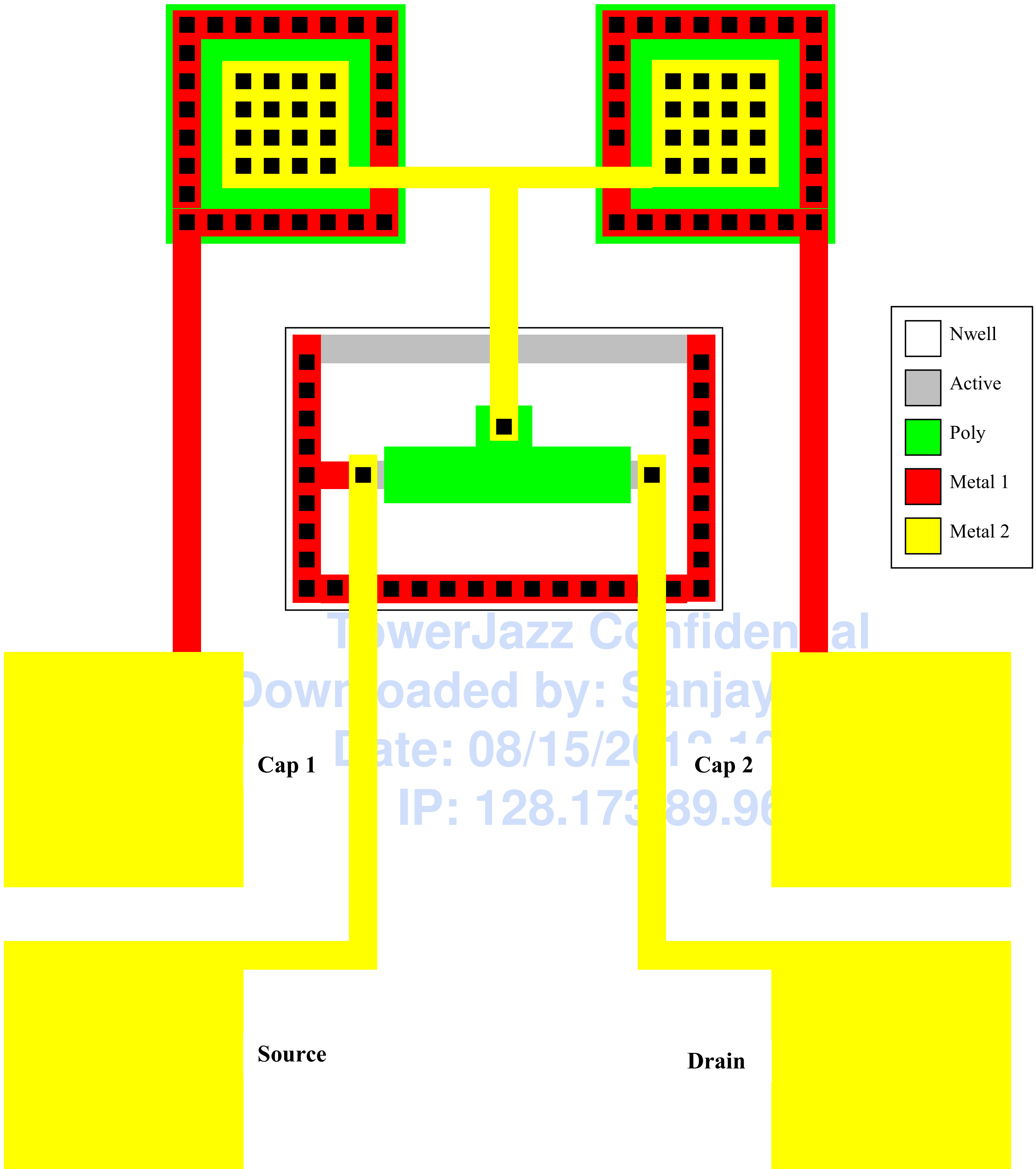


Figure 23: Layout of Capacitor Pair Matching Test Structure (Not to Scale)

Test Description

The capacitor matching test was performed on a Reedholm parametric tester. A new user defined test was added to the Reedholm in order to implement the capacitor matching test in an efficient manner.

The test setup provides for connection inputs (C1, C2, Drain, Source, Substrate), bias inputs (Start Vin, Stop Vin, Step Vin, Source Current, Source Compliance Voltage, Delay Time), and the ability to average multiple measurements.

The following tables describe the measurement connections for this test:

Forward Measurement		
Pad	Node	Source
Cap #1	1	1
Cap #2	0	GND
Drain	0	GND
Source	2	2
Substrate	0	GND

Reverse Measurement		
Pad	Node	Source
Cap #1	0	GND
Cap #2	1	1
Drain	0	GND
Source	2	2
Substrate	0	GND

The following steps describe the measurement:
Connect the terminals as shown for the forward measurement. Ground the Cap #2, Drain, and Substrate node. Force a 1μA current into the Source node. Sweep the Cap #1 node (Vin) from 0V to 4V using 0.4V steps while measuring the voltage at the Source node (Vout).
Calculate the forward slope, intercept, and Rsquared between Vout and Vin through a linear least squares regression. Since the Rsquared values are so close to 1, the value reported is actually 1 – Rsquared.
Connect the terminals as shown for the reverse measurement. Ground the Cap #1, Drain, and Substrate node. Force a 1μA current into the Source node. Sweep the Cap #2 node (Vin) from 0V to 4V using 0.4V steps while measuring the voltage at the Source node (Vout).
Calculate the reverse slope, intercept, and Rsquared between Vout and Vin through a linear least squares regression. Since the Rsquared values are so close to 1, the value reported is actually 1 – Rsquared.
Calculate the percent matching from the following formula:

$$\frac{\Delta C}{C} = 2\frac{S1 - S2}{S1 + S2} = 2\frac{C1 - C2}{C1 + C2}$$

Repeat the test if number of averages is greater than one.

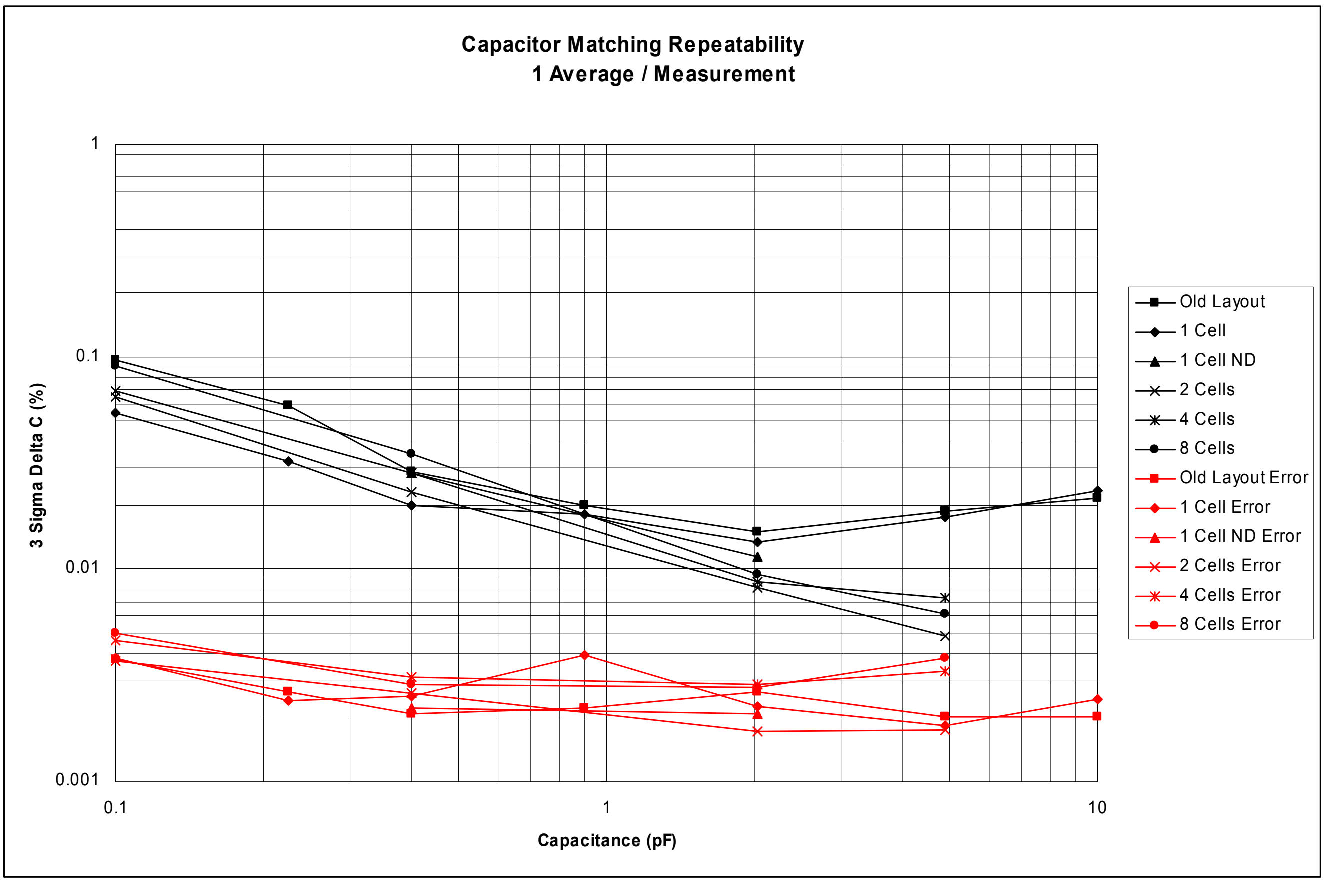
The result returned by the test is the capacitor matching, but the following results can also be extracted: Forward Slope, Forward Intercept, Forward Rsquare, Reverse Slope, Reverse Intercept, Reverse Rsquare, and Sum Rsquare.

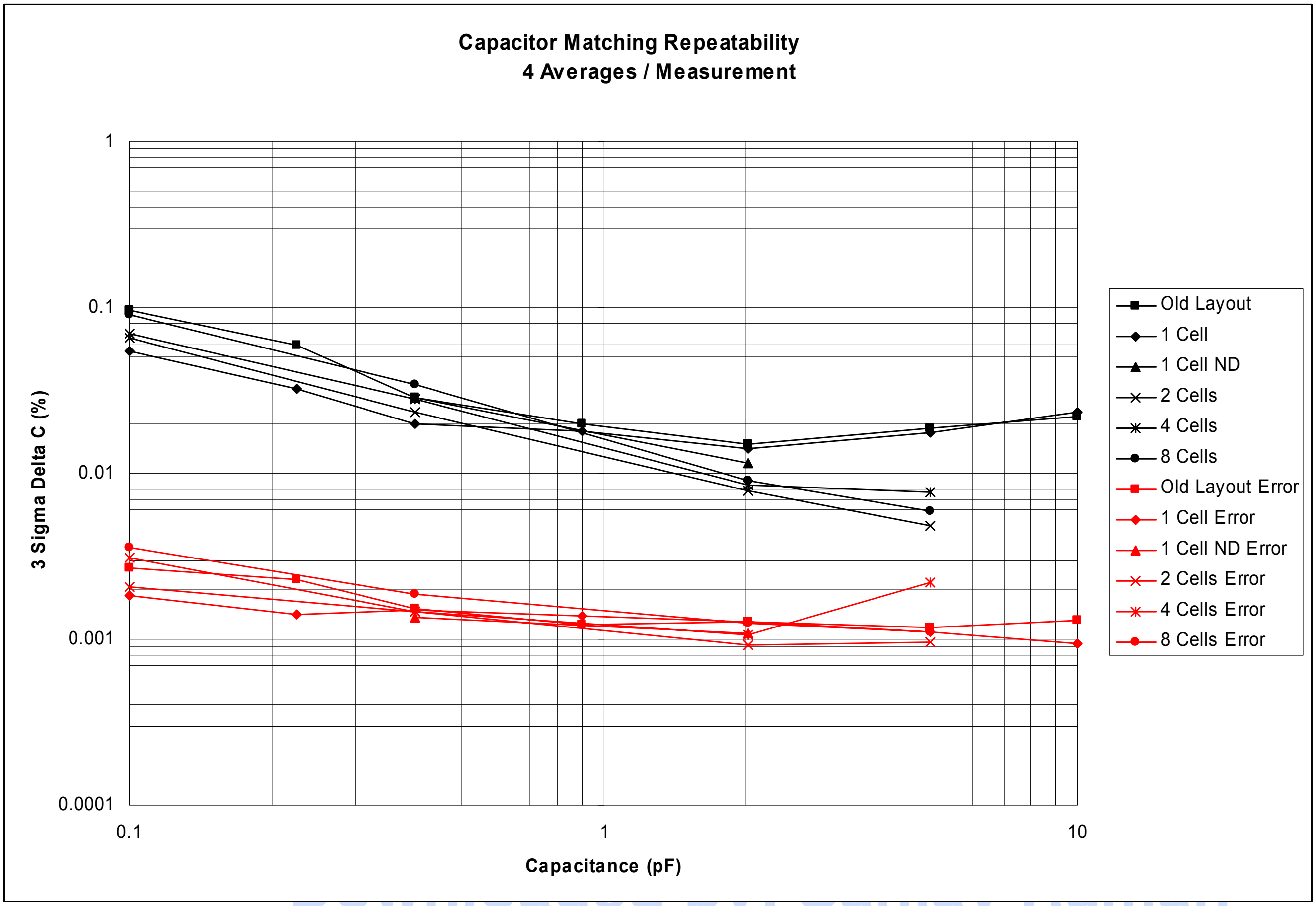
Measurement Repeatability

Since the purpose of matching measurements is to characterize the small differences between two adjacent identically laid out devices, it is important to characterize the repeatability of the measurement. Since both the measurement accuracy and device matching generally degrade as the device geometries are reduced, it is possible obtain overly pessimistic results, as the measurement noise can become dominant.

In order to characterize the repeatability of this test, we have measured all 50 die on wafer 12 of lot B71077.1 two times. We then calculate the difference between the 2 measurements on a die by die basis, and then calculate the 3 sigma of the difference between measurements. The result should represent the worst case measurement error for this test on a particular test structure. The repeatability test has been performed for both the standard test which only uses a single average, and also for a modified test which uses four averages.

We have found that the repeatability is relatively constant versus device size. For most cases the worst case measurement error is significantly less than the matching result. However, we have found that even for the cases where the difference is not as significant, the matching result is very consistent. The results are shown in the following plots:




Capacitor Matching Repeatability
4 Averages / Measurement
1
0.1
0.01
0.001
0.0001
0.1
1
10
3 Sigma Delta C (%)
Capacitance (pF)
Old Layout
1 Cell
1 Cell ND
2 Cells
4 Cells
8 Cells
Old Layout Error
1 Cell Error
1 Cell ND Error
2 Cells Error
4 Cells Error
8 Cells Error

14. Buried Layer Varactor Characterization

Summary

The following figures outline the results of the SBC18 varactor characterization. The buried layer varactor is available in SBC18HX, SBC18QTD, SBC18QTR, and SBC18PT.

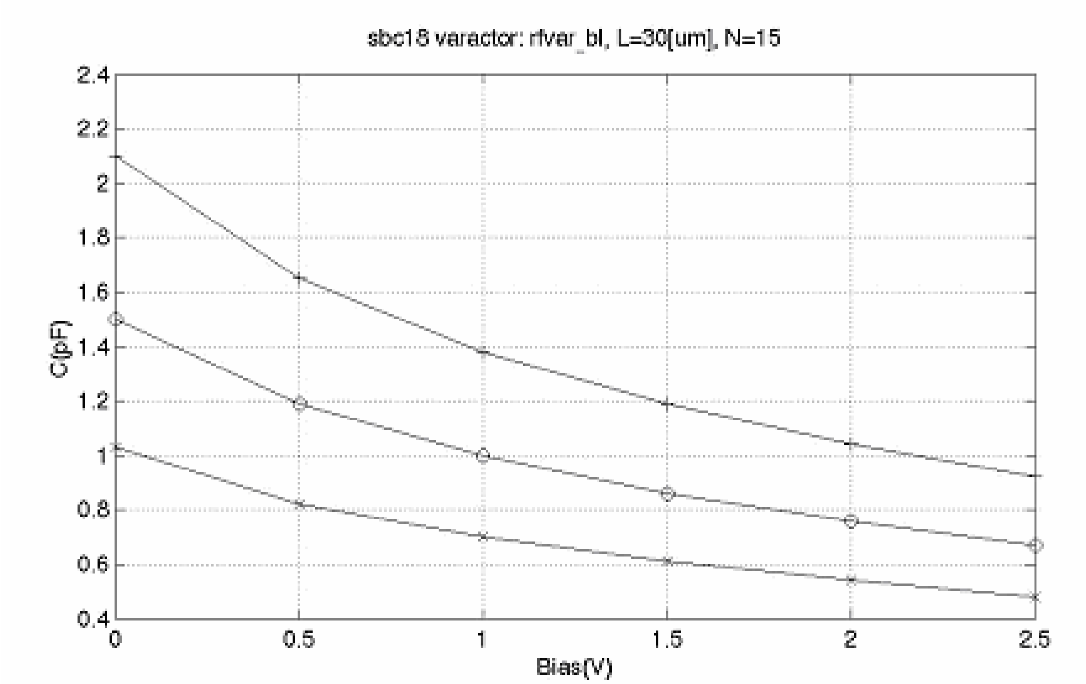


Figure 14.1: Buried Layer Varactor: Capacitance vs. Voltage

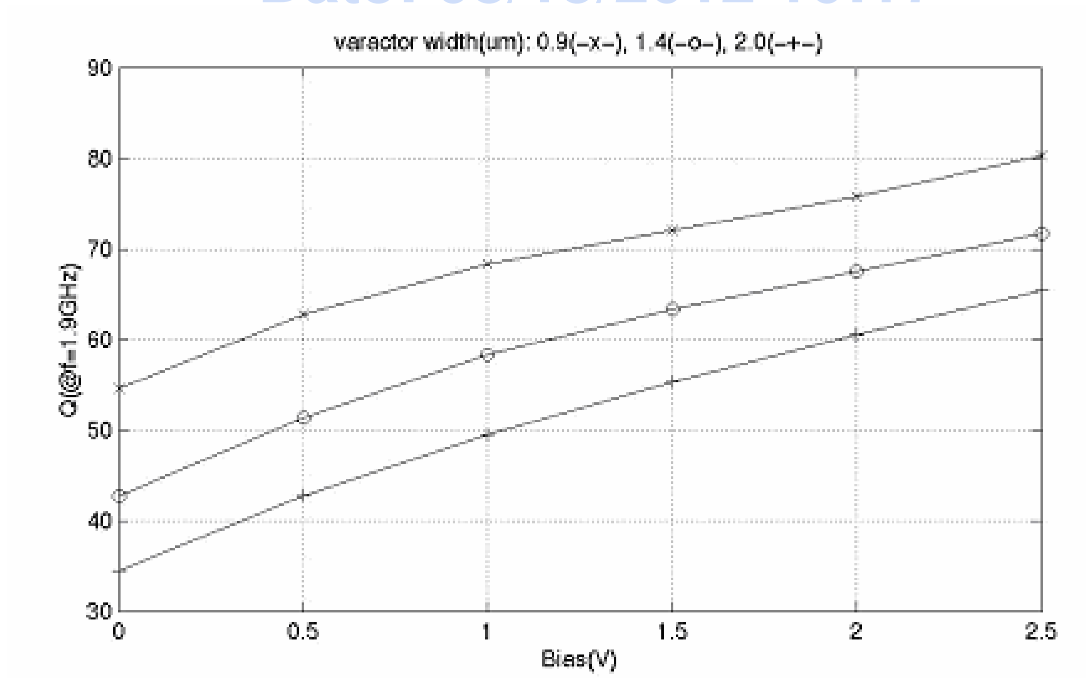


Figure 14.2: Buried Layer Varactor:, Q vs. voltage

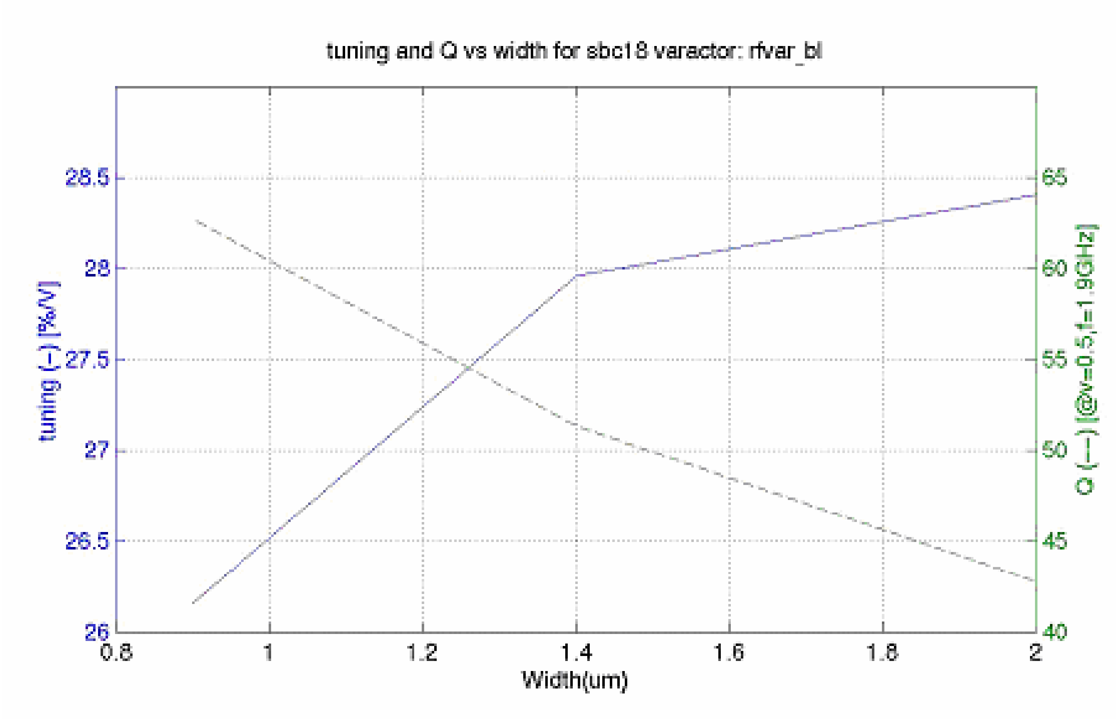


Figure 14.3: Buried Layer Varactor:: Tuning vs. anode width at V=0.5v, 1.9GHz

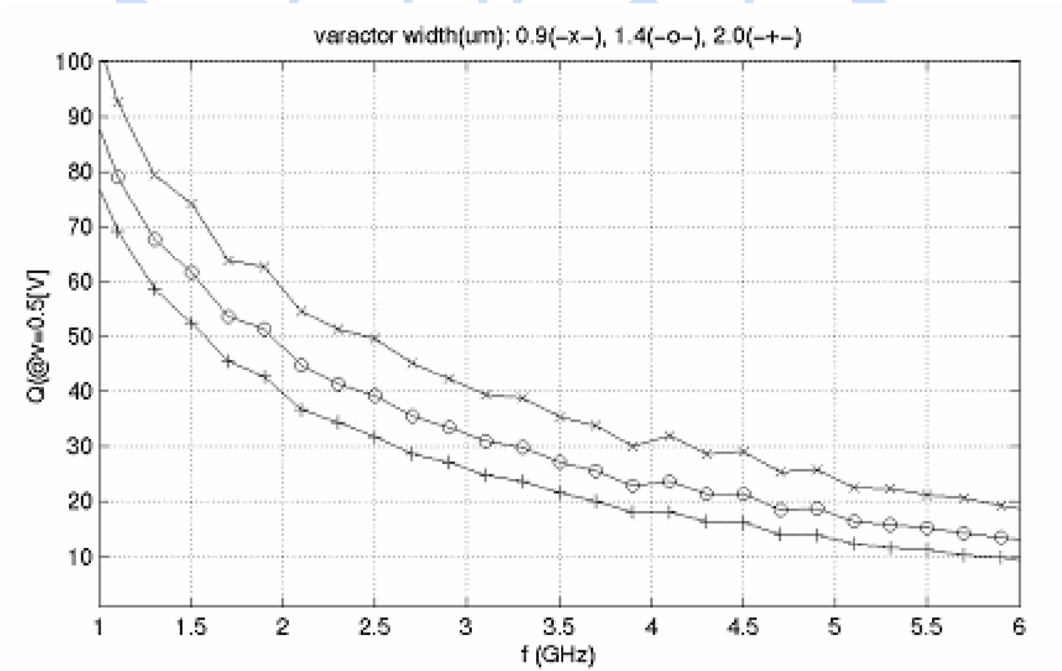


Figure 14.4: Buried Layer Varactor: Q vs. frequency

15. CMOS Varactor Characterization

Summary

The following figures outline the results of the SBC18 varactor characterization. The CMOS varactor is available in SBC18QW and SBC18MW.

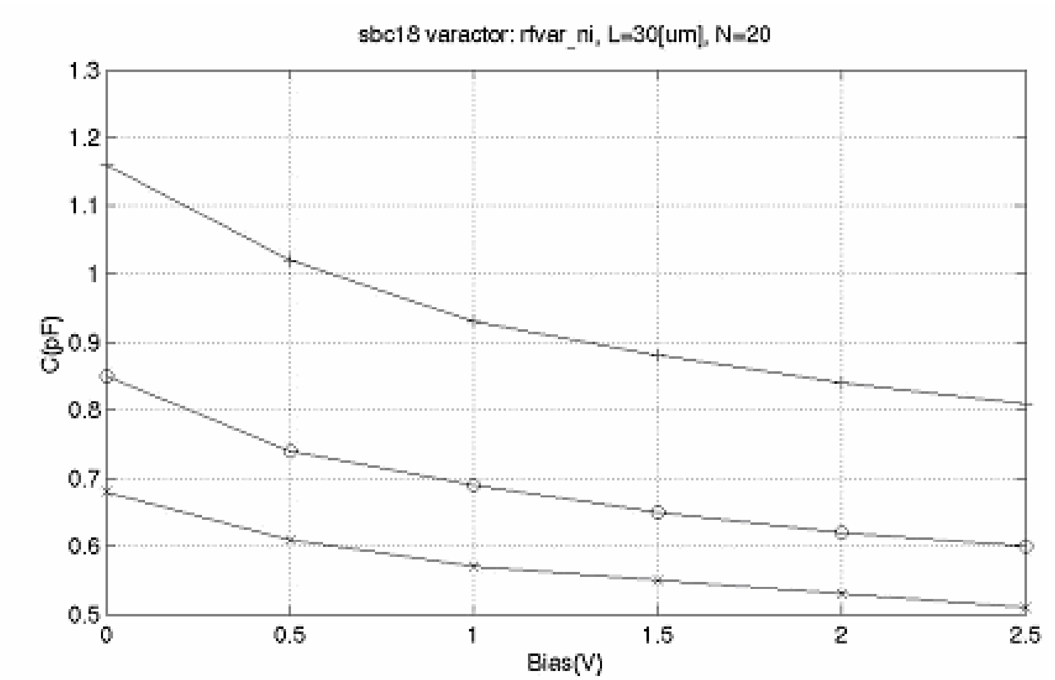


Figure 15.3: Varactor CMOS: Capacitance vs. Voltage

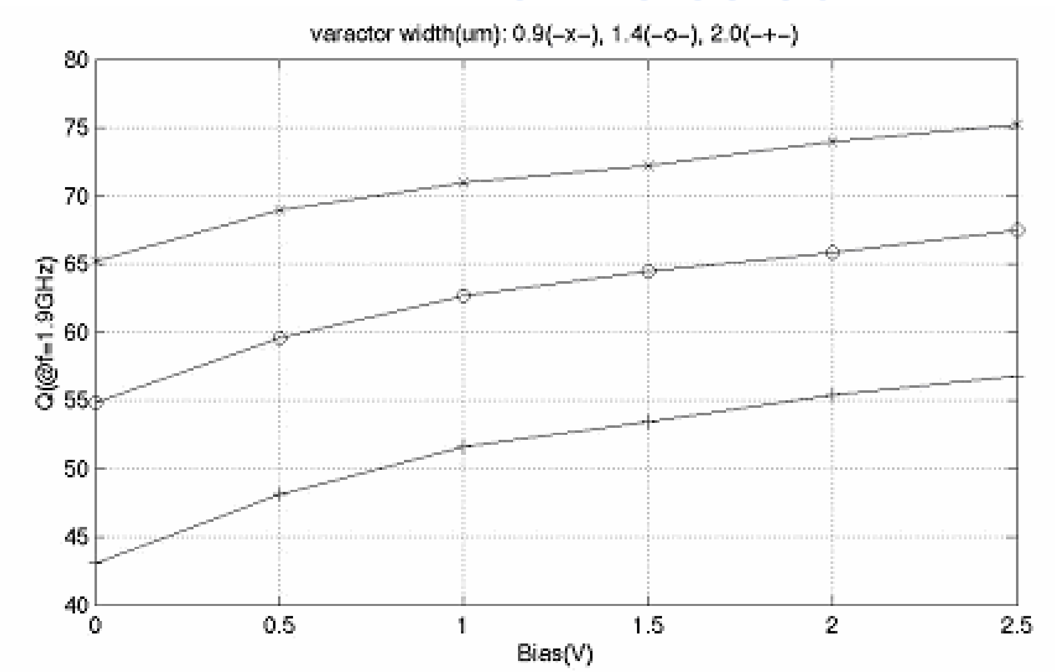


Figure 15.2: CMOS Varactor:, Q vs. voltage

CV Curves, Q vs. Bais

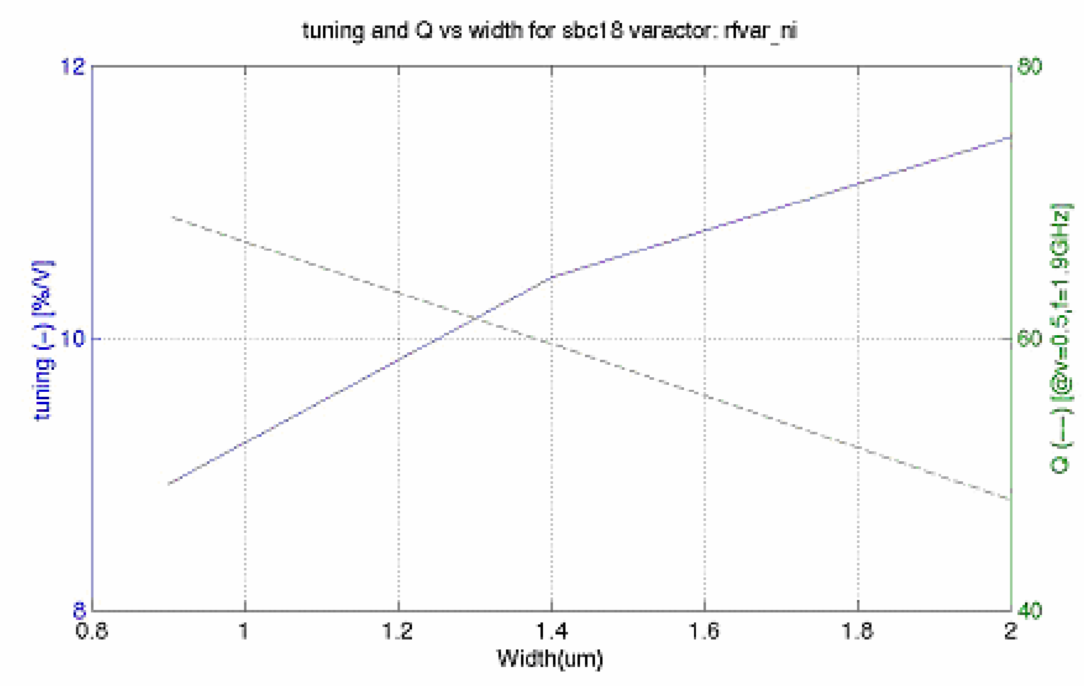


Figure 15.3: CMOS Varactor:: Tuning vs. anode width at V=0.5v, 1.9GHz

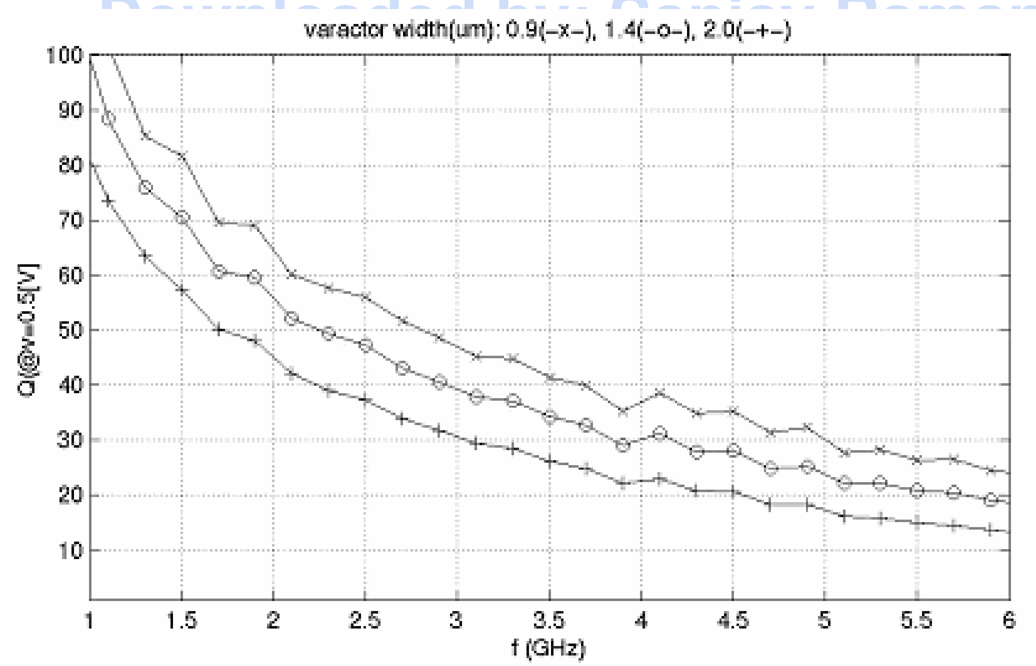


Figure 15.4: CMOS Varactor: Q vs. frequency