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TITLE:

ELECTRICAL PARAMETERS OF THE CA13HC PROCESS

REV	REVISION DESCRIPTION	DATE
01	Initial release.	05/06/05
02	Changed gate lengths for 1.2V FETs from 0.13um to 0.12um. Changed 3.3V nFET gate lengths from 0.35um to 0.36um Updated section 6.3, to change the MIM cap from 2 fF/um2 to 2.8fF/um2. Updated section 4.1.12 to change BV for 2.8ff/um2 MIM cap to > 12V. Corrected units for DNW SW capacitance from pF/m to nF/m in 6.4.3. Reformatted and re-numbered sections.	07/29/05
03	Corrected MT sheet rho values Added dielectric thicknesses and intermetal dapacitances. Added overcoat dielectric thicknesses. Separated conductor thicknesses into a table. Added junction and overlap capacitances for thin gate Added salicided poly sheet rho. Added interconnect current density rules Added stacked 5.6 ff/um2 capacitor rules. Added 3.3V MOS varactor rules	09/02/05
04	Updated MOSFET parameters (secs. 4.1.1, 4.1,2, 4.1.4, 4.1.5, 4.1.9, 4.2.1) Updated MOS varactor parameters (sec. 6.5) Updated M1 sheet rho specs (sec. 4.1.13) Corrected M2-M5 sheet rho max spec. Added lower spec for M1-M6. (sec. 4.1.13) Corrected max area capacitance value for stacked MIM (sec. 6.4)	09/08/06
05	Updated specifications (LSL, USL) for the Unsalicided P-type Poly Resistor Resistance (section 6.1.1); updated end resistance and delta-W. Added high value resistor specs. Added high Vt 1.2V nMOS and pMOS specs. Renamed the process to CA13HC.	11/20/06
06	Section 3.2, Dielectric Thickness – Update thin gate dielectric thicknesses. Section 4, Electrical Parameters – Update CMOS specifications to support 1.5V operation. Section 5, Operating Voltages - Update max DC operating and absolute max voltages.	09/05/07
06	Section 6: Add p+poly salicided resistor specifications	03/23/09

07	Update various thin gate parameters to align with model release 3.0. Primary changes include:
	
	- Short regular Vt NFET (WxL = 10x0.12um)
	  - NOM Vt from 0.39V to 0.36V, Idsat from 5.35mA to 5.6mA
	- Small regular Vt NFET (WxL = 0.15x0.12um)
	  - NOM Vt from 0.31V to 0.29V, Idsat from 76uA to 79uA.
	- Short regular Vt PFET (WxL = 10x0.12um)
	  - No change in Vt, NOM Idsat from -2.35V to -2.5V.
	- Small regular Vt PFET (WxL = 0.15x0.12um)
	  - NOM Vt from -0.34V to -0.25V, Idsat from 35uA to 40uA.
	- Short High Vt NFET (WxL = 10x0.12um)
	  - NOM Vt from 0.59V to 0.58V, Idsat from 3.2mA to 3.4mA.
	- Small High Vt NFET (WxL = 0.15x0.12um)
	  - NOM Vt from 0.50V to 0.48V, Idsat from 47uA to 46uA.
	- Short High Vt PFET (WxL = 10x0.12um)
	  - No change in NOM Vt, Idsat from -1.1mA to -1.4mA.
	- Small High Vt PFET (WxL = 0.15x0.12um)
	  - NOM Vt from -0.48 to -0.34V, Idsat from -21uA to -31uA.
		03/12/10

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1 PURPOSE AND SCOPE

This document covers both process parameters and device parameters for the CA13HC processes. The core CA13HC CMOS may be used for circuits designed for 1.2 to 1.5V Volts operation. The specifications shown below are intended to reflect the mean and ± 3 sigma variation of parameters at 25°C unless otherwise specified.

The CA13HC technology is a dual gate oxide process. The higher voltage transistors are formed with a thicker gate oxide with special masks for the LDD formation. The core CA13HC transistors are referred to as low voltage fets (or 1.2v fets or thin oxide fets) while the thick gate oxide fets are referred to as high voltage fets (3.3v fets or thick oxide fets).

The CA13HC process has six layers of AlCu interconnect metal layers. Design rules through and including contact layer obey 0.13um technology rules while M1 and subsequent layers obey 0.15um technology rules for line and pitch. All contacts and vias use tungsten plugs. It is also a RF/analog/mixed signal process with additional supports for (a) high Vt 1.2V MOS for low leakage, (b) unsalicided poly and nwell resistors, (c) 3.3V MOS varactors, (d) 2.8fF/um2 MIM capacitor on M4, (e) stacked 5.6 fF/um2 MIM capacitors on M4 and M5, (f) a triple well isolation using deep n-well and (g) inductors using 2.8um thick top metal 6.

Summary table:

	No. of metal layers	MIM cap	Stacked MIM cap	High Vt Option (1.2V)	Triple Well	Lateral PNP	Var-actor: p-n, MOS	310 ohm/sq Poly Resistor	High Rs ohm/sq Poly Resistor	MT * thick-ness
CA13HC	6	2.8fF /um2	5.6 fF/um2	Yes	Yes	No	3.3V MOS	Yes	Yes	2.8

MT = topmost metal;

The follow electrical specifications are subject to change after collection of high volume manufacturing data.

2 APPLICABLE DOCUMENTS

Design Rule Document : ***NPB PS-0663***

3 PROCESS PARAMETERS

3.1 Substrate

P type bulk wafer, crystal orientation (100)

Description	Min.	Nom.	Max.	Units
Resistivity of p- bulk	2	3	4	Ω-cm

3.2 Dielectric Thicknesses (final thickness)

Description –	Min.	Nom.	Max.	Units
Gate Oxide-thin (measured by ellipsometer)	21.5	22.5	23.5	Angstroms
Gate Oxide-thin (extracted by leakage current)	21.5	22.5	23.5	Angstroms
Electrical Gate Oxide-thin (for NFET at -2V)		28		Angstroms
Electrical Gate Oxide-thin (for PFET at +2V)		28		Angstroms
Electrical Gate Oxide-thin (for NFET at +1.2V)		30		Angstroms
Electrical Gate Oxide-thin (for PFET at -1.2V)		33		Angstroms
Gate Oxide-thick (measured by ellipsometer)	57	60	63	Angstroms
Electrical Gate Oxide-thick (for NFET at -5.0V; for PFET at +5.0V)				Angstroms
Electrical Gate Oxide-thick (for NFET at +3.3V)	62	65	68	Angstroms
Electrical Gate Oxide-thick (for PFET at -3.3V)	62	65	68	Angstroms
N+Poly/Nwell Gate Oxide-thin (at +1.2V)				Angstroms
N+Poly/Nwell Gate Oxide-thick (at +3.3V)				Angstroms

Note: The Electrical Gate Oxide-thin (for NFET at -2V) and Electrical Gate Oxide-thin (for PFET at +2V) are extracted from the capacitance measurement at accumulation. Electrical Gate Oxide-thin (for NFET at +1.2V) ,Electrical Gate Oxide-thin (for PFET at -1.2V), Electrical Gate Oxide-thick (for NFET at +3.3V) and Electrical Gate Oxide-thick (for PFET at -3.3V) are extracted from capacitance measurement at inversion.

Layer thickness Description	**Min**	**Nominal**	**Max**	**Units**
Poly to Sub (Si under field)	2.10	2.80	3.50	kAngstroms
M1 to Poly 1	3.00	5.25	7.00	kAngstroms
M1 to Diff	4.75	7.00	9.25	kAngstroms
M1 to Si under field	7.45	9.80	12.15	kAngstroms
M2 to M1	5.00	7.00	9.00	kAngstroms
M2 to Poly 1 (field)	13.40	16.45	19.50	kAngstroms
M2 to Diff	15.15	18.20	21.25	kAngstroms
M2 to Si under Field	17.87	21.00	24.13	kAngstroms
M3 to M2	5.00	7.00	9.00	kAngstroms
M3 to M1	16.26	19.20	22.14	kAngstroms
M3 to Poly 1 (field)	25.60	28.65	31.70	kAngstroms
M3 to Diff	26.67	30.40	34.13	kAngstroms
M3 to Si under Field	29.40	33.20	37.00	kAngstroms
M4 to M3	5.00	7.00	9.00	kAngstroms
M4 to M2	16.26	19.20	22.14	kAngstroms
M4 to M1	27.76	31.40	35.04	kAngstroms
M4 to Poly 1 (field)	37.11	40.85	44.59	kAngstroms
M4 to Diff	38.29	42.60	46.91	kAngstroms
M4 to Si under Field	41.03	45.40	49.77	kAngstroms
M5 to M4	5.00	7.00	9.00	kAngstroms
M5 to M3	16.26	19.20	22.14	kAngstroms

M5 to M2	27.76	31.40	35.04	kAngstroms
M5 to M1	39.37	43.60	47.83	kAngstroms
M5 to Poly 1 (field)	48.74	53.05	57.36	kAngstroms
M5 to Diff	49.98	54.80	59.62	kAngstroms
M5 to Si under Field	52.73	57.60	62.47	kAngstroms
M6 to M5	5.00	7.00	9.00	kAngstroms
M6 to M4	16.26	19.20	22.14	kAngstroms
M6 to M3	27.76	31.40	35.63	kAngstroms
M6 to M2	39.37	43.60	48.35	kAngstroms
M6 to M1	51.05	55.80	60.55	kAngstroms
M6 to Poly 1 (field)	60.43	65.25	70.07	kAngstroms
M6 to Diff	61.72	67.00	72.28	kAngstroms
M6 to Si under Field	64.48	69.80	75.12	kAngstroms
Overcoat oxide*	1.80	2.00	2.20	kAngstroms
Overcoat nitride	5.40	6.00	6.60	kAngstroms

* The specifications are for the thickness on top of the metal. The thisckness along the sidewall of the thick top metal is approximately 60% lower than above die to non-conformal deposition of the dielectric film.

3.3 Conductor Thicknesses (final)

Description	Min.	Nom.	Max.	Units
Poly 1 (including polycide)	1.65	1.75	1.85	kAngstroms
Metal 1	3.70	4.20	4.70	kAngstroms
Metal 2, Metal 3, Metal 4, Metal 5	4.40	5.20	6.00	kAngstroms
Metal 6	25.10	28.10	31.10	kAngstroms

4 ELECTRICAL PARAMETERS

4.1 DC Parameters

4.1.1 Threshold Voltages

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 10µm-1.2v fets	0.22	0.25	0.28	-0.215	-0.255	-0.295	volts
10µm x 0.12µm-1.2v fets	0.30	0.36	0.42	-0.30	-0.36	-0.42	volts
0.15µm x 10µm- 1.2v fets	0.03	0.11	0.19	-0.12	-0.22	-0.32	volts
0.15µm x 0.12µm- 1.2v fets	0.17	0.29	0.41	-0.13	-0.25	-0.37	Volts
10µm x 10µm-3.3v fets	0.59	0.67	0.75	-0.73	-0.82	-0.91	Volts
10µm x 0.36µm-3.3v fets	0.56	0.66	0.76				Volts
10µm x 0.30µm-3.3v Pfets				-0.63	-0.73	-0.83	Volts

Note: Threshold voltage, V_T, is calculated from a measured Id versus Vgs curve at Vs=0 and Vd=+50mV (-50mV for P-channel). A line tangent to this curve at the maximum slope point is found. The intercept of this tangent with the Vgs axis is then determined. V_T is defined as the value of the Vgs intercept minus 1/2 Vd.

4.1.1.1 Threshold Voltages for High Vt 1.2V FETs

Description	High Vt N-channel			High Vt P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 10µm-1.2v fets	0.41	0.45	0.49	-0.41	-0.45	-0.49	volts
10µm x 0.12µm-1.2v fets	0.52	0.58	0.64	-0.51	-0.56	-0.61	volts
0.15µm x 10µm- 1.2v fets	0.22	0.32	0.42	-0.23	-0.33	-0.43	volts
0.15µm x 0.12µm- 1.2v fets	0.36	0.48	0.60	-0.22	-0.34	-0.46	Volts

4.1.2 Temperature Dependence of Threshold Voltages

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 10µm for 1.2v fets		-6.0e-4			6.0e-4		Volt/°C
10µm x 10µm for 3.3v fets		-1.00E-3			1.20E-3		Volt/°C

4.1.3 Transconductances

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 10µm-1.2v fets	174	194	214	40.5	43.5	46.5	$\mu A/V^2$
10µm x 10µm-3.3v fets	77	86	95	16	19	22	$\mu A/V^2$

Note: Transconductance is calculated from the maximum slope of transfer curve @Vd=0.05 V and defined as $\mu_0 C_{ox}/2$.

4.1.3.1 Transconductances for High Vt 1.2V FETs

Description	High Vt N-channel			High Vt P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 10µm-1.2v fets	141	161	181	33	36	39	$\mu A/V^2$

Note: Transconductance is calculated from the maximum slope of transfer curve @Vd=0.05 V and defined as $\mu_0 C_{ox}/2$.

4.1.4 Saturation Currents

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm - for 1.2v fets	4.76	5.6	6.44	2.0	2.50	3.0	mA
0.15µm x 0.12µm –for 1.2v fets	55	79	103	28	40	52	µA

Note: Vd=Vg=1.2V or -1.2V for 1.2v N-ch or P-ch fets respectively. The 0.15um wide device was drawn with dogbone active and minimum poly to active spacing, so the current drive is higher than devices with wider poly to active spacing. All the specified structures have isolated transistor.

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.36µm for 3.3v fets	4.7	5.7	6.7				mA
10µm x 0.30µm for 3.3v Pfet				2.4	2.9	3.4	mA
0.60µm x 0.36µm –for 3.3v fets	255	330	405				µA
0.60µm x 0.30µm –for 3.3v Pfet				100	150	200	µA

Note: Vd=Vg=3.3V or –3.3V for N-ch or P-ch fets respectively. All structures have isolated transistor.

4.1.4.1 Saturation Currents for High Vt 1.2V FETs

Description	High Vt N-channel			High Vt P-channel			
	Min	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm - for 1.2v fets	2.72	3.4	4.08	1.05	1.4	1.75	mA
0.15µm x 0.12µm –for 1.2v fets	30	46	62	20	31	42	µA

Note: Vd=Vg=1.2V or -1.2V for 1.2v N-ch or P-ch fets respectively. The 0.15um wide device was drawn with dogbone active and minimum poly to active spacing, so the current drive is higher than devices with wider poly to active spacing. All the specified structures have isolated transistor.

4.1.5 Body Constants

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 10µm - 1.2v fets	0.23	0.25	0.27	0.265	0.29	0.315	$V^{0.5}$
10µm x 0.12µm - 1.2v fets	0.17	0.21	0.25	0.25	0.28	0.31	$V^{0.5}$
0.15µm x 10µm - 1.2v fets	0.145	0.185	0.225	0.12	0.19	0.26	$V^{0.5}$
0.15µm x 0.12µm - 1.2v fets	0.115	0.145	0.175	0.13	0.21	0.29	$V^{0.5}$
10µm x 10µm - 3.3v fets	0.54	0.61	0.68	0.82	0.92	1.02	$V^{0.5}$
10µm x 0.36µm - 3.3v fets	0.40	0.50	0.60				$V^{0.5}$
10µm x 0.30µm - 3.3v Pfet				0.77	0.87	0.97	$V^{0.5}$

Note: Body constant is measured at Vbs=0V and Vbs=-0.6V for N-channel 1.2v devices, and measured at Vbs=0V and Vbs=+0.6V for P-channel 1.2v devices. Body constant is measured at Vbs=0V and Vbs=-1.65V for N-channel 3.3v devices, and measured at Vbs=0V and Vbs=+1.65V for P-channel 3.3v devices.

4.1.6 Effective Channel Lengths / External Resistances

4.1.6.1 Effective Channel Lengths

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm (traditional) – 1.2v fets	0.134	0.149	0.164	0.087	0.102	0.117	µm
10µm x 0.36µm (traditional)- 3.3v fets	0.26	0.30	0.34	0.23	0.27	0.31	µm
10µm x 0.30µm (traditional)- 3.3v Pfet				0.17	0.21	0.25	µm

Note: The traditional method of the effective channel length is simply calculated by the transconductance comparison with a 10µm x 10µm device.

4.1.6.2 External Resistances

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm (Leff2) - for 1.2v fets	12	20	30	10	40	70	Ohms
10µm x 0.36µm (Leff2)- for 3.3v fets	25	45	65				Ohms
10µm x 0.30µm (Leff2)- for 3.3v Pfet				50	90	130	Ohms

Note: The external resistance of transistor is defined as the effective series resistance associated with both drain and source sides of the transistor and is obtained from Leff2 method used in the effective channel length calculation. Due to uncertainties in the accuracy of the above values, they are primarily useful for process control, and the range of values does not reflect the range of values used in SPICE models. The external resistance values for CA13HC FETs may not be accurately measured by the Leeff2 method due to the additional Halo implant that gives a strong lateral variation of doping along the channel; the typical values are provided here for reference.

4.1.7 Subthreshold Slopes

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm - for 1.2v fets		82	100		84	100	mV/decade
10µm x 0.36µm- for 3.3v fets		85	100				mV/decade

10µm x 0.30µm- for 3.3v Pfet					90	100	mV/decade

Note: The subthreshold slope is measured at a drain voltage of 0.05V at RT.

4.1.8 Maximum Substrate Current Densities

Description	**N-channel**			**P-channel**			
	Min.	**Nom.**	**Max.**	**Min.**	**Nom.**	**Max.**	**Units**
10µm x 0.12µm - for 1.2v fets	0.05	0.2	1.0		0.0008	0.02	µA/µm
10µm x 0.36µm- for 3.3v fets	0.5	1.2	3.0		0.06	0.15	µA/µm
10µm x 0.30µm- for 3.3v Pfet					0.09	0.25	µA/µm

Note: Measured at Vd=1.32V for the 1.2v fets and Vd=3.6V for the 3.3v fets with Vg selected for maximum substrate current. The range of peak substrate currents are approximately from Vg=0.7v to 1.3v

4.1.9 Transistor Off Leakage Currents

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm (@25℃) - for 1.2v fets			30			10	nA/µm
10µm x 0.12µm (@85℃) - for 1.2v fets			750			750	nA/µm
10µm x 0.36µm (@25℃)- for 3.3v Nfets			0.01				nA/µm
10µm x 0.36µm (@85℃)- for 3.3v Nfets			0.30				nA/µm
10µm x 0.30µm (@25℃)- for 3.3v Pfets						0.04	nA/µm
10µm x 0.30µm (@85℃)- for 3.3v Pfets						2.0	nA/µm

Note: Vg=0V, Vd=1.32V or –1.32V for the 1.2v N-ch or P-ch fets respectively. Vg=0V, Vd=3.6V or -3.6V for the 3.3v N-ch or P-ch fets respectively. For estimation of circuit standby current only.

4.1.9.1 Transistor Off Leakage Currents for High Vt 1.2V FETs

Description	High Vt N-channel			High Vt P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
10µm x 0.12µm (@25℃) - for 1.2v fets		0.001	0.01		0.001	0.01	nA/µm
10µm x 0.12µm (@85℃) - for 1.2v fets			0.25			0.25	nA/µm

Note: Vg=0V, Vd=1.32V or –1.32V for the 1.2v N-ch or P-ch fets respectively.

4.1.10 Diode Leakage Currents

Description	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
Perimeter - for low voltage junctions			10			20	fA/µm
Area - for low voltage junctions			1			1	fA/µm^2
Perimeter - for high voltage junctions			10			10	fA/µm
Area - for high voltage junctions			1			1	fA/µm^2

Note: Vg=0V, Vd=1.32V or –1.32V for low voltage N-diffusion or standard P-diffusion, respectively, at 25°C. Vg=0V, Vd=3.6V or -3.6V for high voltage N-diffusion or standard P-diffusion, respectively, at 25°C. The area leakage current increases by less than a factor of 2 for each 10°C increase in temperature. The perimeter leakage current increases by a factor of 2 for every 15C increase in temperature.

4.1.11 Breakdown Voltages

Description	N-ch	P-ch	Units
Low voltage fets (1.2v fets):			
10µm x 10µm - 1.2v fets	>2.9	<-2.9	volts
10µm x 0.12µm - 1.2v fets	>2.4	<-2.4	volts
0.6µm x 10µm - 1.2v fets			volts
0.6µm x 0.12µm – 1.2v fets			volts
0.24µm x 10µm - 1.2v fets			volts
0.24µm x 0.12µm – 1.2v fets			volts
0.44µm x 0.12µm – 1.2v fets			volts
High voltage fets (3.3v fets):			
10µm x 10µm - 3.3v fets: (DG masked)	>5.0	<-4.5	volts
10µm x 0.36µm – 3.3v Nfets: (DG masked)	>5.0		volts
10µm x 0.30µm – 3.3v Pfets: (DG masked)		<-4.5	volts
10µm x 0.36µm - 3.3v fets: (DG masked) open-source configuration	>6.0	n/a	volts
Junctions:			
Junction; low voltage junctions (1.2v nominal operation)			volts
Junction; high voltage junctions: (DG masked) (3.3v nominal operation)	>7.0	<-5.0	volts
VFI (field inversion test):			
Poly VFI 50x0.21µm; low voltage junctions			volts
Metal 1 to (N-1) VFI 50x0.21µm; for low voltage junctions			volts
Metal N VFI 50x0.21µm; for low voltage junctions			volts
Poly VFI 50x0.21µm; high voltage junctions:(DG masked)			volts

Metal 1 to (N-1) VFI 50x0.21µm; high voltage junctions: (DG masked)			volts
Metal N VFI 50x0.21µm; high voltage junctions:(DG masked)			volts

Notes: The breakdown voltage is measured at Idrain=1µA for N-channel (or -1µA for P-channel) devices at room temperature. For CA13HC process, please use N= 6.

The open-source configuration is for the high voltage nfet test to verify 5v tolerant operation of input receivers. The configuration is a breakdown voltage test. The breakdown is measured at Idrain=1µA for N-channel at room temperature. The source is open, gate is 3.3v, substrate is grounded.

4.1.12 Dielectric Breakdown Voltages

Description		**Units**
Gate oxide for thin oxide	>2.4	Volts
Gate oxide for thick oxide (TDDB)	>8.0	Volts
Poly to substrate	>200	Volts
Metal 1 to poly 1	>200	Volts
Metal 2 to metal 1	>200	Volts
Metal 3 to metal 2	>200	Volts
Metal 4 to metal 3	>200	Volts
Metal 5 to metal 4	>200	Volts
Metal 6 to Metal 5	>200	Volts
MIM Capacitor	>12.0	Volts

Note: The maximum voltage allowed to be applied to gate oxide is 1.32 V for the thin gate oxides. The maximum voltage allowed to be applied to gate oxide is 3.6 V for the thick gate oxides. The quoted breakdown voltage of thick gate oxide (the TDDB gate oxide accelerated reliability tests) is measured at the rupture of the oxide under voltage ramp of 2V/sec.

4.1.13 Sheet Resistivity

Description	Min.	Nom.	Max.	Units
N-well sheet resistance R_s(under field oxide) †	710	890	1070	Ω/ ☐
End Resistance (Both Ends) – R_{end}†	700	875	1050	Ω - um
N-well ΔW electrical (under field oxide) †	-0.18	-0.28	-0.38	µm
N+ diffusion sheet resistance		7.1	12	Ω/ ☐
P+ diffusion sheet resistance		7.6	12	Ω/ ☐
Salicided poly sheet resistance		7.0	12	Ω/ ☐
Metal 1	100	120	140	mΩ/ ☐
Metal 2-5	69	82	95	mΩ/ ☐
Metal 6	9.0	10.5	12.0	mΩ/ ☐

Note: The sheet resistivity for diffusion or poly is the combination result of resistivities of both silicide and diffusion (poly) layer.
† The total N-well resistance R_{well} can be calculated using the formula and data below:

$$R_{well} = R_S*L/(W-\Delta W) + R_{end}/(W-\Delta W)$$

W is the drawn width and L is the drawn length, respectively. ΔW is used here to account for the difference between the electric width vs. the drawn width caused by the dopant diffusion and the non-ideal photo (well) exposure effects. To correct for the modulation partly caused by retrograde well profiles and shallow trench isolation, the end resistance (including both ends) R_{end} has to be included in the formula to correctly calculate the total N-well resistance.

* The salicided poly resistance R_{poly} can be calculated using the formula below:

$$R_{poly} = R_S*L/(W-\Delta W) + R_{end}/(W-\Delta W)$$

W is the drawn width and L is the drawn length, respectively. ΔW is used here to account for poly patterning effects (photo and etch).

4.2 AC Parameters

4.2.1 Capacitance

Description –	N-channel			P-channel			
	Min.	Nom.	Max.	Min.	Nom.	Max.	Units
Gate oxide capacitance-thin oxide (N+ Poly over N-ch at -2.0V & P+ Poly over P-ch at +2.0V)		12.3			11.3		fF/µm^2
Gate oxide capacitance-thin oxide (N+ Poly over N-ch at +1.2V & P+ Poly over P-ch at –1.2V)		12.5			12.1		fF/µm^2

Gate overlap drain or source for 1.2V FETs (V_{GS}=0V)		470			494		aF/µm
Gate overlap drain or source for 1.2V FETs (V_{GS} = -0.6V for NFET; +0.6V for PFET)		453			432		aF/µm
P+/N+ junction area cap for 1.2V junctions	676	751	826	780	867	954	aF/µm^2
P+/N+ 1.2V junction sidewall to field	67.5	75	82.5	112	124	136	aF/µm
P+/N+ junction sidewall to channel for 1.2V FETs	326	362	398	477	530	583	aF/µm
Gate oxide capacitance-thick oxide (N+ Poly over N-ch at –3.3V & P+ Poly over P-ch at +3.3V)	4.54	4.93	5.40	4.54	4.93	5.40	fF/µm^2
Gate overlap drain or source for 3.3V FETs (V_{GS}=0V)		363			318		aF/µm
Gate oVerlap drain or source for 3.3V FETs (V_{GS} = -1.65V for NFET; +1.65V for PFET)		265			244		aF/µm
P+/N+ junction area cap for 3.3V junctions	598	665	732	666	740	814	aF/µm^2
P+/N+ 3.3V junction sidewall to field	90	100	110	98	109	120	aF/µm
P+/N+ junction sidewall to channel for 3.3V FETs	265	294	323	300	334	367	aF/µm
N-well area capacitance				140	180	220	aF/µm^2
N-well perimeter capacitance				600	750	900	aF/µm

Note: All junction capacitances were measured at zero bias. Due to lack of statistical data for junction and overlap capacitances, the variation in these capacitance values is primarily useful for process control and the range of variation does NOT reflect the range of values used in SPICE models. The metal capacitance values only represent the parallel plate component; capacitance due to fringing effects and additional dummy active patterns are not included here.

Description	Capacitance (aF/um2)			
	Min	Nom.	Max.	Units
Poly to Sub (Si under field)	106.3	132.8	177.1	aF/um2
M1 to Poly 1	53.1	65.8	124.0	aF/um2
M1 to Diff	40.2	49.3	78.3	aF/um2
M1 to Si under field	29.0	36.0	47.3	aF/um2
M2 to M1	41.3	53.1	74.4	aF/um2
M2 to Poly 1 (field)	18.6	22.1	27.1	aF/um2

M2 to Diff	17.0	19.8	23.8	aF/um2
M2 to Si under Field	15.0	17.3	20.3	aF/um2
M3 to M2	41.3	53.1	74.4	aF/um2
M3 to M1	16.8	19.4	22.9	aF/um2
M3 to Poly 1 (field)	11.7	13.0	14.5	aF/um2
M3 to Diff	10.7	12.0	13.7	aF/um2
M3 to Si under Field	9.9	11.0	12.4	aF/um2
M4 to M3	41.3	53.1	74.4	aF/um2
M4 to M2	16.8	19.4	22.9	aF/um2
M4 to M1	10.6	11.8	13.4	aF/um2
M4 to Poly 1 (field)	9.2	10.0	11.0	aF/um2
M4 to Diff	8.7	9.6	10.6	aF/um2
M4 to Si under Field	8.1	8.9	9.9	aF/um2
M5 to M4	41.3	53.1	74.4	aF/um2
M5 to M3	16.8	19.4	22.9	aF/um2
M5 to M2	10.6	11.8	13.4	aF/um2
M5 to M1	7.8	8.5	9.4	aF/um2
M5 to Poly 1 (field)	7.0	7.6	8.2	aF/um2
M5 to Diff	6.7	7.3	8.0	aF/um2
M5 to Si under Field	6.4	6.9	7.5	aF/um2
M6 to M5	41.3	53.1	74.4	aF/um2
M6 to M4	16.8	19.4	22.9	aF/um2
M6 to M3	10.4	11.8	13.4	aF/um2
M6 to M2	7.7	8.5	9.4	aF/um2
M6 to M1	6.1	6.7	7.3	aF/um2
M6 to Poly 1 (field)	5.6	6.1	6.5	aF/um2
M6 to Diff	5.4	5.9	6.4	aF/um2
M6 to Si under Field	5.2	5.6	6.1	aF/um2

4.3 Interconnect Parameters

4.3.1 Intermetal and Intrametal Dielectric Constants

Description	Min.	Nom.	Max.	Units
Poly on field to silicon		4.2		ε/ε0
Metal 1 to Poly		3.9		ε/ε0
Metal N to metal (N-1), N=2 to 6		4.2		ε/ε0
Oxide overcoat		4.2		ε/ε0
Nitride overcoat		7.0		ε/ε0

4.3.2 Contact and Via Resistance

Description	Min.	Nom.	Max.	Units
Metal 1 to N+ silicide		12.5	25.0	Ω/contact
Metal 1 to P+ silicide		12.5	25.0	Ω/contact
Metal 1 to poly 1 silicide		12.5	25.0	Ω/contact
Metal 2 to metal 1 (via) resistance		10.0	25.0	Ω/contact
Metal 3 to metal 2 (via2) resistance		10.0	25.0	Ω/contact
Metal 4 to metal 3 (via3) resistance		10.0	25.0	Ω/contact
Metal 5 to metal 4 (via4) resistance		10.0	25.0	Ω/contact
Metal 6 to metal 5 (via5) resistance		3.0	10.0	Ω/contact

4.4 Interconnect Current Densities for Reliable Operation

4.4.1 DC Operation

Description	@85°C	@110°C	@125°C	Units
Metal 1 (4200 A)	2.0	0.7	0.3	mA/µm
Metals 2, 3, 4, 5 (5200 A)	2.6	0.9	0.4	mA/µm
Metal 6 (28100 A)	16	5.8	2.7	mA/µm
Contact (0.16µm x 0.16µm)	0.5	0.4	0.3	mA/Contact
Via, Via2, Via 3, Via 4 (0.22µm x 0.22µm)	0.61	0.50	0.43	mA/Via
Via 5 (0.36µm x 0.36µm)	1.3	1.0	0.9	mA/Via

Note: Ratings provide 10 FIT reliability for 10 years. For Pulsed DC current operation, use the average current density.

4.4.2 AC Operation

Description	@85°C	@110°C	@125°C	Units
Metal 1	8.0	2.8	1.2	mA/µm
Metals 2, 3, 4, 5	10.4	3.6	1.6	mA/µm
Metal 6	65	23	11	mA/µm
Contact (0.16µm x 0.16µm)	1	0.8	0.6	mA/Contact
Via, Via2, Via 3, Via 4 (0.22µm x 0.22µm)	1.2	1	0.8	mA/Via
Via 5 (0.36µm x 0.36µm)	2.7	2.1	1.8	mA/Via

Note: Ratings provide 10 FIT reliability for 10 years. For Pulsed DC current operation, use the average current density.

5 ELECTRICAL CIRCUIT DESIGN SPECIFICATONS

The following specifications apply to all circuits to be produced using the CA13HC processes. Achievement of this performance level relies on proper circuit designs, and is not an inherent feature of the CA13HC process. It is the responsibility of the circuit designer to meet these criteria.

5.1 Power Supply Voltage

5.1.1 Maximum D.C. Operating Voltage

Description	Min.	Nom.	Max.	Units
The maximum applied D.C. voltage between ANY two terminals for 1.2V FETs		1.5	1.65	Volts
The maximum applied D.C. voltage between ANY two terminals for 3.3V FETs		3.3	3.6	Volts

5.1.2 Absolute Maximum Continuous Ratings

Description	Min.	Nom.	Max.	Units
The maximum applied voltage between ANY two terminals for 1.2V FETs	-0.5		2.0	Volts
The maximum applied voltage between ANY two terminals for 3.3V FETs	-0.5		4.6	Volts

Note: Absolute maximum continuous rating are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation above maximum operating voltage or under absolute-maximum conditions is not implied. These ratings conform to the JEDEC standards JESD8-A and EIA/JESD8-7.

6 ELECTRICAL PARAMETERS OF ANALOG/MIXED SIGNAL COMPONENTS

6.1 Unsalicided P-Poly Resistors

6.1.1 Low Value Unsalicided P-Poly Resistor Resistance

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.	Nom.	Max.	Units
Sheet Resistance – Rs	264	310	357	Ω/ □
End Resistance (Both Ends) – Rend	60	85	110	Ω - um
Delta W	-0.06	-0.05	-0.04	um

6.1.1.1 Maximum Current Density for Unsalicided Poly Resistors

Description	Min.	Nom.	Max.	Units
Jmax (Steady State)			1.3	mA/um

6.1.1.2 Maximum Temperature Rise for Poly Resistors (Steady State)

For P-poly resistors

Single resistor (no similar resistor within 5 um)

$\Delta T <= 0.26 * Rs * Jmax^2$ ℃

Multiple resistors (similar resistor within 5 um)

$\Delta T <= 0.52 * Rs * Jmax^2$ ℃

where, Rs = unsalicided poly sheet resistance (Ohm/square)
Jmax = maximum steady state current density (mA/um)

6.1.2 High Value Unsalicided P-Poly Resistor

Resistance, $R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$

Description	Min.	Nom.	Max.	Units
Sheet Resistance – Rs	850	1000	1150	Ω/ □
End Resistance (Both Ends) – Rend	253	316	379	Ω - um
Delta W	-0.056	-0.046	-0.036	um

6.1.2.1 Maximum Current Density for Unsalicided Poly Resistors

Description	Min.	Nom.	Max.	Units
Jmax (Steady State)			0.2	mA/um

6.1.3 Salicided P-Poly Resistors

$$R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.	Nom.	Max.	Units
Sheet Resistance – Rs		6.5		Ω/ □
End Resistance (Both Ends) – Rend		19		Ω - um
Delta W		0.03		um

Note Min and Max values will be determined after additional manufacturing data has been collected.

6.1.3.1 Maximum Temperature Rise for Poly Resistors (Steady State)

For P-poly resistors

Single resistor (no similar resistor within 5 um)

$\Delta T <= 0.26 * Rs * Jmax^2$ ℃

Multiple resistors (similar resistor within 5 um)

$\Delta T <= 0.52 * Rs * Jmax^2$ ℃

where, Rs = unsalicided poly sheet resistance (Ohm/square)
Jmax = maximum steady state current density (mA/um)

6.1.4 Nwell Resistors

$$\text{Resistance, } R = \frac{Rs \cdot L}{W + \Delta W} + \frac{Rend}{W + \Delta W}$$

Description	Min.	Nom.	Max.	Units
Sheet Resistance – Rs	710	890	1070	Ω/ □
End Resistance (Both Ends) – Rend	700	875	1050	Ω - um
Delta W	-0.38	-0.28	-0.18	um

6.2 Vertical Metal-Insulator-Metal (MIM) Capacitors (2.8fF/μm^2 density)

The vertical MIM capacitors are between Metal 4 and Metal 5 or between Metal 5 and Metal 6. Capacitor has a thin nitride film as the dielectric.

Description	Min.	Nom.	Max.	Units
Area Capacitance	2.34	2.75	3.16	fF/μm^2
Perimeter Capacitance	0.05	0.15	0.25	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate	-70	-50	-30	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient		20		ppm/℃
Absolute Applied Voltage Bias			3.6	V
Leakage current @25C, 3.6 V (area: 60,000um^2)			10	nA

6.3 Stacked Vertical Metal-Insulator-Metal (MIM) Capacitors (5.6fF/μm^2 density)

These stacked vertical MIM capacitors are TM2 to metal 5 capacitors stacked on top of TM to metal 4 capacitors. Each of the capacitors has a thin nitride film as the dielectric.

Description	Min.	Nom.	Max.	Units
Area Capacitance	4.68	5.5	6.32	fF/μm^2

Perimeter Capacitance	0.1	0.3	0.5	fF/μm
Linear Voltage Coefficient (LVCC), polarity with bias on TM plate	-10	0	10	ppm/V
Quadratic Voltage Coefficient (QVCC)	0	20	40	ppm/V^2
Temperature Coefficient		20		ppm/℃
Absolute Applied Voltage Bias			3.6	V
Leakage current @25C, 3.6 V (area: 60,000um^2)			20	nA

6.4 MOS Varactor

This varactor is built with 3.3V N+ poly and gate oxide on Nwell.

Description	Min.	Nom.	Max.	Units
Capacitance@ 1 V (pF) for 3 x 0.5 x 15 x 40 device	4.86	5.03	5.20	pF
Capacitance Sensitivity* (%/V)	36	44	52	%/V
Q (2GHz at 1 V) for 3 x 0.5 x 2 x 10 device	122	163		
Q (5GHz at 1 V) for 3 x 0.5 x 2 x 10 device	49	65		
Q (10GHz at 1 V) for 3 x 0.5 x 2 x 10 device	24.5	32.5		

Capacitance Sensitivity = 2*(Cap @ 0.5V - Cap @ -0.5V)/(Cap @ 0.5V + Cap @ -0.5V)

6.5 Vertical PNP Bipolar Transistor

6.5.1 Beta - Current Gain

Description	**Min.**	**Nom.**	**Max.**	**Units**
25μm x 25μm Beta (Ie = 1μA, 20μA), Vce = -1V	1.3	1.8	2.3	NA
Ic @ Vbe = 0.7V		55.7		uA
Early Voltage	100			V

6.6 Deep N Well Specifications for Triple Well Isolation

6.6.1 Breakdown voltages

Description	Min.	Nom.	Max.	Units
Deep Nwell to isolated pwell junction	6			Volts
Deep nwell to p-substrate junction	6			Volts

6.6.2 Deep Nwell Resistances

Description	Min.	Nom.	Max.	Units
Sheet Resistance*		470		ohm/sq
End Resistance*		3400		ohm-um
Delta W		0.3		um

*Total Resistance = [L / (W + Delta W)] * Sheet Resistance + End Resistance /(W + Delta W)

6.6.3 Deep Nwell Capacitances

Description	Min.	Nom.	Max.	Units
Area capacitance deep nwell to isolated pwell junction		546.6		uF/m^2
Sidewall capacitance deep nwell to isolated pwell junction		1.346		nF/m
Area capacitance deep nwell to p-substrate junction		126.7		uF/m^2
Sidewall capacitance deep nwell to p-substrate junction		3.124		nF/m

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