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TITLE:

CA13HC DESIGN RULES

REV	REVISION DESCRIPTION	DATE
1	Initial release of document.	4/06/05
2	Changes for this revision: Revise section numbering to match other released Design Rule documents; Update Stress, LUP, Bondpad, Best Practices sections with verbiage from CA18 design rules.; Add SoftERC section Added 2.X (description only), 12.A.a (DG width), 5.N.1 and 5.N.2 (minimum area and area enclosed by poly); 40.L (minimum area enclosed by salicide block); Removed 12.D, 12.E, 12.F (conflicting with 2.D.a, 2.E.a, 2.F.a), 5.I (covered by 6.D.d and 11.D.d); 7.H. Updated 5.A.1 (DG gate length) from 0.35um to 0.36um. Added inductor and balun rules (section 5.3). Updated antenna rules to match aluminum backend. Updated figures 2, 12, 61, 59, 14, 40, 7, 17, 27, 37, 47, MC. Corrected layer ordering and description (sections 3.2, 3.3) Removed “Field (F)” implant reference from section 3.2 and chapter 4.	7/29/2005
3	Added stacked vertical MIM capacitor rules. Added maximum metal density rules for M1, M2, M3, M4, and M5. Added MIM cap antenna rules. Removed mask alignment information from section 3.2. Added MOS varactor rules. Removed Boundary, Pin, Device and Marking layers table. Update table 3.1.4.	09/14/05

4	Removed references to NWL, NWH, PWL, PWH. Replaced by adding F (field) and W (nwell) layers. Added HVTN and HVTP layers for high Vt options. Added metal enclosure rules (section 5.9) to prevent accidental generation of any data types other than "0". Removed MC6, MC7, SMC6, SMC7, SMC16 and SMC17 rules. They do not pose any risk to the product. Corrected data-type of ABLB layer from 40 to 53 in section 5.6. Corrected poly thickness description in section 8.1. Included High value resistor design rules. Updated metal dummy fill generation rules to incorporate custom dummy fill block layer. Added rules for standalone TM2 MIM cap on M5 Removed BD.K rule to allow building circuits under pads (CUP). Added DNW.22 specifying list of devices allowed and not allowed inside a deep nwell. Added native nFET rules Added VPNP rules Updated MOSVAR rules. Updated the GDS layer assignment table to make it current. Added a comment in all resistor-related sections to require drawing "resdev" layer (80/0) for lvs purpose. Corrected layer identification for Inductor marking layer from 51 to 118/42. Replace 51.* rules with IML.*. Replaced 52.* rules with NATV.* rules. Corrected artifact marking layer identification from 45/0 to 118/40. Corrected analog blocking layer (ABLB) identification from 95 to 118/53. Renamed the process to CA13HC.	11/01/2006
5	Added new rules 40.C.a, 40.G.a, 40.G.b to include the special cases of ESD FETs. Simplified metal area rules (8.E and 8.E.a) into new 8.E rule. 8.C.b rule clarified, consistent with the implementation in the PDK. Separated 8.C.b rule relating to via into 8.C.b.1 rule, consistent with the PDK. Corrected BD.6 rule to 6um from 3um; removed redundant rule BD.6.a rule (was 6 um) Changed 60um pad pitch to 63um pad pitch	12/21/2006

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1. Purpose and Scope

This document contains the design rules for the CA13HC process. These rules are for all circuit designs to be manufactured using the CA13HC process or the foundry equivalent. The CA13HC process is a CMOS bulk silicon process with 19.5Å gate oxide and 0.12 um minimum drawn gate lengths. CA13HC process includes the dual gate oxide process for interfacing to circuits up to 3.3V nominal with thick gate oxide transistors. These rules are general for designs with nominal Vdd supplies of 1.2V and up to 3.3V for the thick gate oxide transistors. All rules apply to 1.2V nominal operation except where specified. All dimensions are in microns (um) or square microns (um^2). This process has salicided diffusions and poly. The layout grid resolution is 0.005um. The CA13HC design includes six aluminum metal layers.

1.1. Description of Process

CA13HC process includes the dual gate oxide module for interfacing to circuits up to 3.3V nominal with thick gate oxide transistors. A high Vt option is also included for 1.2V MOS for low leakage applications. It has six layers of aluminum metal, 2.8 fF/um^2 metal-insulator-metal (MIM) capacitor on metal 4 or metal 5, stacked 5.6 fF/um2 MIM cap on metal 4 and metal 5, a triple well module by adding a deep nwell mask and implant, MOS varactor, Nwell resistor and unsalicided low value and high value P-poly resistors. Metal 6, the top metal, is 2.8um thick aluminum to support high Q inductors.

Summary table:

	No. of metal layers	MIM cap	Stacked MIM cap	High Vt Option (1.2V)	Triple Well	Lateral PNP	Var-actor: p-n, MOS	310 ohm/sq Poly Resistor	High Rs ohm/sq Poly Resistor	MT * thick-ness
CA13HC	6	2.8fF/ um2	5.6 fF/um2	Yes	Yes	No	3.3V MOS	Yes	Yes	2.8

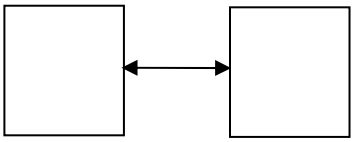
MT = topmost metal;

1.2.

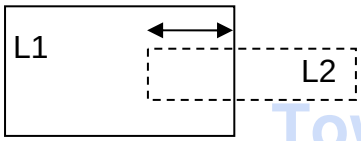
Terminology of Rules

A description of typical terminology used in the design rules is shown below.

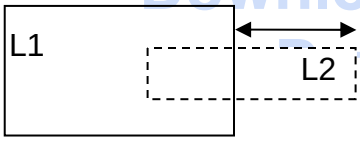
WIDTH OR LENGTH



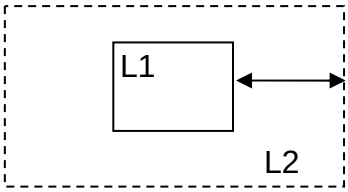
SPACE OR DISTANCE



L2 OVERLAP INTO L1



L2 OVERLAP OUT OF L1



L2 OVERPLOT OF L1
(Note: L1 is covered by L2)

2. Applicable Documents

CA13HC Mask Requirements Specification	NPB-PS-0579
CA13HC Electrical Specification	NPB PS-0577
CA13HC Spice Data Bank	TBD

3. Mask Set Layers

3.1. Legends

3.1.1. Cadence Layout

Layer name and Purpose are the cadence layout tools designation.
Layer description is the intended use of the cadence polygons or text.
Cadence purposes are dg=DRAWING layer, pn=PIN layer, ll=LABEL for text, nt=NET for circuit LVS, rr=RESISTOR for resistor marking, by=BOUNDRY definitions, st=SLOT for slotted vias, fl=FILL for dummy fill and bk=BLOCK for dummy fill.
Type is D=DRAWN layer, G = GENERATED layer, M = MARKING layer.
The dfll layer is the cadence internal layer.

3.1.2. Stream in/out

The gdsii layer is the stream layer from cadence stream out to GDS.
Datatype is the datatype of the streamed out layer that the cadence purposes are to be placed for the cadence layer name. Cadence Purposes map dg to datatype=0 or as designated (e.g. datatype 63), pn to datatype=2, ll to datatype=3, nt to datatype=4, rr to datatype=5, by to datatype=7, st to datatype=20, fl to datatype=31, bk to datatype=30.

3.1.3. Mask layers

Mask name and layer number along with the mask tone (positive or negative), the mask abbreviation and the layer on the wafer to which it aligns.

3.1.4. Cadence, Stream and Mask table

JAZZ Semiconductor C13 Layer Chart (CDS version)

SBC13 — ca18 reserved layers
SBL13
shared sbl/c

Layer Name	Type	dfII Layer #	gdsII Layer #	Layer Description	Purpose: Datatypes	drawing 0	no cfactor 1	pin 2	label 3	net 4	resistor 5	keep out 6	bndry 7	slot 20	block 30	fill 31
cbnd		0	0	Cell Boundary		X										
nwell	D	1	1	Nwell		X	X									
act	D	2	2	Active		X	X									
field	G	3	3	Field Implant		X	X									
nbur	D	4	4	RESERVED		X	X									
poly1	D	5	5	First Poly		X	X	X	X	X	X	X				
cni	D	6	6	N+ Implant		X	X									
cont	D	7	7	Contact		X	X									
metal1	D	8	8	Metal 1		X	X	X	X	X	X	X	X	X	X	X
silox	D	9	9	Silox		X	X									
csink	D	10	10	Collector sinker inplant		X	X									
cpi	D	11	11	P+ Implant		X	X									
dgate	D	12	12	Dual Gate		X	X									
varac	D	13	13	Varactor		X	X									
dn	G	14	14	DN Implant		X	X									
revact	G	15	15	Reverse Active		X	X									
via1	D	17	17	Via1		X	X							X		
metal2	D	18	18	Metal 2		X	X	X	X	X	X	X	X	X	X	X
		19	19													
hvnldd	D	20	20	High Voltage nldd		X	X									
spacec	D	21	21	spacer clear		X	X									
topmm	D	22	22	MIM Top Cap		X	X									
bpoly	D	23	23	Base poly		X	X									
hvpldd	D	24	24	High Voltage pldd		X	X									
via2	D	27	27	Via2		X	X							X		
metal3	D	28	28	Metal 3		X	X	X	X	X	X	X	X	X	X	X
epoly	D	29	29			X	X									
topmm2	D	30	30	Stacked MIM top Cap		X	X									
emtr	D	31	31	Emitter		X	X									
		32	32													
ewin	D	33	33			X	X									
hsimp	D	34	34			X	X									
		35	35													
dnwell	D	36	36	Deep Nwell		X	X									
via3	D	37	37	Via3		X	X							X		
metal4	D	38	38	Metal 4		X	X	X	X	X	X	X	X	X	X	X
hvnpn	D	39	39	High voltage NPN		X	X									
sblk	D	40	40	Salicide Block		X	X									
dtrench	D	41	41			X	X									
hvndrift	D	42	42	High Voltage ndrift		X	X									
lcoll	D	44	44			X	X									
nmosvimp	G	46	46			X	X									
via4	D	47	47	Via4		X	X							X		
metal5	D	48	48	Metal 5		X	X	X	X	X	X	X	X	X	X	X
		49	49													
pmosvimp	G	53	53			X	X									
hvres	D	54	54			X	X									
psm		55	55			X	X									
via5	D	57	57	Via5		X	X							X		
metal6	D	58	58	Metal 6		X	X	X	X	X	X	X	X	X	X	X
pkmsk	G	59	59	P Pocket (PK) Implant		X	X									
hp	G	60	60			X	X									
nkmsk	G	61	61	N Pocket (NK) Implant		X	X									
outline	M	63	not streamed	Cell Outline	63											
nwell2	D	68	68	Nwell2		X										
captype	D	70	70			X										
jazzPad	M	74	74	Jazz provided pads		X										
resdev	M	80	80	Nwell res mark layer		X										
pwe	M	94	94	Pwell Exclude		X										
bumpPad	M	96	96	Bump type pads		X										
reserved		110	110			X										
prBoundary	D	235	63			X										

Cadence, Stream and Mask table (Continued)

JAZZ Semiconductor C13 Layer Chart (CDS version)

SBC13 — ca18 reserved layers
SBL13
shared sbl/c

Layer Name	Type	dfII Layer #	gdsII Layer #	Layer Description	Purpose: Datatype	HV marking layer 40-49	misc marking layer 50-59	misc marking layer 60-69	misc marking layer 70-79
hvnmrk	M	115	115	hvnmrk	0				
hvpmrk	M	116	116	hvpmrk	0				
dataprep		117	117		1 & 2				
artifact	M	118	118	Artifact mark layer		40			
bipolar	M	119	118			41			
L_cell	M	120	118	Inductor mark layer		42			
analog	M	121	118	Analog block layer		43			
diodev	M	122	118	Protect diodes		44			
	M	123	118			45			
reserved	M	124	118			46			
reserved	M	125	118			47			
reserved	M	126	118			48			
hvfet2	M	127	118			49			
varacm	M	128	118				50		
excl	M	129	118				51		
fusemrk	M	130	118	Metal fuse mark layer			52		
ablb	M	131	118	Analog block layer			53		
dblb	M	132	118				54		
HiVTmrk	M	133	118	High Threshold mark layer					83
reserved		134					55		
reserved		135					56		
reserved		136					57		
SRmarkR	M	138	118	Sealring Marking Layer				60	
N_cell	M	139	118					61	
P_cell	M	140	118					62	
natvmrk	M	141	118	Native Marking layer				69	
	M	142	118					64	
schotky	M	143	118					65	
	M	144	118					66	
restmrk	M	145	118	res strip mark layer				67	
fetRFmrk	M	146	118	Marker for RF fets				68	
cram	M	148	118	RAM mark layer					70
crom	M	149	118	ROM mark layer					71
	M	150	118						72
	M	151	118						73
	M	152	118						74
reserved									81
reserved									82

3.2. Mask Process Order

(In order of first use)

Mask Layer	Layer Name	Mask Symbol	Drawn or Generated	Field
36	Deep Nwell	DNW	D	Neg
2	Active	A	D	Pos
15	Reverse active (STI)	RA	G	Neg
3	Field Implant	F	G	Pos
1	Well Implant	W	D	Neg
84	High Vt-N	HVTN	G	Neg
85	High Vt-P	HVTP	G	Neg
12	DG (Dual Gate Oxide)	DG	D	Pos
5	First Poly gate	FP	D	Pos
14	DN Implant	DN	G	Neg
60	HP Implant	HP	G	Neg
61	NK Implant	NK	G	Neg
59	PK Implant	PK	G	Neg
6	N+ Implant	NI	D	Neg
11	P+ Implant	PI	D	Neg
54	High Value Resistor Implant	HR	D	Neg
40	Salicide Block	SB	D	Pos
7	Contact	C	D	Neg
8	First Metal (Metal 1)	M1	D	Pos
17	First Via (Via1)	VA	D	Neg
18	Second Metal (Metal 2)	M2	D	Pos
27	Second Via (Via2)	V2	D	Neg
28	Third Metal (Metal 3)	M3	D	Pos
37	Third Via (Via3)	V3	D	Neg
22	Top MIM Capacitor Plate	TM	D	Pos
38	Fourth Metal (Metal 4)	M4	D	Pos
47	Fourth Via (Via4)	V4	D	Neg
30	Stacked Top MIM cap. Plate	TM2	D	Pos
48	Fifth Metal (Metal 5)	M5	D	Pos
57	Fifth Via (Via5)	V5	D	Neg
58	Sixth Metal (Metal 6)	M6	D	Pos
9	Pad (“Silox”)	S	D	Neg

3.3. Description of Mask Layers:

- **Deep N-well (DNW) – Layer 36**
  This mask defines regions to be implanted with additional deep triple well n-type implant for NFET isolation.

- **Active (A) – Layer 2**
  This mask defines all active areas.

- **Reverse Active (RA) – Layer 15**
  This mask defines all reverse active areas. This layer is generated from active per section 3.5.

- **N-well (W) – Layer 1**
  This mask defines all CMOS regions to receive N-well, PMOS Vt, and PMOS punchthrough implants.

- **Field (F) – Layer 3**
  This mask defines all regions to receive NMOS Vt, NMOS punchthrough, and boron field implants. This layer is generated where HiVT marking layer is drawn (118/83).

- **High Vt-N Implant (HVTN) – Layer 84**
  This mask defines all 1.2V NMOS regions to receive optional high Vt implants. This layer is generated where HiVT marking layer is drawn (118/83).

- **High Vt-P Implant (HVTP) – Layer 85**
  This mask defines all 1.2V PMOS regions to receive optional high Vt implants. It is a generated layer per section 3.4.

- **Dual Gate (DG) – Layer 12**
  This mask defines the areas that are to have thick gate oxides for dual gate oxide process. Drawn DG layers get thick oxide. This layer is generated per section 3.5.

- **First Poly (FP) – Layer 5**
  This mask defines the gate of CMOS transistors. This mask also defines silicided and unsilicided poly resistors.

- **DN Implant (DN) – Layer 14**
  This mask defines regions to receive the thick gate oxide NMOS LDD implant only. It is generated per section 3.5.

- **HP Implant (HP) – Layer 60**
  This mask defines regions to receive the thick gate oxide PMOS LDD implant only. It is generated per section 3.5.

- **NK Implant (NK) – Layer 61**
  This mask defines regions to receive the thin gate oxide NMOS LDD implants and pocket implants. It is generated per section 3.5.

- **PK Implant (PK) – Layer 59**
  This mask defines regions to receive the shared thin gate oxide and thick gate oxide PMOS LDD implants. It is generated per section 3.5.

- **N+ Implant (NI) – Layer 6**
  This mask defines regions to receive the NMOS N+ source/drain implants.

- **P+ Implant (PI) – Layer 11**
  This mask defines regions to receive the PMOS P+ source/drain implants. It is also used to implant the collector of the LPNP, P+ poly resistors, and substrate contacts.

- **High Value Resistor Implant (HR) – Layer 54**
  This mask defines regions to receive the high value resistor implant. This mask in conjunction with SB (layer 40) below is used to form unsalicided high value resistors.

- **Silicide Block (SB) – Layer 40**
  This mask defines regions where silicide formation is blocked. This mask is used to form poly resistors.

- **Contact (C) – Layer 7**
  This mask defines active and poly contacts to metal 1.

- **First Metal (M) – Layer 8**
  This mask defines the first metal layer.

- **Via1 (V1) – Layer 17**
  This mask defines metal 2 to metal 1 contact areas.

- **Second Metal (M2) – Layer 18**
  This mask defines the second metal layer.

- **Via2 (V2) -- Layer 27**
  This mask defines metal 3 to metal 2 contact areas.

- **Third Metal (M3) -- Layer 28**
  This mask defines the third metal layer.

- **Via3–(V3) -- Layer 37**
  This mask defines metal 4 to metal 3 contact areas.

- **Top MIM Capacitor Plate (TM) -- Layer 22**
  This mask defines the top plate of the MIM capacitor.

- **Fourth Metal (M4) -- Layer 38**
  This mask defines the fourth metal layer.

- **Via4 (V4) -- Layer 47**

This mask defines metal 5 to metal 4 contact areas.

- **Stacked Top MIM Capacitor Plate (TM2) – Layer 30**
  This mask defines the top plate of the upper MIM capacitor of the stacked MIM capacitor.

- **Fifth Metal (M5) -- Layer 48**
  This mask defines the fifth metal layer.

- **Via5 (V5) -- Layer 57**
  This mask defines metal 6 to metal 5 contact areas.

- **Sixth Metal (M6) -- Layer 58**
  This mask defines the sixth metal layer.

- **Silox (S) -- Layer 9**
  This mask defines openings in the passivation layer over contact pads.

3.4.

Layer Generation Algorithms:

Note: This section is presented for reference only.

This section, along with sections 3.5.1 and 3.5.2, is reserved for documenting the MaskCAD operations used to generate specific process layers as well as generating dummy active and dummy metal fills. These MaskCAD operations are done after data tape-in at the foundry during data post processing and prior to data tape-out to the mask shop.

Please note that layer 118d40 (CART) is artifact marking layer.

```
chip = EXTENT
resa = lay5 AND lay40        // finds poly resistors only
resb = SIZE resa BY 0.50     // poly resistor exclusion for generated implants
```

Active layer generation

```
//  Finds SRAM data and performs edge extensions on small geometries
a1 = lay2 AND lay118d70
b = int a1 < 0.01 abut ==90 intersecting only region
c = int a1 < 0.6 opposite region
d = size c by 0.02
e = enc a1 d < 0.03 opposite region
f = e interact b == 2          // f = special SRAM sizing
final_active = f OR lay2
```


Reverse Active layer Generation

It is required that the reverse active layer be generated from the active mask data with the following algorithm:

1) Input file is mask active data. Mask active data = (original circuit active data and dummy active data). These elements may be processed separately, but reverse active must be created for both the circuit active data and dummy active filler pattern. (data file 1)

2) Size data file 1 down by 0.26um per edge to eliminated features of size 0.52um or smaller. Then size up the new result by 0.12 um per edge, output the result on layer 15.The final result is active 0.14um per side overplot of reverse active.

3) Scribe fill reverse active layer is drawn with an underplot of 0.24um per side of scribe fill active. Both layer 2 and layer 15 scribe fill data must be drawn on data type 1.

4) Data for frame structures have special needs that differ from circuit data. Most frame structures contain data on layer 2 data type 1 and/or layer 2 data type 0. A distinction is made between data types and the overplot of active to reverse active is different depending on the data type of the layer 2 polygon. Reverse active must be generated with the following algorithm for frame structure data:

4A) Input file is the structure data with dummy active data (if needed) already added to the structure.

4B) Size down layer 2 datatype 0 by 0.36um per edge. Then size up the new result by 0.20 um per edge. This matches exactly the generation for circuit data.
4C) Size down layer 2 datatype 1 by 0.37 um per edge. Then size up the new result by 0.21um per edge. This generates an active overplot of 0.24 um per edge of reverse active for data type 1 polygons.
4D) Boolean OR together the result of 4B and 4C. Output the result on to layer 15 to produce the final reverse active data.

In the case of the frame structure data, this task should be performed only once with the result stored in the maskcad reference drop-in library for repeated use.

Field layer generation algorithm

```
l3 { drn3 =  lay3  AND lay118d40
     pwl1  = lay1  NOT lay118d40          // NWell
     pwl2  = pwl1  OR  lay94              // PWE
     pwl3  = pwl2  OR  (SIZE lay68 BY 0.30)  // NWell2
     pwl4  = pwl3  OR  lay118d69          // Native Mark
     pwl5  = SIZE  pwl4 BY 0.42 OVERUNDER
     pwl6  = SIZE  pwl5 BY 0.42 UNDEROVER
           pwl6  OR drn3 }
```

DN layer generation

```
dn14 { drn14 = lay14 AND lay118d40
       dn1   = lay6  AND lay12
       dn2   = dn1   NOT lay1
       dn3   = dn2   NOT lay118d40
       dn4   = dn3   NOT resb
       dn5   = dn4   NOT (lay118d61 OR lay118d62)
    // Preserve drawn DN within NPN but exclude it from EP regions
       dn6   = dn5   OR  ((lay14 AND lay118d61) NOT lay29)
       dn7   = SIZE  dn6 BY 0.17 UNDEROVER
       dn8   = SIZE  dn7 BY 0.17 OVERUNDER
             dn8 OR drn14 }
```

HP layer generation

```
l60 { drn60 = lay60 AND lay118d40
      hp1  = lay11 AND lay12
      hp2  = hp1   AND lay1
      hp3  = hp2   NOT lay118d40
      hp4  = hp3   NOT resb
      hp5  = hp4   NOT (lay118d61 OR lay118d62)
      hp6  = SIZE  hp5 BY 0.17 UNDEROVER
      hp7  = SIZE  hp6 BY 0.17 OVERUNDER
           hp7   OR drn60 }
```

PK layer generation

```
l59 { drn59 = lay59 AND lay118d40
      pk1  = lay11 AND lay1
```

```
pk2  = pk1   NOT resb
pk3  = pk2   NOT lay118d40
pk4  = pk3   NOT lay12
pk5  = pk4   NOT lay68
pk6  = pk5   NOT (lay118d61 OR lay118d62)
pk7  = SIZE  pk6 BY 0.145 UNDEROVER
pk8  = SIZE  pk7 BY 0.145 OVERUNDER
       pk8   OR drn59 }
```

NK layer generation

```
l61 { drn61 = lay61 AND lay118d40
      nk1  = lay6 NOT lay1
      nk2  = nk1  NOT lay12
      nk3  = nk2  NOT resb
      nk4  = nk3  NOT lay118d40
      nk5  = nk4  NOT lay68
      nk6  = nk5  NOT (lay118d61 OR lay118d62)
      nk7  = SIZE nk6 BY 0.145 UNDEROVER
      nk8  = SIZE nk7 BY 0.145 OVERUNDER
             nk8  OR drn61 }
```

SB layer generation (CA13HC only)

In addition to drawn data, additional SB is generated over dummy active (see Section 3.4.3) by sizing up dummy active by 0.5um

3.4.1. Dummy Metal Layer Generation

Dummy Metal 1 layer generation

Additional floating metal 1 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 8.D. The following method of generation of dummy metal conforms to the process design rule.

1. Generate Jazz metal dummy fill pattern, consisting of 5umX5um squares at a 7 um pitch (2um space). Filler patterns should be skewed from true horizontal and vertical by 1um offset between squares. (data file 0).
2. Merge metal drawing (datatype 0) and customer provided metal fill (datatype 31) to obtain datafile 1.
3. Upsize the merged pattern datafile 1 by 17.5um to obtain data file 2. Note: The 17.5um exclusion may be changed to as low as 10um if the metal density requirements are not met using the default dummy metal fill algorithm.
4. Add customer drawn dummy fill block (datatype 30) to data file 2 above to obtain datafile 3.
5. Subtract datafile 3 from datafile 0 to obtain final metal dummy fill pattern as datafile 4.
6. Add data file 4 to datafile 1 above to make metal 1 mask.

Dummy Metal 2 layer generation

Additional floating metal 2 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 18.D. The following method of generation of dummy metal conforms to the process design rule.

1. Generate Jazz metal dummy fill pattern, consisting of 5umX5um squares at a 7 um pitch (2um space). Filler patterns should be skewed from true horizontal and vertical by 1um offset between squares. (data file 0).
2. Merge metal drawing (datatype 0) and customer provided metal fill (datatype 31) to obtain datafile 1.
3. Upsize the merged pattern datafile 1 by 17.5um to obtain data file 2. Note: The 17.5um exclusion may be changed to as low as 10um if the metal density requirements are not met using the default dummy metal fill algorithm.
4. Add customer drawn dummy fill block (datatype 30) to data file 2 above to obtain datafile 3.
5. Subtract datafile 3 from datafile 0 to obtain final metal dummy fill pattern as datafile 4.
6. Add data file 4 to datafile 1 above to make metal 2 mask.

Dummy Metal 3 layer generation

Additional floating metal 3 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 28.D. The following method of generation of dummy metal conforms to the process design rule.

1. Generate Jazz metal dummy fill pattern, consisting of 5umX5um squares at a 7 um pitch (2um space). Filler patterns should be skewed from true horizontal and vertical by 1um offset between squares. (data file 0).
2. Merge metal drawing (datatype 0) and customer provided metal fill (datatype 31) to obtain datafile 1.
3. Upsize the merged pattern datafile 1 by 17.5um to obtain data file 2. Note: The 17.5um exclusion may be changed to as low as 10um if the metal density requirements are not met using the default dummy metal fill algorithm.
4. Add customer drawn dummy fill block (datatype 30) to data file 2 above to obtain datafile 3.
5. Subtract datafile 3 from datafile 0 to obtain final metal dummy fill pattern as datafile 4.
6. Add data file 4 to datafile 1 above to make metal 3 mask.

Dummy Metal 4 layer generation

Additional floating metal 4 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 38.D. The following method of generation of dummy metal conforms to the process design rule.

1. Generate Jazz metal dummy fill pattern, consisting of 5umX5um squares at a 7 um pitch (2um space). Filler patterns should be skewed from true horizontal and vertical by 1um offset between squares. (data file 0).
2. Merge metal drawing (datatype 0) and customer provided metal fill (datatype 31) to obtain datafile 1.
3. Upsize the merged pattern datafile 1 by 17.5um to obtain data file 2. Note: The 17.5um exclusion may be changed to as low as 10um if the metal density requirements are not met using the default dummy metal fill algorithm.
4. Add customer drawn dummy fill block (datatype 30) to data file 2 above to obtain datafile 3.
5. Subtract datafile 3 from datafile 0 to obtain final metal dummy fill pattern as datafile 4.
6. Add data file 4 to datafile 1 above to make metal 4 mask.

Dummy Metal 5 layer generation

Additional floating metal 5 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 48.D. The following method of generation of dummy metal conforms to the process design rule.

1. Generate Jazz metal dummy fill pattern, consisting of 5umX5um squares at a 7 um pitch (2um space). Filler patterns should be skewed from true horizontal and vertical by 1um offset between squares. (data file 0).
2. Merge metal drawing (datatype 0) and customer provided metal fill (datatype 31) to obtain datafile 1.
3. Upsize the merged pattern datafile 1 by 17.5um to obtain data file 2. Note: The 17.5um exclusion may be changed to as low as 10um if the metal density requirements are not met using the default dummy metal fill algorithm.
4. Add customer drawn dummy fill block (datatype 30) to data file 2 above to obtain datafile 3.
5. Subtract datafile 3 from datafile 0 to obtain final metal dummy fill pattern as datafile 4.
6. Add data file 4 to datafile 1 above to make metal 5 mask.

Dummy Metal 6 layer generation

Additional floating metal 6 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 58.D. The following method of generation of dummy metal conforms to the process design rule.

7. Generate Jazz metal dummy fill pattern, consisting of 9umX9um squares at a 13 um pitch (4um space). Filler patterns should be skewed from true horizontal and vertical by 1um offset between squares. (data file 0).
8. Merge metal drawing (datatype 0) and customer provided metal fill (datatype 31) to obtain datafile 1.
9. Upsize the merged pattern datafile 1 by 25um to obtain data file 2. Note: The 25um exclusion may be changed to as low as 10um if the metal density requirements are not met using the default dummy metal fill algorithm.
10. Add customer drawn dummy fill block (datatype 30) to data file 2 above to obtain datafile 3.
11. Subtract datafile 3 from datafile 0 to obtain final metal dummy fill pattern as datafile 4.
12. Add data file 4 to datafile 1 above to make metal 6 mask.

3.4.2. Dummy Metal, Poly, Active Fill Exclusions

To prevent metal fill from causing mismatch on FETs, capacitors, and resistors, and to eliminate additional parasitic capacitance on RF components, the following procedures will be followed.

1) All "white areas" of chip within ABLB (i.e. no features drawn in Nwell, active, poly, TM, TM2 or metal) will receive metal fills on all required metal layers as specified in Section 3.5.1.

2) Analog and RF blocks will be identified by drawing a marking border (ABLB Layer 118 (datatype 53)) 1um outside the analog/RF circuit regions. Normal metal fill rules as specified in Section 3.5.1 will be used to generate metal fill outside this border. All areas within ABLB layer must obey special RF metal overplot rules (See Section 5.10)

3) For inductor areas of the circuit, an Inductor Marking Layer (IML layer 118/42) will be drawn. All mask areas containing layer 51 will not have any metal fill generated on any metal layer. This procedure will prevent fill from being placed in white space in the open region inside an inductor.

4) Dummy metal fill can be excluded in each individual metal layer by adding the dummy fill block marking layer, which is the metal layer number, datatype 30 (e.g., 8/30, 18/30, 28/30, 38/30, 48/30, and 58/30). However, metal density rules specified in the metal layer design rules in Section 4 must be met. Additionally, larger metal overplot rules of vias and larger minimum metal area rules, which are also applicable for regions within analog block border (ablb layer 118 (datatype 53)) regions and described in Section 5.11, are triggered for ALL metal layers within dummy fill block marking layer for any metal.

5) Customer provided dummy metal fill can be added in each metal layer. All customer provided dummy metal fill must be drawn on regular metal (datatype 0), and enclosed and coincident with dummy metal fill marking layer which is the metal layer number, but datatype 31 (e.g., 8/31, 18/31, 28/31, 38/31, 48/31, and 58/31). The customer provided dummy metal fill must not interact with the drawing metal (datatype 0), and must not interact with any contacts/vias.

6) There is no provision to allow customers to define exclusion regions for dummy active fill. Guidelines for dummy active generation are described in Section 3.5.3 and 3.5.4. Note that these guidelines are applicable for dummy active fill below inductors, MIM capacitors, and pads.

7) Dummy poly fill can be excluded in certain regions by adding the dummy poly block marking layer, which is the poly layer number 5, datatype 30. However, poly density rules specified in the poly layer design rules in Section 4 must be met.

8) Customer provided dummy poly fill is disallowed as it affects dummy active layer generation. Soft_ERC check will flag any unconnected poly as floating_poly error (see Section 11).

The following rules are checked for dummy metal fill integrity

Rule No.	Rule Name
7.FILL	Layer 7 is not allowed within layer 8, datatype 31
8.FILL	Layer 8, datatype 31 is not coincident with layer 8, datatype 0
17.FILL	Layer 17 is not allowed within layer 8, datatype 31 or layer 18, datatype 31
18.FILL	Layer 18, datatype 31 is not coincident with layer 18, datatype 0
27.FILL	Layer 27 is not allowed within layer 18, datatype 31 or layer 28, datatype 31
28.FILL	Layer 28, datatype 31 is not coincident with layer 28, datatype 0
37.FILL	Layer 37 is not allowed within layer 28, datatype 31 or layer 38, datatype 31
38.FILL	Layer 38, datatype 31 is not coincident with layer 38, datatype 0
47.FILL	Layer 47 is not allowed within layer 38, datatype 31 or layer 48, datatype 31
48.FILL	Layer 48, datatype 31 is not coincident with layer 48, datatype 0
57.FILL	Layer 57 is not allowed within layer 48, datatype 31 or layer 58, datatype 31
58.FILL	Layer 58, datatype 31 is not coincident with layer 58, datatype 0

3.4.3. Dummy Active Generation

When the active features of the circuit design allow large open areas without active features, additional non-functional active features (dummy active) must be added to insure a uniform topography for CMP process.

The rules below are not checked but used while establishing layer generation algorithm

Rules 2.P through 2.Y are required to enable planarization process methods used for shallow trench isolation. A preferred generation method is described at the end of this section as a simple and effective way to meet the requirements of rules 2.P through 2.Y.

Rules 2.P through 2.Y are not checked since the dummy active pattern is algorithmically generated. It is assumed correct by generation.

Rule No.	Rule Name	
2.P	Maximum active to active space without dummy fill (um)	10
2.U	Minimum dummy active separation from active (um) -- distance that floating dummy active feature must be from circuit active feature	2.5
2.V	Minimum dummy active separation from N-well edge (including N-well resistors) (See Note 2) (um)	2.0
2.W	Minimum dummy active separation from poly (um)	2.0
2.Y	Dummy active is not allowed inside N-well resistors (See Note 2)	

Note 2: Rule 2.V and Rule 2.Y: A “resdev” marking layer (Layer 80) is used to mark all the N-well resistors.

Illustration 3-1: Dummy Active Generation

Dummy active generation algorithm: The following method for generation of dummy active conforms to the process design rules.

1) A staggered array of dummy active squares is created with the data center at chip center. 5um X5um features with 3.0um separations. (data file 1) (See Illustration 3-1: Dummy Active Generation)

2) The circuit active pattern is sized up by 5um (half of Rule 2.P) per edge. Merge features and then size active pattern down by 2.5um ((half of Rule 2.P) - Rule 2.U) per edge. (data file 2)

3) Size poly layer up by 2um (Rule 2.W) per edge (data file 3)

4) Size up N-well resistor "resdev" marking layer (layer 80) by 2um (data file 4)

5) Create a path 4.0um wide centered on All N-well boundaries. (data file 5) (Rule 2.V)

6) Add Data files (2+3+4+5 = data file 6)

7) Subtract data file 6 from dummy active array (data file 1) - (data file 6)= (data file 7) to yield dummy active array which has cut outs for the placement of circuit active data.

8) Size up circuit active pattern by 2.5um per edge (data file 8). Subtract data file 8 from data file 7 to yield final dummy active array (data file 9) = (data file 7) - (data file 8).

9) Size down final dummy active array (data file 9) by 0.20um per edge to eliminate slivers and then size up by 0.20um per edge to yield final dummy active array with no slivers. (data file 10)

10) Add data file 10 (no sliver final dummy active array) to the Layer 2 data for the original design. (data file 11)

11) Make active mask for circuit from data file 11. (Merged circuit active data and sized dummy active array)

See table in Section 3.5.4 for other exclusion regions in dummy active fill

The dummy active does not get covered by any generated N+ or P+ implant for CA13HC only.

3.4.4. Dummy Poly Fill Generation

The following method for generation of dummy poly conforms to the process design rules.

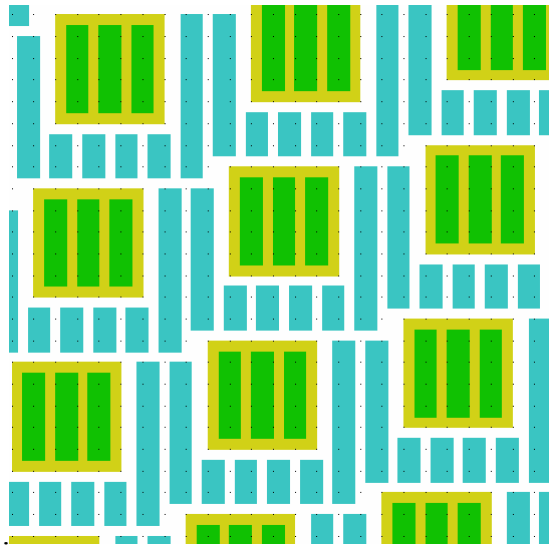
1) Exclusion regions in dummy active and dummy poly fill

	For dummy active	For dummy poly
spacing to Active	2.5	2.5
spacing to Poly	2.0	2.0
spacing to nwell junction	2.0	2.0
spacing to nwell resistor marking (layer 80)	2.0	2.0
spacing to Artifact marking (layer 118/40)	0.3	0.3
spacing to metal 1	N/A	2.0
spacing to TM (MIM capacitor)	N/A	5.0
spacing to fuse marking (layer 118/52)	N/A	10.0
spacing to inductor marking (layer 118/42)	N/A	25.0
spacing to bond pad	N/A	10.0
spacing to dummy poly block marking (layer 5, datatype 30)	N/A	5.0
Spacing to native implant	5.0	5.0
Keep Partials	Yes	Yes
Keep Only Rectangles	No	Yes

2) Dummy Poly fill is not generated within partial dummy actives, i.e., dummy actives which are not 5um x 5um

3) Within the 5um x 5um dummy active, three 4x1 stripes of dummy poly are generated with 0.5um space to active edge and in between poly.

4) Within the field area, dummy poly is generated with feature width of 1um and space of 0.5um to active edge and in between poly. The minimum length of dummy poly is 2um and the maximum length is 7.5um



Dummy active Dummy Poly

Illustration 3-2: Examples of dummy poly fill

4. CMOS and backend Design Rules

4.1. Active "A" (Layer 2)

Mask 2: This defines active areas (P-ch/N-ch FETs), diffused interconnect, and areas to be used for N-well and P-well (substrate) contacts. It is a positive mask and is aligned to the Zero layer. See Illustration 2

Rule No.	Rule Name	CA13HC Thin ox	CA13HC Thick ox (DG)
2.A	Minimum transistor width for thin gate oxide transistors	0.15	
2.A.a	Minimum transistor width for thick gate oxide transistors, (DG mask)		0.40
2.B	Minimum active conductor width	0.15	0.15
2.C	Minimum spacing	0.21	
2.C.a	Minimum spacing for thick gate oxide		0.28
2.D	Minimum spacing from N+ outside the N-well to P+ inside the N-well	0.62	
2.D.a	Minimum spacing from N+ outside the N-well to P+ inside the N-well for thick gate oxide		0.86
2.E	Minimum spacing from P+ diffusion inside the N-well to N-well edge	0.31	
2.E.a	Minimum spacing from P+ diffusion inside the N-well to N-well edge for thick gate oxide		0.43
2.F	Minimum spacing from N+ diffusion outside the N-well to N-well edge.	0.31	
2.F.a	Minimum spacing from N+ diffusion outside the N-well to N-well edge for thick gate oxide		0.43
2.G	Minimum spacing from N+ to P+ in the same type well and at the same potential (butted diffusion).	0.0	0
2.H	Minimum spacing from N+ diffusion inside the N-well to N-well edge (except in the case of N-well resistors, see Rules 2.I, 2.I.a, Note 1)	0.20	0.20
2.I	Minimum N+ diffusion extension into the N-well as N-well tie for N-well resistors (See Note 1)	0.60	0.60
2.I.a	Minimum N+ diffusion overlap area of the N-well as N-well tie for N-well resistors (See Note 1)	0.50 (um^2)	0.50 (um^2)
2.J	Minimum spacing P+ diffusion outside the N-well to N-well edge	0.20	0.20
2.K	Minimum width of a butted thin oxide diffusion region	0.30	0.30
2.L	Minimum active area	0.122 (um^2)	0.122 (um^2)
2.X	Unimplanted active is not allowed. Actives must be implanted with N+ or P+ implant.		

Note 1: Rules 2.H, 2.I, 2.I.a: A marking layer (Layer 80) is used to mark all the N-well resistors.

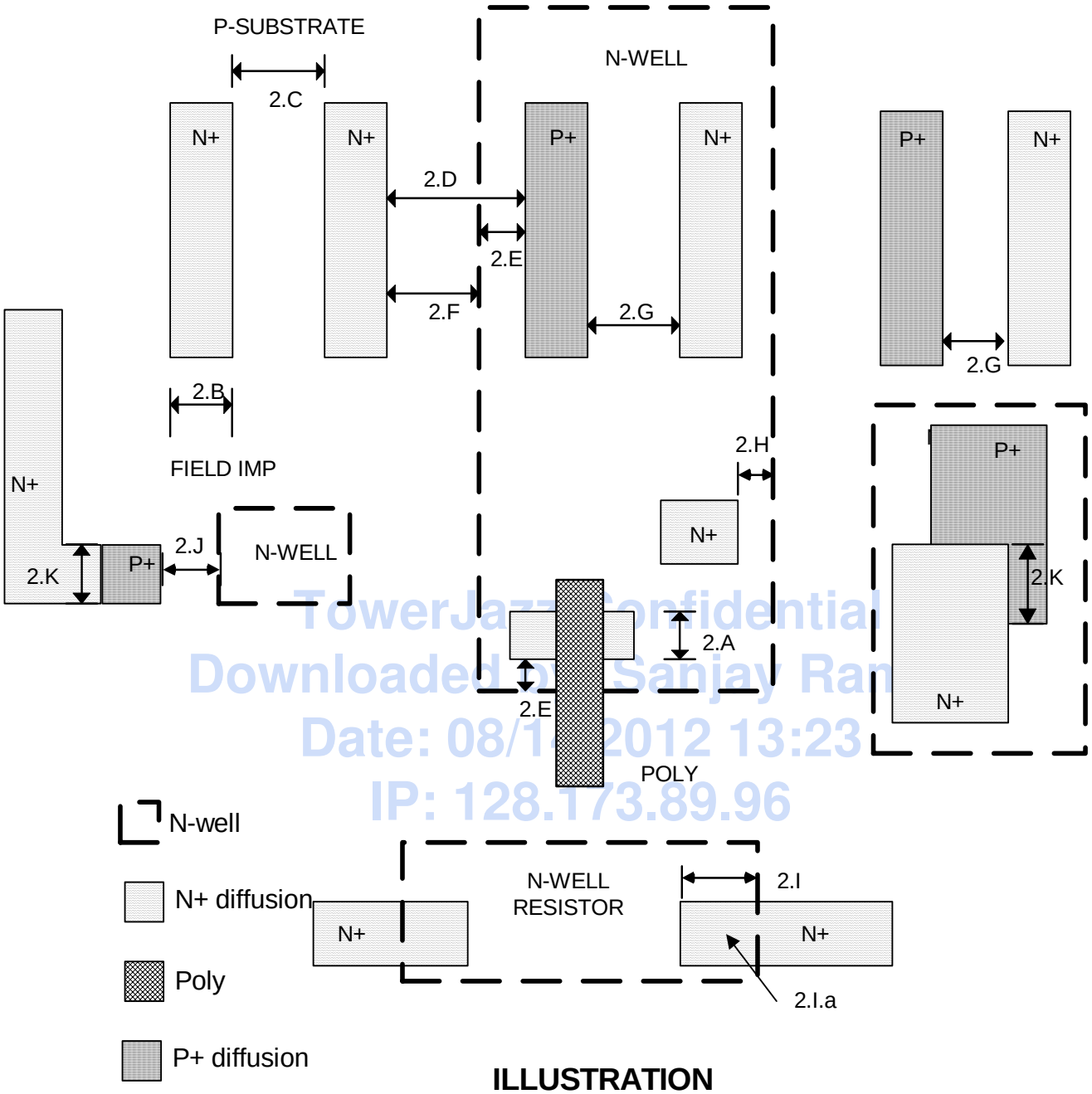


ILLUSTRATION 2

4.2. Reverse Active "RA" (Layer 15)

Mask 15: This mask is the reverse of the active mask. The reverse active mask is a negative mask and is aligned to the Zero layer. See Illustration 15.

Rule No.	Rule Name	CA13HC
15.A	Reverse active feature required over all active which are larger than this minimum size	0.52X0.52
15.B	Minimum reverse active size	0.24
15.C	Active extension beyond reverse active feature (applied only when reverse active feature is present)	0.14
15.BAD	No drawn data for layer is allowed except for artifact	

Note 1: Reverse active rules are not checked since the mask is algorithmically generated. It is assumed correct by generation.

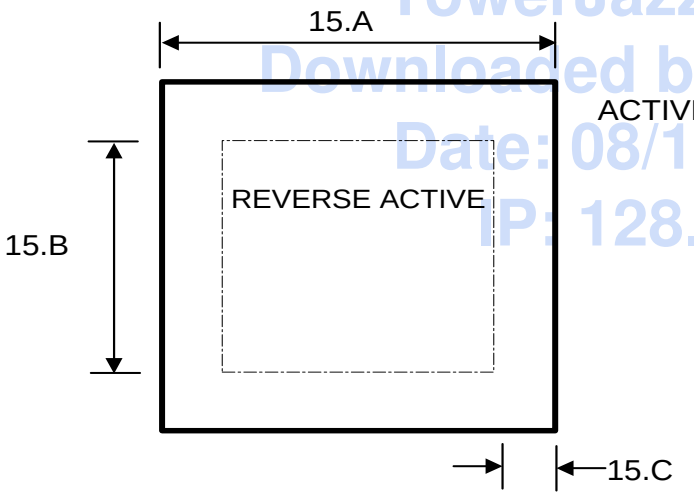


ILLUSTRATION 15

4.3.

Drawn N-well Implant "W" (Layer 1)

Mask 1: This drawn layer defines the N-well regions in which phosphorus is implanted. All PFETs with thin and thick gate oxide are located in N-well regions. The N-well reticles, NWL and NWH, are negative (dark field) masks and are aligned to the Zero layer. The N-well edges are defined by the photoresist edge after developing. See Illustration 1.

Rule No.	Rule Name	CA13HC Thin ox	CA13HC Thick ox (DG)
1.A	Minimum N-well width	0.62	0.62
1.A.a	Minimum N-well width for N-well used as a resistor	1.80	1.80
1.B	Minimum space between two thin gate ox N-wells at the same potential (if smaller then merge)	0.62	
1.C	Minimum space between two thin gate ox N-wells at different potentials, or a notch in the same potential region	1.00	
1.D	Minimum space between a thin gate ox N-well and a thick gate ox N-well or between two thick gate ox N-wells		1.2
1.E	Minimum N-well area	1.0 (um^2)	1.0 (um^2)

Note 1: A marking layer (Layer 80) is used to mark all the N-well resistors to be excluded from dummy active generation (see Section 3.1).

Note 2: Active design rules require additional drawn active to be added near large N-well resistor areas. See Section 3.1 for details.

4.4. Field Implant "F" (Layer 3)

Mask 3: The field implant layer is a derived layer (see section 3.4). This mask is a positive mask and is aligned to the zero layer. The field implant edge is defined by the photoresist edge after developing.

Rule No.	Rule Name	
3.A	Minimum Field Implant width	0.62
3.B	Minimum spacing Field Implant to Field	0.62
3.BAD	No drawn data is allowed for layer 3	

4.5.

HVt Implant Marking Layer 118/83

HVt implant marking layer is used to differentiate "high" Vt (threshold voltage) transistors from standard transistors.

Rule No.	Rule Name	
118.HVT. A	Minimum HVt marking layer width	0.62
118.HVT.B	Minimum Hvt marking layer space	0.62
118.HVT.A1	Minimum HVt marking layer opening (min. resist area opening)	1.00
118.HVT.A2	Minimum HVt marking layer area (min resist area)	1.00
118.HVT.C	Minimum HVt overplot of gate active	0.12
118.HVT.D	Minimum spacing HVt marking layer to gate active	0.12
118.HVT.BADDG	No DG layer allowed inside HVt marking layer	
118.HVT.BADPWE	No HVt marking layer inside pwe	
118.HVT.BADCMOS	HVt marking layer only allowed over active CMOS devices, diodes and ties (and not allowed over all other devices such as PNPs, varactors, n-well resistors, polycaps… etc.). HVt marking layer can not interact with native fet marking layer and pwe marking layer.	

4.6.

High Vt-P Implant "HVTP" (Layer 1: Datatype 82)

Mask HVP: The high Vt-P implant layer is a generated layer (see section 3.4). This mask is a negative mask. The HVP implant edge is defined by the photo-resist edge after developing.

Rule No.	Rule Name	
1.HVTP.A	Minimum HVP Implant width	0.62
1.HVTP.B	Minimum spacing HVP Implant to HVP	0.62
1.HVTP.A1	Minimum HVP layer opening (min. resist area opening)	1.00
1.HVTP.B1	Minimum HVP layer area (min resist area)	1.00
1.HVTP.BAD	No drawn data is allowed for layer HVP	

4.7. High Vt-N Implant "HVTN" (Layer 1: Datatype 81)

Mask HVN: The high Vt-N implant layer is a generated layer (see section 3.4). This mask is a negative mask. The HVN implant edge is defined by the photo-resist edge after developing.

Rule No.	Rule Name	
1.HVTN.A	Minimum HVN Implant width	0.62
1.HVTN.B	Minimum spacing HVN Implant to HVN	0.62
1.HVTN.A1	Minimum HVN layer opening (min. resist area opening)	1.00
1.HVTN.B1	Minimum HVN layer area (min resist area)	1.00
1.HVTN.BAD	No drawn data is allowed for layer HVN	

4.8.

DG: Dual Gate Oxide "DG" (Layer 12)

Mask 12: This mask defines the areas that are to have thick gate oxides for dual gate oxide process. This mask is a positive mask and is aligned to the zero layer. DG layer defines the well type as low voltage or high voltage type. See Illustration 12.

Rule No.	Rule Name	CA13HC
12.A	Minimum Dual Gate mask overplot of thick oxide active	0.27
12.A.a	Minimum Dual Gate mask width	0.70
12.B	Minimum space Dual Gate mask to Dual Gate mask, merge if space less than 0.86 um	0.86
12.C	Minimum space from Dual gate mask to active for thin oxide active	0.27

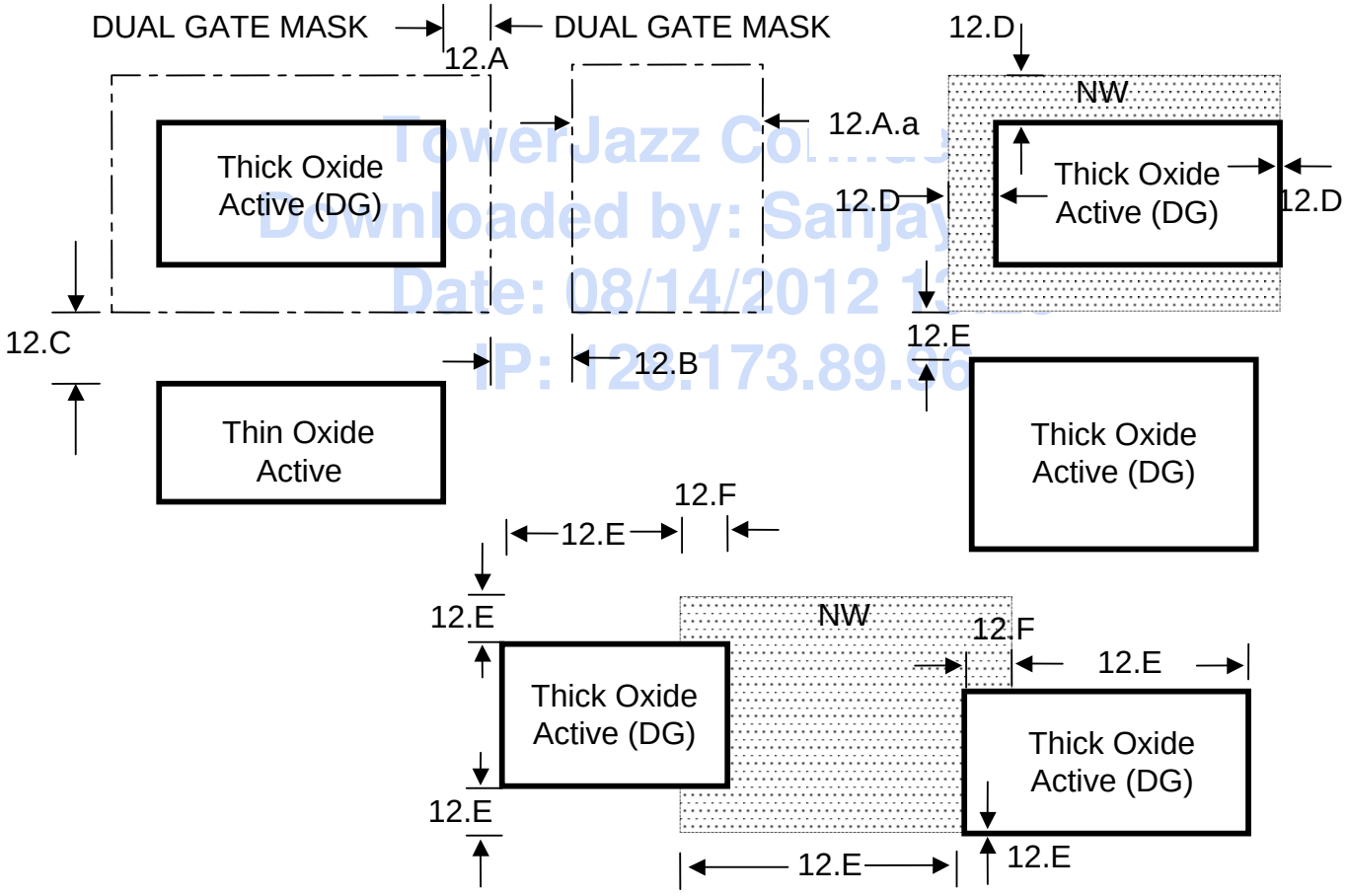


ILLUSTRATION 12

4.9. First Polysilicon Gate "FP" (Layer 5)

Mask 5: This mask defines the areas that are to become gates, capacitors, and poly interconnects. This mask is a positive mask and is aligned to the zero layer. See Illustration 5.

Rule No.	Rule Name	CA13HC	CA13HC
		Thin ox	Thick ox (DG)
5.A	Minimum gate length for thin gate oxide transistors	0.12	n/a
5.A.1	Minimum gate length for thick gate oxide Nfet transistors	N/a	0.36
5.A.2	Minimum gate length for thick gate oxide Pfet transistors	N/a	0.30
5.B	Minimum width of conductors	0.12	0.15
5.C	Minimum poly overlap of gate on field for thin gate oxide transistors	0.18	
5.C.b	Minimum poly overlap of gate on field for thick gate oxide transistors		0.30
5.D	Minimum poly to poly space on field	0.19	0.19
5.D.b	Minimum poly to poly space on active	0.19	
5.D.b.1	Minimum poly to poly space on active		0.25
5.E	Minimum spacing of poly on diffusion to field edge	0.23	0.23
5.F	Minimum spacing of poly on field to adjacent diffusion	0.06	0.06
5.G	Bent gates are not allowed on active		
5.G.a	Minimum poly width for 45 degree bent poly line on field region if bent line length >= 0.39 um	0.16	n/a
5.H	Minimum spacing between active covered by DG and poly edge of thin oxide transistor	0.34	
5.H.a	Minimum DG mask overplot of thick oxide transistor gate poly		0.34
5.J	Minimum spacing from poly edge to the edge of a butted diffusion that is parallel to the thin oxide transistor channel	0.40	
5.K	Minimum density of poly layer pattern	14%	n/a
5.L	Intrinsic (Un-Implanted) poly lines are not allowed. Poly lines must be implanted with N+ or P+ implants.		
5.M	Poly line ends must be rectangular. Other shapes are forbidden		
5.N.1	Minimum area of a poly island (um^2)	0.09	0.09
5.N.2	Minimum area of enclosed by poly (um^2)	0.25	0.25

Note 1: The maximum allowable active run without contact is 17um.
Note 2: Active design rules require additional drawn active to be added near large poly areas. See Section 3.1 for details.

** ROM considerations: Word lines can be 0.12 um wide, however it is preferred that they are strapped with metal to shunt the higher polysilicide sheet resistance due to narrower lines. The antenna rules of section AN of this document apply to ROM word lines even if only one bit is programmed with an active diffusion.

4.9.1. Additional rules for salicided poly resistors (Coming soon – this device is currently not offered in CA13HC).

Following 5.SR.* rules apply to low sheet resistance salicided resistors. Low sheet resistance silicided poly resistors are fabricated by implanting the entire poly resistor including contact regions with P+ implant and completing the standard silicidation process. This resistor requires no additional masks or process steps.

Silicided resistors should be drawn without dogbone ends, that is, the minimum width is determined by minimum poly that contains at least one contact (see SR.D). For wider resistors, the maximum number of contacts in a direction perpendicular to the length should be used to reduce end resistance. See illustration SR for implementation of these rules.

Rule No.	Rule Name	
5.SR.A	Minimum P+ Overplot of Silicided Resistor	0.20
5.SR.B	Minimum Space N+ Implant to Silicided Resistor	0.20
5.SR.C	Minimum Space Active to Silicided Resistor	0.20
5.SR.D	Minimum width Silicided Resistor	0.30
5.SR.F	Minimum Analog block border (layer 118/43) overplot of silicided resistor (not shown)	1.00
5.SR.G	Minimum Nwell overplot of silicided resistor (not shown)	0.50
5.SR.H	Minimum Nwell spacing of silicided resistor (not shown)	0.50

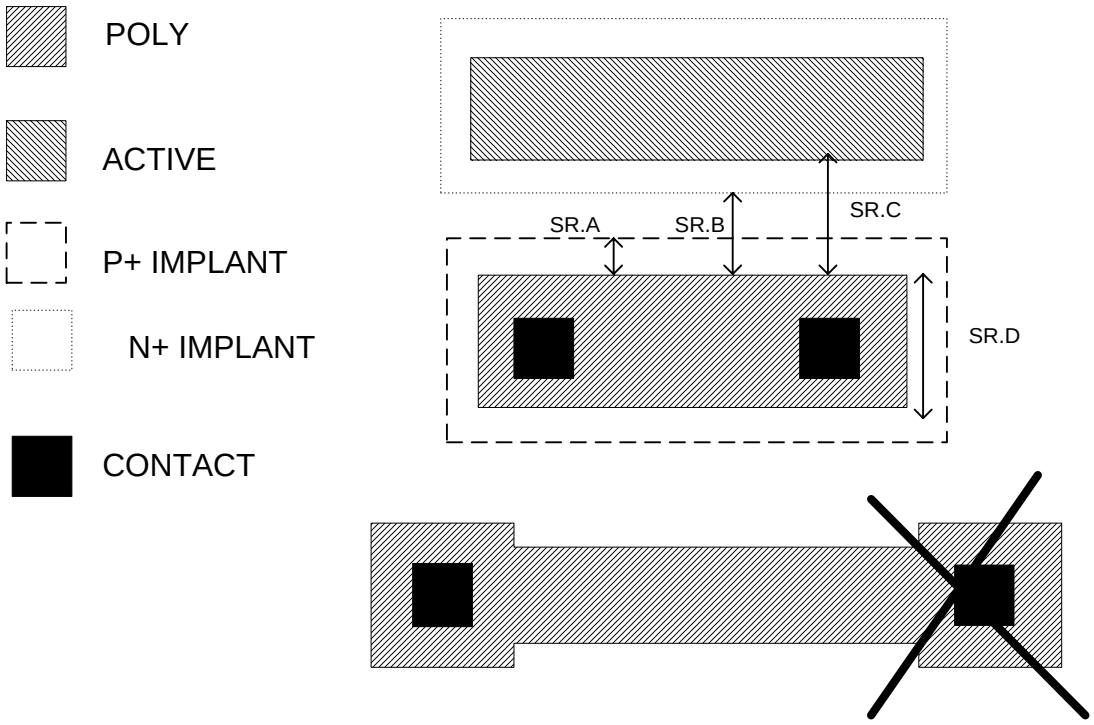


ILLUSTRATION SR

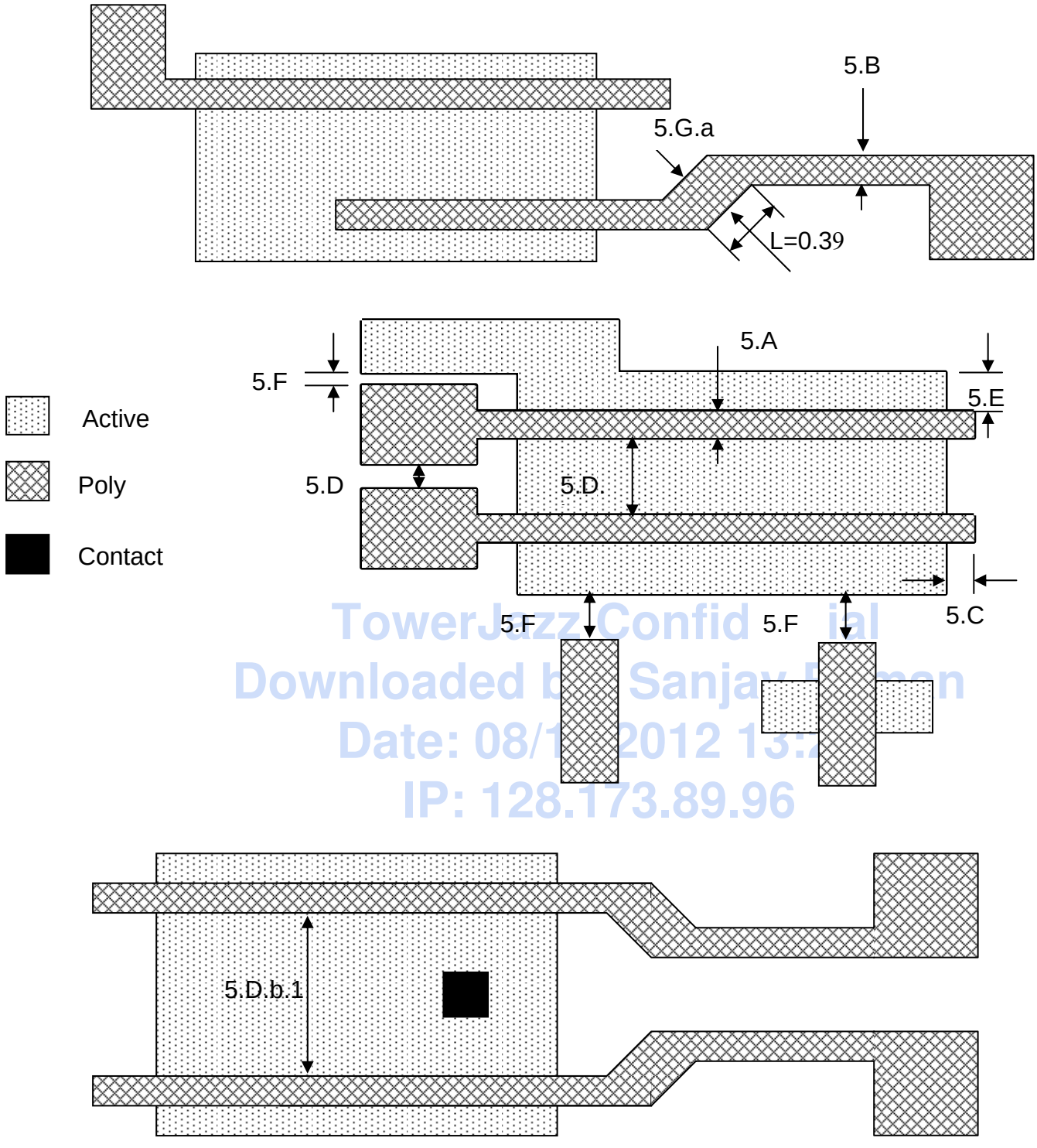


ILLUSTRATION 5

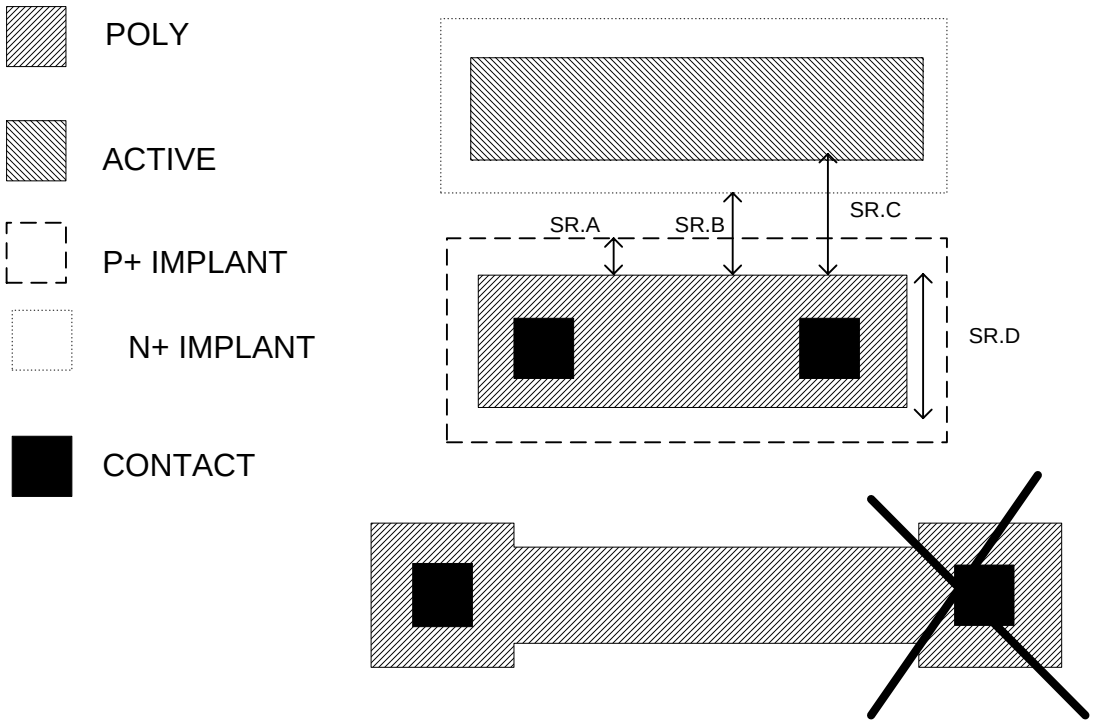


ILLUSTRATION SR

4.10. N+ Implant "NI" (Layer 6)

Mask 6: This mask defines all of the "N+ active" areas and is a negative mask. This mask allows Arsenic to be implanted in all "N+ active" areas (drains, sources, and gates of NFETs, topside N-well ties/guardbars and N+ interconnects). The N+ implant layer is allowed to cross N-well boundaries to meet the following rules. This mask is aligned to the zero layer. See Illustration 6.

Rule No.	Rule Name	CA13HC
6.A.a	Minimum N+ implant (inside N-well) overplot of N-well tie/guardbar (over field)	0.03
6.A.b	Minimum N+ implant (outside N-well) overplot of N+ diffusion edge (over field) if distance to related Poly is > 0.27 um. Check perpendicular to active edge.	0.18
6.A.b.1	Minimum N+ implant (outside N-well) overplot of N+ diffusion edge (over field) if distance to related Poly is =< 0.27 um. Check perpendicular to active edge.	0.30
6.A.c	Minimum N+ implant (outside N-well) overplot of N+ diffusion edge (over field) of a butted diffusion edge.	0.00
6.B.a	Minimum width of N+ implant	0.31
6.C.a	Minimum N+ implant (outside N-well) space to P-substrate tie/guardbar (over field)	0.03
6.C.b	Minimum N+ implant (inside N-well) space to P+ diffusion edge (over field)	0.18
6.C.c	Minimum N+ implant (inside N-well) space to P+ diffusion edge (over field) of a butted diffusion edge.	0.00
6.D.d	Minimum N+ implant space to pfet gate for an extension of a butted N+/P+ line closer than 0.35um (see Illustration 11)	0.27
6.E.a	Minimum spacing of N+ implant to N+ implant (merge rule)	0.31
6.F.a	Minimum spacing of butted active edge in substrate to parallel P-substrate tie field edge	0.18
6.F.b	Minimum spacing of butted active edge in substrate to parallel N+ active field edge	0.18
6.I	Implant poly lines on field to ensure low resistance of silicided poly lines. Minimum implant overplot of poly for both N+ and P+ combined as a whole	0.2
6.J	Minimum N+ implant area	0.250 um**2
6.K	Overlapping of N+ and P+ is not allowed	

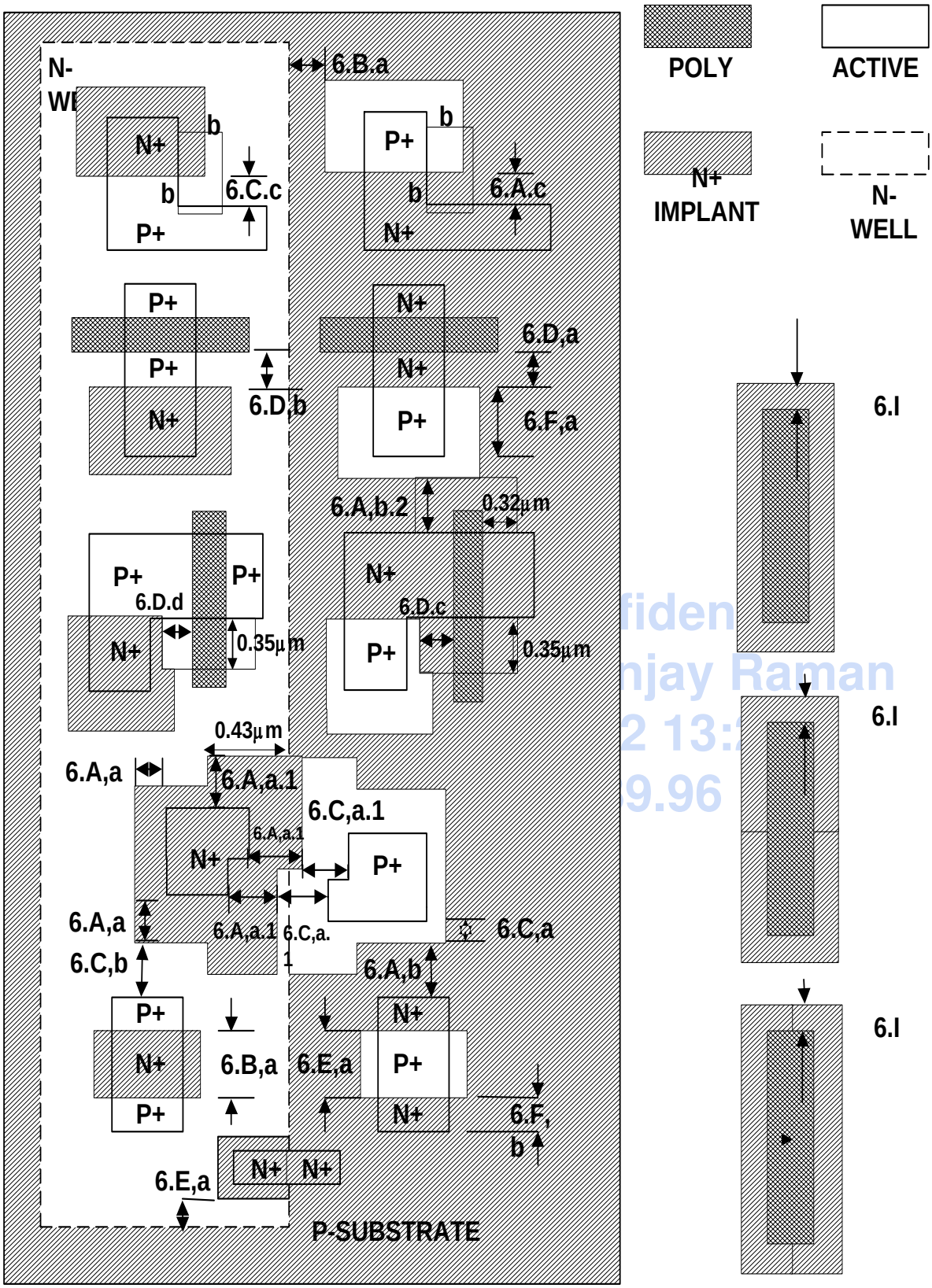


ILLUSTRATION 6

4.11.

P+ Implant "PI" (Layer 11)

Mask 11: This mask defines all of the "P+ active" areas and is a negative mask. This mask allows Boron to be implanted in all "P+ active" areas (drains, sources, and gates of PFETs, topside P-substrate ties/guardbars and P+ interconnects). The P+ implant layer is allowed to cross N-well boundaries to meet the following rules. This mask is aligned to the zero layer. See Illustration 11.

Rule No.	Rule Name	CA13HC
11.A.a	Minimum P+ implant (outside N-well) overplot of P-substrate tie/guardbar (over field)	0.03
11.A.b	Minimum P+ implant (inside N-well) overplot of P+ diffusion edge (over field) if distance to related Poly is > 0.27 um. Check perpendicular to active edge.	0.18
11.A.b.1	Minimum P+ implant (inside N-well) overplot of P+ diffusion edge (over field) if distance to related Poly is =< 0.27 um. Check perpendicular to active edge.	0.30
11.A.c	Minimum P+ implant (inside N-well) overplot of P+ diffusion edge (over field) of a butted diffusion edge.	0.00
11.B.a	Minimum width of P+ implant	0.31
11.C.a	Minimum P+ implant (inside N-well) spacing to N-well tie/guardbar (over field)	0.03
11.C.b	Minimum P+ implant (outside N-well) spacing to N+ diffusion edge (over field)	0.18
11.C.c	Minimum P+ implant (outside N-well) spacing to N+ diffusion edge (over field) of a butted diffusion edge.	0.00
11.D.d	Minimum P+ implant space to nfet gate for an extension of a butted N+/P+ line closer than 0.35um (see Illustration 11)	0.27
11.E.a	Minimum spacing of P+ implant to P+ implant (merge rule)	0.31
11.F.a	Minimum spacing of butted active edge in N-well to parallel N-well tie field edge	0.18
11.F.b	Minimum spacing of butted active edge in N-well to parallel P+ active field edge	0.18
11.I	Implant poly lines on field to ensure low resistance of silicided poly lines. Minimum implant overplot of poly for both N+ and P+ combined as a whole	0.2
11.J	Minimum P+ implant area	0.250 um**2

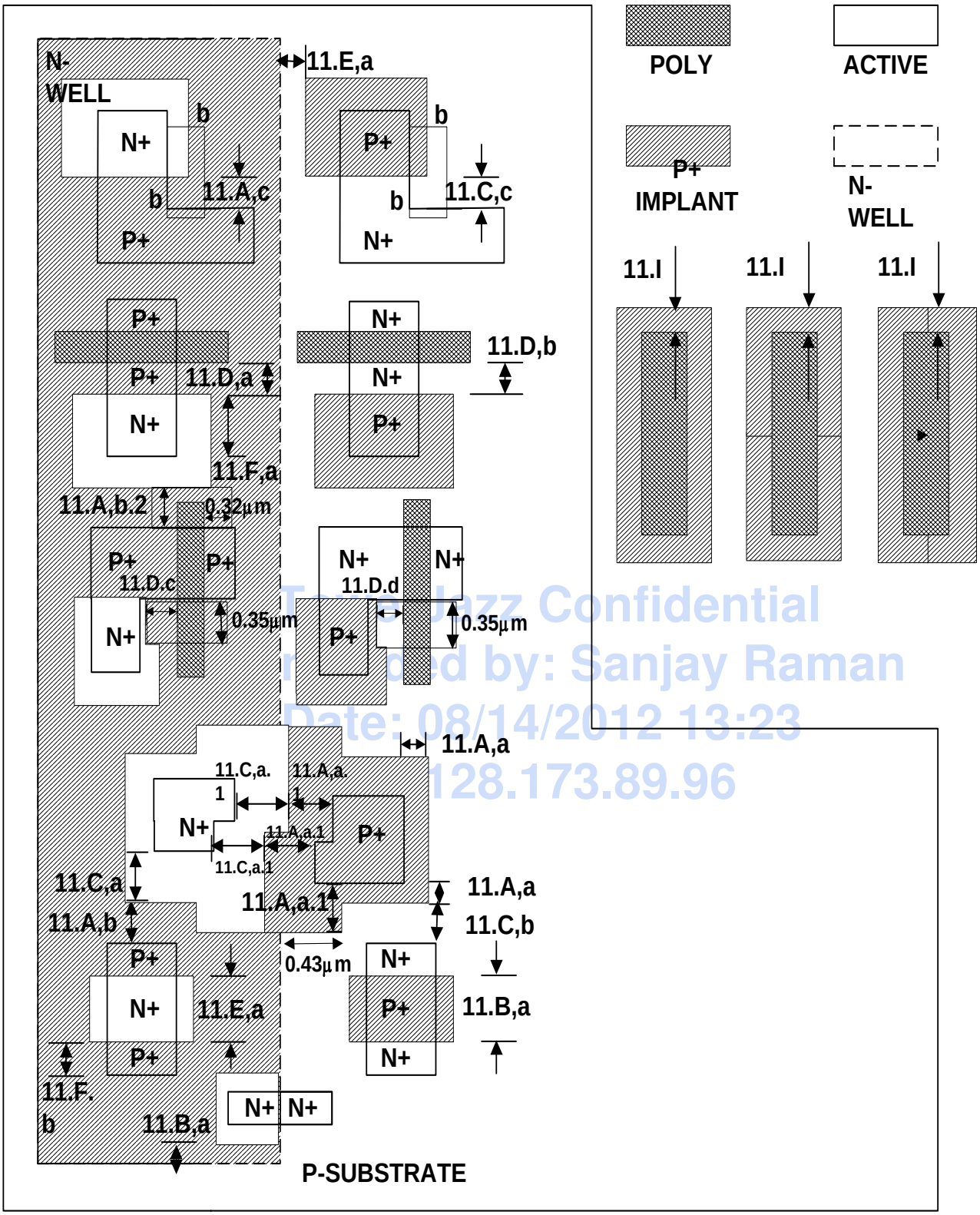


ILLUSTRATION 11

4.12.

NK Implant "NK" (Layer 61)

Mask 61: This mask defines LDD (N-type) and pocket (P-type) implants into the thin gate oxide NFETs. This mask is aligned to the zero layer. See Illustration 61. This layer is a derived layer

Rule No.	Rule Name	
61.A	Minimum width of NK implant	0.31
61.B	Minimum spacing of NK implant to NK implant	0.31
61.BAD	No drawn data is allowed for layer 61	

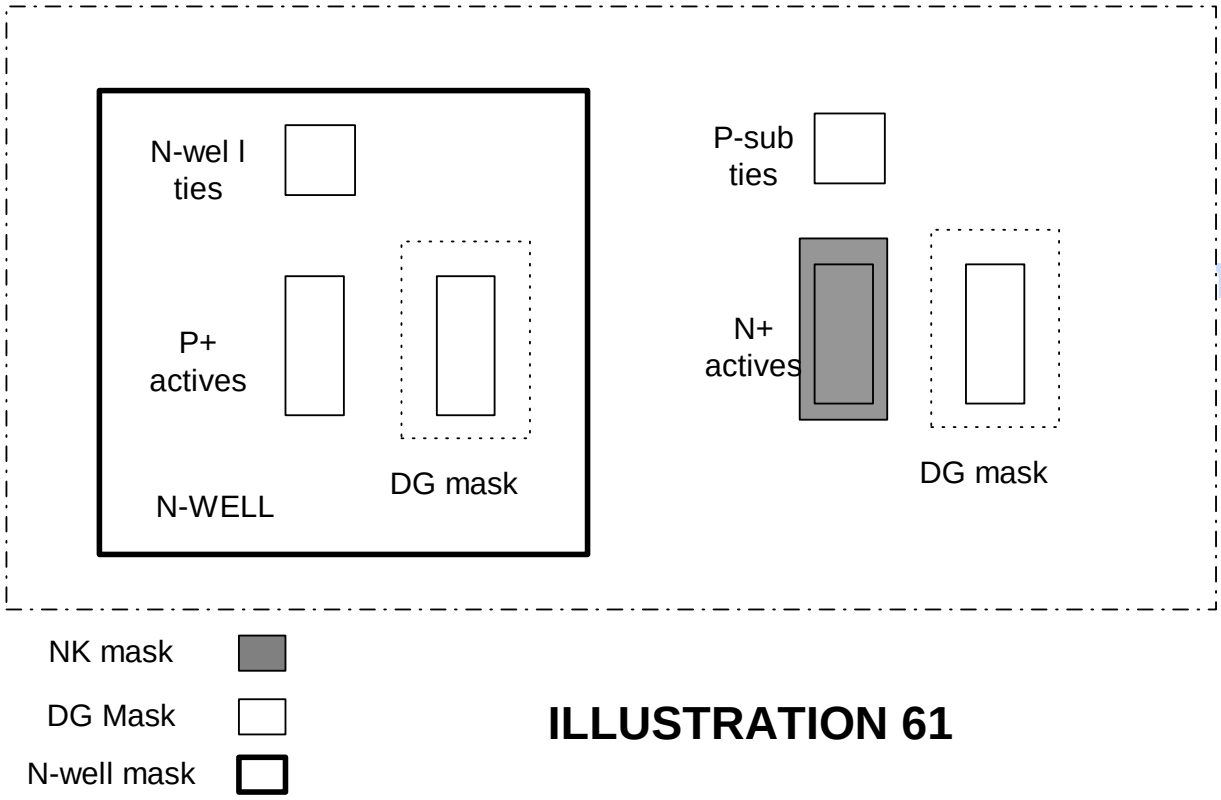


ILLUSTRATION 61

4.13. PK Implant "PK" (Layer 59)

Mask 59: This mask defines LDD (P-type) and pocket (N-type) implants into the thin gate oxide PFETs. This mask is aligned to the zero layer. See Illustration 59. This layer is a derived layer. It is a negative tone mask.

Rule No.	Rule Name	
59.A	Minimum width of PK implant	0.31
59.B	Minimum spacing of PK implant to PK implant	0.31
59.BAD	No drawn data is allowed for layer 59	

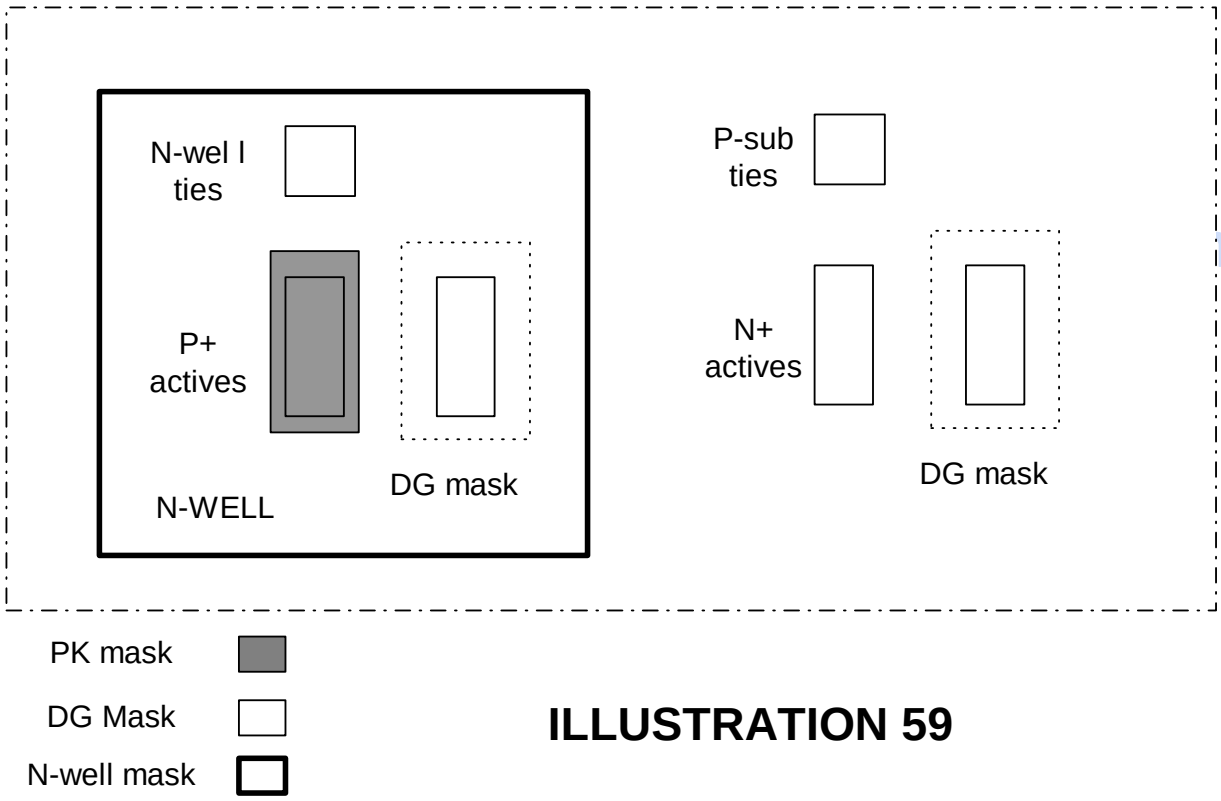


ILLUSTRATION 59

4.14. DN Implant "DN" (Layer 14)

Mask 14: This mask defines LDD implant into the thick gate oxide NFETs that are defined by the DG (Dual gate mask, layer 12). This mask is aligned to the zero layer. See Illustration 14. This layer is a derived layer. It is a negative tone mask.

Rule No.	Rule Name	
14.A	Minimum width of DN implant	0.31
14.B	Minimum spacing of DN implant to DN implant	0.31
14.BAD	No drawn data is allowed for layer 14, except in LDFETs	

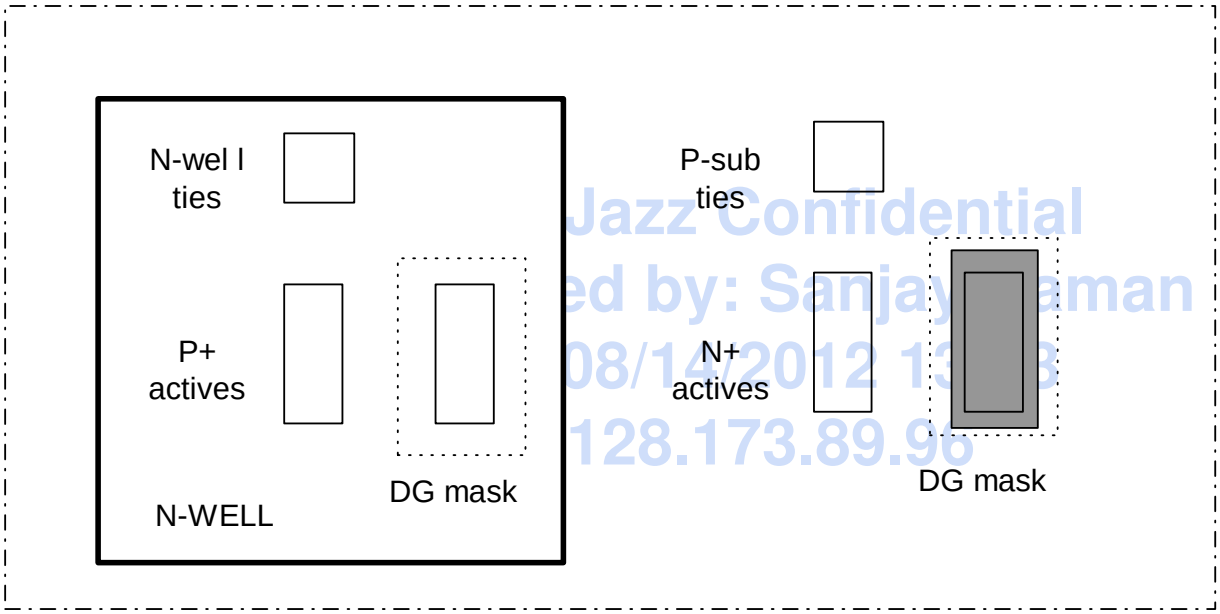


ILLUSTRATION 14

4.15.

HP Implant "HP" (Layer 60)

Mask 60: This mask defines LDD implant into the thick gate oxide PFETs that are defined by the DG (Dual gate mask, layer 12). This mask is aligned to the zero layer. See Illustration. This layer is a derived layer. It is a negative tone mask

Rule No.	Rule Name	
60.A	Minimum width of HP implant	0.31
60.B	Minimum spacing of HP implant to HP implant	0.31
60.BAD	No drawn data is allowed for layer 60, except in LDFETs	

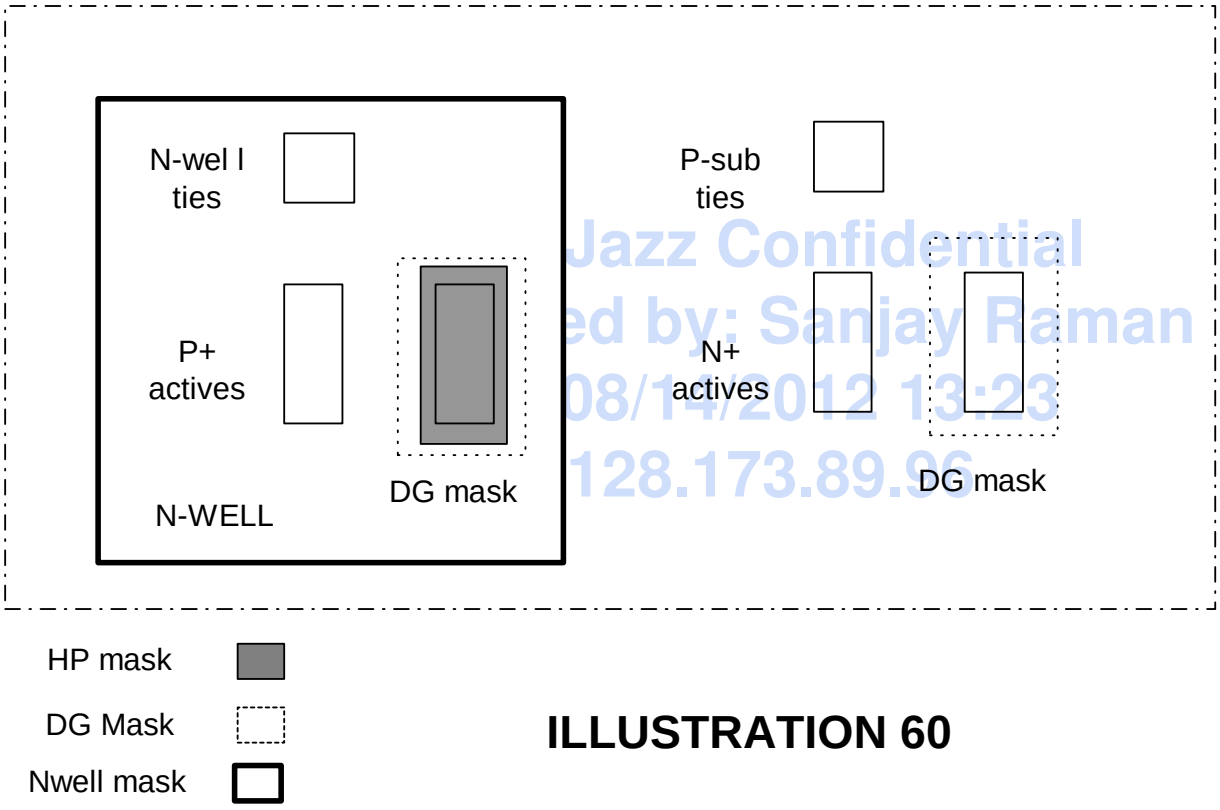


ILLUSTRATION 60

4.16.

High Value Resistor (Layer 54)

The HR layer defines polysilicon regions over field oxide, which does not receive silicide but receive the HR implant. High Value resistor Implant (HR) is a negative mask and aligns to ZL. See Illustration HR. A "resdev" marking layer (80/0) must enclose the high value resistor for lvs-purposes.

Rule No.	Rule Name	
HR.A	Minimum HR Implant overplot of P-poly resistor.	0.40
HR.B	Minimum Length Silicide Block (defines resistor length)	2.00
HR.C	Minimum Space HR to HR	0.50
HR.D	Minimum width of HR	0.70
HR.E	Minimum analog block boundry (ABLB, 118/43) overplot of poly-resistor (not shown)	1.00
HR.BAD	PI Implant is not allowed on high value un-salicided resistor	

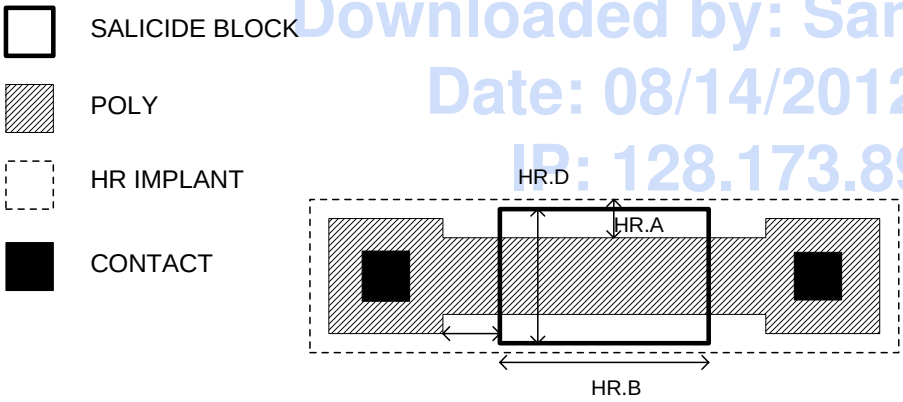


ILLUSTRATION HR

4.17. Salicide Block "SB" (Layer 40)

Mask 40: This mask defines active regions or polysilicon regions over field oxide, which does no receive salicide. Salicide block is used to define un-salicided active regions or P+ poly resistors. This mask is a positive mask and is aligned to the zero layer. See Illustration 40. A "resdev" marking layer (80/0) must enclose the low value resistors for lvs-purposes.

Rule No.	Rule Name	CA13HC

40.A	Minimum width of salicide block	0.43
40.B	Minimum space salicide block to salicide block	0.43
40.C	Minimum space salicide block to unrelated active	0.22
40.C.a	Minimum space salicide block to ESD FET source (a FET where salicide block covers the drain)	0.15
40.D	Minimum space salicide block to poly on active	0.38
40.E	Minimum overplot of salicide block to related diffusion	0.22
40.F	Minimum overplot of active to salicide block	0.22
40.G	Minimum overplot of salicide block to poly resistor	0.22
40.G.a	Minimum overlap of salicide block on gate poly	0.15
40.G.b	Minimum extension of gate poly beyond salicide block	0.15
40.H	Minimum area of salicide block	1.0 (um^2)
40.I	Minimum space salicide block to unrelated poly	0.30
40.J	Minimum overplot of PI to P-poly resistor	0.20
40.K	Minimum space NI to P+ poly resistor	0.20
40.L	Minimum area enclosed by salicide block	1.0 (um^2)
40.M	Minimum length of salicide block (defines unsalicided resistor lengths)	2.0
40.N	Minimum space salicide block to contact on active	0.3

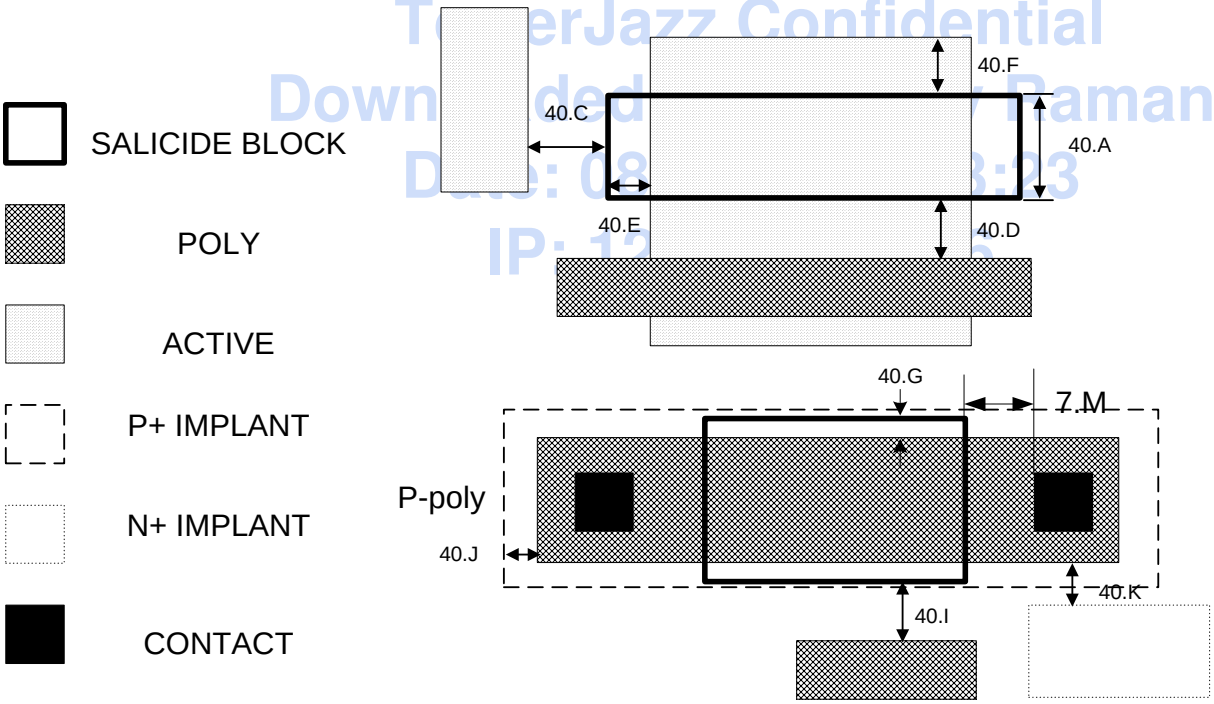


ILLUSTRATION 40

4.18.

Contact "C" (Layer 7)

Mask 7: This mask defines metal 1 to P+ diffusions, metal 1 to N+ diffusions, and metal 1 to poly contact areas. This mask is a negative mask and is aligned to the zero layer. See Illustration 7.

Rule No.	Rule Name	CA13HC
7.A	Minimum/maximum contact size	0.16X0.16
7.B	Minimum contact to contact space	0.18
7.B.a	Minimum contact to contact space in a contact array with 3 by 3 or more contacts	0.20
7.C	Minimum spacing diffusion contact to unrelated poly	0.11
7.D	Minimum spacing poly contact on field to diffusion (channel region)	0.14
7.E	Minimum poly extension beyond contact	0.07
7.F	Minimum active extension beyond contact	0.07
7.G	Minimum butting implant (N+ or P+) overplot of contact	0.09
7.I	Contact on the edge of n+/p+ implant boundary is not allowed over active	
7.J	Poly contacts are not allowed over active areas.	
7.K	45 degree-rotated contacts are not allowed.	
7.L	Non silicided contacts are not allowed	
7.M	Minimum space contact to salicide block (see Illustration 40)	0.22

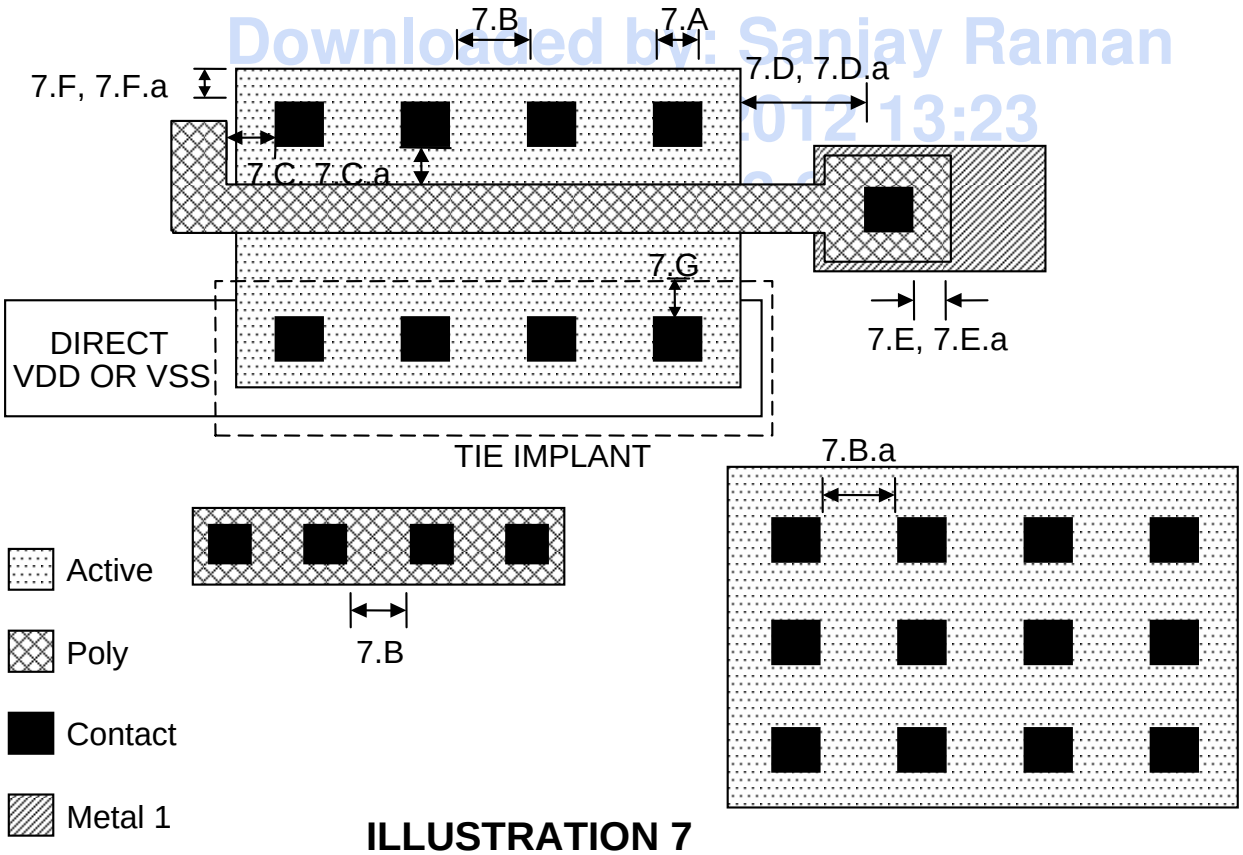


ILLUSTRATION 7

4.19.

Metal 1 "M1" (Layer 8)

Mask 8: This mask defines the first layer metal interconnection for a circuit. The mask is a positive mask and is aligned to the zero layer. See Illustration 8.

Rule No.	Rule Name	CA13HC
8.A	Minimum metal 1 line width	0.19
8.B	Minimum metal 1 to metal 1 space	0.20
8.B.a	Minimum metal 1 to metal 1 space for one or both metal 1 width and length are greater than 10um (metal 1 polygon larger than 10um x 10um). This includes all attachments to a large metal 1 polygon and extending out with a run of 1.0um or less.	0.60
8.C	Minimum metal 1 overplot of contacts (see note 2)	0.005
8.C.a	Minimum metal 1 overplot of contact at two opposite sides of contact (see Illustration 8)	0.05
8.C.b	Minimum metal 1 overplot of contact at two opposite sides of contact (see Illustration 8), if metal1 area is less than 0.205 um^2	0.10
8.C.b.1	Minimum metal 1 overplot of via1 at two opposite sides of contact (see Illustration 8), if metal1 area is less than 0.205 um^2	0.10
8.D	Minimum metal 1 density (total metal 1 area / chip area)(see Note1)	30%
8.E	Minimum metal 1 area	0.144 (um^2)
8.F	Maximum metal 1 density (total metal 1 area / chip area)(see Note1)	60%

Note 1: Run density check to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements. See section 3.4.1 and 3.4.2 for dummy metal fill. Additional floating metal 1 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 8.D. The following method of generation of dummy metal conforms to the process design rule.

Note2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8.

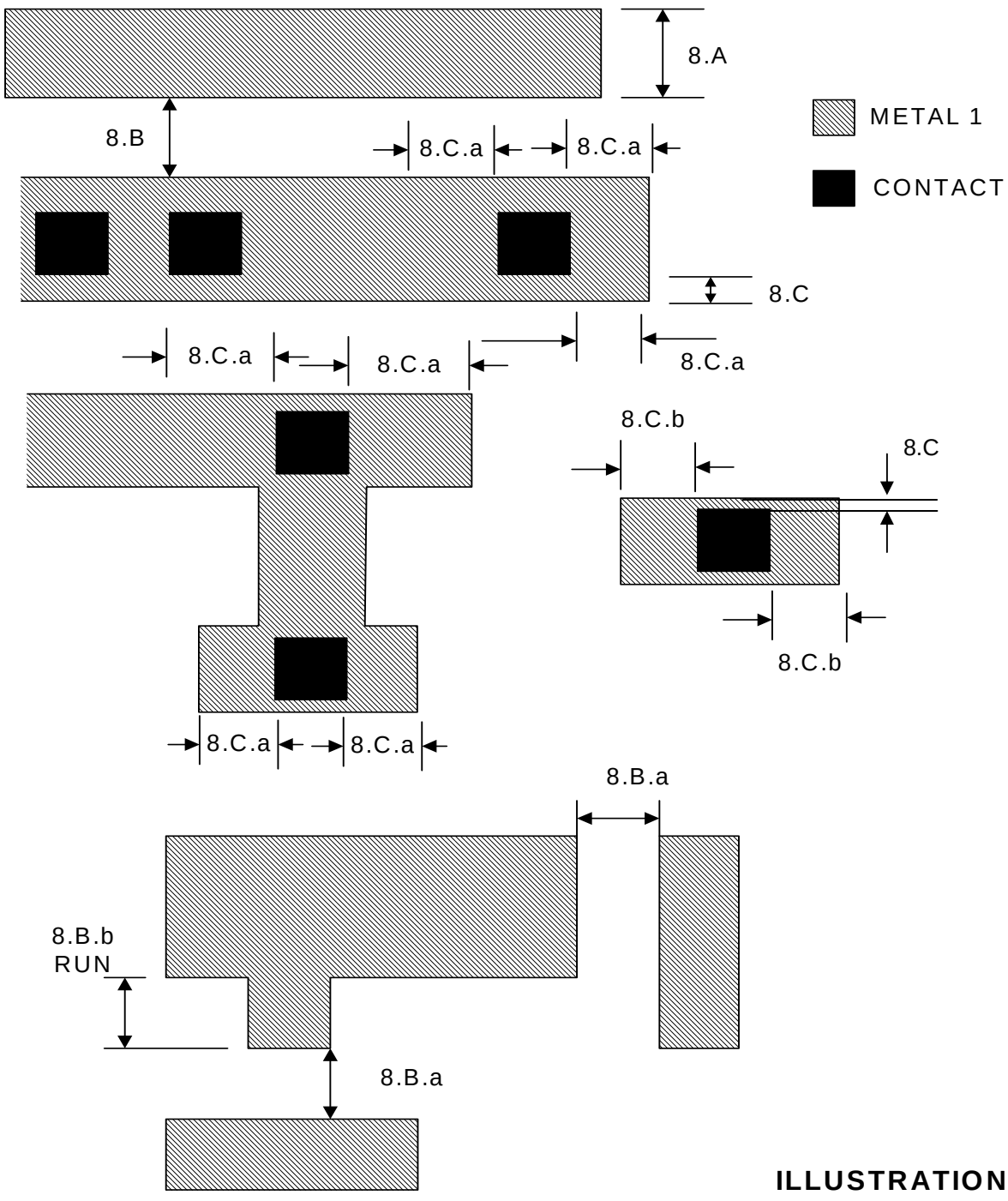


ILLUSTRATION 8

4.20.

Via1 "VA" (Layer 17)

Mask 17: This mask defines metal 1 to metal 2 contact areas. This mask is a negative mask and is aligned to the zero layer.

Rule No.	Rule Name	CA13HC
17.A	Minimum/maximum via1 size	0.22X0.22
17.B	Minimum metal 1 overplot of via1 (see note 1)	0.01
17.B.a	Minimum metal 1 overplot of via1 at two opposite sides of via1 (see Illustration 17)	0.05
17.C	Minimum via1 to via1 space	0.22
17.C.a	Minimum via1 to via1 space in a via1 array with 3 by 3 or more via1s	0.28
17.D	Via1s may be placed over poly or diffusion contacts	
17.E	45 degree-rotated via1 is not allowed.	

Note1: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

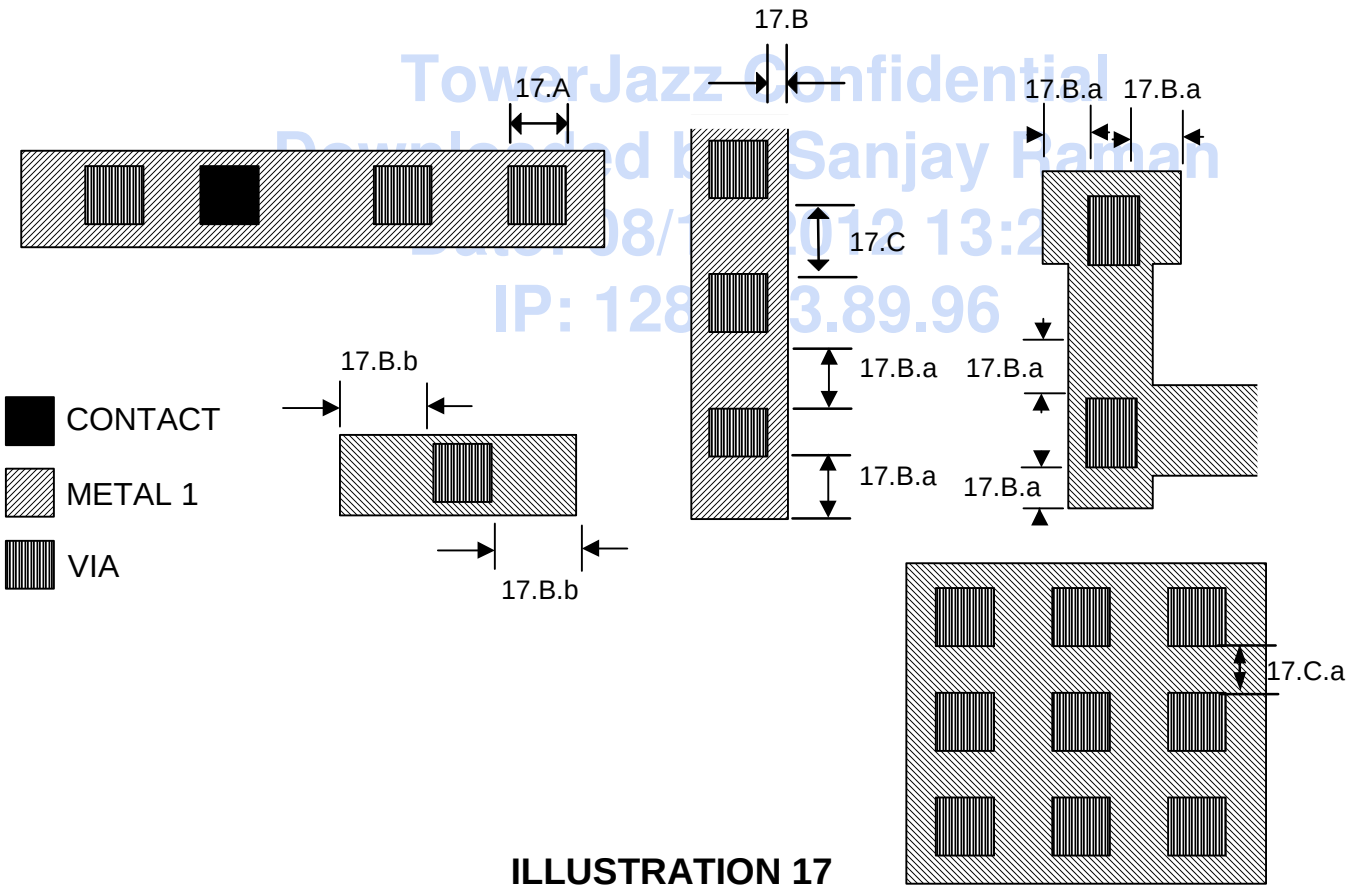


ILLUSTRATION 17

4.21. Metal 2 "M2" (Layer 18)

Mask 18: This mask defines the second metal interconnections. The mask is a positive mask and is aligned to the zero layer. See Illustration 18.

Rule No.	Rule Name	CA13HC
18.A	Minimum metal 2 width	0.24
18.B	Minimum spacing metal 2 to metal 2	0.24
18.B.a	Minimum spacing metal 2 to metal 2 for one or both metal 2 width and length are greater than 10um (metal 2 polygon larger than 10um x 10um). This includes all attachments to a large metal 2 polygon and extending out with a run of 1.0um or less.	0.60
18.C	Minimum metal 2 overplot of via1 (see note 2)	0.01
18.C.a	Minimum metal 2 overplot of via1 at two opposite sides of via1 (see Illustration 18)	0.05
18.C.b	Minimum metal 2 overplot of via1 and via2, if metal2 area is less than 0.205 um^2	0.08
18.D	Minimum metal 2 density (total metal 2 area / chip area) (See Note 1)	30%
18.E	Minimum metal 2 area	0.144 (um^2)
18.F	Maximum metal 2 density (total metal 2 area / chip area) (See Note 1)	60%

Note 1: Run density check to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements. See section 3.4.1 and 3.4.2 for dummy metal fill. Additional floating metal 2 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 18.D. The following method of generation of dummy metal conforms to the process design rule.

Note2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8.

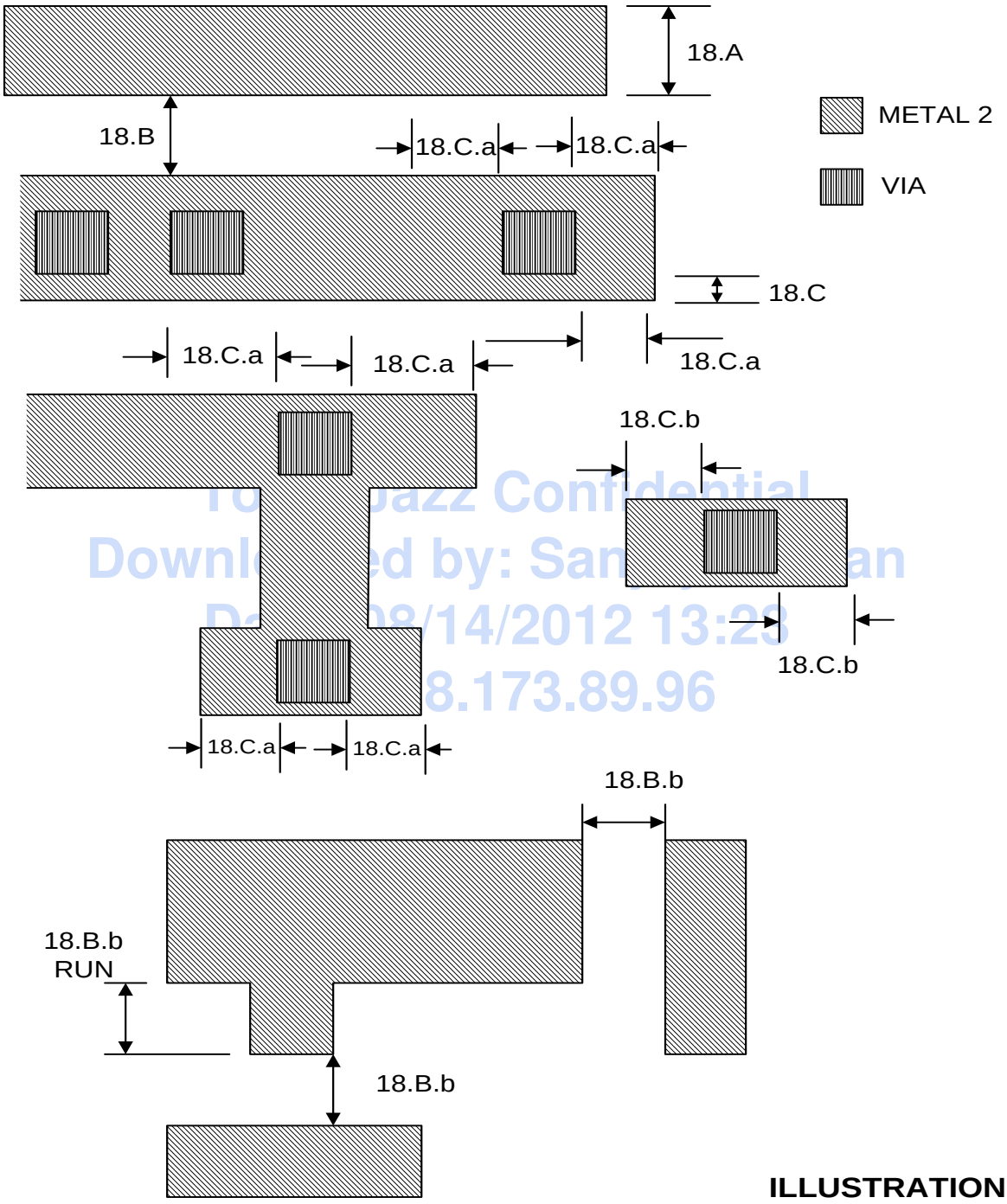


ILLUSTRATION 18

4.22.

Via2 "V2" (Layer 27)

Mask 17: This mask defines metal 2 to metal 3 contact areas. This mask is a negative mask and is aligned to the zero layer.

Rule No.	Rule Name	CA13HC
27.A	Minimum/maximum via2 size	0.22X0.22
27.B	Minimum metal 2 overplot of via2 (see note 1)	0.01
27.B.a	Minimum metal 2 overplot of via2 at two opposite sides of via2 (see Illustration 27)	0.05
27.C	Minimum via2 to via2 space	0.22
27.C.a	Minimum via2 to via2 space in a via-2 array with 3 by 3 or more via2s	0.28
27.D	Via2s may be placed over poly, diffusion contacts or via1s	
27.E	45 degree-rotated via2 is not allowed.	

Note1: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

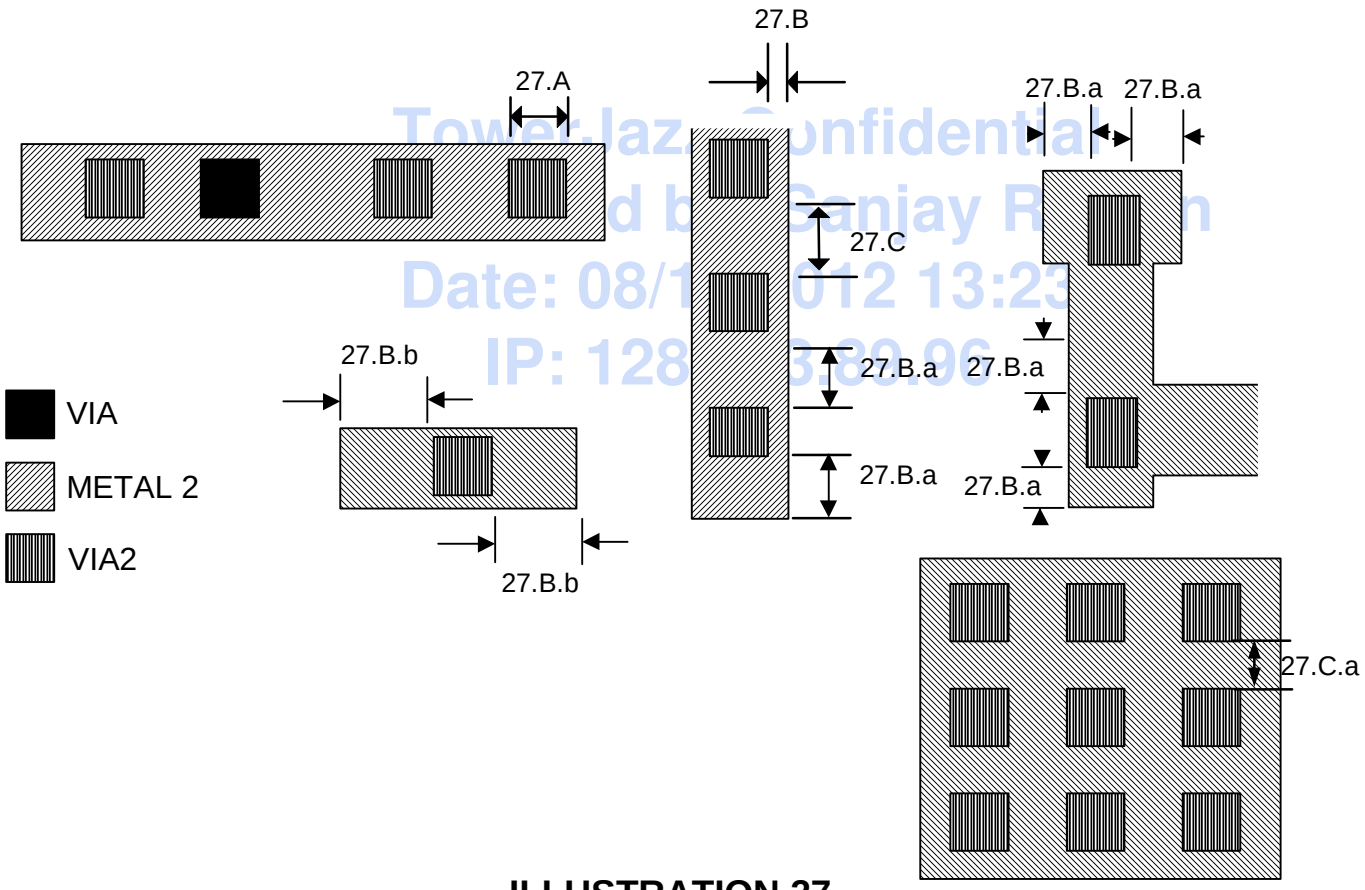


ILLUSTRATION 27

4.23.

Metal 3 "M3" (Layer 28)

Mask 28: This mask defines the third metal interconnects. The mask is a positive mask and is aligned to the zero layer. See Illustration 28.

Rule No.	Rule Name	CA13HC
28.A	Minimum metal 3 width	0.24
28.B	Minimum spacing metal 3 to metal 3	0.24
28.B.a	Minimum spacing metal 3 to metal 3 for one or both metal 3 width and length are greater than 10um (metal 3 polygon larger than 10um x 10um). This includes all attachments to a large metal 3 polygon and extending out with a run of 1.0um or less.	0.60
28.C	Minimum metal 3 overplot of via2 (see note 2)	0.01
28.C.a	Minimum metal 3 overplot of via2 at two opposite sides of via2 (see Illustration 28)	0.05
28.C.b	Minimum metal 3 overplot of via2 and via3, if metal3 area is less than 0.205 um^2	0.08
28.D	Minimum metal 3 density (total metal 3 area / chip area) (See Note 1)	30%
28.E	Minimum metal 3 area	0.144 (um^2)
28.F	Maximum metal 3 density (total metal 3 area / chip area) (See Note 1)	60%

Note 1: Run density check to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements. See section 3.4.1 and 3.4.2 for dummy metal fill. Additional floating metal 3 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 28.D. The following method of generation of dummy metal conforms to the process design rule.

Note2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

4.24.

Via3 "V3" (Layer 37)

Mask 37: This mask defines metal 3 to metal 4 contact areas. This mask is a negative mask and is aligned to the zero layer.

Rule No.	Rule Name	CA13HC
37.A	Minimum/maximum via3 size	0.22X0.22
37.B	Minimum metal 3 overplot of via3 (see note 1)	0.01
37.B.a	Minimum metal 3 overplot of via3 at two opposite sides of via3 (see Illustration 37)	0.05
37.C	Minimum via3 to via3 space	0.22
37.C.a	Minimum via3 to via3 space in a via3 array with 3 by 3 or more via3s	0.28
37.D	Via3s may be placed over contacts, via1s or via2s	
37.E	45 degree-rotated via3 is not allowed.	

Note1: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

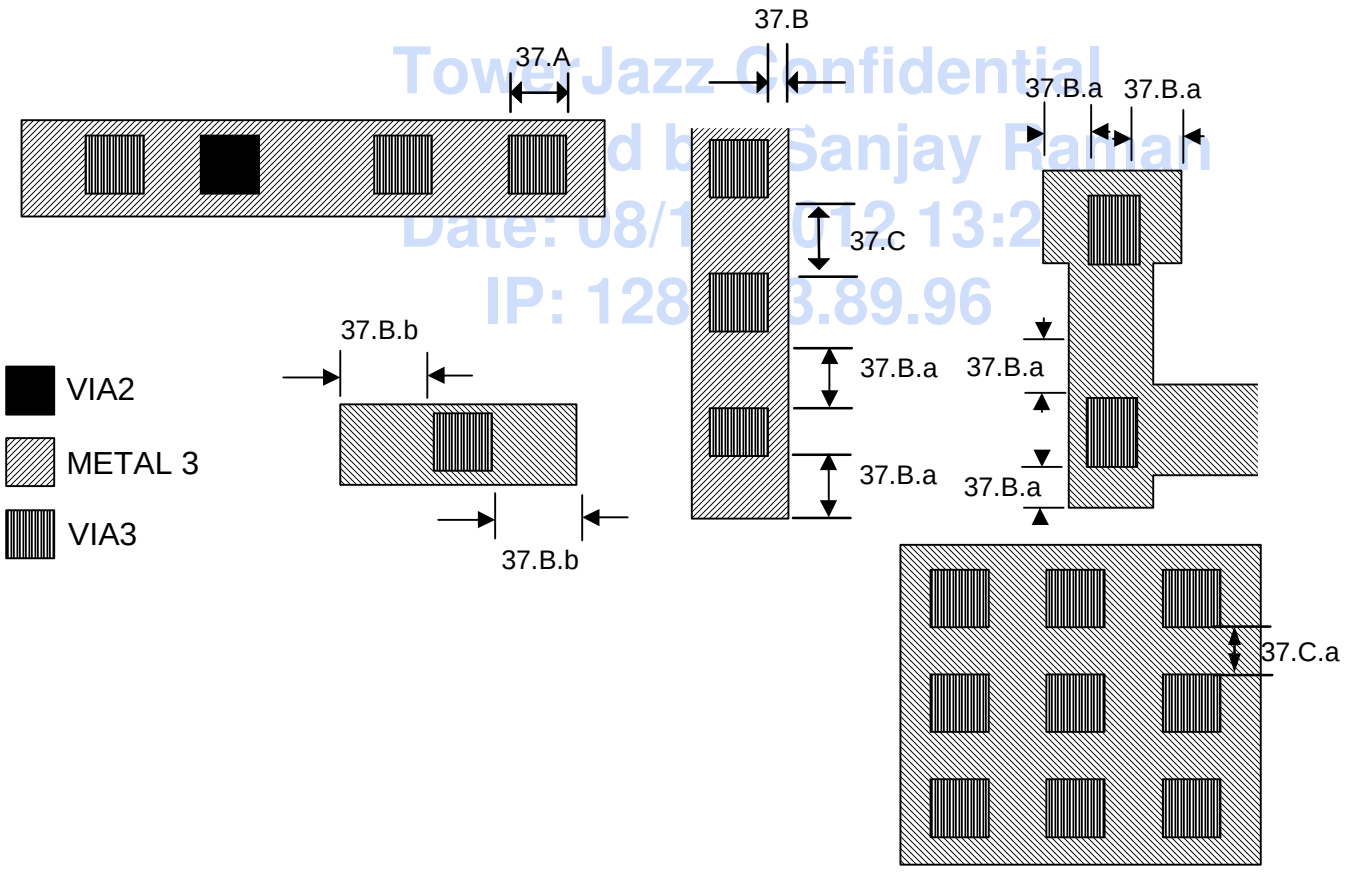


ILLUSTRATION 37

4.25. Metal 4 "M4"(Layer 38)

Mask 38: This mask defines the fourth metal interconnects. The mask is a positive mask and is aligned to the zero layer. See Illustration 38.

Rule No.	Rule Name	CA13HC
38.A	Minimum metal 4 width	0.24
38.B	Minimum spacing metal 4 to metal 4	0.24
38.B.a	Minimum spacing metal 4 to metal 4 space for one or both metal 4 width and length are greater than 10um (metal 4 polygon larger than 10um x 10um). This includes all attachments to a large metal 4 polygon and extending out with a run of 1.0um or less.	0.60
38.C	Minimum metal 4 overplot of via3 (see note 2)	0.01
38.C.a	Minimum metal 4 overplot of via3 at two opposite sides of via3 (see Illustration 38)	0.05
38.C.b	Minimum metal 4 overplot of via3 and via4, if metal4 area is less than 0.205 um^2	0.08
38.D	Minimum metal 4 density (total metal 4 area / chip area) (See Note 1)	30%
38.E	Minimum metal 4 area	0.144 (um^2)
38.F	Maximum metal 4 density (total metal 4 area / chip area) (See Note 1)	60%

Note 1: Run density check to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements. See section 3.4.1 and 3.4.2 for dummy metal fill. Additional floating metal 4 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 38.D. The following method of generation of dummy metal conforms to the process design rule.

Note2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

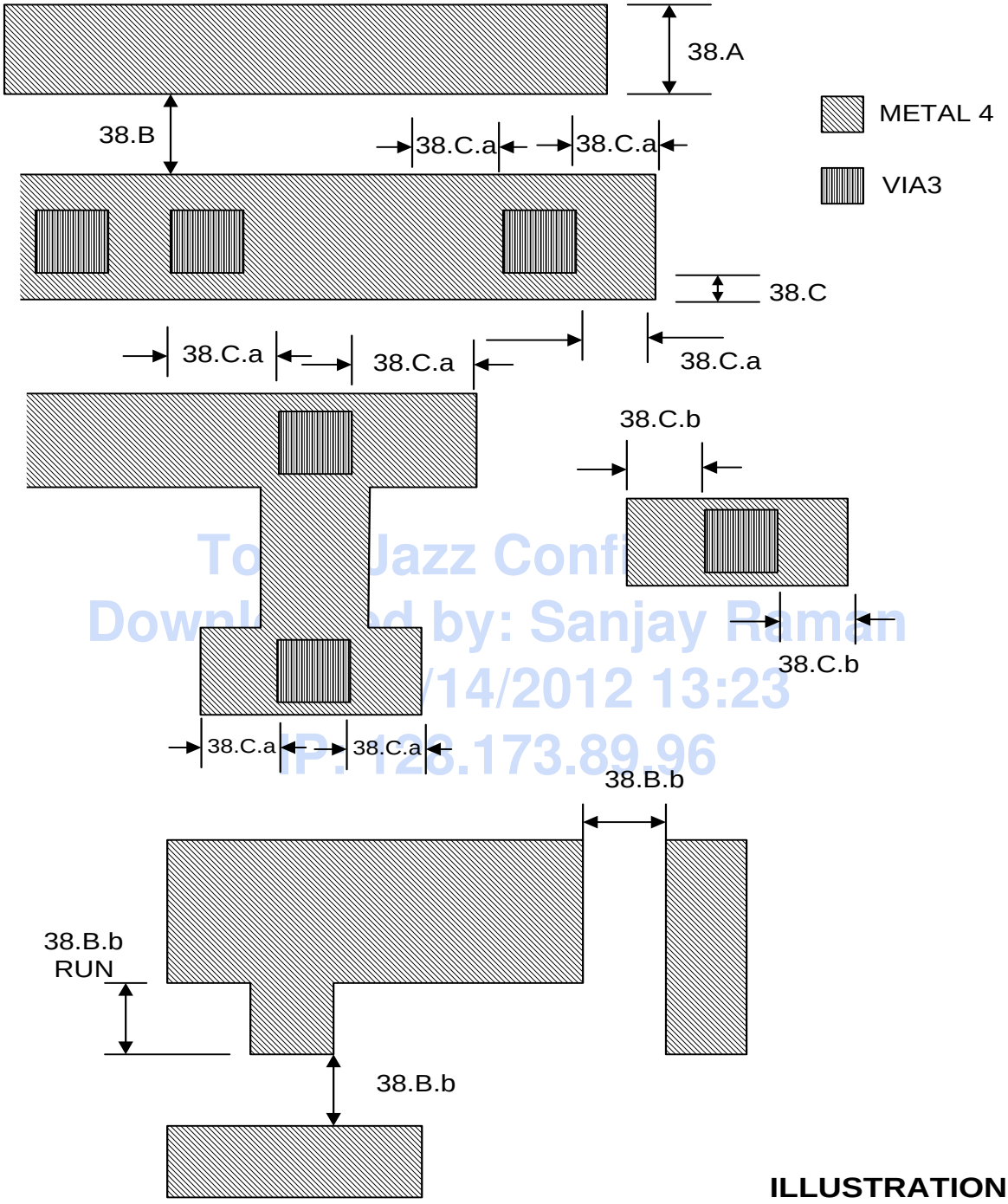


ILLUSTRATION 38

4.26. Via4 "V4" (Layer 47)

Mask 47: This mask defines metal 4 to metal 5 contact areas. This mask is a negative mask and is aligned to the zero layer.

Rule No.	Rule Name	CA13HC
47.A	Minimum/maximum via4 size	0.22X0.22
47.B	Minimum metal 4 overplot of via4 (see note 1)	0.01
47.B.a	Minimum metal 4 overplot of via4 at two opposite sides of via4 (see Illustration 47)	0.05
47.C	Minimum via4 to via4 space	0.22
47.C.a	Minimum via4 to via4 space in a via4 array with 3 by 3 or more via4s	0.28
47.D	Via4s may be placed over contacts, via1s, via2s or via3s	
47.E	45 degree-rotated via4 is not allowed.	

Note1: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

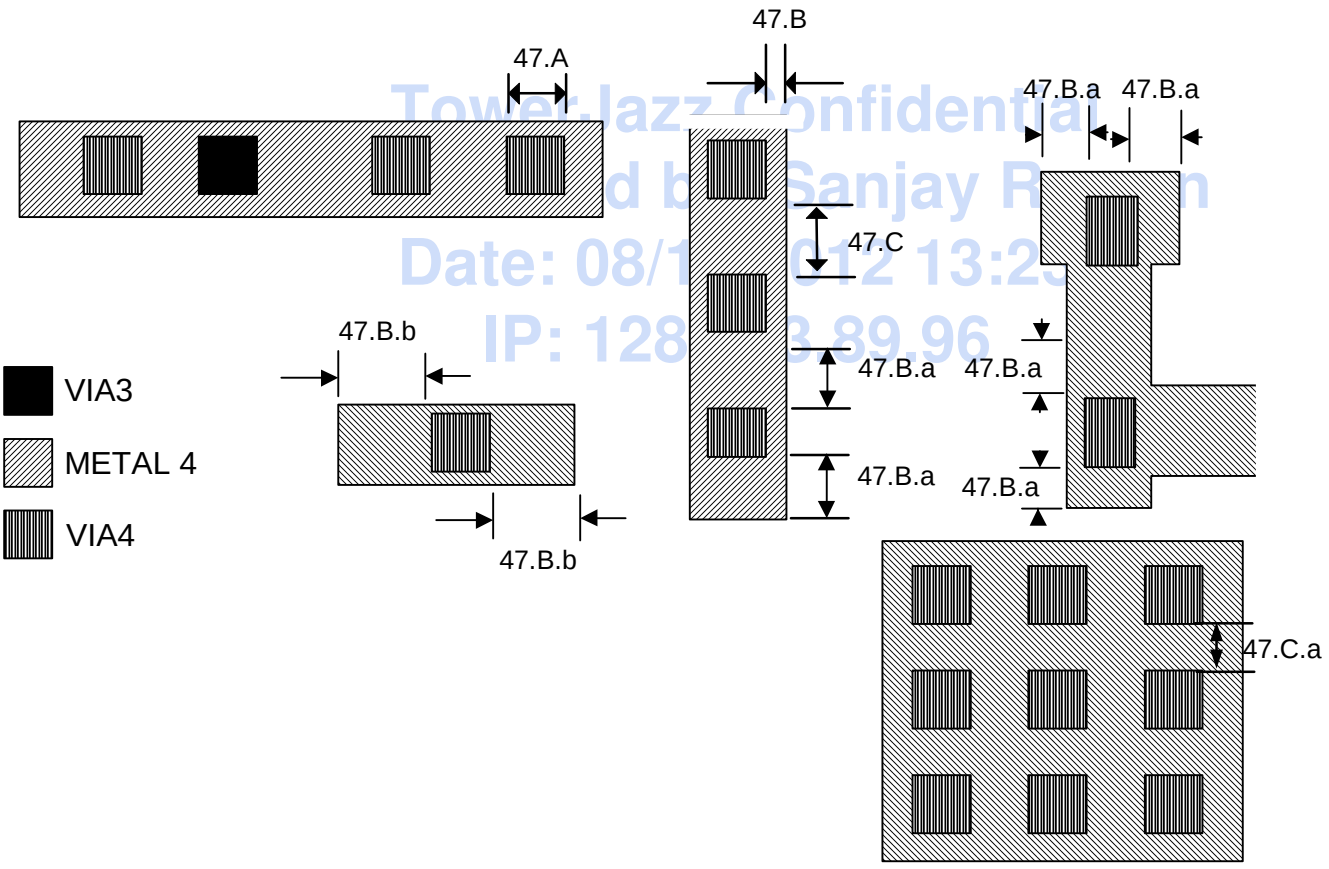


ILLUSTRATION 47

4.27.

Metal 5 "M5" (Layer 48)

Mask 48: This mask defines the fifth metal interconnects. The mask is a positive mask and is aligned to the zero layer. See Illustration 48.

Rule No.	Rule Name	CA13HC
48.A	Minimum metal 5 width	0.24
48.B	Minimum spacing metal 5 to metal 5	0.24
48.B.a	Minimum spacing metal 5 to metal 5 space for one or both metal 5 width and length are greater than 10um (metal 5 polygon larger than 10um x 10um). This includes all attachments to a large metal 5 polygon and extending out with a run of 1.0um or less.	0.60
48.C	Minimum metal 5 overplot of via4 (see note 2)	0.01
48.C.a	Minimum metal 5 overplot of via4 at two opposite sides of via4 (see Illustration 38)	0.05
48.C.b	Minimum metal 5 overplot of via4 and via5, if metal-5 area is less than 0.205 um^2	0.08
48.D	Minimum metal 5 density (total metal 5 area / chip area) (See Note 1)	30%
48.E	Minimum metal 5 area	0.144 (um^2)
48.F	Maximum metal 5 density (total metal 5 area / chip area) (See Note 1)	60%

Note 1: Run density check to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements. See section 3.4.1 and 3.4.2 for dummy metal fill. Additional floating metal 5 patterns should be added to the circuit and the PCMs to achieve the density specified by Rule 48.D. The following method of generation of dummy metal conforms to the process design rule.

Note2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

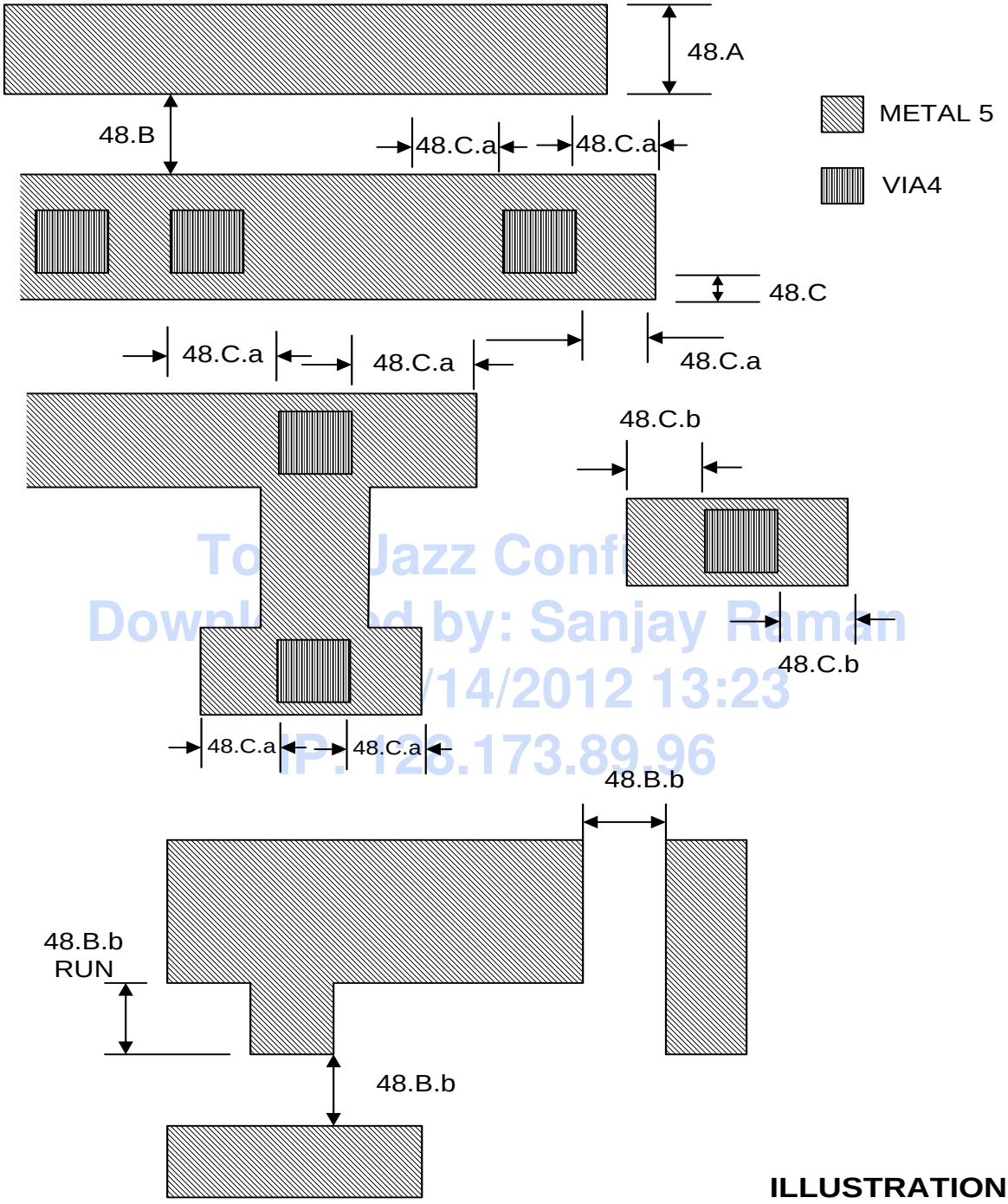


ILLUSTRATION 48

4.28.

Via5 "V5" (Layer 57)

Mask 57: This mask defines metal 5 to metal 6 contact areas. This mask is a negative mask and is aligned to the zero layer.

Rule No.	Rule Name	CA13HC
57.A	Minimum/maximum via5 size	0.36X0.36
57.B	Minimum metal 5 overplot of via5 (see note 1)	0.01
57.B.a	Minimum metal 5 overplot of via5 at two opposite sides of via5 (see Illustration 57)	0.05
57.C	Minimum via5 to via5 space	0.35
57.D	Via5s may be placed over contacts, via1s, via2s, via3s and via4s	
57.D	45 degree-rotated via5 is not allowed.	

Note1: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layers 118/53). See section 5.8

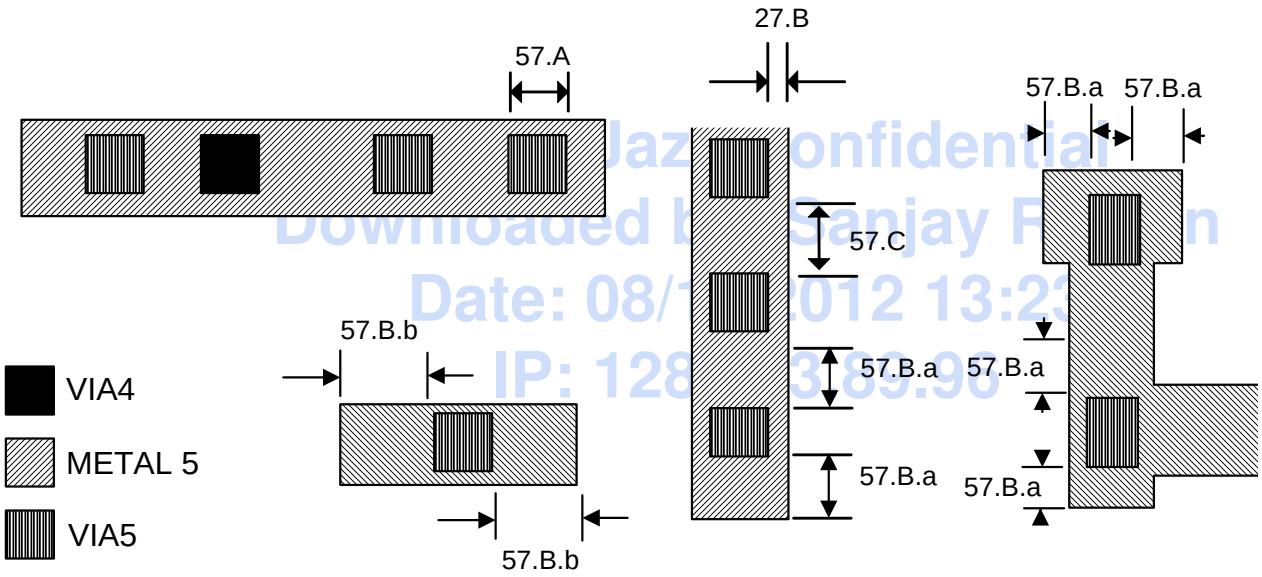


ILLUSTRATION 57

4.29. Metal 6 (layer 58)

Mask 58: This mask defines the top (or sixth) metal interconnects, inductors and bonding pads for a circuit. The mask is a positive tone mask and is aligned to ZL. See Illustration 58.

Rule No.	Rule Name	CA13HC
58.A	Minimum metal 6 width	2.50
58.B	Minimum metal 6 to metal 6 space	2.00
58.C	Metal 6 overplot of via5 (see note 2)	0.35
58.D	Minimum metal 6 density (total metal 6 area / chip area). See Note 1	25%
58.E	Minimum metal 6 area	6.25 (um^2)
58.F	Maximum metal 6 density (total metal 6 area / chip area). See Note 1	60%

Note 1: Run density check in Calibre to find out if Jazz default dummy (floating) metal fill algorithm will meet metal density requirements. See Section 3.4 for dummy metal fill generation.
Note 2: Use special metal overplot rules for analog and RF blocks (areas covered by analog block layer 118, datatype 53). See section 5.6.

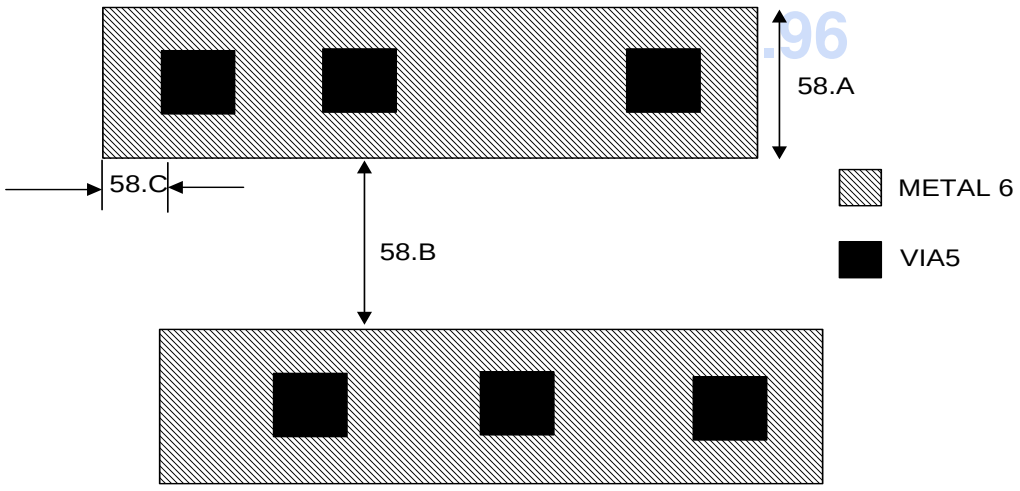


ILLUSTRATION 58

4.30.

Protective Overcoat "S" (Layer 9)

Mask 9: This layer provides overcoat protection for the chip. This mask is a negative mask and is aligned to the zero layer. See the section on bonding pads for related rules.

Rule No.	Rule Name	
9.A	Minimum passivation overcoat width	4
9.B	Minimum spacing passivation overcoat to passivation overcoat	4

5.

Design Rules for RF and Mixed Signal Components

5.1. Resistor Rules

5.1.1. Poly Resistor Rules

For low value unsalicided poly resistors, please refer to design rules for Salicide Block (SB) layer 40. For high value unsalicided poly resistor rules, refer to design rules for HR (layer 54).

5.1.2. N-Well resistor Rules

For N-well resistor rules, please refer to design rules for N-well (layer 1).

5.2. Vertical Metal Insulator Metal (MIM) Capacitor

5.2.1. Rules of 2.8fF/um^2 density MIM capacitor on M4

This defines high unit area capacitor structures (MIM caps) fabricated using metal 4 (Layer 38) as the lower plate and top capacitor metal (TM) as the upper plate. See Illustration MC. Layer 22 is a positive mask.

Rule No.	Rule Name	CA13HC
MC1	Minimum TM width/length	1.50
MC2	Minimum TM Overplot of Via4, when via4 is on both TM and metal 4	0.50
MC3	Minimum Space TM to Via4, when via4 is not over TM	0.50
MC4	Minimum Overplot of Metal 4 to TM	1.00
MC5	Minimum Space TM to TM	0.80
MC9	Minimum via4 to via4 space on TM (for TM area > 400um^2)	3.50
MC9.a	Minimum via4 to via4 space on TM (for TM area < 400um^2)	1.00
MC10	Maximum via4 to via4space on TM	4.50
MC11	Minimum space capacitor TM to via3 (No Via3 is allowed below TM layer)	0.50
MC21	Minimum Analog block border (layer 118/53) overplot of TM*	2.00

Note 1: For best matching results it is recommended that a minimum via4 to TM space of 2.0 um be maintained.

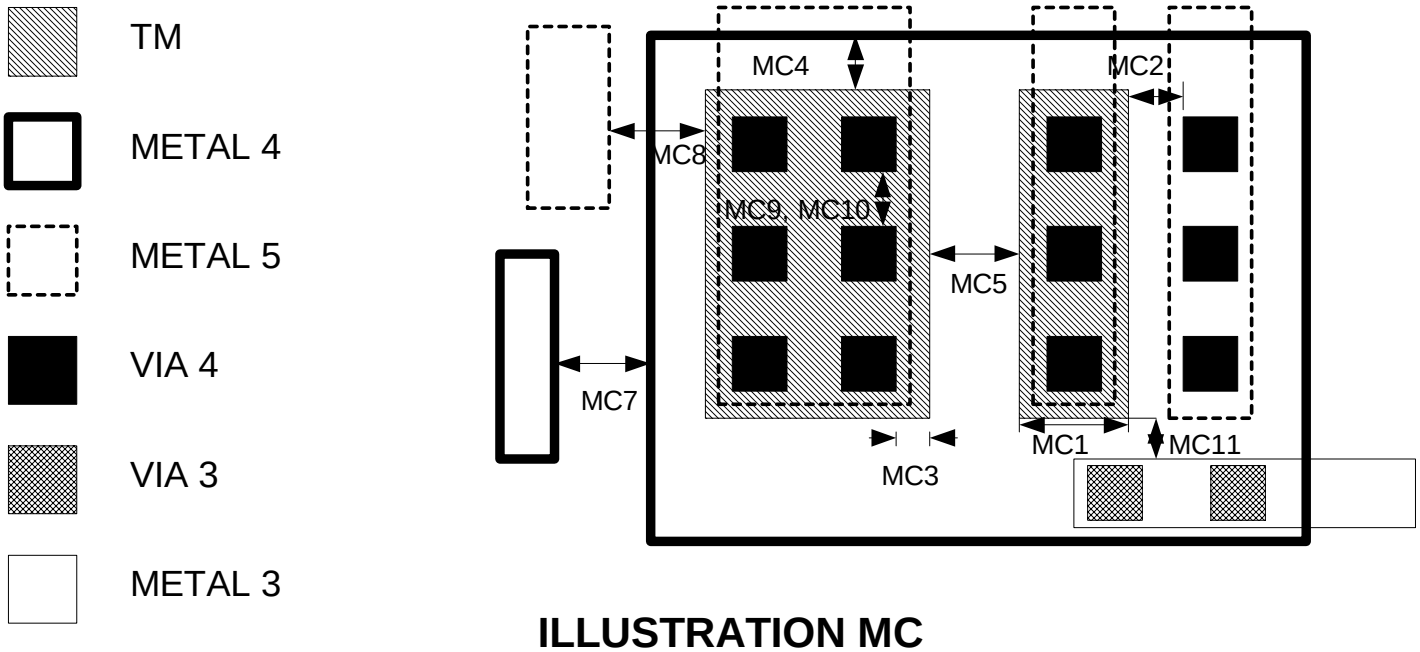


ILLUSTRATION MC

5.2.2. Rules of 2.8fF/um^2 density MIM capacitor on M5

This defines high unit area capacitor structures (MIM caps) fabricated using metal 5 (Layer 48) as the lower plate and top capacitor metal (TM2) as the upper plate. See Illustration MC2. Layer 30 is a positive mask.

Rule No.	Rule Name	CA13HC
MC2_1	Minimum TM2 width/length	1.50
MC2_2	Minimum TM2 Overplot of Via5, when via5 is on both TM2 and metal 5	0.50
MC2_3	Minimum Space TM2 to Via5, when via5 is not over TM	0.50
MC2_4	Minimum Overplot of Metal 5 to TM2	1.00
MC2_5	Minimum Space TM2 to TM2	0.80
MC2_6	Minimum Space TM to TM2	0.80
MC2_9	Minimum via5 to via5 space on TM2 (for TM2 area > 400um^2)	3.50
MC2_9.a	Minimum via4 to via5 space on TM2 (for TM2 area < 400um^2)	1.00
MC2_10	Maximum via5 to via5 space on TM 2	4.50
MC2_11	Minimum space capacitor TM2 to via4	0.50
MC2_21	Minimum Analog block border (layer: 118/53) overplot of TM2*	2.00

MC2_22	Minimum spacing between TM2 (layer 30) and TM (layer 22)	0.80
MC2_BAD1	No Via4 allowed under TM2 EXCEPT when TM is coincident with TM2.	

Note 1: For best matching results it is recommended that a minimum via5 to TM2 space of 2.0 um be maintained.

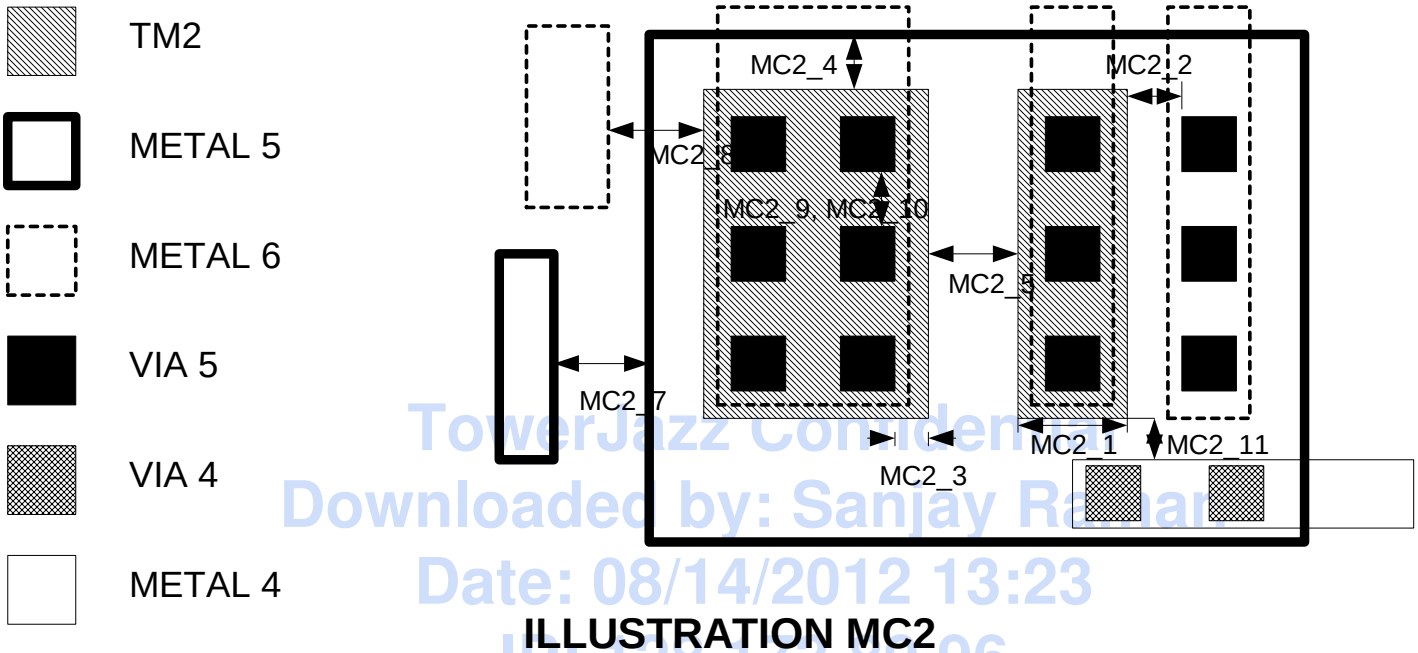
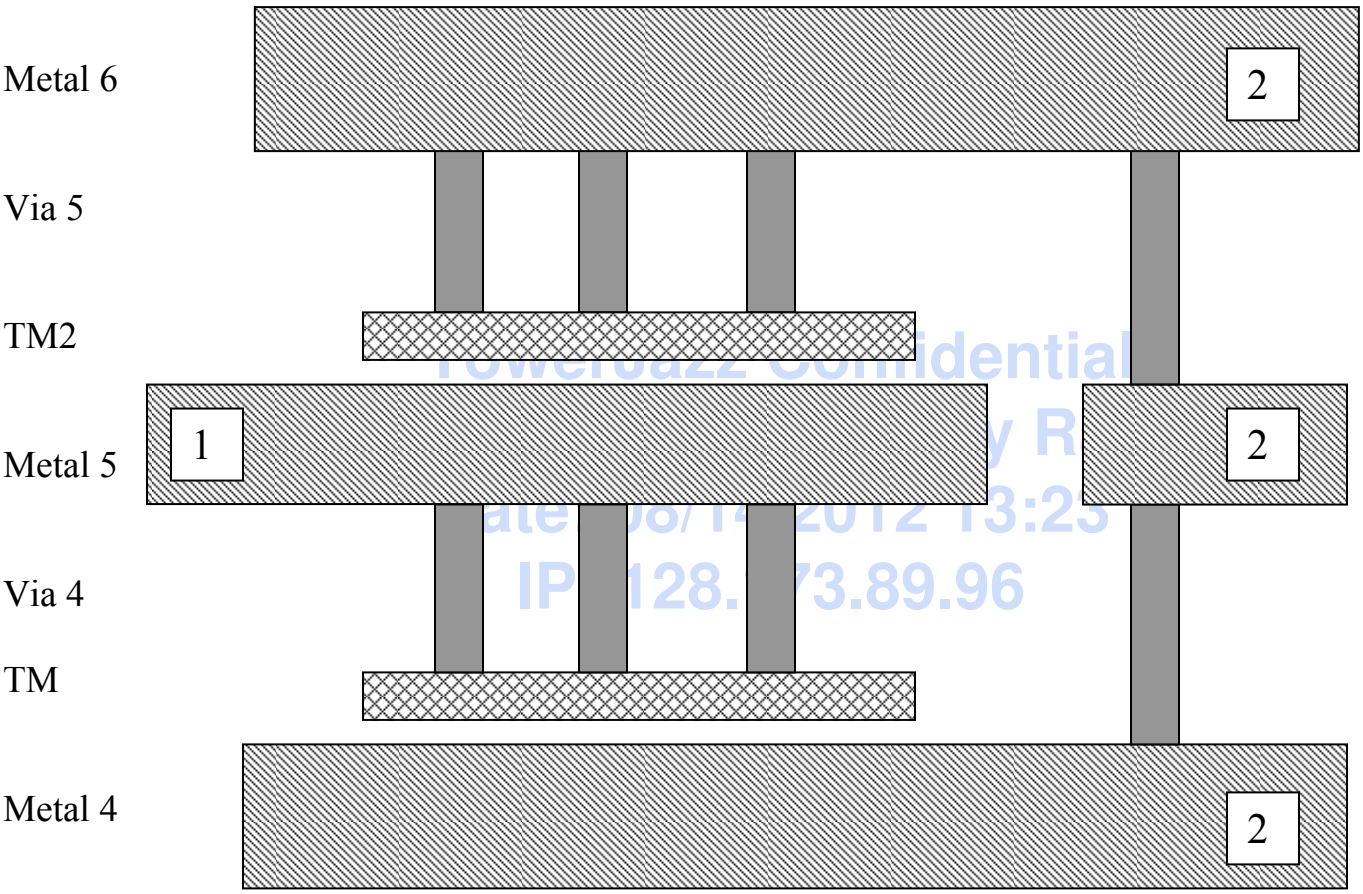


ILLUSTRATION MC2

5.2.3. Rules of 5.6fF/μm^2 density Stacked Metal-Insulator-Metal capacitor

This defines high unit area capacitor structures (Stacked MIM caps) fabricated using metal 4 (Layer 38) as the lower plate and top capacitor metal (TM, layer 22) as the upper plate of the bottom capacitor of the stacked capacitor and metal 5 (Layer 48) as the lower plate and top capacitor 2 metal (TM2, layer 30) as the upper plate of the upper capacitor of the stacked capacitor. Layer TM is connected to lower plate Metal 5 by an array of Via 4's and is one node of the capacitor (See Node 1 in the schematic below). Lower plate M4 is connected to related metal 6 (metal 6 connected to TM2 by an array of Via5) and is the second node of the capacitor (See Node 2 in the schematic below).



Schematic of the Stacked MIM capacitor

See Illustration SMC

Layer 22 and layer 30 are positive masks. Layer 30 is the additional mask layer needed in stacked MIM capacitors versus regular MIM capacitors between Metal 4 and TM. The stacked 5.6fF/μm^2 MIM capacitors have to be covered by marking layer 70.

Rule No.	Rule Name	CA13HC
SMC1	Minimum TM width/length	1.50
SMC2	Minimum TM Overplot of Via4, when via4 is on both TM and metal 4	0.50
SMC3	Minimum Space TM to Via4, when via4 is not over TM	0.50
SMC4	Minimum Overplot of Metal 4 to TM	1.00
SMC5	Minimum Space TM to TM	0.80
SMC9	Minimum via4 to via4 space on TM (for TM area > 400um^2)	3.50
SMC9.a	Minimum via4 to via4 space on TM (for TM area < 400um^2)	1.00
SMC10	Maximum via4 space on TM	4.50
SMC11	Minimum TM2 width/length	1.50
SMC12	Minimum TM2 Overplot of Via5, when via5 is on both TM2 and metal5	0.50
SMC13	Minimum Space TM2 to Via5, when via5 is not over TM2	0.50
SMC14	Minimum Overplot of Metal 5 to TM2	1.00
SMC15	Minimum Space TM2 to TM2	0.80
SMC19	Minimum via5 to via5 space on TM2 (for TM2 area > 400um^2)	3.50
SMC19.a	Minimum via5 to via5 space on TM2 (for TM2 area < 400um^2)	1.00
SMC20	Maximum via5 space on TM2	4.50

Rule No.	Rule Name	CA13HC
SMC21	Minimum Analog block border (layer 118/53) overplot of TM2*	2.00
SMC22	Minimum space capacitor TM to via3 (No Via3 is allowed below TM layer)	0.50
SMC24	Capacitor bottom plate metal 4 must be connected with related metal 6 (metal 6 connected to TM2)	
SMC25	TM2 and TM Polygons must be coincident WHENEVER TM and TM2 intersect. (e.g. Only two configurations allowed between TM2 and TM: (1) TM2 and TM are not overlapping or (2) TM2 and TM are coincident.).	

* Not shown in illustration SMC

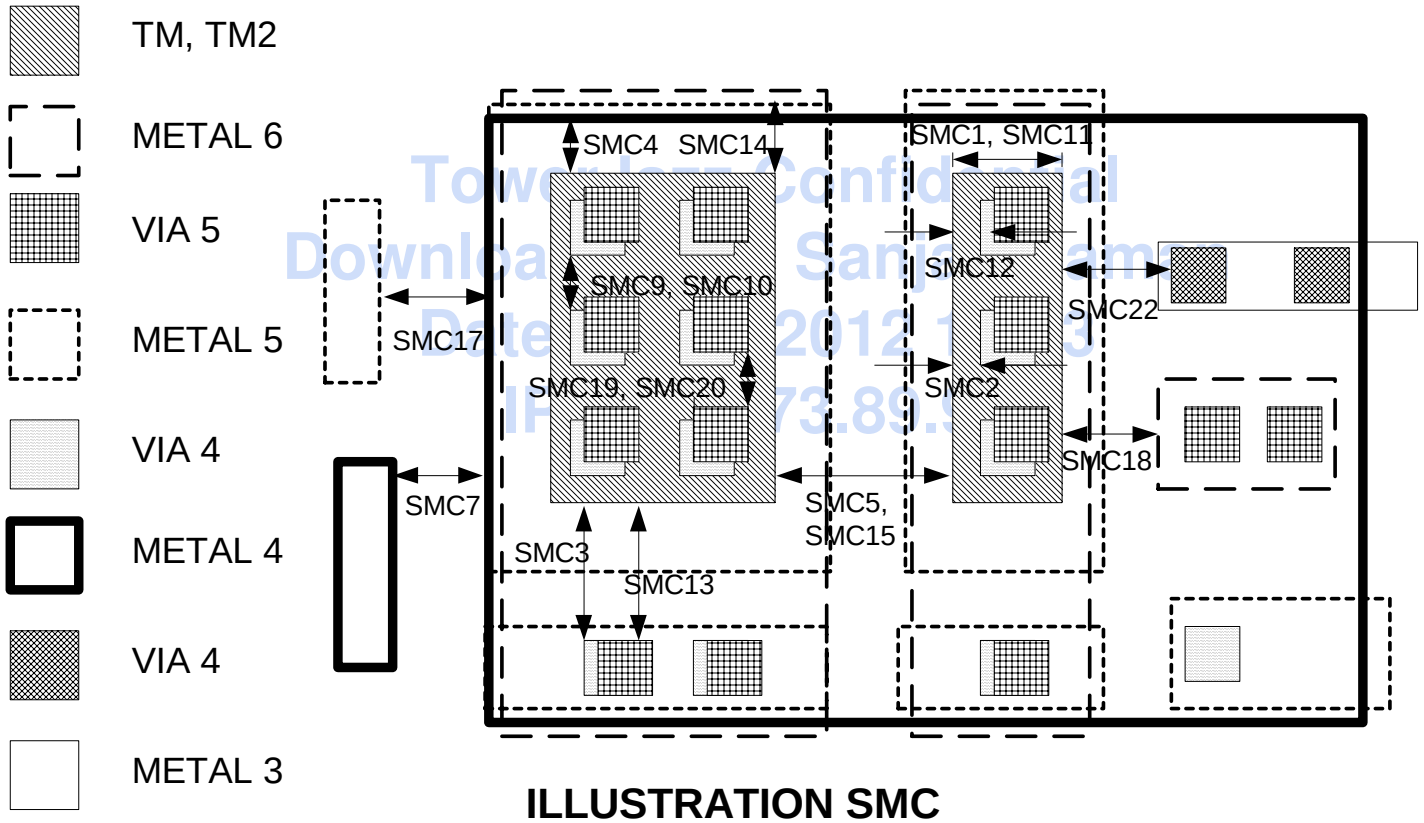


ILLUSTRATION SMC

5.3.

MOS Varactor

MOS varactor is an array of fixed size capacitors. The MOS varactors have to be covered with varactor marking layer (layer 118, Data type 50).

The MOS varactor uses the thick gate oxide.

Rule No.	Rule Name	CA13HC
MVAR.1.A	Minimum Gate length	0.36
MVAR.1.B	Maximum Gate length	2.0
MVAR.2a	Minimum Active width	2.0
MVAR.2b	Maximum Active width	8.0
MVAR.3	Minimum/Maximum spacing of gate to field edge	0.345
MVAR.4	Minimum NI overplot of active	0.18
MVAR.5	Minimum/Maximum N-well extension from active (along gate length)	0.20
MVAR.6	Minimum/Maximum N-well extension from active (along active width)	0.53
MVAR.7	Minimum/Maximum distance of active contact to gate poly	0.115
MVAR.8	Minimum/Maximum distance of gate contact to active edge	0.14
MVAR.9	Minimum width of metal 1 contacted to active	0.30
MVAR.10	Minimum width of metal 1 contacted to gate	0.19
MVAR.11	Minimum/Maximum active spacing between slices (not shown)	0.44
MVAR.12	Minimum/Maximum gate poly spacing between fingers (not shown)	0.39

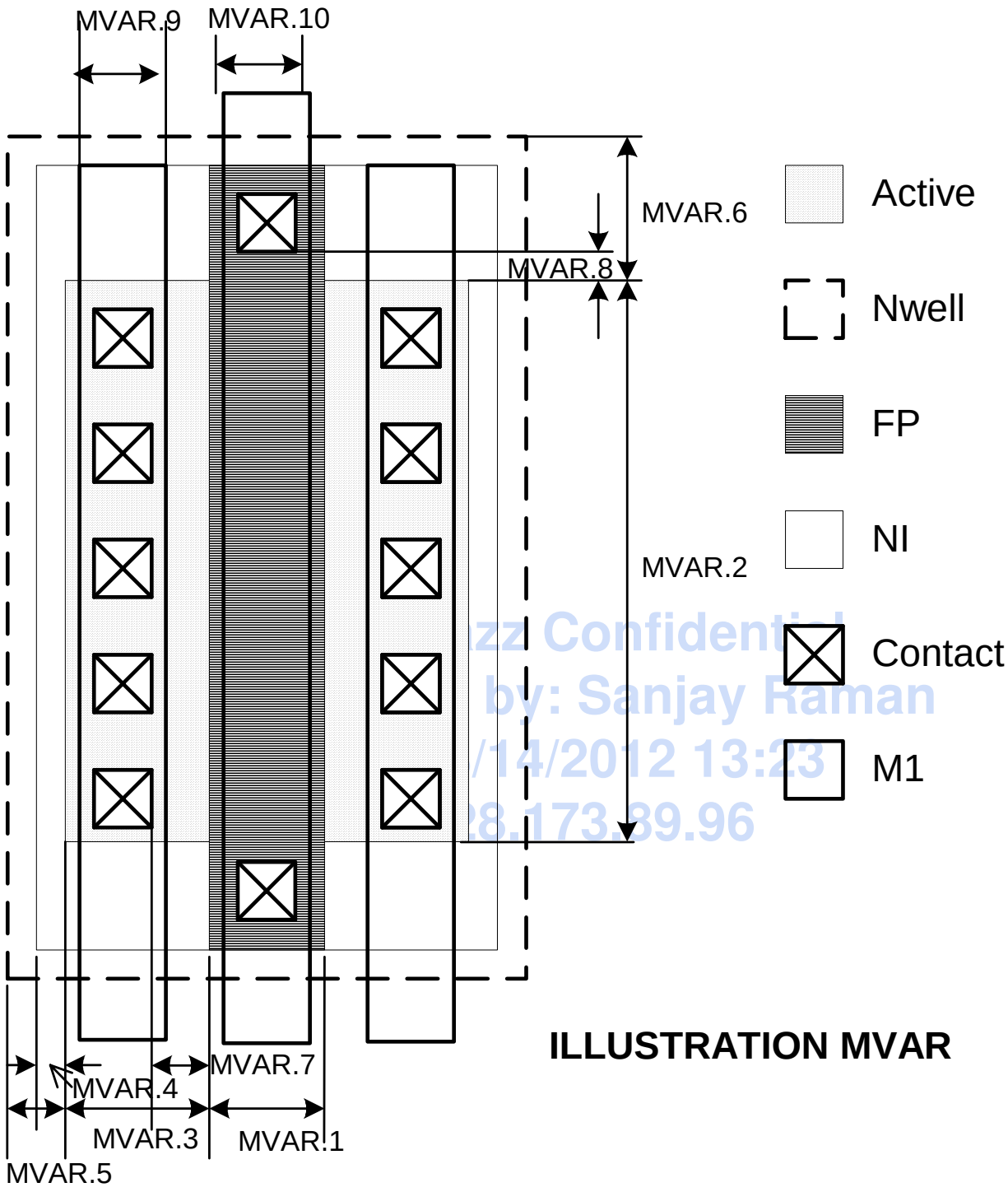


ILLUSTRATION MVAR

5.4. Inductors and Baluns

All inductors and baluns must be covered with inductor marking layer (layer 118/42). Layer 118/42 is used during layer generation to prevent any metal fill from being generated near inductors per the following.

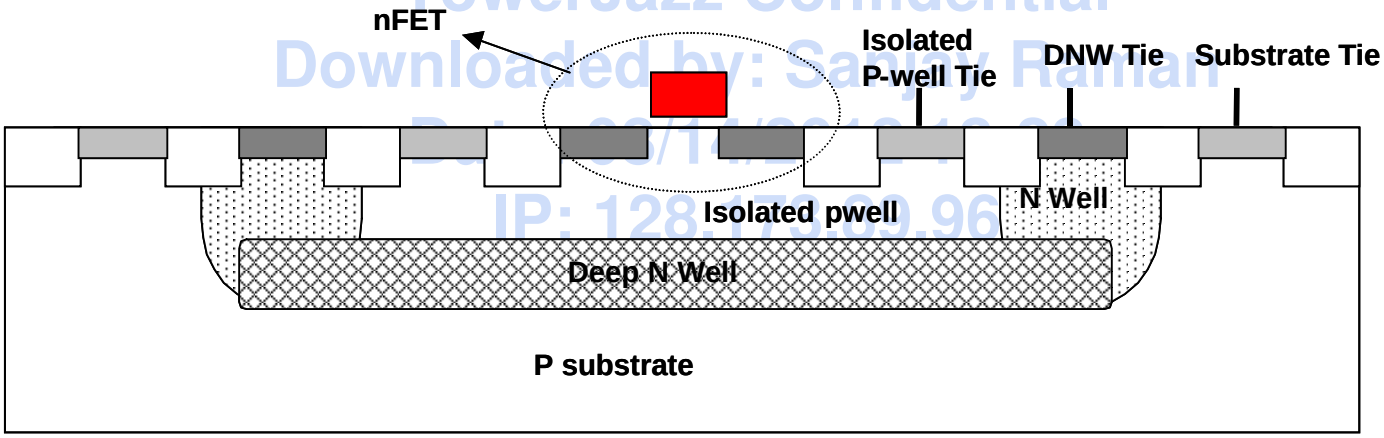
Rule No.	Rule Name	CA13
IML.A	IML overplot of Inductors.	5.00
IML.B	Minimum space IML to unrelated active, poly, metals, and TM.	25.00

Note: Inductor extent must be covered with analog block border (layer 118/53) also. See rule 94.F in Section 5.6 for pwell layer generation blocking

5.5. Deep Nwell "DNW" (Layer 36) [triple well fets]

The triple well process consists of an additional deep nwell layer using an additional N implant masking step in the p-substrate region. The deep nwell is surrounded by nwell. In this manner, an nFET can be isolated by the triple well consisting of deep nwell and surrounding nwell. In addition, the isolated pwell inside can be biased separately from the common p-substrate outside. See Illustration DNW.

The Deep N-well (DNW) mask, layer 36, is used to define the extents of the deep n well region. It is a negative mask and aligns to the zero layer. Isolated pwell by the Deep nwell/nwell can be biased separately using p+ taps. The substrate tie is located outside the deep nwell.



The DNW layer can be drawn around a circuit block or an element. This allows a different bias to be applied to the isolated pwell than the bias applied to the p-substrate. Inside the drawn DNW layer, the verification rules of the triple well process are implemented for DRC and LVS.

During schematic entry, the triple well may be implemented by specifying or wiring a secondary substrate net that is different from the local substrate. Any required biasing may then be applied to the secondary net that is different from the bias applied to the local substrate.

Rule No.	Rule name	CA13HC
DNW.1	Minimum width of DNW	3.0

DNW.2	Minimum space between DNW	10.0
DNW.3	Minimum NW overlap into the DNW	2.0
DNW.4	Minimum NW overlap out of the DNW	2.5
DNW.5	Minimum spacing of physically unrelated NW to DNW	6.0
DNW.6	DNW must be surrounded by NW	
DNW.7	A p+ tie must exist for each isolated pwell	
DNW.8	Each DNW extent must be connected to a n+ tie through its surrounding nwell	
DNW.9	Minimum space DNW to p_cell marking layer (118/62), vertical pnp marking layer (118/62), varactor marking layer (118/50)	6.0
DNW.10	Minimum isolated P-well to isolated P-well spacing for isolated p-wells at different potential	2.0
DNW.20	Latchup rule – Maximum space in X or Y directions between any point in an N+ active diffusion and its nearest isolated pwell p+ tie	10.0
DNW.21	Latchup rule – A substrate tie of > 0.25um^2 must be placed directly between an Nwell and any Nfet gate within 10um of the Nwell	
DNW.22	Following devices not allowed inside DNW: MOS varactor, native FET, Inductors, VPNP, Nwell resistor. Following devices are allowed inside DNW: 1.8V/3.3V/1.8V-high-Vt FETs, RFFETs, Polycaps, diodes, poly resistors, MIM caps	

5.6.

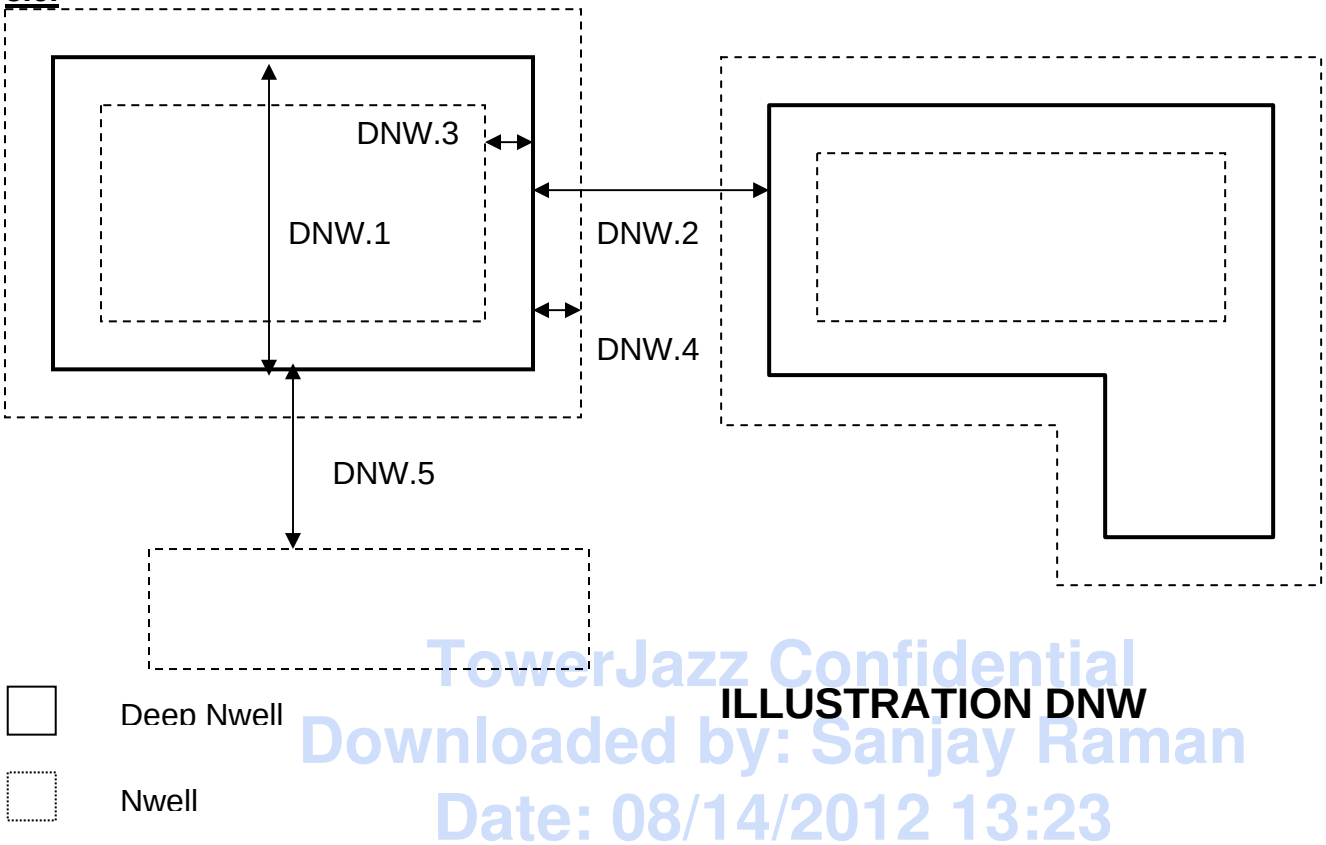


ILLUSTRATION DNW

3.3V Native NFETs (Coming soon - This device is currently not offered in CA13HC)

The native NFETs are very low threshold voltage FET devices. The natvimp marking layer (Layer 118/69) is used for LVS recognition of these devices. The native FET is a 3.3V device. The 3.3V native FET does not require any additional mask. Unlike the 3.3V standard nFET, the 3.3V native FET does not get the implants from the field mask layer.

See Section 3.5 for layer generation information

See Illustration 52 for rules

Rule No.	Rule name	
NATV.A	Minimum width of natvmrk layer	0.86
NATV.B	Minimum space natvmrk layer to natvmrk layer	0.86
NATV.C	Minimum/maximum natvmrk layer overplot of n+ active	0.26
NATV.D	Minimum space natvmrk layer to active	0.52
NATV.E	Minimum space natvmrk layer to Nwell	1.66
NATV.G	Minimum gate length of native FET for thick gate oxide oxide transistors (DG mask)	1.0
NATV.H	Minimum poly overlap of gate on field when gate active is within natvmrk layer	0.35
NATV.I	Number of active regions allowed within a natvmrk layer is one	
NATV.J	P+ implant layer is not allowed within natvmrk layer	
NATV.K	No bend gate is allowed within natvmrk layer	
NATV.L	All active area within natvmrk layer must be enclosed by DG layer	

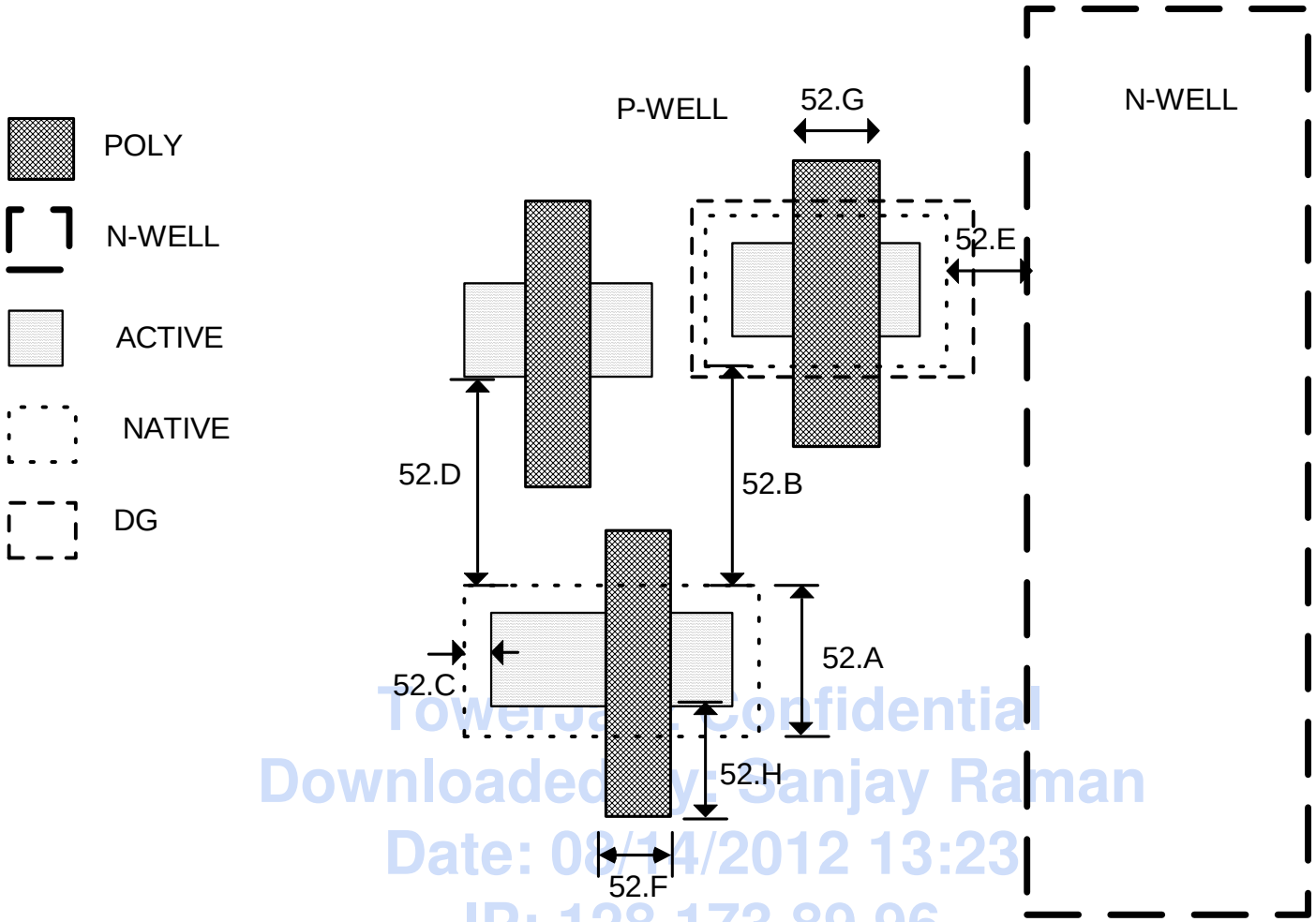


ILLUSTRATION 52

5.7.

Bipolar Vertical PNP Transistors

The parasitic vertical bipolar PNP transistors, for use in analog designs, are formed from a P+ diffusion in the N-well (emitter), an N-well (base) with an N+ diffusion guard-ring, and the P- substrate (collector) with a P+ diffusion ring. See figure BP. The vertical PNP must be enclosed by marking layer 118/62.

Rule No.	Rule Name	
BI.A	Minimum emitter size (P+ diffusion inside N-well). Emitter is always square.*	3.0 x 3.0
BI.B	Minimum spacing P+ emitter diffusion inside N-well to N+ base diffusion.	0.38
BI.C	Minimum N+ base diffusion width	0.42
BI.D	Minimum N-well overplot of N+ base diffusion (Same as rule 2.H)	0.12
BI.E	Minimum spacing N+ base diffusion to P+ collector diffusion in substrate	0.36
BI.F	Minimum P+ collector diffusion width	0.60
BI.G	N+ base diffusion must surround P+ emitter diffusion.	
BI.H	P+ collector diffusion must surround N+ base diffusion.	
BI.J	Maximum space contact to contact in the emitter, base and collector.	0.80

Note : Only the following emitter sizes are allowed 3x3 μm^2, 5.4x5.4 μm^2, 11x11 $\mu m^2$and 25x25 μm^2

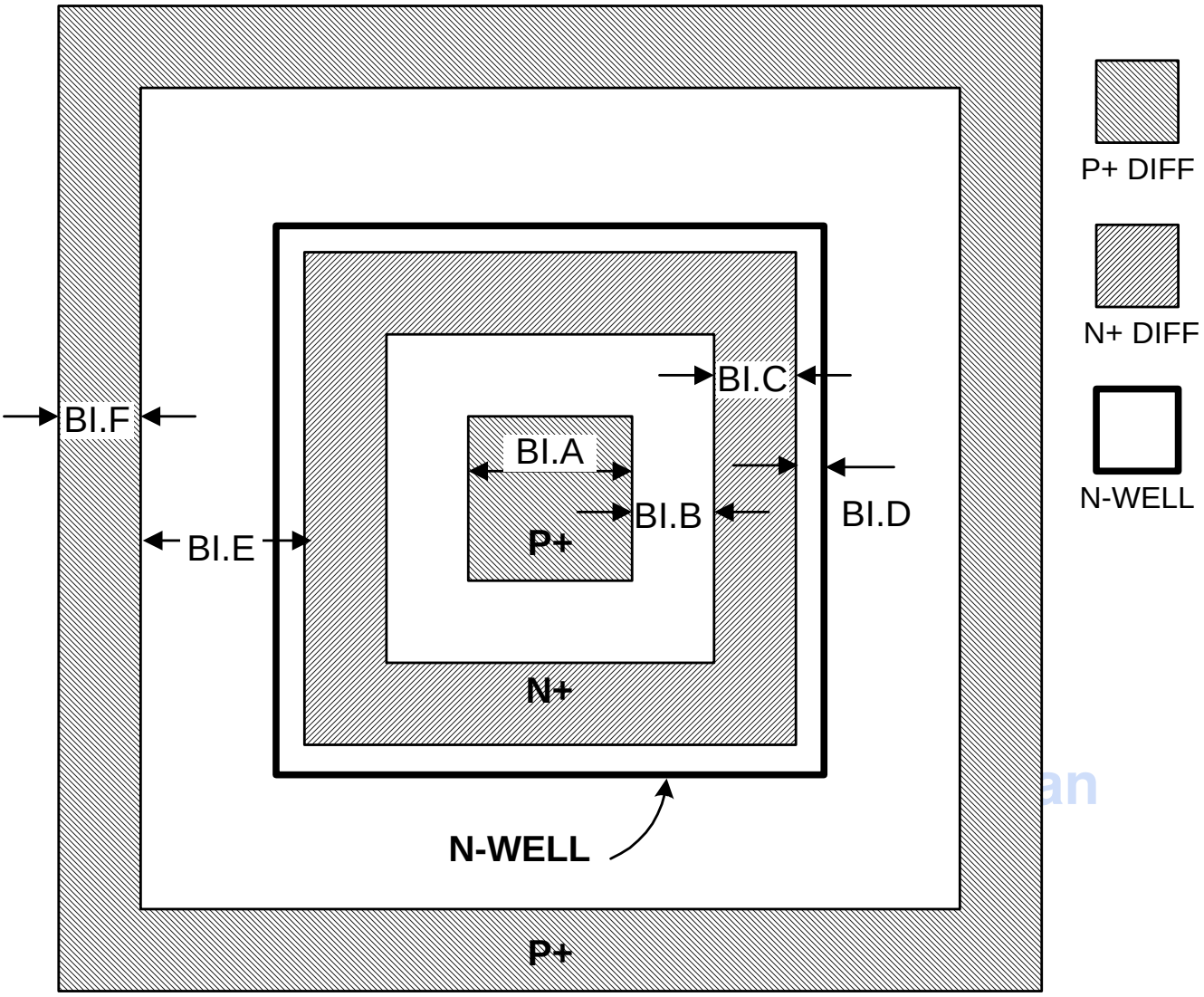


ILLUSTRATION BP

5.8. Metal overplot of contacts and vias for RF and Analog sections

These rules assure consistent low resistance contacts/vias for analog and RF designs. These rules apply only to regions inside the layer ABLB (118 datatype 53 region)

Rule No.	Rule Name	CA13HC	
OP.A	Metal 1 overplot of contact	0.07	um
OP.B	Metal 1 overplot of via1	0.07	um
OP.C	Metal 2 overplot of via1	0.07	um
OP.C	Metal 2 overplot of via2	0.07	um
OP.C	Metal 3 overplot of via2	0.07	um

OP.F	Metal 3 overplot of via3	0.07	um
OP.G	Metal 4 overplot of via3	0.08	um
OP.H	Metal 4 overplot of via4	0.15	um
OP.I	Metal 5 overplot of via4	0.15	um
OP.J	Metal 5 overplot of via5	0.15	um
OP.K	Metal 6 overplot of via 5	0.40	um
M1A	Minimum Metal 1 area	0.30	um^2
M2A	Minimum Metal 2 area	0.34	um^2
M3A	Minimum Metal 3 area	0.34	um^2
M4A	Minimum Metal 4 area	0.34	um^2
M5A	Minimum Metal 5 area	0.44	um^2
M6A	Minimum Metal 6 area	6.25	um^2

5.9.

P-Well Exclusion Rules

Layer PWE (layer 94) can be used to block field (pwell) implant under regions without shallow trench isolation and without any active devices. It can be applied inside or outside DG regions. PWE inside DG regions will affect layer generation of PWH while outside DG regions will affect PWL generation. See Sections 3.6 and 3.7 for field layer generation

Rule No.	Rule name	CA13HC
94.A	Minimum width of PWE layer (layer 94)	1
94.B	Minimum space PWE layer to PWE layer	1
94.C	Minimum space PWE layer (layer 94) to active (Note: PWE is not allowed on drawn active)	1
94.D	Minimum space PWE layer (layer 94) to nwell	2
94.E	No dnw is allowed within PWE layer	
94.F	PWE layer (layer 94) must be coincident with IML (layer 118, datatype 42)	
94.G	Generated dummy active fill inside PWE must be covered by silicide block (this is a post layer generation rule check)	

* PWE layer may be drawn without enclosing IML.
** At present, the PWE layer is allowed for processes with inductors only.

Note: Jazz models have not been verified when PWE layer is present. Customers may use PWE layer (layer 94) at their own risk.

5.10. Metal Pin Layer Rules

These rules are applicable for the metal Pin layers

Rule No.	Rule Name
8.Pin	Metal 1 Pin layer must be covered by metal 1 drawing layer
18.Pin	Metal 2 Pin layer must be covered by metal 2 drawing layer
28.Pin	Metal 3 Pin layer must be covered by metal 3 drawing layer
38.Pin	Metal 4 Pin layer must be covered by metal 4 drawing layer
48.Pin	Metal 5 Pin layer must be covered by metal 5 drawing layer
58.Pin	Metal 6 Pin layer must be covered by metal 6 drawing layer

5.11. Metal enclosure rules for GDS different data-types

These rules are applicable for the metal GDS data-types with an exception of data-type "31" (customer metal fill) and datatype 30 (metal fill block). These rules will prevent accidental use of alternate data-types by a user that would potentially cause product to fail due to incomplete design rule check.

Rule No.	Rule Name
8.ENCL	All Metal1 GDS data-types, with an exception of data-type 31 (customer metal fill) and datatype 30 (metal fill block) must be enclosed by data-type "0"
18.ENCL	All Metal2 GDS data-types, with an exception of data-type 31 (customer metal fill) and datatype 30 (metal fill block) must be enclosed by data-type "0"
28.ENCL	All Metal3 GDS data-types, with an exception of data-type 31 (customer metal fill) and datatype 30 (metal fill block) must be enclosed by data-type "0"
38.ENCL	All Metal4 GDS data-types, with an exception of data-type 31 (customer metal fill) and datatype 30 (metal fill block) must be enclosed by data-type "0"
48.ENCL	All Metal5 GDS data-types, with an exception of data-type 31 (customer metal fill) and datatype 30 (metal fill block) must be enclosed by data-type "0"
58.ENCL	All Metal6 GDS data-types, with an exception of data-type 31 (customer metal fill) and datatype 30 (metal fill block) must be enclosed by data-type "0"

6. Stress Relief Rules

6.1. Metal Stress Relief Rules

Stress relief rules are additional metal rules that reduce stress effects. The inserted slits should be aligned with the long axis parallel to the metal line. The inserted slits should be aligned with the long axis parallel to the metal line. These rules do not apply to metal within 17 microns of pad metal. See Illustration ST.

Rule No.	Rule Name		CA13HC
ST.A	Maximum metal bus width without adding slits		30
ST.B	Maximum spacing between coaxial metal slits (recommended minimum = 10um)		25
ST.C	Minimum slit width:	a) metal 1	1.0
		b) metal 2	1.0
		c) metal 3	1.0
		d) metal 4	1.0
		e) metal 5	1.0

		f) metal 6	2.0
ST.E	Minimum spacing from chip corner (defined by pad edges) to metal 1, metal 2, metal 3, metal 4, metal 5 or metal 6 when die size is > 25mm^2		275
ST.E.1	Minimum spacing from chip corner to metal 1, metal 2, metal 3, metal 4, metal 5 or metal 6 when die size is ≤ 25mm^2.		125
ST.E.2	Minimum spacing from chip corner to metal 1, metal 2, metal 3, metal 4, metal 5 or metal 6 is 150um when die size is ≤ 25mm^2 for CA13HC		
ST.F	Metal at the chip corners should be at an angel of 45 degrees. These corners may be designed by using stair-stepped polygons with sides of about 5um per step.		
ST.G	No active circuitry (active layer, poly) is allowed within a square area 200um X 200um from chip corner when die size > 25mm^2.		
ST.G.1	No active circuitry (active layer, poly) is allowed within a square area 125um X 125um from chip corner when die size ≤ 25mm^2		
ST.I	Minimum space between any slit and metal edge		10

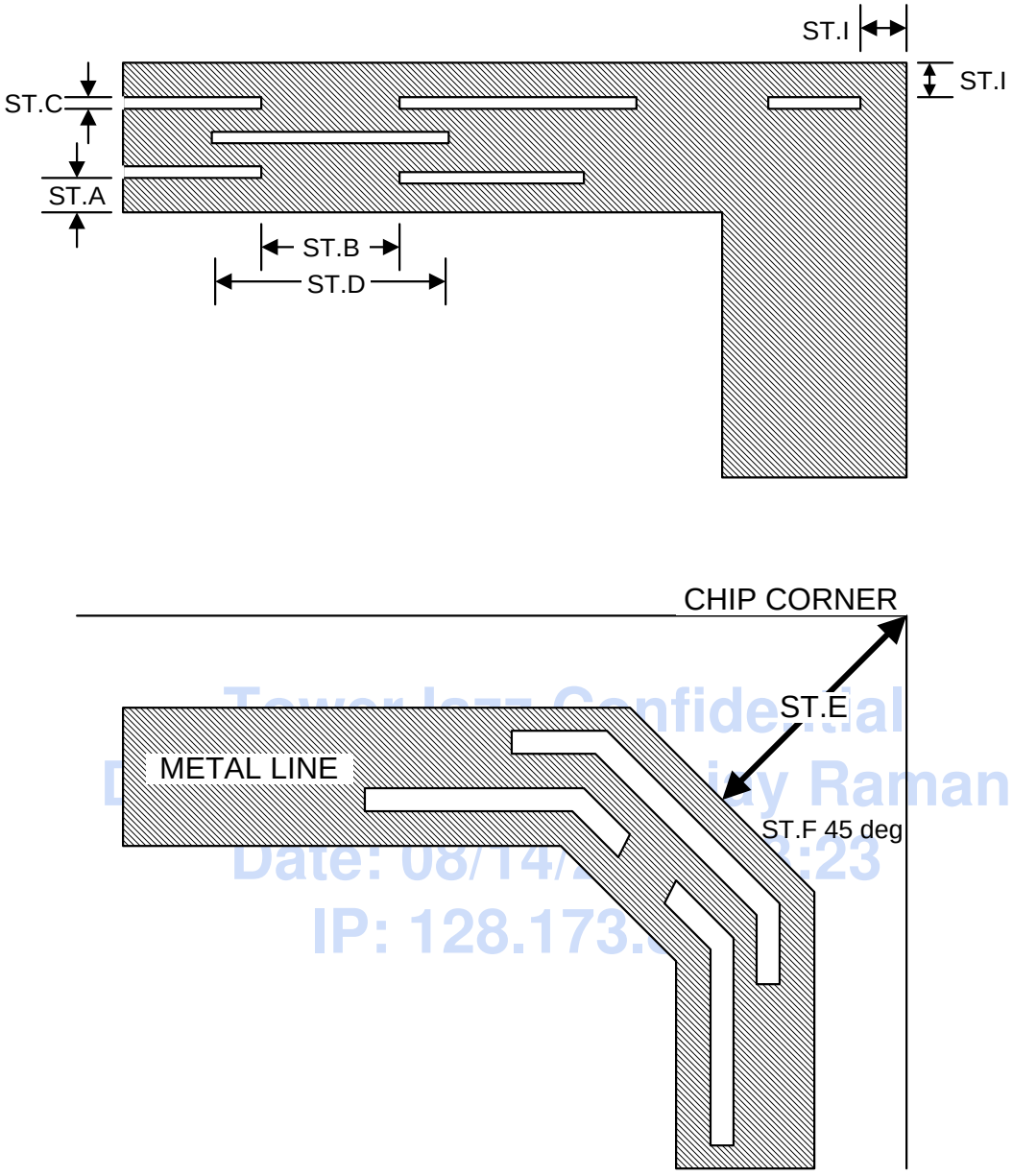


ILLUSTRATION ST

6.2.

Capacitor Stress Relief Rules (Not shown)

The stress relief rules of the MIM capacitor, built on M4 only using TM, are described below

Rule No.	Rule Name	
MC12	Capacitor TM space to die edge	>100
MC13*	Maximum width of bottom metal of capacitor where either die size x or y dimension < 6350um	250 um
MC14*	Maximum width of bottom metal of capacitor where both die size x and y dimension > 6350um	200 um
MC15	Maximum width of TM where either die size x or y dimension < 6350um	250 um
MC16	Maximum width of TM where both die size x and y dimension > 6350um	200 um

* The standard Metal stress relief rules apply beyond the capacitor extent

The stress relief rules of the MIM capacitor, built on M5 only using TM2, are described below

Rule No.	Rule Name	
MC2_12	Capacitor TM space to die edge	>100
MC2_13*	Maximum width of bottom metal of capacitor where either die size x or y dimension < 6350um	250 um
MC2_14*	Maximum width of bottom metal of capacitor where both die size x and y dimension > 6350um	200 um
MC2_15	Maximum width of TM where either die size x or y dimension < 6350um	250 um
MC2_16	Maximum width of TM where both die size x and y dimension > 6350um	200 um

* The standard Metal stress relief rules apply beyond the capacitor extent

The stress relief rules of the stacked MIM capacitor, built using TM and TM2, are described below

Rule No.	Rule Name	
SMC41	Minimum space capacitor TM to die edge	100 um
SMC42*	Maximum width of bottom metal 4 of capacitor	200 um
SMC43	Maximum width of TM	200 um
SMC44	Minimum space capacitor TM2 to die edge	100 um
SMC45*	Maximum width of bottom metal 5 of capacitor	200 um
SMC46	Maximum width of TM2	200 um

7. Bonding Pad Design Rules

This section gives the rules for designing bonding pads and their relationships to nearby and connecting conductors.

All customers must have their pad designs and layout verified and approved by their packaging vendor prior to pad layout.

CA13HC may have four types of pads. The Jazz wire bonding pads are marked with layer 74 only and should follow the rules in Section 8.1. The custom wire bond pads (not marked with layer 74 or layer 96) should follow rules of Section 8.2. The Jazz bump pads are marked with layer 96 and layer 74. The custom bump pads are marked with layer 96 only and should follow rules of Section 8.3.

7.1. Jazz Wire Bond Pads

Notes:

1) The CA13HC wire bond pads do not contain any metal 1, metal 2, metal 3, via1s, or via2s. The pads are composed of metal 4 only in quadruple level metal designs, metal 5 only in five level metal designs and metal 6 only in six level metal designs.

2) The minimum pad pitch is 63um. However, Jazz assembly house and probing house is not qualified yet for 63um pads. Customers must qualify their own assembly and probing house.

7.1.1. Jazz Rectangular Wire Bond Pads

This section describes rules for Jazz rectangular wire bond pads. See illustration BD . These pads are also used in jazz digital I/O cells.

Rule No.	Rule Name		
		80um pad pitch	63um pad pitch
BD.A.a	Minimum/maximum bond pad opening in protective overcoat layer for single pads. The narrow dimension must be parallel to the chip edge.	105 x 66	94 X 51
BD.A.b	Minimum/maximum bond pad opening in protective overcoat layer for double pads. The long dimension must be parallel to the chip edge.	105 x 132	94 X 102
BD.B	Minimum spacing bond pad opening to bond pad opening	14	9
BD.B.a	Minimum spacing bond pad opening to bond pad opening for CA13HC only	14	12
BD.D.a	Minimum pad metal overplot of pad opening for the dimension perpendicular to the chip edge	4.0	3.0
BD.D.a.1	Maximum pad metal overplot of pad opening (except pad to circuit side)	7.0	3.0

Rule No.	Rule Name		80um pad pitch	63um pad pitch
BD.F	Minimum spacing pad metal to pad metal		6	6
BD.H	Minimum space between pad metal (s) and:			
		a) unrelated poly	10	9
		b) unrelated metal 1	10	9
		c) unrelated metal 2	10	9
		d) unrelated metal 3	10	9
		e) unrelated metal 4	10	9
		f) unrelated metal 5	10	9
		g) unrelated metal 6	10	9
		h) related metal 1	10	9
		i) related metal 2	10	9
		j) related metal 3	10	9
		k) related metal 4	10	9
		l) related metal 5	10	9
		m) related metal 6	10	9
		n) via1	10	9
		o) via2	10	9
		p) via3	10	9
		q) via4	10	9
		r) via5	10	9
BD.J.a	Minimum width of metal 1, metal 2 ,metal 3, metal 4, metal 5, metal 6 connected to and within 10um of the pad (measured parallel to the pad edge)		42	42
BD.L	Minimum spacing between metal connections to the pad and a corner of the bonding pad.		6	6
BD.M.a	All bonding pads shall consist of at least 3 pad corners (defined in rule BD.L)			

Rule No.	Rule Name		
		80um pad pitch	63um pad pitch
BD.M.b	OR bonding pads shall consist of at least two pad corners (as defined in rule BD.L) and an opposite edge length (L) without connections	L=6	L=6
BD.N	Pad metal(s) must have a direct connection to diffusion or a tie.		

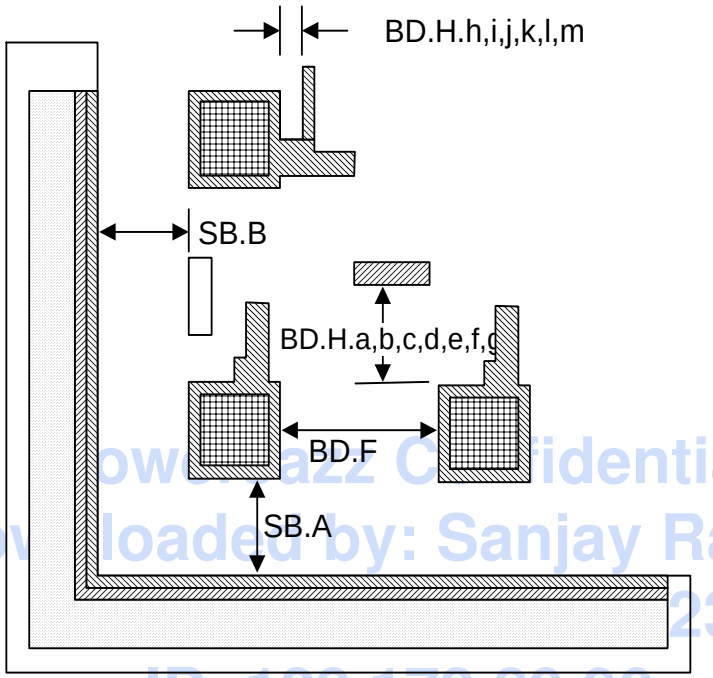


ILLUSTRATION BD

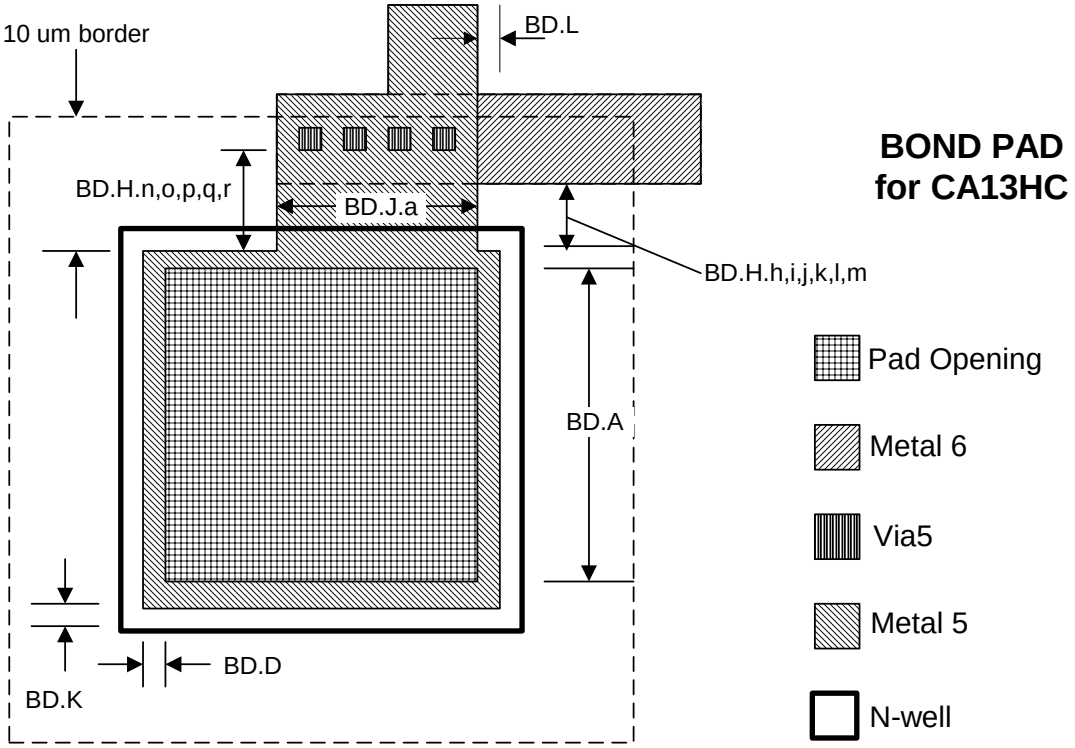


ILLUSTRATION BD (continued)

7.1.2. Jazz Octagonal Wire Bond Pads

This section describes rules for octagonal wire bond pads enclosed with Jazz pad marking layer. See illustration OBD.

Rule No.	Rule Name	
OBD.A	Minimum/Maximum center portion pad opening in the Y direction	59
OBD.B	Minimum/Maximum total pad opening in the Y direction	105
OBD.C	Minimum top metal overplot pad opening.	4
OBD.D	Minimum/Maximum top/bottom portion pad opening in the Y dimension	23
OBD.E	Minimum/Maximum top edge/bottom edge pad opening in the X dimension	20
OBD.F	Minimum/Maximum center portion pad opening in the X dimension	66
OBD.G	Minimum/Maximum width of top metal connecting metal pad to pad border.	23.4
OBD.H	Minimum (floating) N-well extension beyond pad metal. Reliability guideline: A floating well must be used under bonding pads to reduce the likelihood of leakage from pad to substrate caused by cracking of the dielectric between the pad metal and the substrate.	2

Notes:

1) The bonding pads are composed of metal 6 in the CA13HC process

2) For the purpose of defining design rules, the octagonal opening is divided into three sections, top, center and bottom (See OBD).

3) The Y dimension is along the longer axis, the X dimension is along the short axis of the pad.

6) Bond pad rules BD.B to BD.N in the previous section apply to octagonal pad layout.

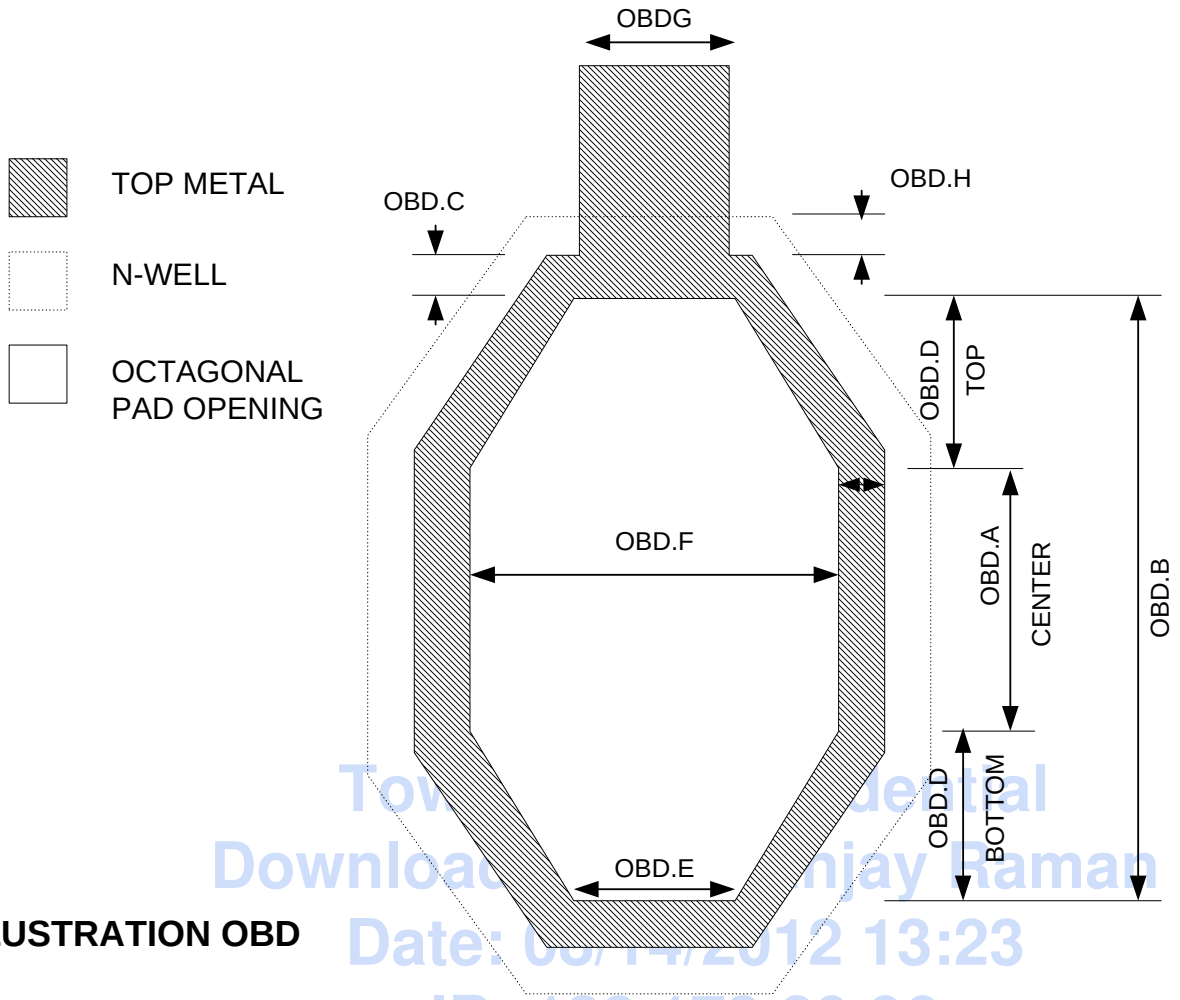


ILLUSTRATION OBD

7.2.

Custom Wire Bond Pads

These rules are applied when the Jazz pad marking layer (layer 74) or the bump pad marking layer (layer 96) does not cover the pad. Custom wire bond pads may be made using the guidelines provided in this section.

Rule No.	Rule Name	
BD.1	Minimum width of bond pad opening.	6
BD.2	Maximum width of bond pad opening.	140
BD.3	Only 90 degree and 135 degree inside corners are allowed for pad opening	
BD.4	Maximum area of bond pad opening per pad	15,000
BD.5	Minimum pad metal overplot opening	3
BD.5.a	Maximum pad metal overplot opening	5
BD.6	Minimum spacing pad metal to pad metal	6

The following rules are recommended and are not checked.

Rule No.	Rule Name	
BD.7	Minimum width of any metal or poly connected to and within 13um of the pad opening (unchecked rule)	12
BD.8	Minimum space between pad opening and unrelated poly, and metal layers other than top metal. The top metal is the same metal layer as pad metal layer (unchecked rule)	8
BD.9	Minimum space between bond pad opening and non-pad-metal top metal (unchecked rule).	13
BD.10	No vias or contacts are allowed below pad opening (unchecked rule)	
BD.11	Layers used to provide shielding for RF applications, such as Metal1, poly, and active must enclose the pad opening (unchecked rule)	
BD.12	In the absense of any shielding layers, Nwell must be present below the pad. Minimum (floating) N-well extension beyond pad metal = 0.5um (unchecked rule)	
BD.13	Pad metal(s) must have a direct connection to diffusion or a tie (unchecked rule)	

7.3.

Custom Bump Pads

These rules are applied when the bump pad marking layer (layer 96) covers the pad and the Jazz pad marking layer (layer 74) does not cover the pad. Custom bump pads may be made using the guidelines provided in this section.

Rule No.	Rule Name	
BMP.1	Minimum width of bump pad opening.	6
BMP.2	Maximum width of bump pad opening.	140
BMP.3	Maximum area of bump pad opening per pad	15,000
BMP.4	Minimum pad metal overplot of bump pad opening	3
BMP.5	Maximum pad metal overplot bump pad opening	25
BMP.6	Minimum N for N-sided polygonal bump pad opening (Circular bump pad opening is recommended)	8 (octagonal)
BMP.7	All sides of the polygonal bump pad opening must have the same length	

The following rules are recommended and are not checked.

Rule No.	Rule Name	
BMP.8	No top via allowed below bump pad opening	
BMP.9	Minimum spacing pad metal to pad metal (unchecked rule)	10
BMP.10	Minimum width of any metal or poly connected to and within 10um of the bump pad opening (unchecked rule)	12
BMP.11	Minimum space between bump pad metal and non-pad-metal top metal (unchecked rule).	5
BMP.12	Pad metal(s) must have a direct connection to diffusion or a tie (unchecked rule)	

8.

Antenna Rules

8.1. Restriction of Polysilicon and Metal Areas on Field

Poly, metal 1, metal 2, metal 3, metal 4 and metal 5 conductors over field have restrictions. These restrictions are for 1) total area, and 2) ratio of conductor area to gate area provided:

A. the conductors on field are not connected to a diffusion (or tie) directly or through a previous (not subsequent) conductor layer or
B. the conductors on field are connected to a diffusion (or tie) of specific area directly or through a previous (not subsequent) conductor layer (Rules AN.H)
C. and the conductors of A) or B) above are attached to a channel area (poly on active) either directly or through a previous layer.

The term "antenna area" is used to refer to the total conductor area of that layer that meets the conditions A) or B) and C) above a) on field and channel for poly antennas or b) total conductor area for all metal layers. The term connected total gate area refers to the total channel area connected either directly or indirectly to an antenna.

Rules AN.G and AN.H use the following definitions for antenna perimeter area:

- Antenna perimeter area= 2 * (Length + Width) * thickness
- Using: poly thickness=1750A, M1 thickness = 4200A, M2 to Mn-1 thickness=5200A, Top metal thickness=28100A

See Illustration AN.

Rule	Rule Name	CA13HC	
AN.A	Maximum poly area of poly antenna	15,000	um^2
AN.B	Maximum metal 1 area of metal 1 antenna	15,000	um^2
	(It is highly recommended that all poly antennas be connected by metal 1 to diffusion, i.e. eliminating as many as possible poly and metal 1 antennas.)		
AN.C.a	Maximum metal 2 area of metal 2 antenna	15,000	um^2
AN.C.b	Maximum metal 3 area of metal 3 antenna	15,000	um^2
AN.C.c	Maximum metal 4 area of metal 4 antenna	15,000	um^2
AN.C.d	Maximum metal 5 area of metal 5 antenna	15,000	um^2
AN.C.e	Maximum metal 6 area of metal 6 antenna	0	um^2
AN.D	Maximum ratio of poly area of poly antenna to connected total gate area	35	
AN.E.a	Maximum ratio of metal 1 antenna area to total connected gate area (without a protection diode)	200	
AN.E.b	Maximum ratio of metal 2 antenna area to total connected gate area (without a protection diode)	200	
AN.E.c	Maximum ratio of metal 3 antenna area to total connected gate area (without a protection diode)	200	
AN.E.d	Maximum ratio of metal 4 antenna area to total connected gate area (without a protection diode)	200	

AN.E.e	Maximum ratio of metal 5 antenna area to total connected gate area (without a protection diode)	200	
AN.E.f	Maximum ratio of metal 6 antenna area to total connected gate area (without a protection diode)	0	
AN.F	Maximum ratio of poly perimeter area of poly antenna to connected total gate area	200	
AN.G.a	Maximum accumulative ratio of metal 1 perimeter area to total connected gate area (without a protection diode or if the diode area is < 0.58x0.58um^2)	400	
AN.G.b	Maximum accumulative ratio of metal 2 perimeter area to total connected gate area (without a protection diode or if the diode area is < 0.58x0.58um^2)	400	
AN.G.c	Maximum accumulative ratio of metal 3 perimeter area to total connected gate area (without a protection diode or if the diode area is < 0.58x0.58um^2)	400	
AN.G.d	Maximum accumulative ratio of metal 4 perimeter area to total connected gate area (without a protection diode or if the diode area is < 0.58x0.58um^2)	400	
AN.G.e	Maximum accumulative ratio of metal 5 perimeter area to total connected gate area (without a protection diode or if the diode area is < 0.58x0.58um^2)	400	
AN.G.f	Maximum accumulative ratio of metal 6 perimeter area to total connected gate area (without a protection diode or if the diode area is <=0.58x0.58um^2)	0	
AN.H.a	Maximum accumulative ratio of metal 1 perimeter area to total connected gate area, if a diode > 0.58x0.58um^2 is connected.	400* (diode area-.5) +2400	
AN.H.b	Maximum accumulative ratio of metal 2 perimeter area to total connected gate area, if a diode >= 0.58x0.58um^2 is connected.	400* (diode area-.5) +2400	
AN.H.c	Maximum accumulative ratio of metal 3 perimeter area to total connected gate area, if a diode >= 0.58x0.58um^2 is connected.	400* (diode area-.5) +2400	
AN.H.d	Maximum accumulative ratio of metal 4 perimeter area to total connected gate area, if a diode >= 0.58x0.58um^2 is connected.	400* (diode area-.5) +2400	
AN.H.e	Maximum accumulative ratio of metal 5 perimeter area to total connected gate area, if a diode >= 0.58x0.58um^2 is connected.	400* (diode area-.5) +2400	
AN.H.f	Maximum accumulative ratio of metal 6 perimeter area to total connected gate area, if a diode >= 0.58x0.58um^2 is connected.	400* (diode area-.5) +2400	

8.2.

Restriction of Number of Contacts and Vias Attached to the Gate

The total number of contacts, via 1, via 2, via 3, via 4, and via 5 over poly, metal 1, metal 2, metal 3, metal 4 and metal 5 conductors respectively, have restrictions on the ratio of contact/via area to gate area. These restrictions apply provided:

A. the contacts/vias are not connected to a diffusion (or tie) directly or through a previous (not subsequent) conductor layer or
B. the contacts/vias are connected to a diffusion (or tie) of specific area directly or through a previous (not subsequent) conductor layer (Rules AN.K)
C. the contacts/vias of A) or B) above are attached to a channel area (poly on active) either directly or through a previous layers (applicable to bond pads also).

The term antenna area is used to refer to the total contact or via area of that layer that meets the conditions A) or B) and C) above. The term connected total gate area refers to the total channel area connected either directly or indirectly to a contact/via intensive antenna.

Rule No.	Rule Name	CA13HC
AN.I	Maximum ratio of total contact antenna area to total connected gate area	10
AN.J.a	Maximum ratio of total via1 antenna area to total connected gate area when no protection diode is used.	20
AN.J.b	Maximum ratio of total via2 antenna area to total connected gate area when no protection diode is used.	20
AN.J.c	Maximum ratio of total via3 antenna area to total connected gate area when no protection diode is used.	20
AN.J.d	Maximum ratio of total via4 antenna area to total connected gate area when no protection diode is used.	20
AN.J.e	Maximum ratio of total via5 antenna area to total connected gate area when no protection diode is used.	20
AN.K.a	Maximum ratio of total via1 antenna area to total connected gate area, if a protection diode >= 0.58x0.58um^2 is implemented	83.3* (diode area–2.7) +300
AN.K.b	Maximum ratio of total via2 antenna area to total connected gate area, if a protection diode >= 0.58x0.58um^2 is implemented	83.3* (diode area–2.7) +300
AN.K.c	Maximum ratio of total via3 antenna area to total connected gate area, if protection a diode >= 0.58x0.58um^2 is implemented	83.3* (diode area–2.7) +300
AN.K.d	Maximum ratio of total via4 antenna area to total connected gate area, if a protection diode >= 0.58x0.58um^2 is implemented	83.3* (diode area–2.7) +300
AN.K.e	Maximum ratio of total via5 antenna area to total connected gate area, if a protection diode >= 0.58x0.58um^2 is implemented	83.3* (diode area–2.7) +300

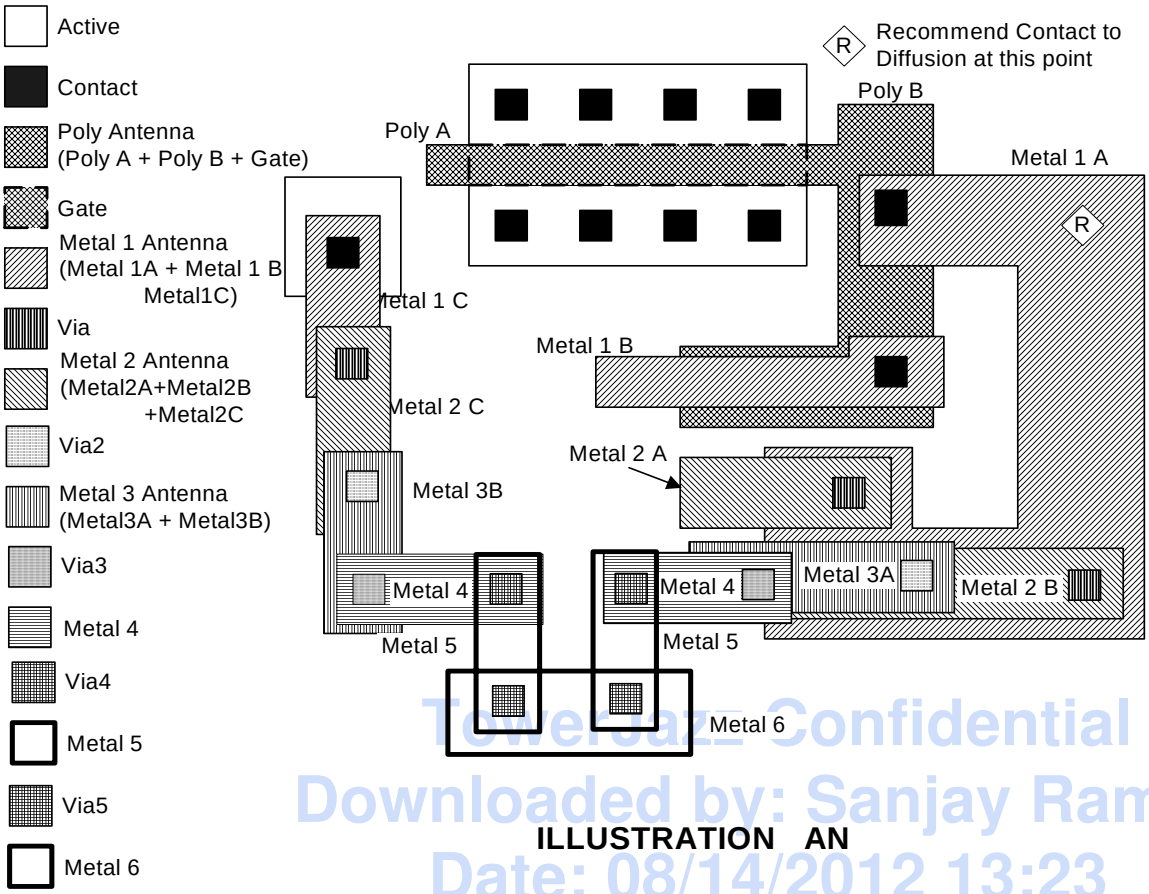


ILLUSTRATION AN

8.3. Special Antenna Rules for MIM Capacitors

Poly, metal 1, metal 2, metal 3, metal 4, and metal 5 conductors over field have restrictions on 1) total area, and 2) ratio of conductor area to TM area provided A) the conductors on field are not connected to a diffusion (or tie) directly or through a previous (not subsequent) conductor layer and B) the conductors are attached to a capacitor area (TM on metal 4) either directly or through a previous layer. The term antenna area is used to refer to the total conductor area of that layer that meets the conditions A) and B) above.

Antenna rules for single layer MIM capacitor (2.8 ff/um2) on M4

Rule No.	Rule Name	CA13HC
SA.0	Maximum ratio of metal 2 antenna connected to the intersection of the Metal 4 bottom capacitor plate and TM. See Note 3	N/A

SA.1	Maximum ratio of metal 3 antenna area to total connected TM area or to the intersection area of Metal 4 bottom capacitor plate and TM. See Note 3	N/A
SA.2	Maximum ratio of metal 4 antenna area to total connected TM area or to the intersection area of Metal 4 bottom capacitor plate and TM. See Note 3	20
SA.3	Maximum ratio of metal 5 antenna area to total connected TM area or to the intersection area of Metal 4 bottom capacitor plate and TM. See Note 3	20
SA.4	Maximum ratio of metal 6 antenna area to total connected TM area or to the intersection area of Metal 4 bottom capacitor plate and TM. See Note 3	0

Note 3: The connecting path from the metal antenna layer to the MIM capacitor should include all connecting paths through metal layers metal 6, metal 5, metal 4, metal 3, metal 2, metal 1, and poly, which are not protected by diodes.

Antenna rules for single layer MIM capacitor (2.8 ff/um2) on M5

Rule No.	Rule Name	CA13HC
SA2.0	Maximum ratio of metal 2 antenna connected to the intersection of the Metal 4 bottom capacitor plate and TM2. See Note 3 above	N/A
SA2.1	Maximum ratio of metal 3 antenna area to total connected TM2 area or to the intersection area of Metal 4 bottom capacitor plate and TM2. See Note 3 above	N/A
SA2.2	Maximum ratio of metal 4 antenna area to total connected TM2 area or to the intersection area of Metal 4 bottom capacitor plate and TM2. See Note 3 above	N/A
SA2.3	Maximum ratio of metal 5 antenna area to total connected TM2 area or to the intersection area of Metal 4 bottom capacitor plate and TM2. See Note 3 above	20

SA2.4	Maximum ratio of metal 6 antenna area to total connected TM area or to the intersection area of Metal 4 bottom capacitor plate and TM. See Note 3	0

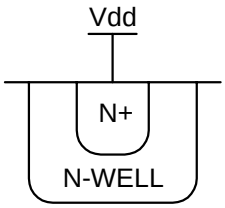
Antenna rules for stacked MIM capacitor (5.6 ff/um2)

Rule No.	Rule Name	CA13HC
SMA.2	Maximum ratio of metal 4 antenna area to total connected TM2 area.	N/A
SMA.3	Maximum ratio of metal 5 antenna area to total connected TM2 area	20
SMA.4	Maximum ratio of metal 6 antenna area to total connected TM2 area	0

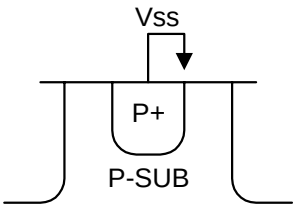
9. Latchup Rules

9.1. Definition of Terms for Latchup Rules

Active diffusion:	An active diffusion is any FET source/drain, P+ active in a Nwell, or N+ active in the substrate.
Guard bar:	A guard-bar is defined as 1) a N+active tie solidly strapped to the appropriate power bus in an N-well containing no active diffusion (Figures LR.1) or 2) a substrate tie separated from any active diffusion. (Figures LR.2)

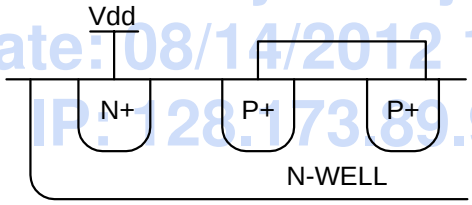


LR.1 N+ GUARD-BAR



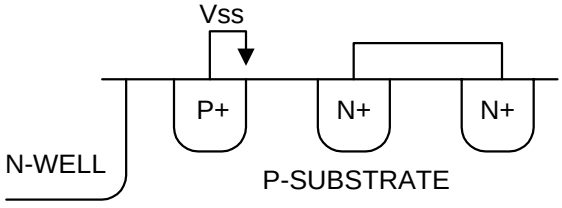
LR.2 P+ GUARD-BAR

Well-tie:	A Nwell tie is defined as a N+ active in an N-well solidly strapped to the appropriate power bus, for a N- well containing P+ active diffusion. Figure LR.3



LR.3 N-WELL TIE

Substrate-tie:	A substrate-tie is defined as a P+ active in the substrate solidly strapped to the appropriate bus, for the substrate containing N+ active diffusion. Figure LR.4



LR.4 P-SUBSTRATE TIE

Periphery:	For the purposes of latch-up, the device periphery is defined as any geometry less then or equal to 60um from any diffusion directly connected to an I/O pad.

I/O pad:	Any pad other than power supply pads.
Directly Connected	Connected by metal 1, metal 2, metal 3, metal 4, metal 5, metal 6, poly or diffusion.

9.2.

Latchup Rules

See Figures LR5 and LR6.

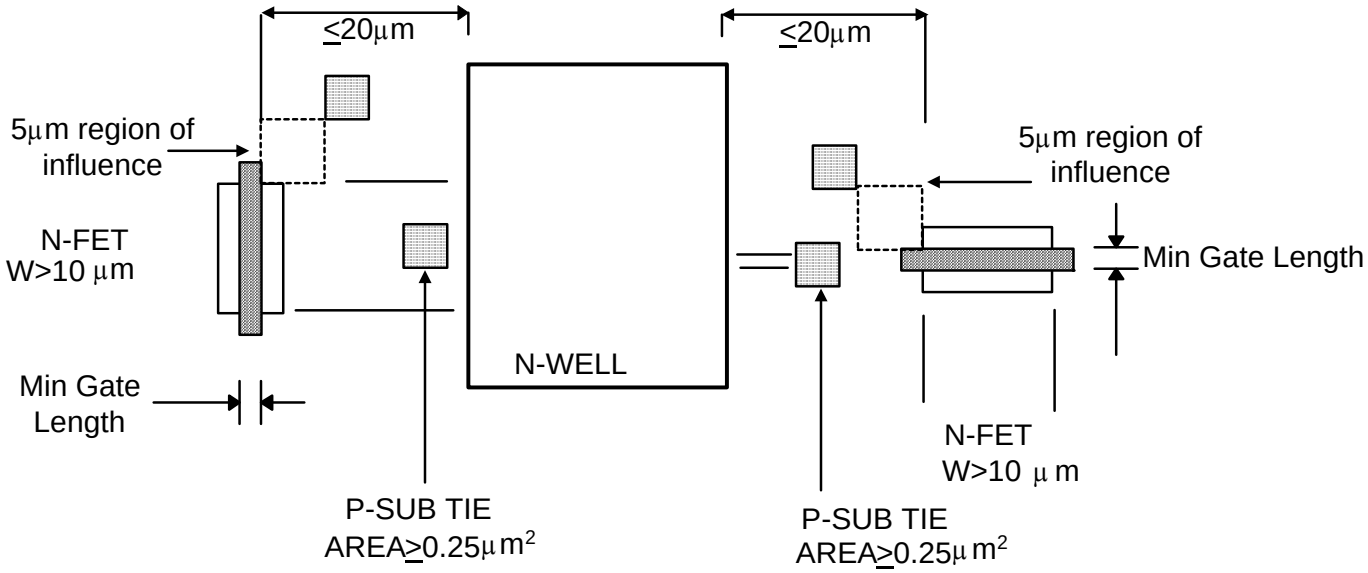
9.2.1. Latch-up rules for circuitry in the device periphery:

Rule No.	Rule Name	CA13HC
LUP.A.a	Maximum space between any points in a peripheral P+ active diffusion and its nearest well-tie contact in the same well	35
LUP.A.b	Maximum space between any points in a peripheral N+ active diffusion and its nearest substrate-tie contact.	35
LUP.B.C	Minimum space between an N+ diffusion in the substrate to a P+ diffusion in an N-well:	
LUP.B.C.a	Tag all N+ diffusions connected to a pad (excluding power supply pads).	
LUP.B.C.c	Minimum space between all P+ diffusions (in N-wells that are connected to Vdd) from all N+ diffusions identified in LUP.B.C.a.	50
LUP.B.C.d	Tag all P+ diffusions connected to a pad (excluding power supply pads).	
LUP.B.C.f	Minimum space between all N+ diffusions (except high potential N+ tied to VDD or VESD) in the substrate from all P+ diffusions identified in LUP.B.C.d.	50
LUP.D	All wells in the periphery (except the floating wells under pads and Nwell resistors) must be surrounded by a well-tie. An external ring of P+ guard-bar is recommended.	
LUP.D.a	Minimum diffusion width of P+ guard bar (see note D&E)	0.5
LUP.D.b	Minimum diffusion width of well-tie	0.5
LUP.D.c	Latch-up rules LUP.D and LUP.D.b do not apply for N-wells which are used as well resistors. An external ring of P+ guard-bar must surround n-well resistors in the periphery.	
	Minimum diffusion width of unbroken P+ guard bar	0.5
LUP.D.d	Minimum diffusion width of P+ guard bar for butted ties.	0.3
LUP.E	All substrate areas containing N+ active diffusions in the periphery must be surrounded by P+ guard bar. An external ring of N+ guard-bar is recommended.	
LUP.E.a	Minimum diffusion width of N+ guard bar (see note D&E)	0.5
LUP.E.b	Minimum diffusion width of N+ guard bar for butted ties.	0.3
LUP.F.a	Any P+ diffusion directly connected to an I/O pad must be contained in an isolated well. Well isolation is defined in Rule LUP.D. (A P+ region connected to a pad must be in a well)	
LUP.F.b	Any N+ diffusion directly connected to an I/O pad must be isolated from other N+ diffusions. This isolation is defined in Rule LUP.E. (Does not apply to Nwell drain resistors on an I/O pad)	
LUP.G.a	Maximum separation between adjacent power bus contacts in a guard bar, well tie, or substrate-tie diffusion. A maximum of 20um is recommended.	100
LUP.G.b	Maximum separation between adjacent power bus contacts in a guard, well tie, or substrate-tie diffusion for crossings of connections to a double bonded pad.	300

Note: D&E	An external P+ guard bar or an external N+ guard bar may surround more than one unbroken N-well tie ring or substrate tie ring of rule LUP.D.b or LUP.E.b respectively. If the side of a P+ guard bar that is facing the die edge is unobstructed then part or all of the die-edge facing side may be omitted, i.e. need not totally surround the N-well(s).	

9.2.2. Latch-up rules for internal circuitry

Rule No.	Rule Name	CA13HC
LUP.H	All N-wells must contain a guard-bar or a well-tie diffusion except for Nwells under pads.	
LUP.I.a	Maximum space in X or Y directions between any point in a P+ active diffusion and its nearest well-tie contact in the same well	30
LUP.I.b	Maximum space in X or Y directions between any point in an N+ active diffusion and its nearest substrate contact.	30
LUP.I.c	A substrate tie of $\geq 0.25um^2$ must be placed directly between an Nwell and any Nfet gate of 1) drawn Nfet width > 10um, 2) minimum gate length and 3) within 20um of the Nwell. If this rule cannot be followed due to space limitations between the Nwell and the NFET gate in transistors of width of 20um or less, there is a region of influence by a substrate tie that is defined as 5um from the edge of the gate/active edge where the required tie may be placed. This rule applies to NFETs with any orientations.	
LUP.I.d	A substrate tie of $>0.25um^2$ must be placed directly between an Nwell and any Nfet gate of 1) drawn Nfet width >10um, 2) minimum gate length, 3) within 20um of the Nwell and 4) Nfet has thick gate oxide (DG mask). This rule applies to NFETs with any orientations. The region of influence rule, in rule LUP.I.c does not apply for these thick gate oxide fets (DG).	



LUP.I.c Special Nfet Psub-Tie Rules

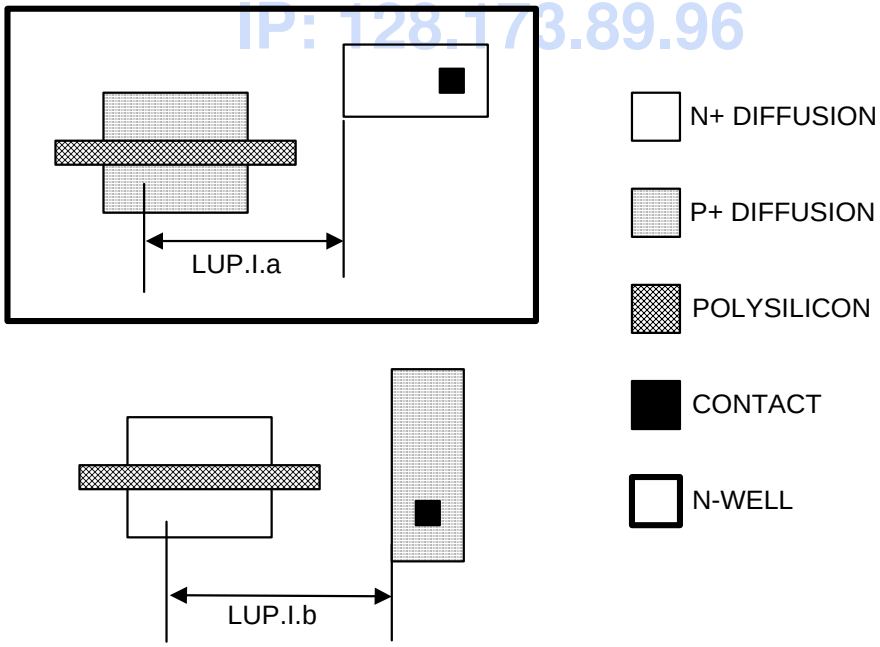


ILLUSTRATION LR.5 Latch-up rules for internal circuitry

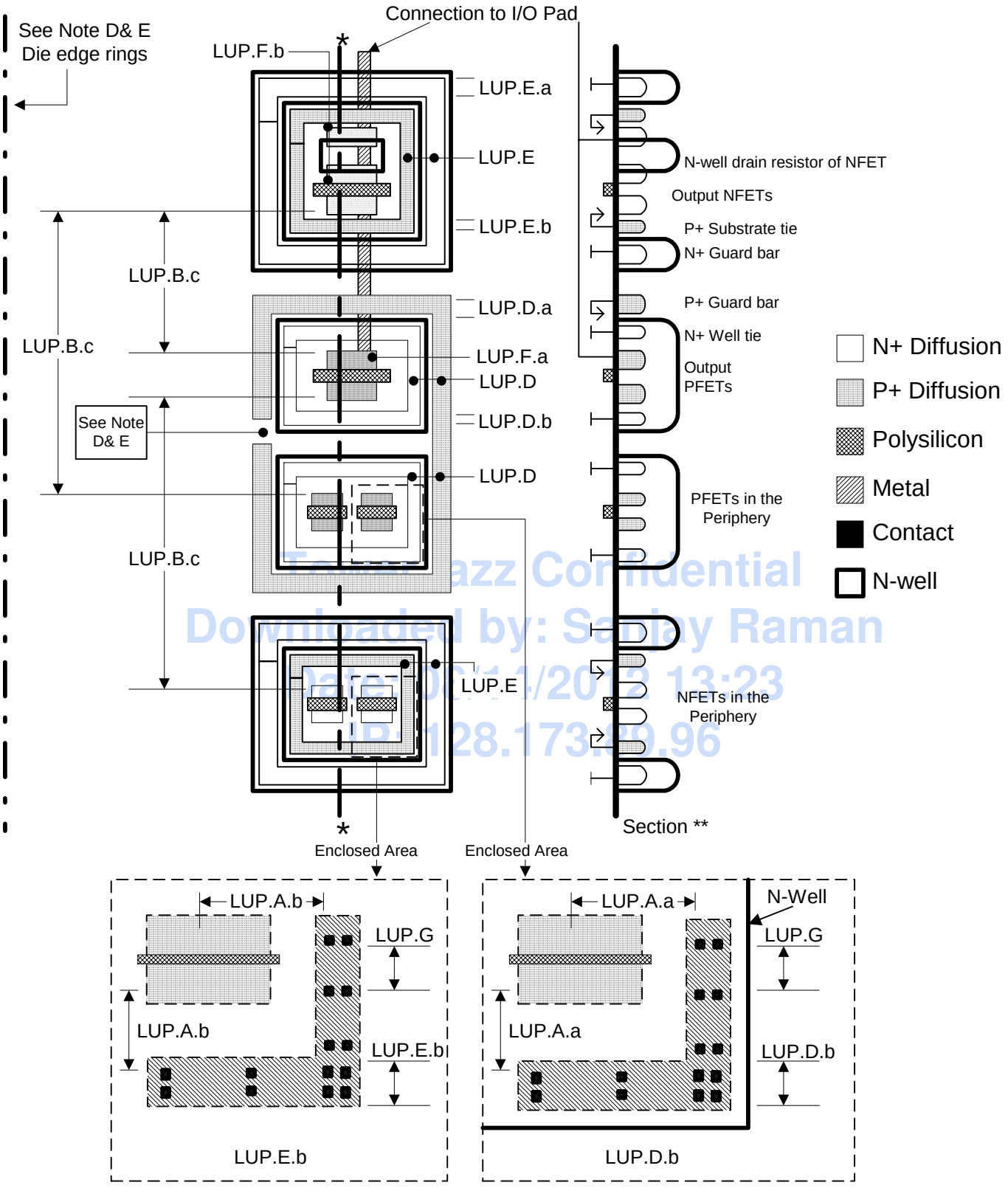


ILLUSTRATION LR.6 Latch-up rules for device periphery

10. Miscellaneous Guidelines

10.1. Artifact Regions

Artifact regions are defined to be regions within the artifact marking layer (layer 118, datatype 40). Provision for artifact region is made to allow customers to draw non circuit data such as company logo, part number, revision number or letters. Only basic manufacturing design rules are checked. All other checks, such as LVS, are not performed within artifact regions.

1) Jazz does not require to have any non circuit data such as company logo, part number, revision number or letters

2) Basic manufacturing DRC violations within the artifact regions are flagged by *.artifact design rule checks

3) As drawn data is preserved within artifact regions. Only dummy active and reverse active layer generations are performed within the artifact regions. No other layer generation is performed within the artifact regions.

4) It is recommended to place the layer identifications and company logo on the same side of the chip, within 1,000um of the design data extends.

The following guidelines may be used for artifacts.
Use minimum number of layers such as metals and/or poly in artifact regions.

If contact or via layers *must* be used, they must consist of a field of minimum sized contacts and vias (i.e. no large-area contacts or vias), with all poly and metal overplots consistent with the design rules. Text or artifacts on contact and via layers must have an underlying metal or poly plate and an overlying metal plate.
According to CMOS mask naming convention, the letters I, O, Q, S, X, and Z are not allowed. The following part number and revision letter/characters are acceptable for symbolic designs:

A B C D E F G H J K L M N P R T U V W Y

1 2 3 4 5 6 7 8 9 0 -

10.2.

Good Layout Procedures for Enhanced Yields

Good circuit layout procedures can enhance yields. Some suggested practices are:

1) Allow more than minimum spaces for metals and poly wherever possible.
2) Allow extra overplot of contacts, via via2s, via3s and via4s wherever possible.
3) Allow more than minimum spaces for active wherever possible.
4) Place extra substrate and well ties in the circuits and it is best to put the ties between transistors and the well boundaries for latchup immunity.
5) Eliminate or minimize the antennas, including the ROM area.
6) Do not allow small slivers and slits to be generated on the reticles.
7) Move the contacts, vias, via2s, via3s and via4s in from the metal edge by an extra 0.25um for wide metal lines with a line of many (>4) contacts, vias, via2s, via3s and via4s.
8) Avoid the use of angled polygons. Try to step the angled line with large steps, if possible. If you must use angled polygons, try to use only 45-degree sides. These hints will significantly help to reduce the size of the generated Mebes (CATS) data.
9) Use slits in metal layers (for stress relief reasons) at corner intersection that maintain good current flow.
10) Design rule ST.D (recommended minimum/maximum slit length of 100/300um), this is an unchecked rule. Please pay attention when tapping large current in/out of a slotted line and make sure that the current loading is even on both sides of the slit.

Procedures 1, 2, 3, 4 and 5 are the most important practices that can improve yields and reliability margin.

General practice for analog/RF sections

1) Larger devices match better (except for very large devices which can match worse).
2) Keep matched devices close together, as matching degrades with distance.
3) Use symmetric layouts to improve matching (mirror image layouts do not prevent offsets caused by resist thickness variations).
4) Be aware of offsets caused by temperature variations across the die.
5) Reduce contact and via resistance variations by using extra contacts and vias where possible.
6) Use dummy capacitors to improve capacitor matching. Use common centroid layouts for larger capacitors.
7) Use dummy resistors to improve resistor matching. Use the same orientation and width for matched resistors.
8) Use common centroid FETs to improve matching. Use the same orientation and current flow direction for matched FETs. Be aware that source/drain capacitance can be affected by the presence of adjacent active.
9) Minimize antennas on matched FETs.

11. Scribe Line and Die Seal Rings

This section describes the rules for the scribe lane and the die seal rings. See illustrations BD in Section 8.1.1 and SB. All rules in this Scribe Line section are drawn dimensions and polarities.

11.1. Die Seal Rings

Every circuit placed on wafer is required to have a die seal ring. This includes all circuits placed on test chips and MPW (multi project wafers) runs. The die seal rings are made of two components; white space and rings. White space is the separation of the circuit data to the ring data and is 13um wide – it is truly blank space. The actual ring data is 12um wide and made of layers: Active, P+ Implant, Contact, Metals and Vias. The final structure looks like a P+ Substrate tie with all layers of metal. The outermost edge of the ring data is line-on-line with the edge of the scribe lane.

The figure below shows the relationship between circuit, scribe, and seal ring data. Seal rings in essence expand the circuit data by 25um on each edge (13um white space and 12um rings).

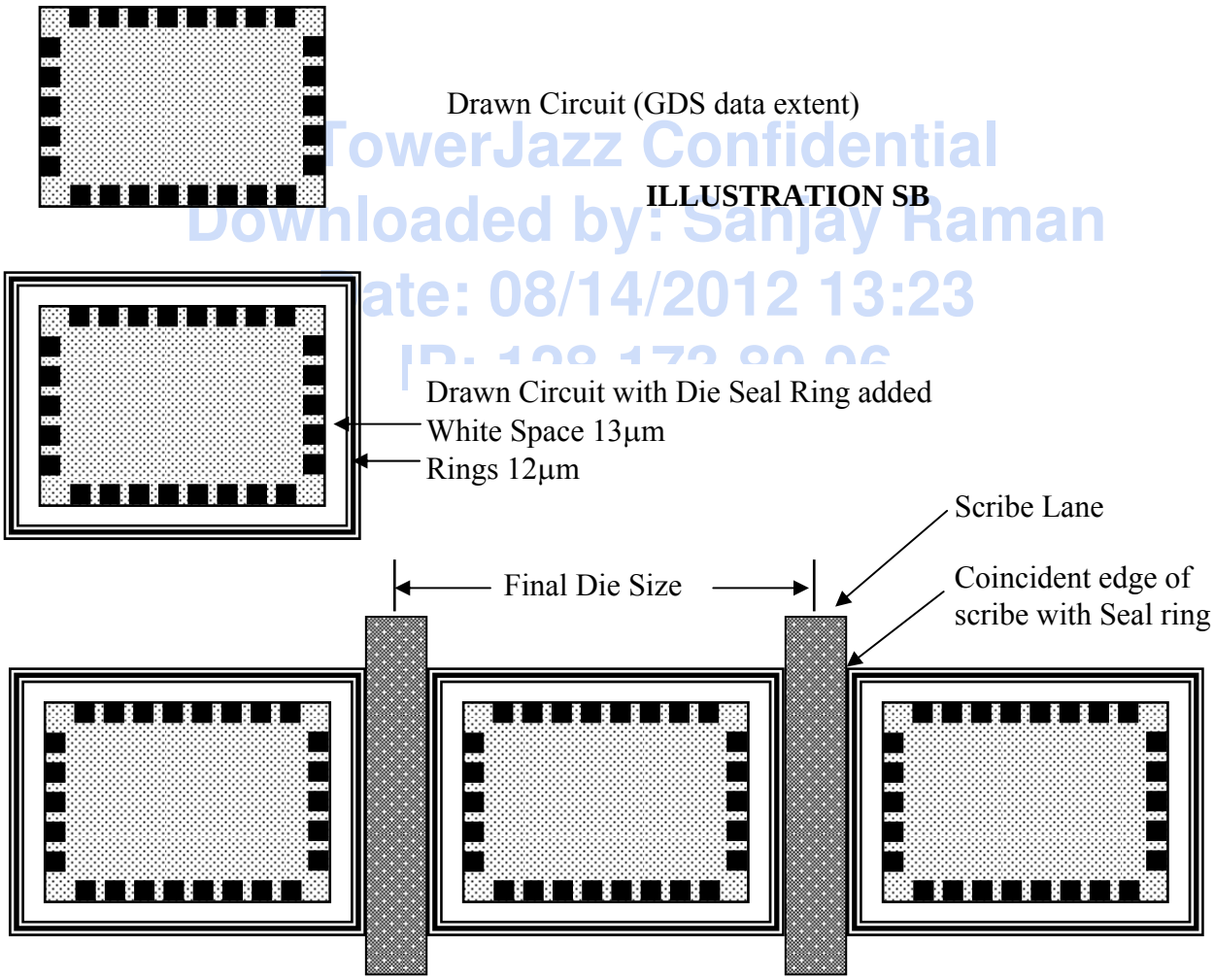


ILLUSTRATION SB

Die Seal Rings are added by Jazz ONLY to the circuit data. Jazz does not recommend customers to do die seal ring. If absolutely necessary, contact Jazz representative.

The following rules are not checked and are for reference only

Rule No.	Rule Name		CA13HC
SB.A	Width of white space (rings to any layer of circuit)		13
SB.B	Total width of white space and rings		25
SB.C	Width of:	a) Active Ring	12
		b) Reverse - Active ring	6
		c) Contact ring	3 contact slots
		d) Metal 1 ring	6.35
		e) Via1 ring	2 via slots
		f) Metal 2 ring	6.35
		g) Via2 ring	3 via2 slots
		h) Metal 3 ring	6.35
		j) Via3 ring	2 via3 slots
		k) Metal 4 ring	6.35
		g) Via4 ring	3 via4 slots
		h) Metal 5 ring	6.35
		j) Via5 ring	2 via5 slots
		k) Metal 6 ring	6.35
		l) P+ implant ring	12
		m) N+ implant ring	none
		n) N-well ring	none
		o) Field implant ring	none
SB.D	Minimum scribe line width:		Contact Jazz representative
SB.E	Scribe lanes do not have silox opened		

Note1: The contact and via slot widths are equal to the width of the square contacts or vias allowed in the corresponding process variant

12.

Soft ERC Rules

The soft ERC checks identify layout topology that could induce electrical failure. Some definitions of terminology include,

Ntap: n+ active inside nwell
Ptap: p+ active inside p substrate
Digital substrate: Substrate region not covered by layer 62
Analog substrate: Substrate region covered by layer 118/43

Check Name	Check Description
Floating_poly	Poly is not connected to a Jazz supported device terminal or bond pad
Floating_met1_net	Metal 1 is not connected to a Jazz supported device terminal or bond pad
Floating_ met2_net	Metal 2 is not connected to a Jazz supported device terminal or bond pad
Floating_ met3_net	Metal 3 is not connected to a Jazz supported device terminal or bond pad
Floating_ met4_net	Metal 4 is not connected to a Jazz supported device terminal or bond pad
Floating_gate	Gate is not connected to a Jazz supported device terminal or bond pad
Floating_dpsub	Digital substrate with active component does not have ptap
Floating_apsub	Analog substrate with active component does not have ptap
SOFT.N	Ntap has no connection to power, ground, or pFET terminal
Nwell_no_tap	Nwell with active component has no ntap
SOFT.P	Ptap has no connection to ground
SOFT.PC	Ptap has no connection to bonding pad
Ptap_pwr	Ptap is connected to a power pad
Ntap_gnd	Ntap is connected to ground pad
Gate_pwr_gnd	Power or ground is connected to both source and drain of the same transistor
Power_pdiff_in_grounded_nwell	Forward biased diode between power and ground
Shorting_thru_nwell	Ntaps at different potential are shorted thru nwell
Shorting_thru_dpsub	Ptaps at different potential are shorted through digital substrate
Shorting_thru_apsub	Ptaps at different potential are shorted thru analog substrate