$2Q = 2 \cdot \frac{}{2R_s \cdot \omega C_{gs}} \quad R_s \omega C_{gs}$

$= Q_u \rightarrow$ unloaded Q

↑ loaded-Q

7) overall noise factor including gate noise

$$F = 1 + \frac{R_g}{R_s} + \frac{1}{2Q}\frac{\gamma}{\alpha}\left(\frac{\omega}{\omega_T}\right) + \left(2Q + \frac{1}{2Q}\right)\left(\frac{\omega}{\omega_T}\right)^2 \frac{\delta}{5} + \frac{1}{2Q}\cdot|c|\sqrt{\frac{\delta\gamma}{5}}\left(\frac{\omega}{\omega_T}\right)$$

due to R_g

due to $\bar{i}_d$

due to $\bar{i}_g$

due to correlated component of $\bar{i}_g$

~~2Q → loaded Q~~

~~Q → unloaded Q~~

~~2Q → Q_{cs}~~

$\bar{i}_d$

$\propto \frac{1}{Q}, \propto \frac{1}{\omega_T}$

$\propto C_{gs}, \propto \frac{C_{gs}}{g_m}$

$\propto W, \propto W^{\frac{1}{2}}$

$\propto W^{\frac{3}{2}}$

$\bar{i}_g$

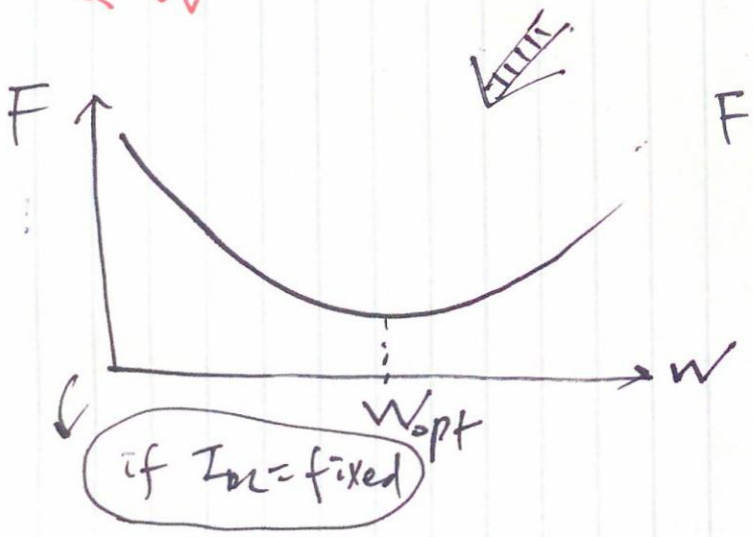
$\propto Q, \propto \omega_T$

$\propto \frac{1}{C_{gs}}, \propto \frac{C_{gs}}{g_m}$

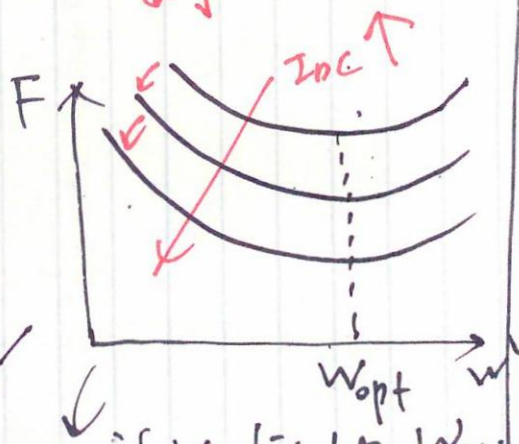
$\propto \frac{1}{W}, \propto W^{\frac{1}{2}}$

$\propto \frac{1}{\sqrt{W}}$

$\propto W^{3/2}$



if I_{DC} = fixed



if W = fixed to W_{opt} then increase g_m to increase f_T → increase I_{DC}

some remarks

- α, δ, γ & c are process parameters
- only design parameter is I_{DC} and device width, W
- if we assume I_{DC} = constant there is an optimum W for the input transistor, where F will be minimum