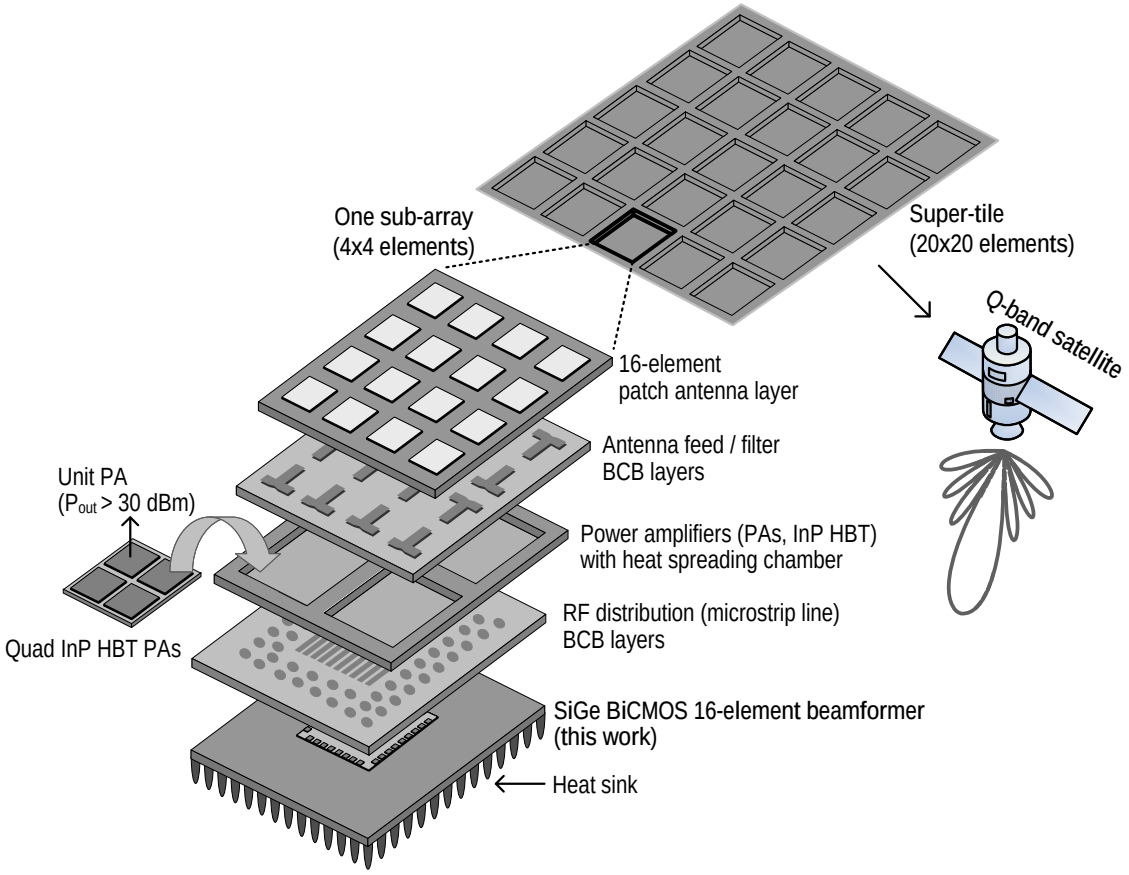

Fig. 1. A tile-based array architecture. One super-tile is composed of 5×5 tiles (sub-arrays) and each tile contains 16 elements (4×4). Multi-layer integration allows the optimization of each layer in terms of thermal, mechanical and electrical performances.

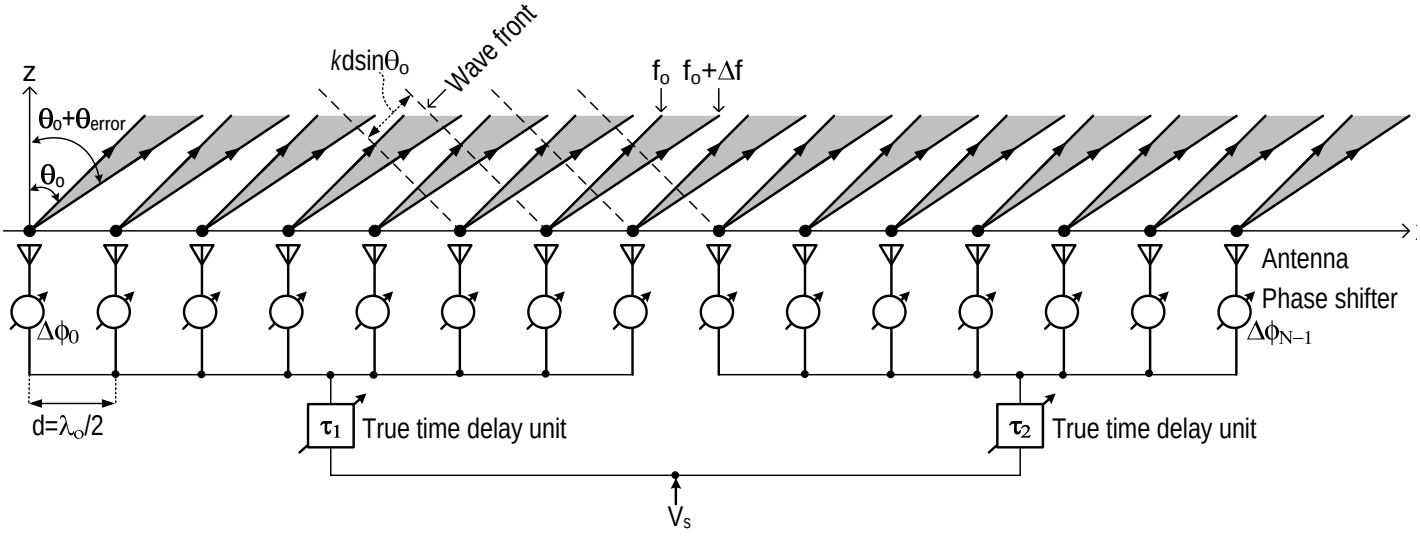

Fig. 2. 16-element phased-array with a combination of phase shifters at the element level and true time delay (TTD) units at the sub-array level for wideband operation (N=16).