

Jazz Semiconductor

CA18 Design Manual

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Revision Number	Revision Description	Date
01	Initial release.	12/16/03
02	<p>Document fully rewritten. Please refer to the following release highlights for details:</p> <p>Documented new device naming conventions for CA18HR.</p> <p>Expanded corner and statistical model sections of each device chapter.</p> <p>Added espec vs. model tables for resistor, MIM capacitor, and vertical PNP chapters.</p> <p>Completely re-wrote CMOS chapters 2 and 3 to account for new scalable model.</p> <p>Added MOS varactor documentation to chapter 5.</p> <p>Updated resistor and inductor chapters with new device names, model verification, etc.</p> <p>Added chapter 9: CA18 diodes.</p>	09/24/04
03	<p>Moved Chapter 10: Appendix to Chapter 11.</p> <p>Added Chapter 10: Deep Nwell</p> <p>Updated figure 7.6: Poly capacitor cross section</p>	12/17/04

04	<p>Added device cross sections to each chapter.</p> <p>Added substrate ring resistance and RF noise model documentation to Chapter 3: RF CMOS Model.</p> <p>Added Appendix A: Additional Model Consideration. This section documents supplemental statistical, corner, and parasitic extraction model behavior.</p> <p>Updated sub-circuit schematics for all capacitor, resistor, varactor devices.</p> <p>Updated Inductor chapter to be valid for Toolbox 1.4 including new model verification plots.</p> <p>Updated Resistor, Varactor, Capacitor, Inductor, VPVP, and Diode chapters to be more uniform.</p> <p>Added more detailed mismatch sections to Resistor and Capacitor chapters.</p> <p>Exchanged SBC18 voltage dependent Rnwell data for CA18 data.</p> <p>Added metal option layout descriptions for varactors.</p> <p>Added Deep Nwell vs. NON Deep Nwell MOSFET characterization to Deep Nwell Chapter</p>	03/11/05
05	<p>Updated MOSFET chapters with new TOX variation in corner and stat models. Updated RF MOSFET chapter to include documentation of new gate and substrate resistance models and new Y-parameter plots.</p> <p>Updated MOS Varactor chapter to reflect new TOX variation.</p> <p>Added PCM notes section to each chapter statistical model section, spelling out differences between PCM and ESPEC limits.</p> <p>Updated Appendix A layout parasitics table MIM entry.</p>	11/28/05

06	<p>Updated Introduction chapter to define new 1.8V/3.3V super set process options CA18QD/PD/HD and well as new 1.8V/5V options CA18HA/HP/HB</p> <p>Update component device list in Chapter 1.0</p> <p>Updated all device cross sections</p> <p>Added PCM notes section to each chapter statistical model section, spelling out differences between PCM and ESPEC limits</p> <p>MOSFET: Updated documentation to reflect new TOX variation in corner and stat models. Updated RF MOSFET chapter to include documentation of new gate and substrate resistance models and new Y-parameter plots.</p> <p>High Voltage MOSFET: added new chapter documenting high voltage and LDMOS devices available to CA18HP/HA/HB</p> <p>Inductor: Re-wrote chapter to include latest JIT4.0 definitions</p> <p>Varactor: Updated Table 6.3 with latest rvar_ni espec and simulation data. Update model verification plots in Figure 6.5, and Figure 6.6. Updated Table 6.7 with the latest mosvar_1p8 espec and simulation data. Updated MOS Varactor documentation to reflect new TOX variation</p> <p>Resistor: Update Table 7.2 for low value resistor espec and simulation data. Added high value resistor espec and simulation data</p> <p>PNP: updated Table 9.2 with latest espec and simulation data. Update Figure 9.4 with updated pnp beta playback</p> <p>Added X-Sigma Corner Model Chapter</p> <p>Updated Appendix A</p>	12/07/07
07	<p>Updated HV MOS labels with correct operating voltages</p> <p>Updated cross-sections for 40V LD-MOS devices</p>	07/07/08

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1.0 Introduction

This document is intended to serve as a modeling design guide for CA18, the Jazz Semiconductor 0.18um Analog/RF CMOS process family. Please refer to the following documents for additional information about the CA18 process definitions and its variants:

NPB PS-0176 CA18QD/PD/HD Design Rules

NPB PS-0173 CA18QD/PD/HD Electrical Specifications

NPN PS-0711 CA18HA/HP/HB Application Note

NPB PS-0643 CA18 ESD Design Manual

The CA18 technology offers an array of CMOS transistor voltage pairings. These pairings include dual gate 1.8V plus 3.3V variants as well as 1.8V plus 5V variants. The 1.8V/3.3V CA18 paring is available in three super-set flavors: CA18QD/PD/HD, differentiated by metal layer count. CA18QD is the four level metal super-set, CA18PD is the five level metal super-set, and CA18HD is the six layer metal super-set. Jazz super-set technologies offer a variety of technology modules that may be added or removed from the design infrastructure in order to create real-time technology component combinations. Table 1.1 lists the devices available to each super set process variant. Removable modules are highlighted in green.

TABLE 1.1 CA18 1.8V/3.3V super-set process device availability table

Devices	CA18QD	CA18PD	CA18HD
3.3V FET	X	X	X
1.8V FET	X	X	X
1.8V/3.3V Diodes	X	X	X
3.3V Native FET	X	X	X
Vertical PNP	X	X	X
Low Value Poly Resistor	X	X	X
High Value Poly Resistor	X	X	X
Salicided Poly Resistor	X	X	X
Nwell Resistor	X	X	X
Varactor (P+/Nwell)	X	X	X
MOS Varactor	X	X	X
2fF MIM Capacitor	X	X	X
4fF Stacked MIM Capacitor	X	X	X
Deep Nwell	X	X	X
Square/Octagonal Inductors	X	X	X

Table 1.2 lists legacy 1.8V/3.3V CA18 process variants also available (new designs must use super set process design kits).

TABLE 1.2 Legacy 1.8V/3.3V 0.18um process variants

Devices	CA18QW1	CA18QW5	CA18PW1	CR18PW54	CA18HW1	CA18HR
3.3V FET	X	X	X	X	X	X
1.8V FET	X	X	X	X	X	X
Diodes	X	X	X	X	X	X
3.3V Native FET						X
Vertical PNP	X	X	X	X	X	X
Low Value Poly Resistor	X	X	X	X	X	X
Salicided Poly Resistor	X	X	X	X	X	X
Nwell Resistor	X	X	X	X	X	X
Varactor (P+/Nwell)				X		X
MOS Varactor						X
1fF MIM Capacitor		X		X		
2fF MIM Capacitor						X
4fF Stacked MIM Capacitor						X
Deep Nwell/ 8V LDMOS						X
Inductors				X		X

Table 1.3 lists the available 1.8V/5V CA18 process variants

TABLE 1.3 1.8V/5V CA18 variants

Devices	CA18HP	CA18HA	CA18HB
5V FET	X	X	X
12V LDMOS	X	X	X
20-40V LDMOS		X	
RFLDMOS	X		X
5v Diodes	X	X	X
40v Diodes		X	
Vertical PNP	X	X	X
40V Vertical NPN		X	
Low Value Poly Resistor	X	X	X
Salicided Poly Resistor	X	X	X
Nwell Resistor?	X	X	X
Varactor (P+/Nwell)?	X	X	X
MOS Varactor?	X	X	X
Varactor (P+/Nwell)	X	X	X
2fF MIM Capacitor	X	X	X
4fF Stacked MIM Capacitor	X	X	X
Lateral MIM Capacitor		X	
Deep Nwell?	X	X	
Inductors	X	X	X
SOI			X

Table 1.4 lists the different interconnect options available in CA18.

TABLE 1.4 CA18 interconnect options

Variant	Metal Layers	Top Metal Thickness
CA18QD	4	2.8
CA18QW1	4	0.85
CA18QW5	4	0.85
CA18PD	5	2.8
CA18PW1	5	0.85
CR18PW54	5	2.8
CA18HD	6	2.8
CA18HW1	6	0.85
CA18HR	6	2.8
CA18HA	6	2.8
CA18HD	6	2.8
CA18HB	6	2.8

For super-set process design kit setup instructions please refer to the kit installation guide or load the Cadence **CIW -> JAZZ -> Application Notes -> Process Variant and Layer Setup** utility. A sample snapshot of this setup feature is pictured below for ca18hd.

FIGURE 1.1 Process Variant and Layer Setup design kit utility



1.1 Device List and Description

The CA18QD/PD/HD/HA/HP process variants does not share the same device naming convention used in legacy processes. Throughout this document the authors will refer to device names using the CA18QD/PD/HD conventions. Please refer to the “Appendix B: Additional CA18 Process Variants ” on page 359 for CA18QW1, CA18QW5, CR18PW54 and CA18HW1 definitions.

FETs:

- nfet (analog NFET, thin oxide (1.8V), 3-terminal with implicit bulk pin, sub-circuit model NFETs)
- nfet_4 (analog NFET, thin oxide (1.8V), 4-terminal with explicit bulk pin, sub-circuit model NFETs)
- nfet_cascode (cascode NFET, thin oxide (1.8V), 4-terminal, sub-circuit model NFET_dg)
- nfet_vt0 (native NFET, thick oxide (3.3V), 3-terminal, sub-circuit model NFETs_vt0)
- pfet (analog PFET, thin oxide (1.8V), 3-terminal with implicit bulk pin, sub-circuit model PFETs)
- pfet_4 (analog PFET, thin oxide (1.8V), 4-terminal with explicit bulk pin, sub-circuit model PFETs)
- pfet_cascode (cascode PFET, thin oxide (1.8V), 4-terminal, sub-circuit model PFET_dg)
- nfet3p3 (analog NFET, thick oxide (3.3V), 3-terminal with implicit bulk pin, sub-circuit model n3p3fets)
- nfet3p3_4 (analog NFET, thick oxide (3.3V), 4-terminal with explicit bulk pin, sub-circuit model n3p3fets)
- nfet3p3_cascode (cascode NFET, thick oxide (3.3V), 4-terminal, sub-circuit model n3p3fet_dg)
- nfet3p3_ids (8V LDMOS NFET, thick oxide (3.3V), 3-terminal with source shorted p-bulk, sub-circuit model n3p3fets_id)
- pfet3p3_ids (8V LDMOS PFET, thick oxide (3.3V), 3-terminal with source shorted n-bulk sub-circuit model p3p3fets_id)
- pfet3p3 (analog PFET, thick oxide (3.3V), 3-terminal with implicit bulk pin, sub-circuit model p3p3fets)
- pfet3p3_4 (analog PFET, thick oxide (3.3V), 4-terminal with explicit bulk pin, sub-circuit model p3p3fets)
- pfet3p3_cascode (cascode PFET, thick oxide (3.3V), 4-terminal, sub-circuit model p3p3fet_dg)
- nfet_rf (RF NFET, thin oxide (1.8V), 4-terminal with explicit bulk pin, sub-circuit model NFET_rf)
- pfet_rf (RF PFET, thin oxide (1.8V), 4-terminal with explicit bulk pin, sub-circuit model PFET_rf)
- nfet3p3_rf (RF n3p3fet, thick oxide (3.3V), 4-terminal with explicit bulk pin, sub-circuit model n3p3fet_rf)
- pfet3p3_rf (RF p3p3fet, thick oxide (3.3V), 4-terminal with explicit bulk pin, sub-circuit model p3p3fet_rf)
- passgate (thin oxide (1.8V) passgate, schematic based)*

- passgate3p3 (thick oxide (3.3V) passgate, schematic based)*
- nfet5p0 (analog NFET, ultra thick oxide (5V), 3-terminal with implicit bulk pin, sub-circuit model n5p0fets)
- nfet5p0_4 (analog NFET, ultra thick oxide (5V), 4-terminal with explicit bulk pin, sub-circuit model n5p0fets)
- nfet5p0_vt0 (native NFET, ultra thick oxide (5V), 3-terminal, sub-circuit model n5p0fets_vt0)
- pfet5p0 (analog PFET, ultra thick oxide (5V), 3-terminal with implicit bulk pin, sub-circuit model p5p0fets)
- pfet5p0_4 (analog PFET, ultra thick oxide (5V), 4-terminal with explicit bulk pin, sub-circuit model p5p0fets)
- nfet5p0_ld40 (40V Vds LDMOS non-isolated nfet, ultra-thick oxide (5V), 3-terminal with source shorted p-bulk, sub-circuit model nfp0fet_ld40s)
- pfet5p0_ld40 (40V Vds LDMOS pfet, ultra-thick oxide (5V), 4-terminal with source shorted n-bulk, sub-circuit model pfp0fet_ld40s)
- nfet5p0_ld40_iso (40V Vds LDMOS isolated nfet, ultra-thick oxide (5V), 4-terminal with source shorted p-bulk, sub-circuit model nfp0fet_isold40s)
- nfet5p0_ld12 (12V LDMOS non-isolated NFET, ultra thick oxide (5V), 3-terminal with source shorted p-bulk, sub-circuit model n5p0fets_lds)
- pfet5p0_ld12 (12V LDMOS PFET, ultra thick oxide (5V), 4-terminal with source shorted n-bulk sub-circuit model p5p0fets_lds)
- nfet5p0_ld12_iso (12V LDMOS isolated NFET, ultra thick oxide (5V), 4-terminal with source shorted p-bulk, sub-circuit model n5p0fets_isolds)
- nfet5p0_rfld (20V RFLDMOS NFET, ultra thick oxide (5V), 3-terminal with source shorted p-bulk, sub-circuit model nfet5p0_rflds)

Junction Diodes:

- dn (n+/sub junction diode, thin oxide (1.8V), 2-terminal, primitive model ndiode)
- dp (p+/well junction diode, thin oxide (1.8V), 2-terminal, primitive model pdiode)
- dn3p3 (n+/sub junction diode, thick oxide (3.3V), 2-terminal, primitive model n3p3diode)
- dp3p3 (p+/well junction diode, thick oxide (3.3V), 2-terminal, primitive model p3p3diode)
- dn5p0 (non-isolated n+/sub junction diode, ultra thick oxide (5V), 2-terminal, sub circuit model n5p0diode)
- dn5p0_iso (isolated n+/sub junction diode, ultra thick oxide (5V), 2-terminal, subcircuit model n5p0diode)
- dp5p0_3 (p+/well junction diode, ultra thick oxide (5V), 3-terminal, subcircuit model dp5p0_3)
- dnwell (nwell to p substrate modeling diode, 2-terminal, primitive model nwdiode)

- diso (deep nwell to isolated psub modeling diode, 2-terminal, primitive model dnw_pwell)
- diso40p0_3 (40V deep nwell to isolated psub modeling diode, 3-terminal, subcircuit model diso40p0_3)
- ddnw (deep nwell/nwell to p substrate diode, representing Deep Nwell layer connectivity, , primitive model dnw_pwell)
- ddnw40p0 (40V deep nwell/nwell to p substrate diode, representing Deep Nwell layer connectivity, , primitive model dnw_pwell)

Resistors:

- rnwell (Nwell resistor, 3-terminal, sub-circuit model rw3t)
- rppoly_lo (unsalicated poly resistor, 3-terminal, sub-circuit model rpp3t)
- rppoly_hi (high value unsalicated poly resistor, 3-terminal, sub-circuit model rph3t)
- rppoly_sal (salicated poly resistor, 3-terminal, sub-circuit model rps)
- r_dummy (dummy resistor for LVS, 2-terminal)

Capacitors:

- cpoly (poly cap over well, thin oxide (1.8V), 3-terminal, sub-circuit model pc)
- cpoly3p3 (poly cap over well, thick oxide (3.3V), 3-terminal, sub-circuit model pc3p3)
- cpoly5p0 (poly cap over well, ultra thick oxide (5V), 3-terminal, sub-circuit model pc5p0)
- cmim2 (2fF MIM capacitor over substrate, 3-terminal, sub-circuit model c3t_mim2)
- cmimw2 (2fF MIM capacitor over well, 3-terminal: plus-minus-well, sub-circuit model c3t_mimw2)
- csmim4 (4fF stacked MIM capacitor over substrate, 3-terminals, sub-circuit model c3t_smim4)
- csmimw4 (4fF stacked MIM capacitor over well, 3-terminals: plus-minus-well, sub-circuit model c3t_smimw4)
- cmimw2_4 (2fF MIM capacitor over well, 4-terminal: plus-minus-well-sub, sub-circuit model c3t_mimw2)
- csmimw4_4 (4fF stacked MIM capacitor over well, 4-terminals: plus-minus-well-sub, sub-circuit model c3t_smimw4)

Please refer to Table 8.1 on page 311 for complete capacitor naming conventions and specifications.

NPNs:

- vn timer model, 3-terminal, sub-circuit model vn timer

PNPs:

- vnpnp: 4 discrete models: PNP_a (25x25), PNP_b (11x11), PNP_c (5.4x5.4), PNP_d (3x3) (thin oxide (1.8V), 3-terminal, primitive model)

Varactors:

- var_{ni} (non-implanted varactor, 3-terminal, sub-circuit model rfvar_{ni})

- var_{mos} (MOS varactor, 3-terminal, sub-circuit model mosvar_1p8)

Inductors:

- ind (top metal square planar inductor, 3-terminal, sub-circuit model ind_3u)

- ind_{oct} (top metal octagonal planar inductor, 3-terminal, sub-circuit model ind_3u)

- ind_{diff} (top metal square differential inductor, 4-terminal, sub-circuit model inddiff_3u)

- ind_{diff}_{oct} (top metal octagonal planar inductor, 3-terminal, sub-circuit model inddiff_3u)

Fuse:

- fuse_{m5rf} (metal fuse, 2-terminal, sub-circuit resistor model fuse) *

ESD FETs

- nfet_{esd} (esd NFET with well resistor and guard ring, schematic based)

- pfet_{esd} (esd PFET with guard ring, schematic based)

NOTE: For ESD guidelines please refer to document NPB PS-0643

* Data not available

1.2 Device Model Availability

The CA18 models were verified using Cadence Spectre. Hspice, ADS, and Eldo simulators are also supported in selected processes.

TABLE 1.5 Device Model availability

Device	DC	AC	RF	Noise	Corner	Statistical	Mismatch
1.8V FET	X	X	X	X	X	X	X
3.3V FET	X	X	X	X	X	X	X
5V FET	X	X		X	X	X	X
5V High Voltage LD FETs (HA)	X	X	X		X	X	
3.3V High Voltage LD FETs (HD,PD,QD)	X	X	X				
5V RF LDMOS (HP)	X	X	X				
3.3V/5V Native FET	X	X		X	X	X	X
Vertical PNP	X	X			X	X	
Salicided Poly Resistor	X	X	X		X	X	X

TABLE 1.5 Device Model availability

Device	DC	AC	RF	Noise	Corner	Statistical	Mismatch
Low Value Unsalicided Poly Resistor	X	X	X	X	X	X	X
High Value Unsalicided Poly Resistor	X	X	X	X	X	X	X
Nwell Resistor	X	X			X	X	
Stacked / Single MIM Cap	X	X	X		X	X	X
1.8V/3.3V/5V Poly Capacitor	X	X			X	X	
P+ / Nwell Varactor	X	X	X		X	X	
MOS Varactor	X	X	X		X	X	
1.8V/3.3V Diodes	X	X			X	X	
Inductor	X	X	X		X	X	X
Interconnect	X	X					
ESD Devices	X						

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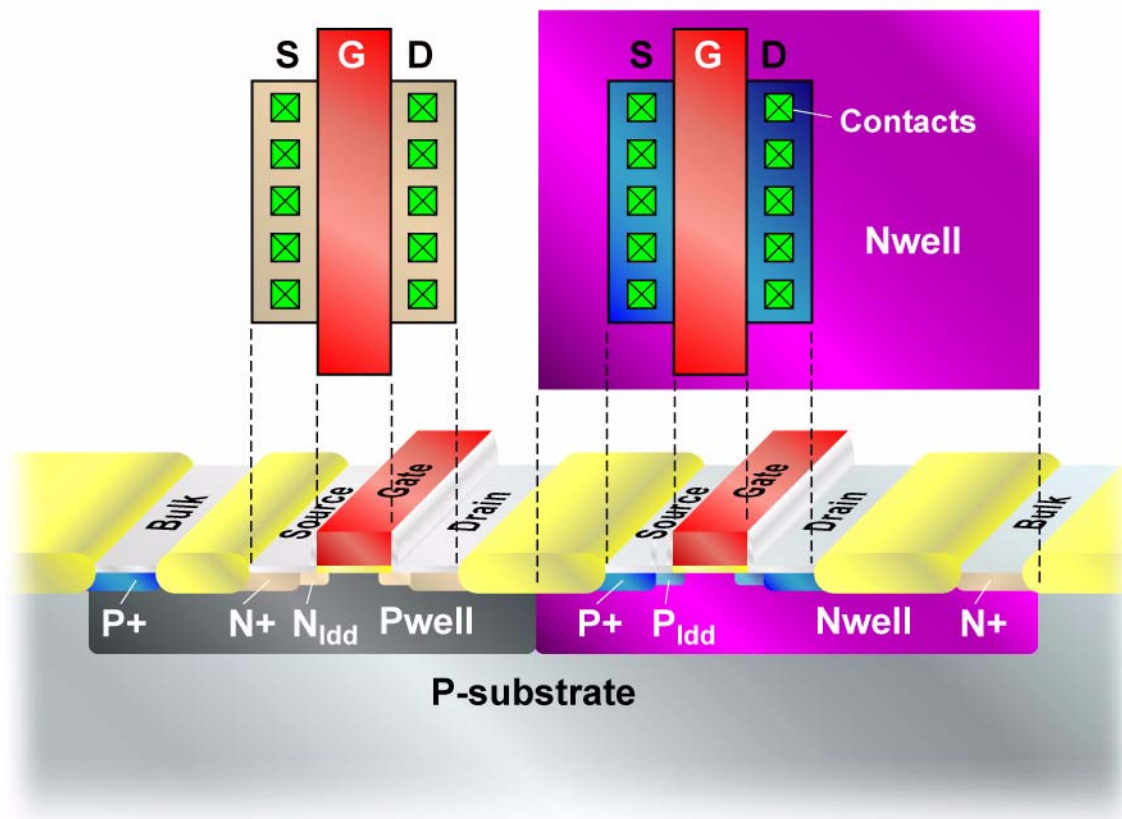
2.0 MOSFET Model

2.1 Device Description

The CA18 process family supports multiple mixed-signal (MS) models which includes thin gate-oxide 1.8V FETs, thick gate-oxide 3.3V fets, and thick gate-oxide 5.0V fets. In addition to these core devices, zero mask-adder “free” native 3.3V and 5.0V NFETs are available. The native devices have a negative threshold voltage. Note that the 3.3V and 5.0V FETs are not available together in any CA18 process variant. The 1.8V FETs are available in all CA18 variants. The 3.3V FETs are available in CA18HD,PD, and QD, while the 5V FETs are available in CA18HA and HP.

The cross-section of a representative CMOS device is illustrated in Figure 2.1.

FIGURE 2.1 NFET and PFET cross section



2.2 Model Description

TABLE 2.1 Model summary for Fets

Property	1.8V1.8V Fets
Model name	nfet, pfet
Temperature Range	-40 to 125°C

TABLE 2.1 Model summary for Fets

Property	1.8V1.8V Fets	
Channel Length	0.18μm ≤ L ≤ 100μm	
Channel Width	0.22μm ≤ W ≤ 100μm	
No. of fingers	1 ≤ NF ≤ 100	
Bias Range	Vgs : 0 ~ 1.8V, Vds : 0 ~ 1.8V, Vbs : 0 ~ 1.8V	

Property	3.3 v Fets	3.3 v Native Fets
Model name	nfet_3p3, pfet_3p3	nfet3p3_vt0
Temperature Range	-40 to 125°C	-40 to 125°C
Channel Length	0.36μm ≤ L ≤ 100μm for NFET 0.30μm ≤ L ≤ 100μm for PFET	1μm ≤ L ≤ 100μm
Channel Width	0.40μm ≤ W ≤ 100μm	0.40μm ≤ W ≤ 100μm
No. of fingers	1 ≤ NF ≤ 100	1 ≤ NF ≤ 100
Bias Range	Vgs : 0 ~ 3.3V, Vds : 0 ~ 3.3V, Vbs : 0 ~ 3.3V	Vgs : -0.5 ~ 3.3V, Vds : 0 ~ 3.3V, Vbs : 0 ~ 3.3V

Property	5.0 v Fets	5.0 v Native Fets
Model name	nfet5p0, pfet5p0	nfet5p0_vt0
Temperature Range	-40 to 125°C	-40 to 125°C
Channel Length	0.6μm ≤ L ≤ 100μm for NFET	1.2 μm ≤ L ≤ 100μm
Channel Width	0.7μm ≤ W ≤ 100μm	0.4 μm ≤ W ≤ 100μm
No. of fingers	1 ≤ NF ≤ 100	1 ≤ NF ≤ 100
Bias Range	Vgs : 0 ~ 5.0V, Vds : 0 ~ 5.0V, Vbs : 0 ~ 5.0V	Vgs : -1 ~ 5.0V, Vds : 0 ~ 5.0V, Vbs : 0 ~ 5.0V

Using these models outside of the specified ranges may generate simulation errors.

2.2.1 Scalable model

A completely scalable BSIM3v3 model was used to fit devices of all geometries. A limited set of model parameters were made geometry dependent to improve model accuracy, as per the equation inside BSIM3v3:

$$P = P0 + \frac{LP}{L_{eff}} + \frac{WP}{W_{eff}} + \frac{PP}{(L_{eff} \times W_{eff})} \quad (\text{EQ 1})$$

where P is the effective parameter value, with P0, LP, WP, and PP defining the geometric dependencies of the parameter.

A scalable model is highly desirable as it maintains the “physical” nature of the model. Parameters such as DVT0, that define the short channel threshold voltage behavior of a MOSFET, are physically extracted. In contrast to the scalable modeling approach, the “binned” model methodology divides the channel length and width space into multiple “bins” and model parameter sets for each of the bins are independently extracted. Eq. 1 is used to make the model parameters continuous across bin boundaries. Parameters such as DVT0 have no physical meaning. A significant advantage of the scalable model approach is in the corner and statistical modeling. These models are generated by changing process specific model parameters such as mobility and channel length, and are intuitively more accurate if the original model was physically extracted.

2.2.2 “Golden” die selection

A rigorous Quality Assurance (QA) methodology was used to select the “golden” die on which detailed measurements are performed and the model parameters extracted. Electrical specifications (E-spec) such as threshold voltage, saturation current, body constant were measured over multiple die to select the die closest to the E-spec of the technology. The geometry dependence of these parameters was also plotted to ensure a clean set of measurements. The following checklist encompasses the measured data QA:

TABLE 2.2 Measured data QA checklist

Critical parameters (I_{dsat} for the small and short device, V_{th} for the 4 corners large, narrow, short, and small) vs. Electrical Specifications within 5%
Plot V_{th} vs. Length and Width
Plot V_{th} vs. Temperature for large device
Plot I_{dsat} vs. Length and Width
Plot I_{dsat} vs. Temperature for short channel device
Plot Body constant vs. Length and Width
Plot Body constant vs. Temperature
Plot subthreshold slope (ST) vs. L and W

Any inconsistencies observed during the QA procedure results in either the deletion of the relevant measured data point or a physical re-measurement of that parameter or sweep.

2.2.3 1.8V thin gate-oxide model parameter extraction devices:

1.8V thin gate-oxide devices were measured using the Agilent IC-CAP characterization and modeling software. Table 2.3 lists the devices that were measured at 25C, 125C and -40C.

TABLE 2.3 List of sizes of the measured 1.8V thin-oxide N and P FETs

W=10u	L=0.18, 0.2, 0.22, 0.25, 0.3, 0.4, 0.6, 1, 2, 10um	Large W, Scale channel length
L=10um	W=0.22,0.3,0.4,0.6,1, 2u	Large L, Scale channel width
W=0.22um	L=0.18, 0.2um	Small devices
L=0.18um	W=0.3,0.4um	Minimum L, scale channel width

Table 2.4 lists the various characteristics measured for each of the FETs listed in Table 2.3 .

TABLE 2.4 List of measured characteristics for 1.8V thin gate-oxide FETs

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
I_d Vs. V_{gs}	Threshold -Linear	0.05	-0.5 to 1.8, 50mV steps	0 to -1.5, in -0.3V steps
I_d Vs. V_{gs}	Threshold - Saturation	1.8	-0.2 to 1.8, 50mV steps	0 to -1.5, in -0.3V steps
I_d Vs. V_{ds}	Output	0 to 1.8V, 50mV steps	0.6 to 1.8V, 0.3 V steps	0
I_d Vs. V_{ds}	Output with back bias	0 to 1.8V, 50mV steps	0.6 to 1.8V, 0.3 V steps	-1.5

2.2.4 Dog-bone effect for thin gate-oxide devices

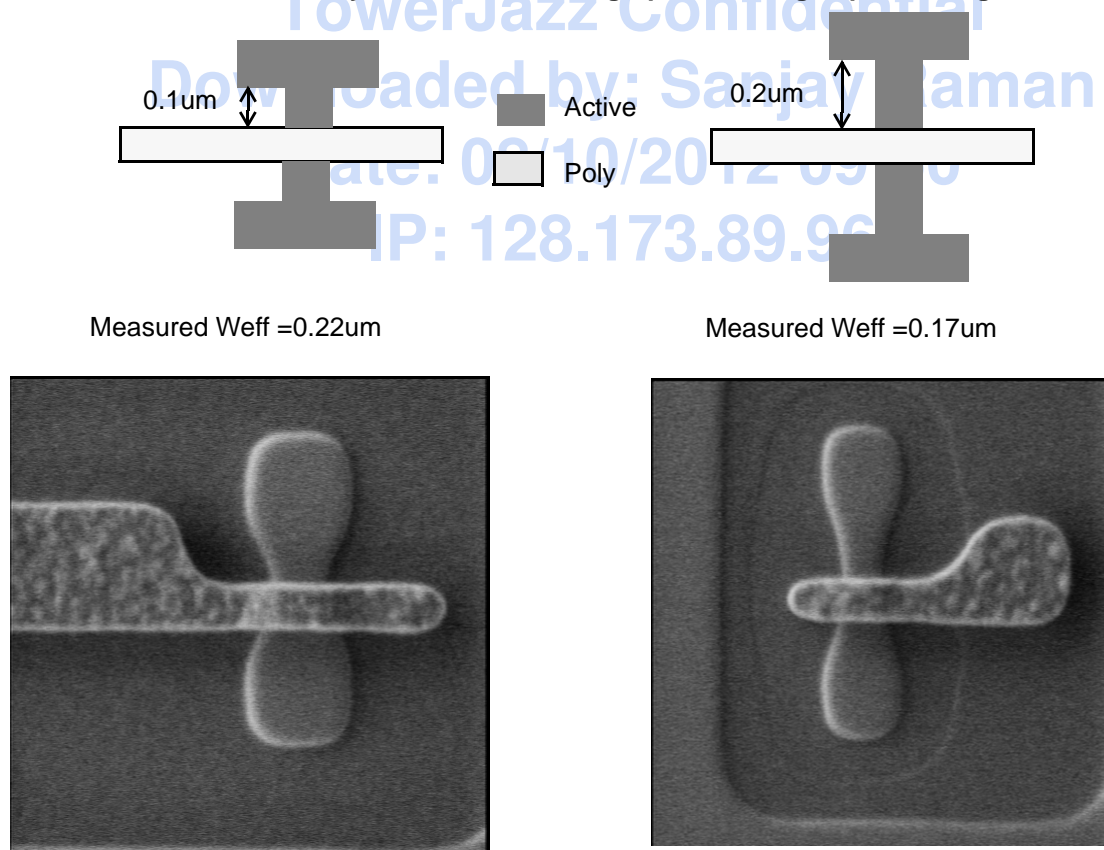
The CA18 design rules allow a minimum drawn standard FET width of 0.22μm. FETs with W smaller than 0.42μm require a dog-bone layout to make contact with the source/drain regions. The effective width of the narrow FETs ($W < 0.42\mu\text{m}$) increases as a result of the dog-bone layout. This effect is dominant for small channel lengths ($L < 0.6\mu\text{m}$). To account for the increase in W_{eff} , ΔW was gradually reduced for dog-boned FETs for small channel lengths by using the BSIM3v3 parameters WL and WW in Eq. 2:

$$\Delta W = WINT + \frac{WL}{L^{WLN}} + \frac{WW}{W^{WLN}} + \frac{WWL}{L^{WLN} \times W^{WLN}} \quad (\text{EQ 2})$$

SEM micrographs of the small device ($W/L=0.22/0.18\mu\text{m}$) with varying active-shoulder edge to gate-poly edge spacing are shown in Figure 2.2. The impact of shrinking the gate-poly edge to active edge spacing from 0.2μm to the minimum design rule can be clearly seen in the measured W_{eff} values that increase from 0.17μm to 0.22μm. This can result in a large spread in the measured values of the saturation current (I_{dsat}) for these devices. These are captured in the corner E-specs of this parameter for the small devices.

No dog-bone layout is required for thick-oxide FETs, even with minimum channel width of 0.4μm.

FIGURE 2.2 Schematic of layout and SEM micrographs showing impact of dog-bone on W_{eff} .



2.2.5 3.3V thick gate-oxide model parameter extraction devices:

3.3V thick gate-oxide devices were measured using the Agilent IC-CAP characterization and modeling software. Table 2.5 lists the devices that were measured at 25C, 125C and -40C.

TABLE 2.5 List of measured characteristics for 3.3V thick gate-oxide FETs

NFET		
W=10um	L=0.36, 0.38, 0.42, 0.5, 0.6, 0.8, 1, 2, 10um	Large W, Scale channel length
L=10um	W=0.4, 0.5, 0.6, 1, 2um	Large L, Scale channel width
W=0.4um	L=0.36, 0.38, 0.42um	Small devices
L=0.36um	W=0.5, 0.6um	Minimum L, scale channel width
PFET		
W=10um	L=0.3, 0.32, 0.36, 0.42, 0.5, 0.6, 0.8, 1, 2, 10um	Large W, Scale channel length
L=10um	W=0.4, 0.5, 0.6, 0.8, 2um	Large L, Scale channel width
W=0.4um	L=0.32, 0.36um	Small devices
L=0.3um	W=0.5, 0.6um	Minimum L, scale channel width

Table 2.6 lists the various characteristics measured for each of the FETs listed in Table 2.5 .

TABLE 2.6 List of measured characteristics for 3.3V thick-oxide FETs

Characteristic	Type	V _{DS} (V)	V _{GS} (V)	V _{BS} (V)
Id Vs. Vgs	Threshold - Linear	0.05	0 to 3.3, 100mV steps	0 to -3, in -0.6V steps
Id Vs. Vgs	Threshold - Saturation	3.3	0 to 3.3, 100mV steps	0 to -3, in -0.6V steps
Id Vs. Vds	Output	0 to 3.3V, 100mV steps	0.55 to 3.3V, 0.55 V steps	0
Id Vs. Vds	Output with back bias	0 to 3.3V, 100mV steps	0.55 to 3.3V, 0.55 V steps	-3

2.2.6 3.3V thick gate-oxide native NFET model parameter extraction devices

3.3V thick gate-oxide native NFET devices were measured using the Agilent IC-CAP characterization and modeling software. Table 2.7 lists the devices that were measured at 25C, 125C and -40C. Table 2.8 lists the various characteristics measured for each of the FETs listed in Table 2.7 .

TABLE 2.7 List of sizes of the measured thick-oxide 3.3V Native NFETs

NFET		
W=10um	L=1, 1.2, 2, 5, 10um	Large W, Scale channel length
L=10um	W=0.4, 0.5, 0.6, 1.2, 2, 5, 10um	Large L, Scale channel width
W=0.4um	L=1.2um	Small device
L=1.2um	W=0.4, 0.5, 0.6, 1.2, 5um	Short L, scale channel width

TABLE 2.8 List of measured characteristics for 3.3V thick-oxide native NFETs

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold - Linear	0.05	-1 to 3.3, 50mV steps	0 to -3, in -0.6V steps
Id Vs. Vgs	Threshold - Saturation	3.3	-1 to 3.3, 50mV steps	0 to -3, in -0.6V steps
Id Vs. Vds	Output	0 to 3.3V, 50mV steps	-0.55 to 3.3V, 0.55 V steps	0
Id Vs. Vds	Output with back bias	0 to 3.3V, 50mV steps	-0.55 to 3.3V, 0.55 V steps	-3

2.2.7 5V thick gate-oxide model parameter extraction devices:

5V thick gate-oxide devices were measured using the Agilent IC-CAP characterization and modeling software. Table 2.9 lists the devices that were measured at 25C, 125C and -40C. Table 2.10 lists the various characteristics measured for each of the FETs listed in Table 2.9 .

TABLE 2.9 List of sizes of the measured 5V thick-oxide N & P Fets

NFET		
W=10um	L= 0.6, 0.7, 0.8, 0.9,1.4,1.9, 9.9 um	Large W, Scale channel length
L=9.9um	W = 0.6, 0.8, 1.2, 2, 10 um	Large L, Scale channel width
W x L	0.6 x 0.7, 0.7 x 0.7 um	Small Devices
L=0.6um	W = 10 um	Minimum L, scale channel width
PFET		
W=10um	L= 0.6, 0.7, 0.8, 0.9, 1, 1.5, 2, 10 um	Large W, Scale channel length
L=10um	W = 0.6, 0.8, 1, 1.2, 2, 10 um	Large L, Scale channel width
W x L	0.6 x 0.6, 0.7 x 0.8, 0.8 x 0.6 um	Small devices
L=0.6um	W = 0.6, 0.8, 1.2, 10	Minimum L, scale channel width

TABLE 2.10 List of measured characteristics for 5V thick-oxide FETs

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold - Linear	0.05	0 to 5, 50mV steps	0 to -4, in -0.8V steps
Id Vs. Vgs	Threshold - Saturation	5	0 to 5, 50mV steps	0 to -4, in -0.8V steps
Id Vs. Vds	Output	0 to 5V, 50mV steps	1 to 5V, 1 V steps	0
Id Vs. Vds	Output with back bias	0 to 5V, 50mV steps	1 to 5V, 1 V steps	-4

2.2.8 5V thick gate-oxide native NFET model parameter extraction devices:

5V thick gate-oxide native NFETs were measured using the Agilent IC-CAP characterization and modeling software. Table 2.11 lists the devices that were measured at 25C, 125C and -40C. Table 2.12 lists the various characteristics measured for each of the FETs listed in Table 2.11 .

TABLE 2.11 List of sizes of the measured 5V thick-oxide native NFets

NFET		
W=10um	L= 1.2, 1.5, 2, 5, 10um	Large W, Scale channel length
L=10um	W = 0.4, 1, 2, 5, 10 um	Large L, Scale channel width
W x L	0.4 x 1 um	Small Device
L=1.2um	W = 10 um	Minimum L, scale channel width

TABLE 2.12 List of measured characteristics for 5V thick-oxide native NFETs

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold - Linear	0.05	-1 to 5, 100mV steps	0 to -4, in -1V steps
Id Vs. Vgs	Threshold - Saturation	5	-1 to 5, 100mV steps	0 to -4, in -1V steps
Id Vs. Vds	Output	0 to 5V, 100mV steps	0 to 5V, 1 V steps	0
Id Vs. Vds	Output with back bias	0 to 5V, 100mV steps	0 to 5V, 1 V steps	-4

2.3 Parameter Extraction

2.3.1 IV parameters

BSIM3v3.2 model parameters were physically extracted using BSIM3 Modeling Package [1, 2]. Local optimization of selected parameters to the appropriate regions of the measured device characteristics was performed to better fit the measured data. RMS fitting errors were typically less than 1% on the I_D - V_{DS} curves and less than 3% on the g_{out} - V_{DS} curves. Maximum fitting errors were typically less than 3% on the I_D - V_{DS} curves and less than 15% on the g_{out} - V_{DS} curves. RMS fitting errors were typically less than 1% on the I_D - V_{GS} curves and less than 2% on the g_m - V_{GS} curves. Maximum fitting errors were typically less than 3% on the I_D - V_{GS} curves and less than 5% on the g_m - V_{GS} curves.

The temperature dependence of the model parameters was captured by using the relevant BSIM3v3 parameters to fit the measured data at -40C and 125C. The large channel threshold voltage in the linear and saturation regions, high field and back bias dependent mobility, the short channel threshold voltage and saturation currents, and the temperature dependence of the series drain/source resistances were fit to the measured data.

2.3.2 Capacitance parameters

Junction capacitances were measured for bottom, field sidewall, and channel sidewall intensive structures. This capacitance was characterized for biases ranging from a small forward bias (0.2V) to a reverse bias equal to 1.8V for the 1.8V thin-oxide devices, 3.3V for the 3.3V thick-oxide devices, and 5V for the 5V thick-oxide devices. Capacitance data for 5V native fets is currently not available. The measured values were separated

into bottom (CJ), field sidewall (CJSW) and channel sidewall components (CJSWG) parameters by simultaneously solving the 3 equations.

The gate oxide capacitance was measured on two large area test structures. The first structure is a MOS capacitor and allows the accumulation and depletion region CV parameters to be extracted. The second structure is a MOS transistor which allows the inversion region CV parameters to be extracted. The gate capacitance was fitted by using CAPMOD=3 model in BSIM3v3.2. This model takes into account quantum mechanical and poly depletion effects. The maximum error in fitting the intrinsic gate capacitances in inversion was less than 3%.

The gate-to-source/drain overlap capacitances and their bias dependencies were measured on very wide multi-finger FETs and channel lengths of 0.18 μm for standard devices, 0.36 μm for 3.3V thick gate-oxide devices, 1 μm for 3.3V thick gate-oxide native devices, and 0.6 μm for 5V thick gate-oxide devices. The gate overlap capacitance is a function of both the gate to source/drain bias, and the substrate bias. Only the gate to source/drain bias dependence is currently modeled in BSIM3v3.2.

The accuracy of the extracted capacitance parameters for the 1.8V thin and 3.3V thick-oxide FETs was verified by matching the measured delay times of a set of 10 ring-oscillators for each device type. The measured and simulated delay/stage for various ring-oscillator configurations are shown for the low and high voltage FETs in Table 2.13 .

TABLE 2.13 Ring oscillator delay/stage.

Transistor	Ring Osc. load	Measured delay/stage (ps)	Simulated delay/stage (ps)
1.8V	No load	42.4	41.1
	2x N-gate	136.1	142.4
	5x N-gate	170.7	175.4
	2x P-gate	141.5	144.7
3.3V	No load	78.6	80.2
	2x N-gate	189.8	196.2
	5x N-gate	225.3	230.1
	2x P-gate	196.9	205.2
	5x P-gate	229.4	242.3

The model parameter set fitted to the measurements is referred to as the “measured” case.

2.4 Model Verification

The simulated IV and CV characteristics of the various MOSFETs are compared with the measured data in Figures 2.3 through 2.146. The device description is included in the figure caption and has the format of “max_operating_voltage_fet_Type_WxL_plotType_temperature”. For e.g. 1p8v_NFET_10x10_idvg_25C refers to the I_{drain} Vs. V_{gate} characteristic at 25C of a thin oxide NFET with $W=10\mu\text{m}$ and $L=10\mu\text{m}$.

The CV plots show 6 different plots of MOSFET capacitances. The top 3 plots are for junction capacitance from area, perimeter, and perimeter-under-gate intensive structures. The bottom-left plot is for the oxide capaci-

tance from a pure MOS capacitor, which the bottom-middle plot is the oxide capacitance in a large area MOSFET. Finally, the bottom-right plot is for an large channel width transistor with the bulk floating and captures the overlap capacitance from gate to source/drain.

The IV plots show the threshold and output characteristics of the MOSFET. The threshold curves are a set of 6 plots, for I_d vs. V_{gs} in the linear region (top-left), I_d vs. V_{gs} in the saturation region (top-middle), and sub-threshold I_d vs. V_{gs} (top-right). The transconductance in the linear region (bottom left), transconductance in the saturation region (middle-right), and the substrate current vs. gate bias in saturation are shown in the second row. The output curves are a set of 4 plots: I_d vs. V_{ds} (top-left), I_d vs. V_{ds} with back-bias (top-right), and g_{ds} vs. V_{ds} (bottom-left), and g_{ds} vs. V_{ds} with back-bias (bottom-right).

Finally, the blue-circles are the measured data, and solid red lines are the model prediction.

FIGURE 2.3 1p8_NFET_cv_25C

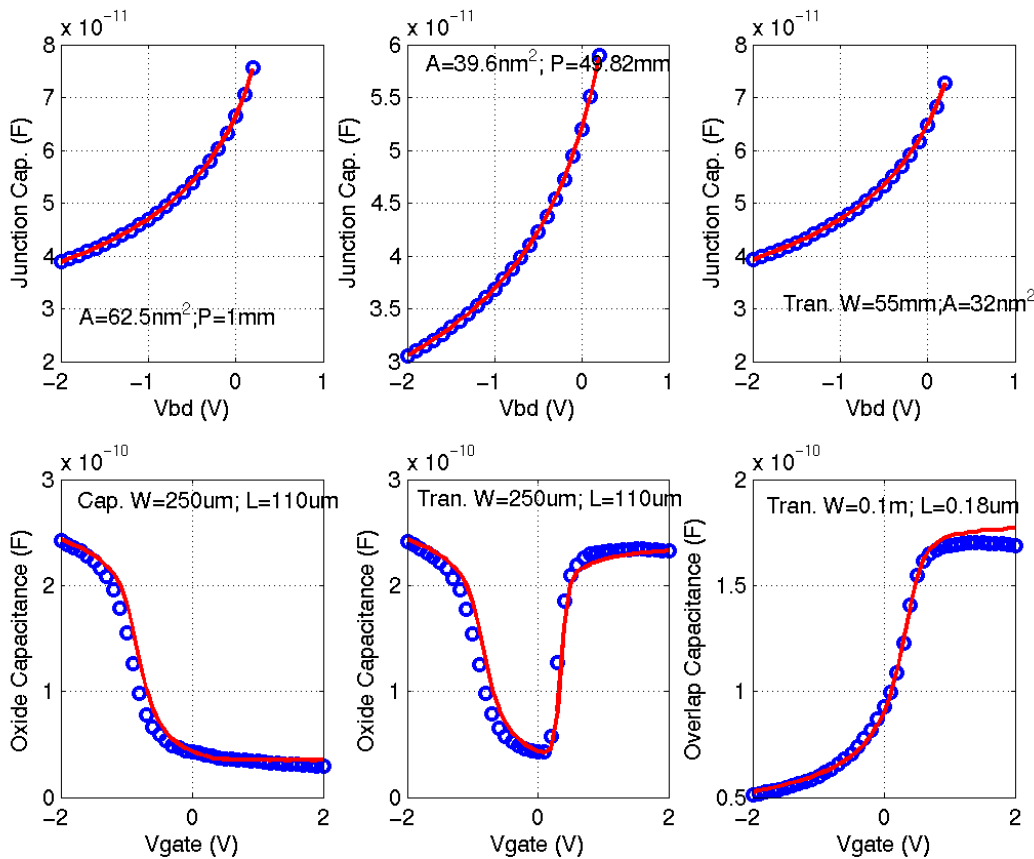
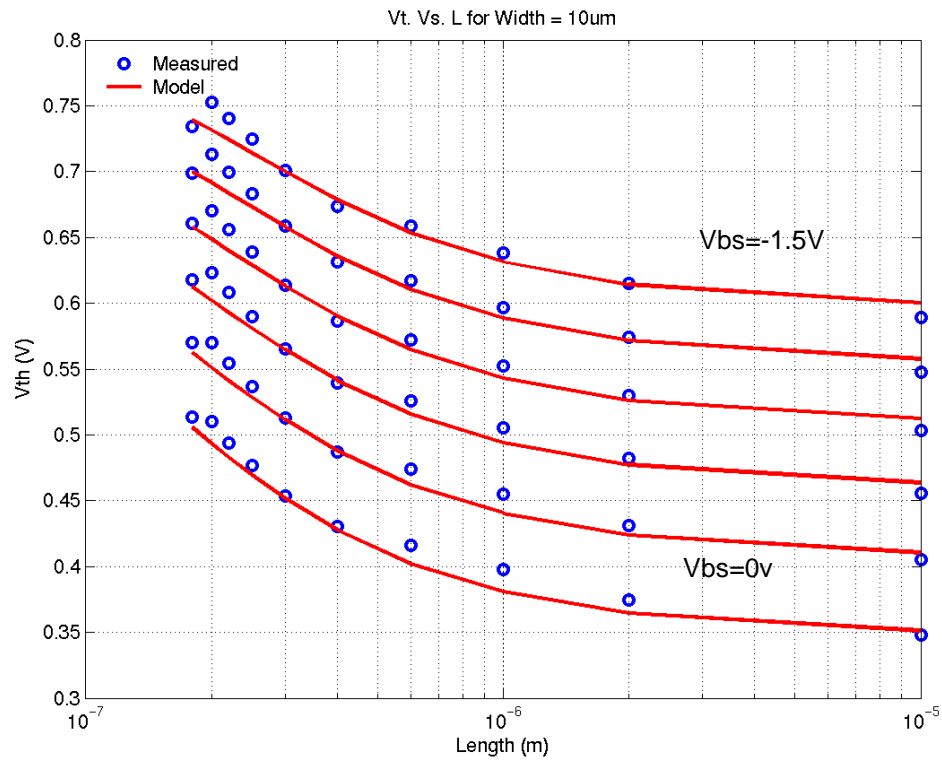


FIGURE 2.4 1p8v_NFET_vtVsL_25C



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IP: 128.173.89.96

FIGURE 2.5 1p8v_NFET_vtVsW_25C

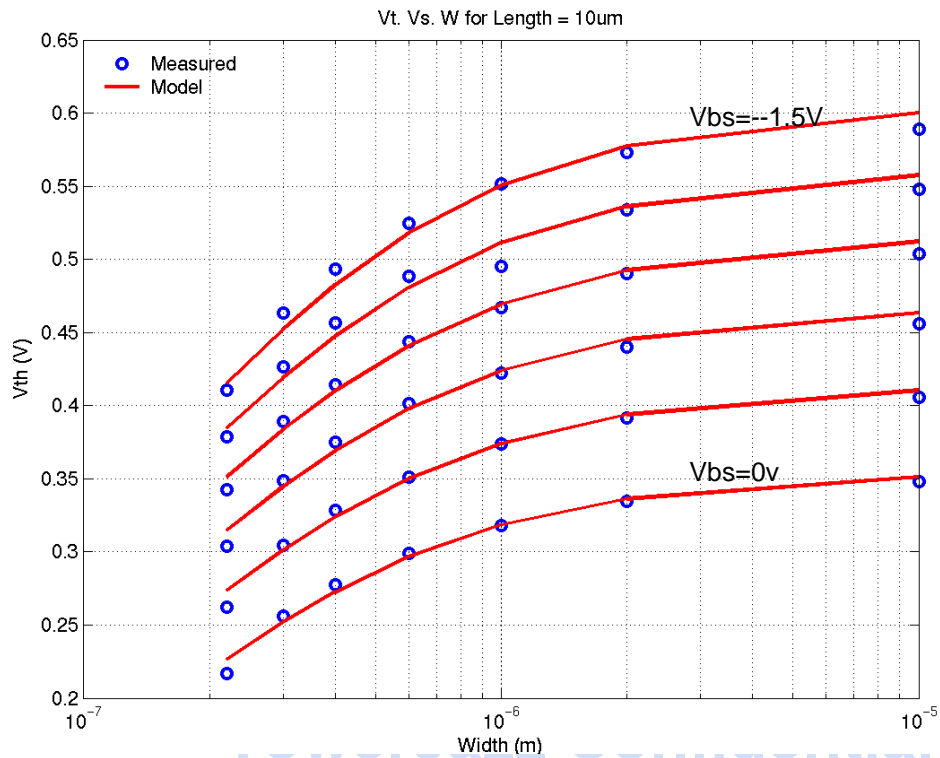


FIGURE 2.6 1p8v_NFET_10x10_idvd_25C

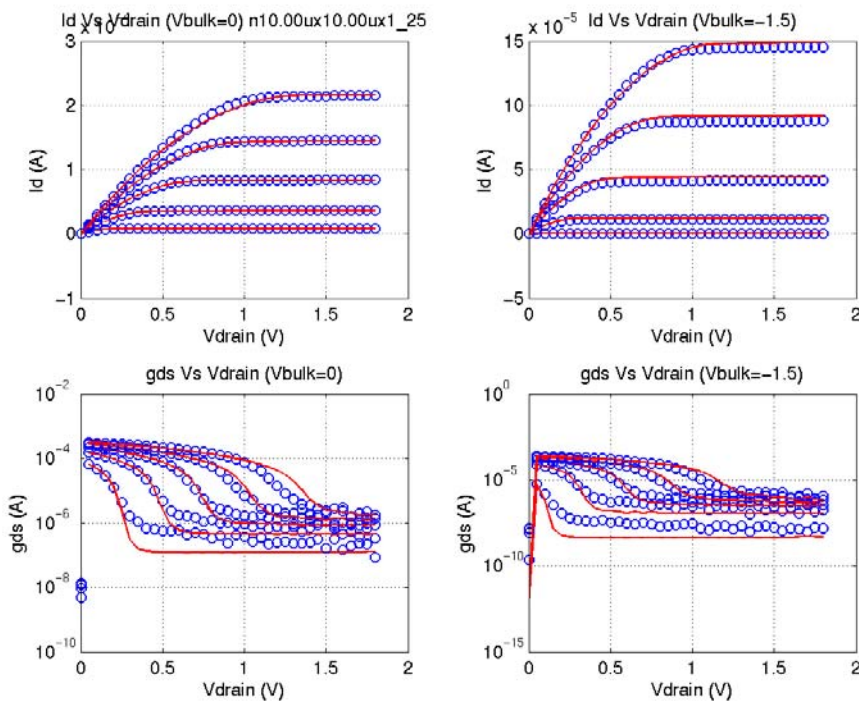


FIGURE 2.7 1p8v_NFET_10x0p18_idvg_25C

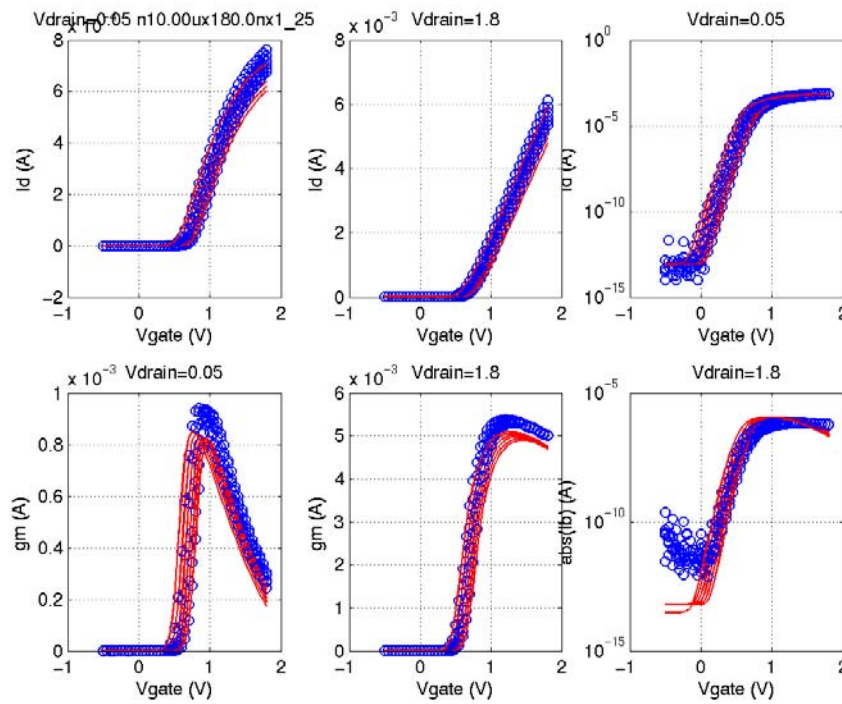


FIGURE 2.8 1p8v_NFET_10x0p18_idvd_25C

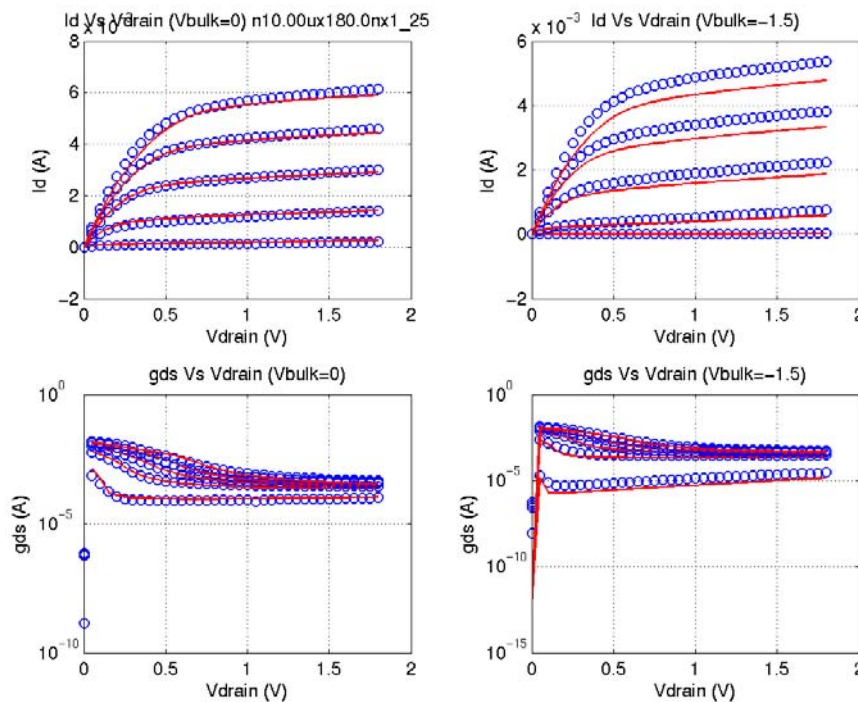


FIGURE 2.9 1p8v_NFET_0p22x10_idvg_25C

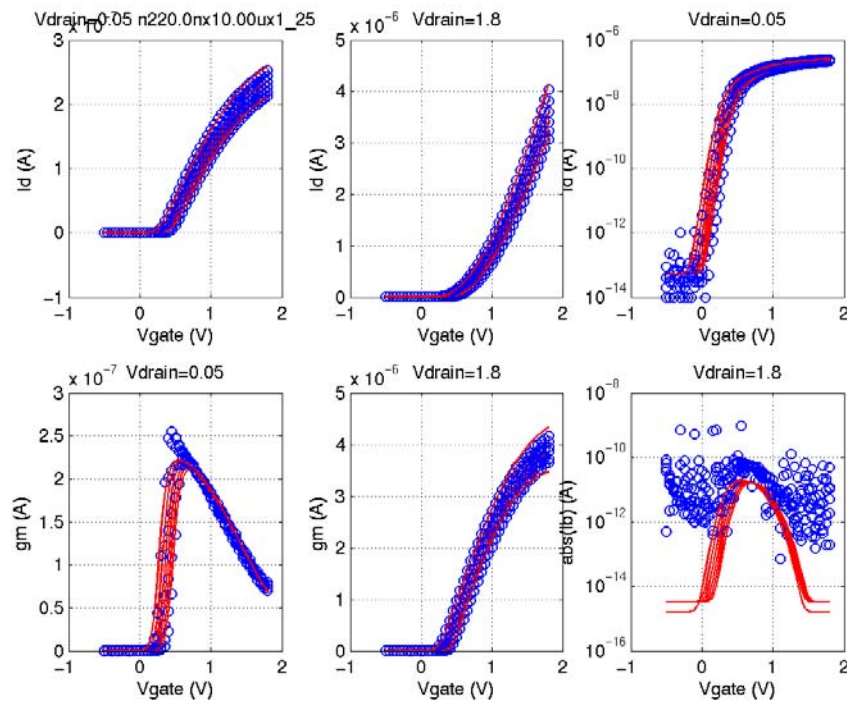


FIGURE 2.10 1p8v_NFET_0p22x10_idvd_25C

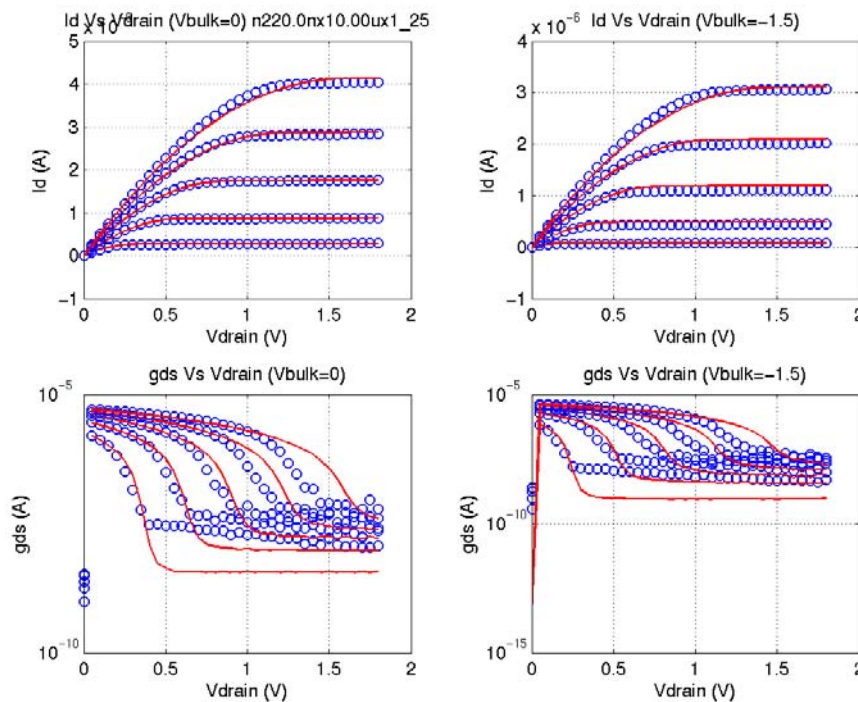


FIGURE 2.11 1p8v_NFET_0p22x0p18_idvg_25C

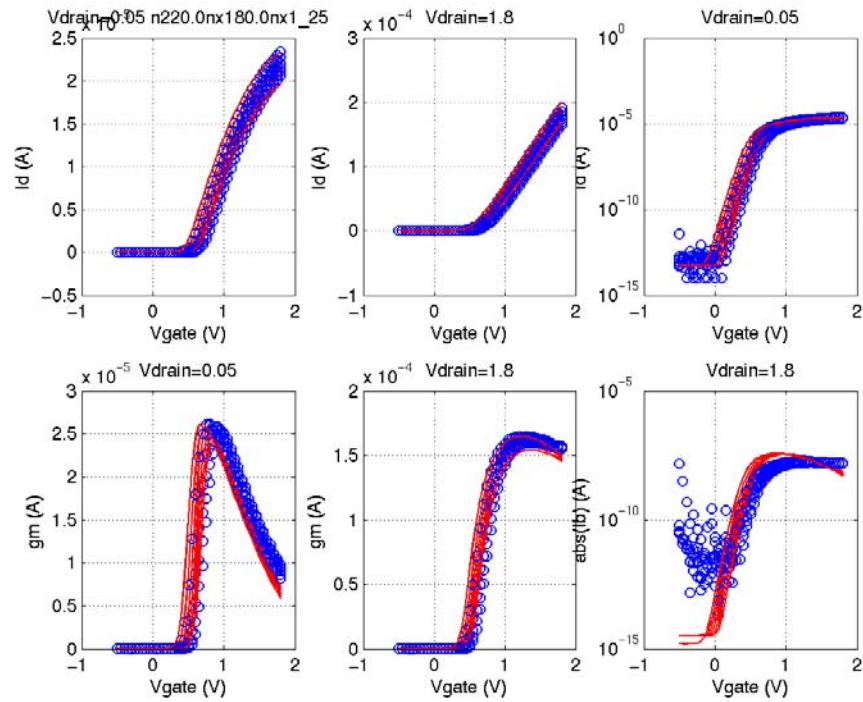


FIGURE 2.12 1p8v_NFET_0p22x0p18_idvd_25C

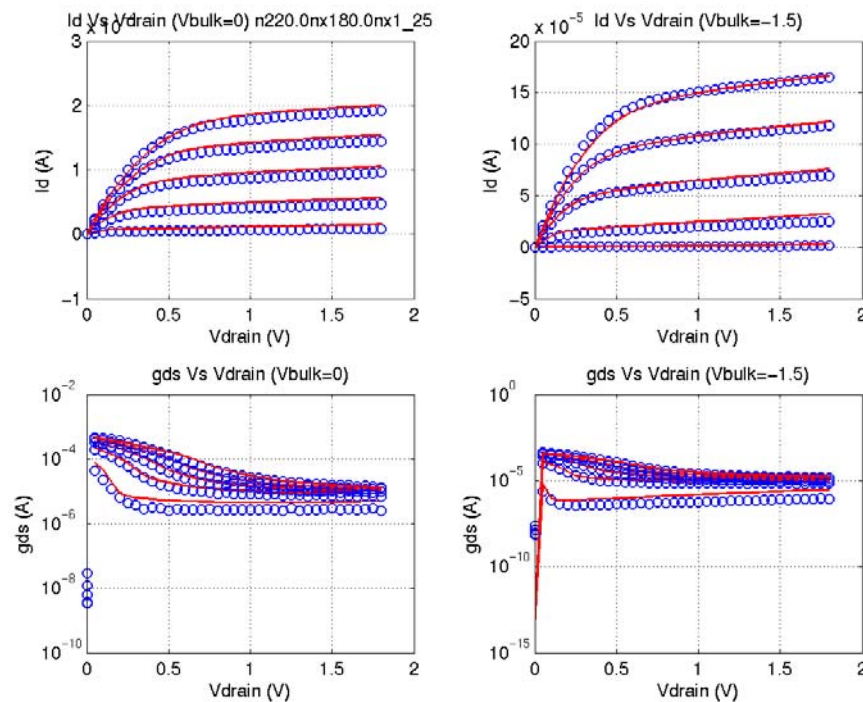


FIGURE 2.13 1p8v_NFET_0p4x0p18_idvg_25C

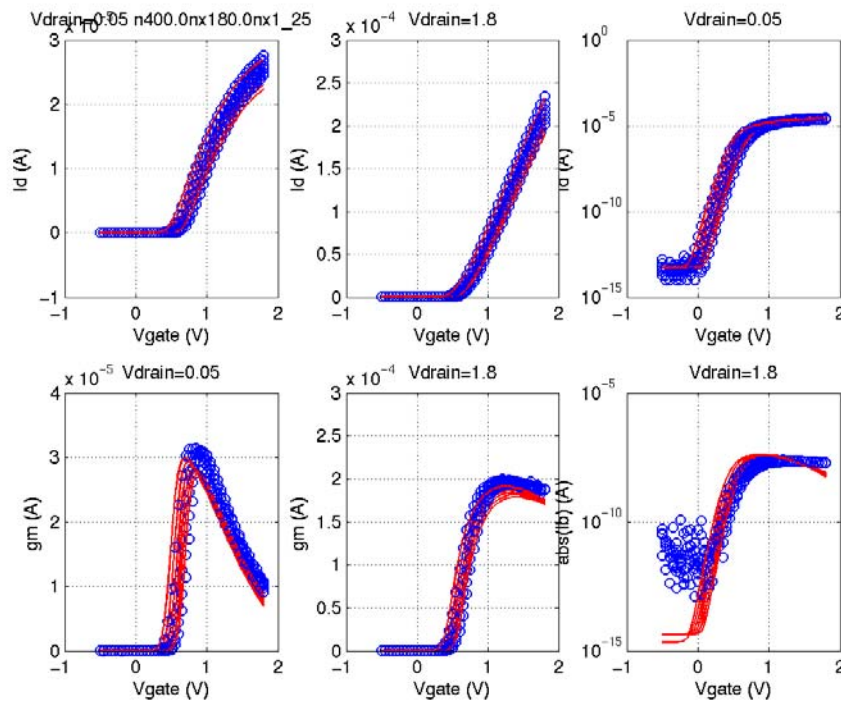


FIGURE 2.14 1p8v_NFET_0p4x0p18_idvd_25C

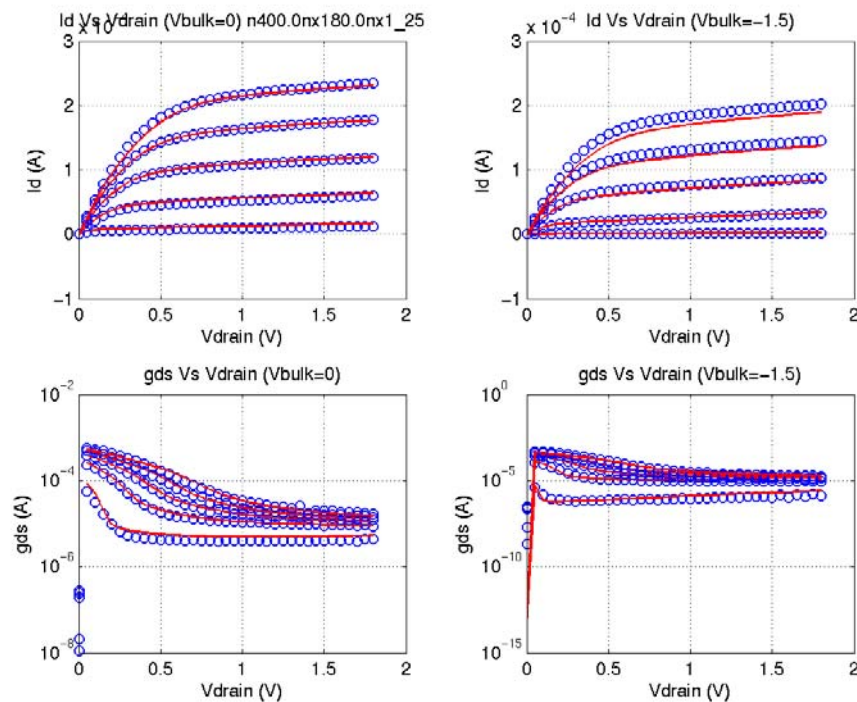


FIGURE 2.15 1p8v_NFET_10x0p25_idvg_25C

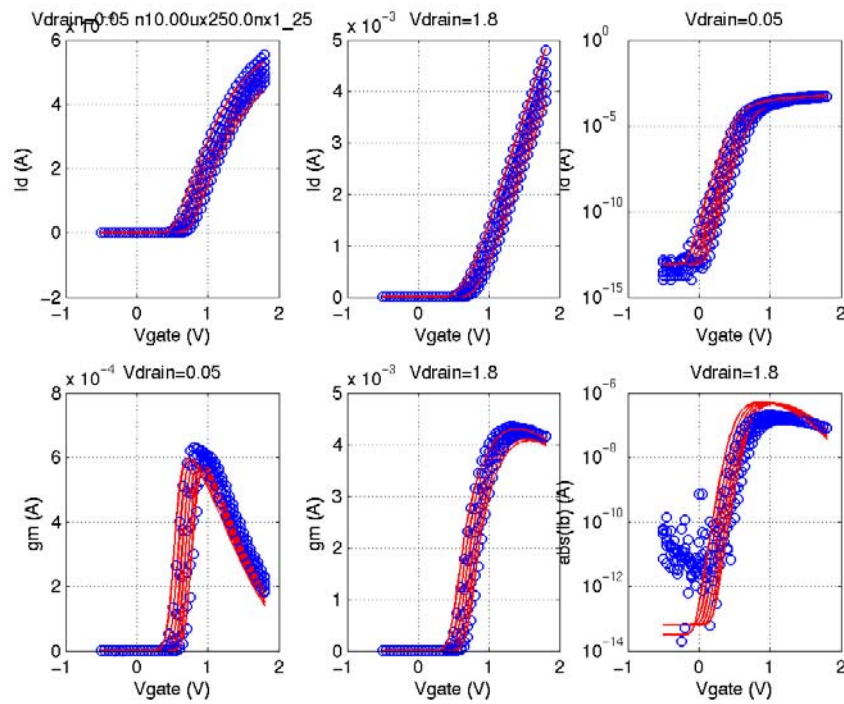


FIGURE 2.16 1p8v_NFET_10x0p25_idvd_25C

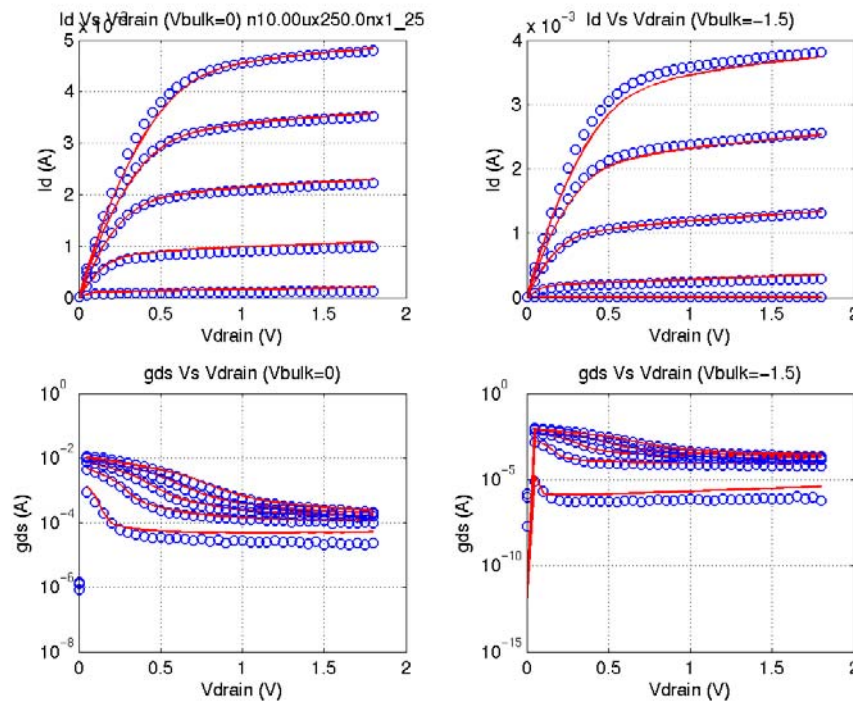


FIGURE 2.17 1p8v_NFET_10x0p18_idvg_-40C

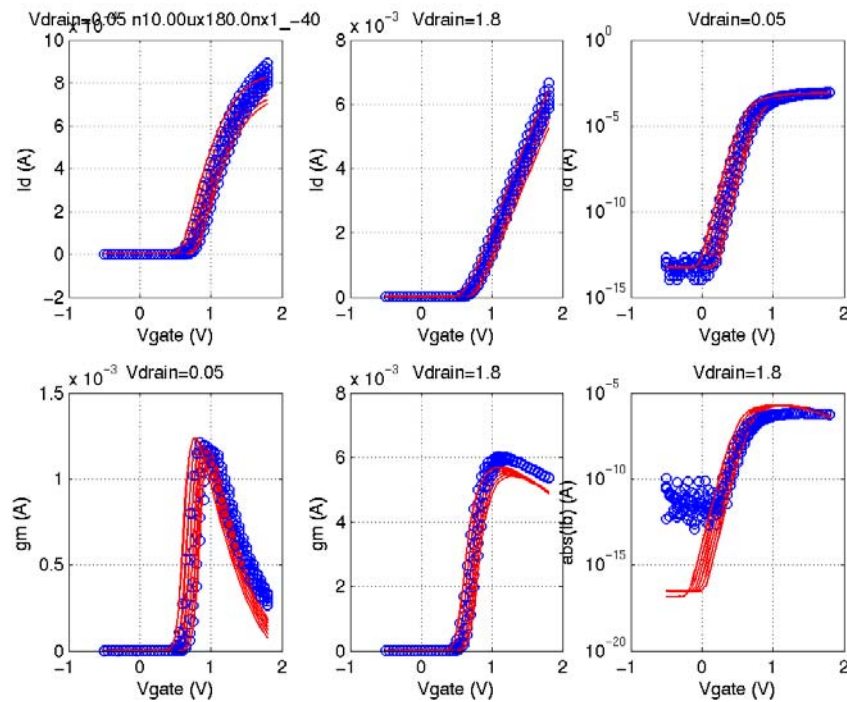


FIGURE 2.18 1p8v_NFET_10x0p18_idvd_-40C

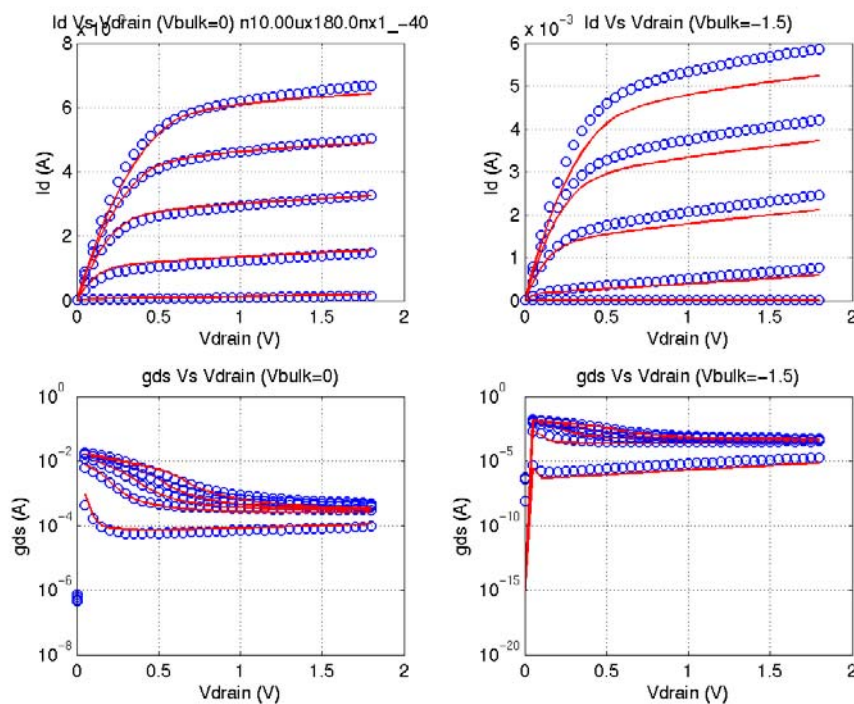


FIGURE 2.19 1p8v_NFET_10x0p18_idvg_125C

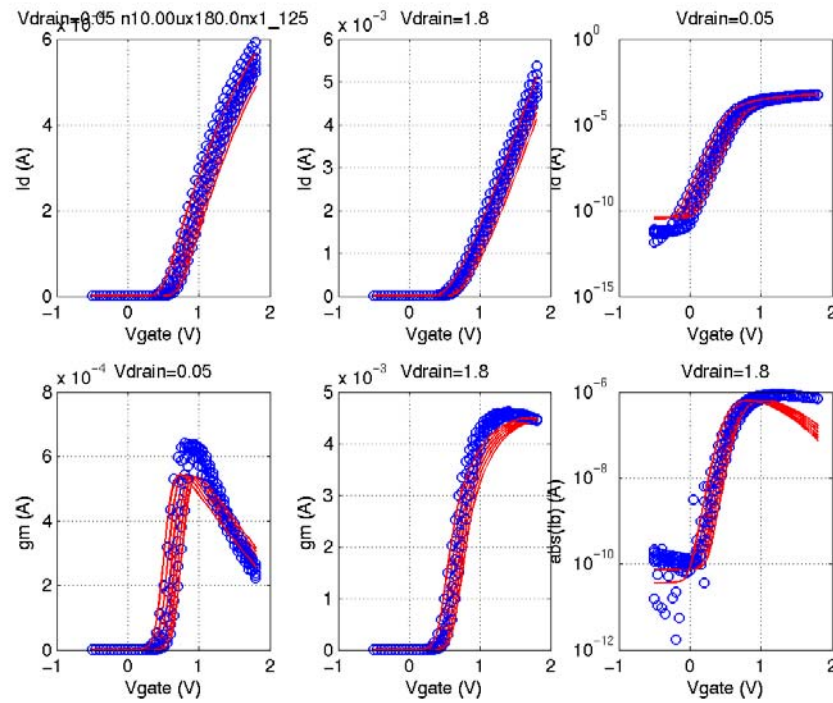


FIGURE 2.20 1p8v_NFET_10x0p18_idvd_125C

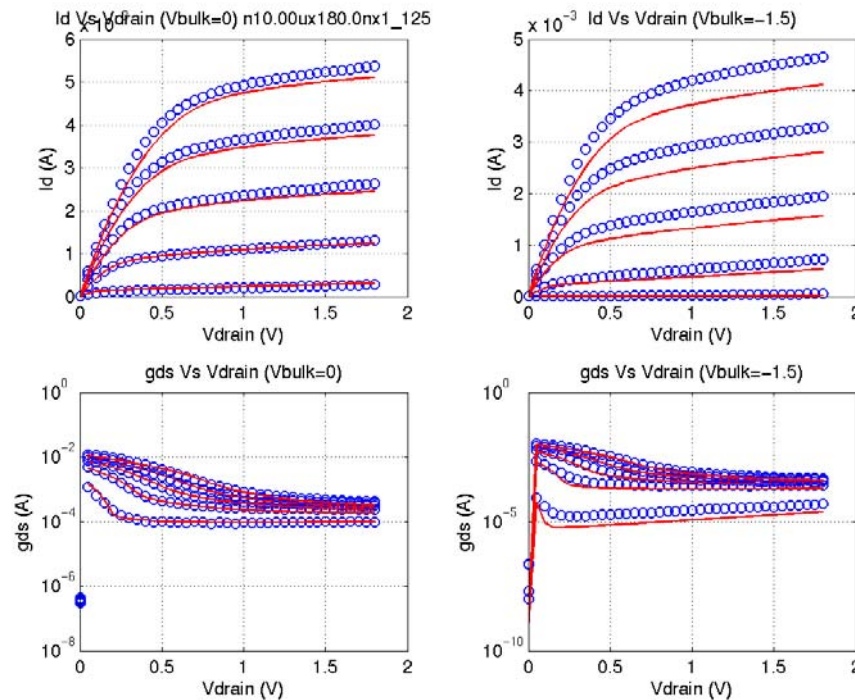


FIGURE 2.21 1p8_PFET_cv_25C

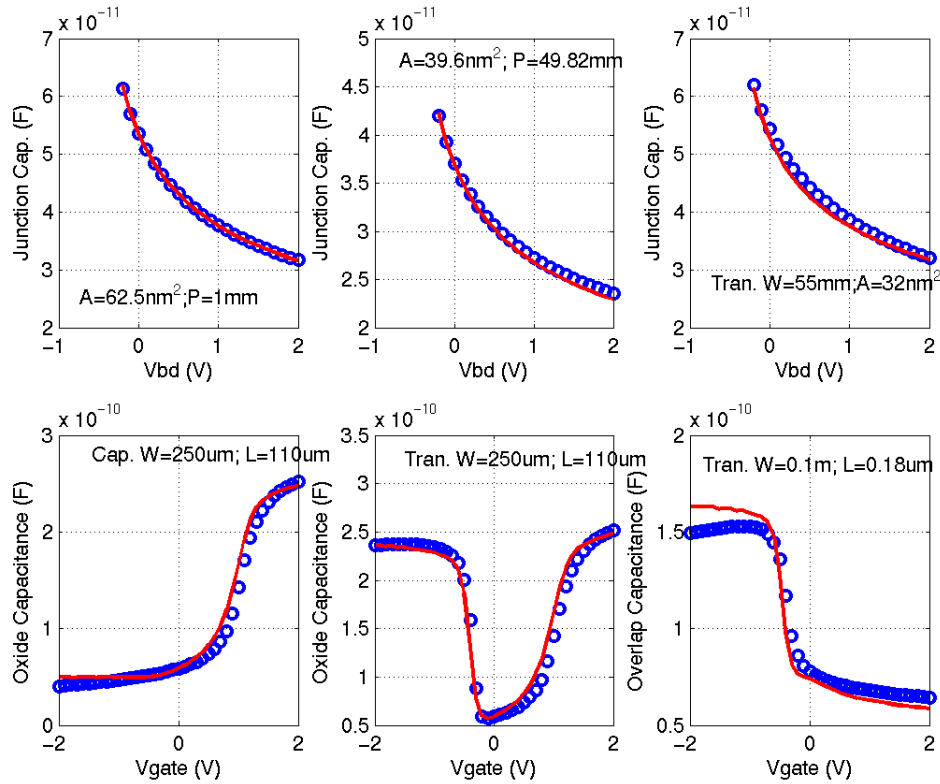


FIGURE 2.22 1p8v_PFET_vtVsL_25C

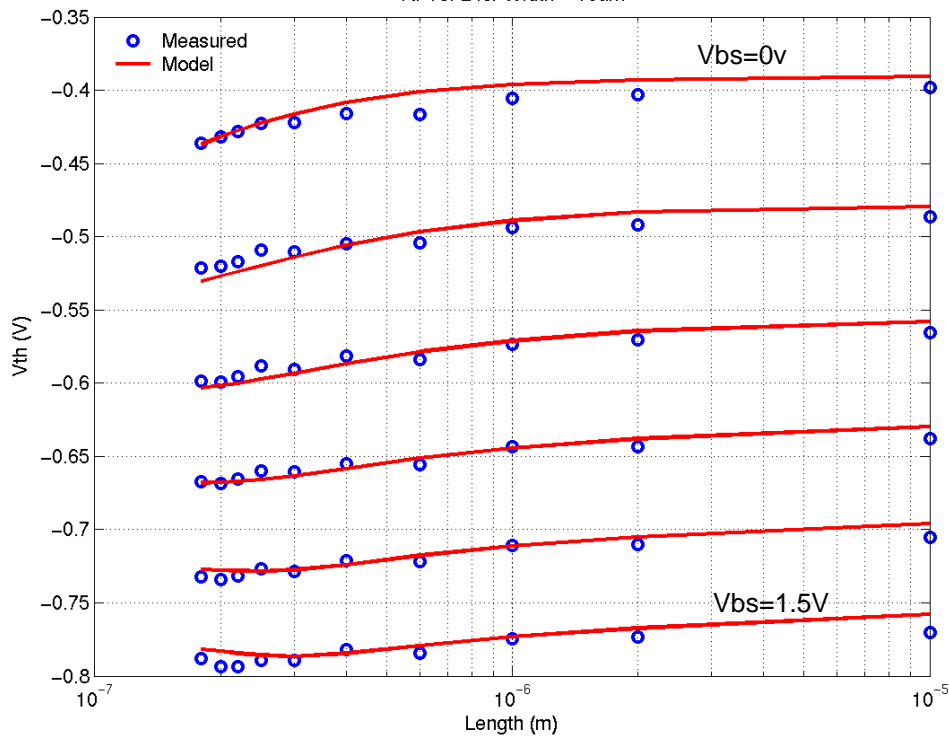


FIGURE 2.23 1p8v_PFET_vtVsW_25C

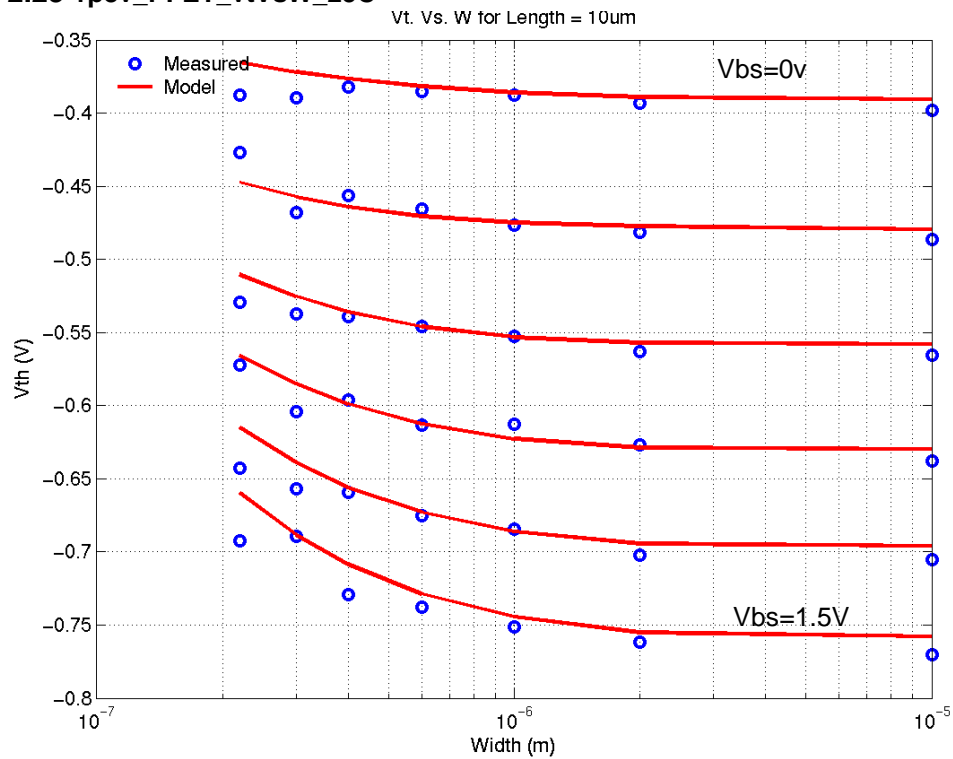


FIGURE 2.24 1p8v_PFET_10x10_idvg_25C

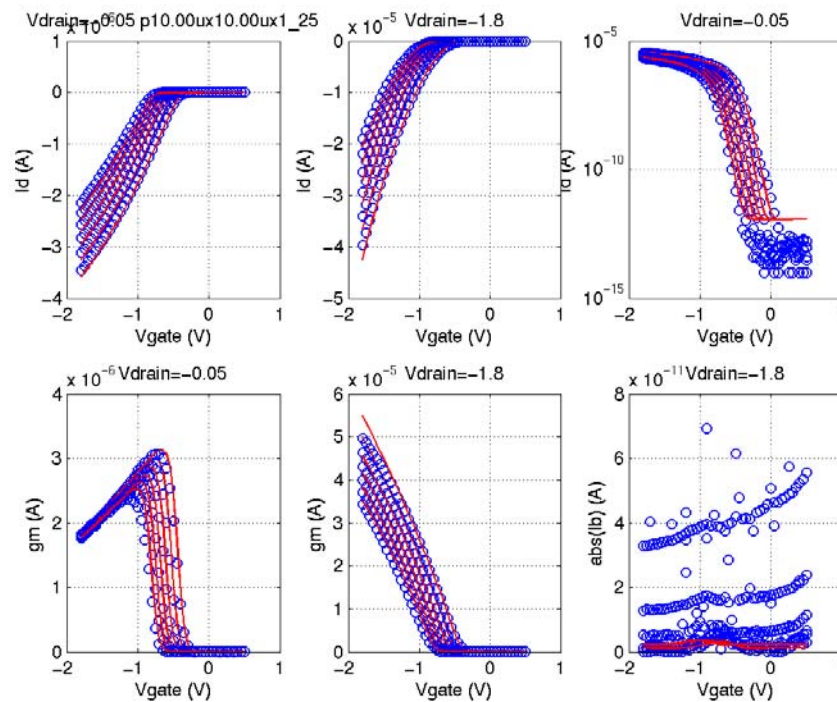


FIGURE 2.25 1p8v_PFET_10x10_idvd_25C

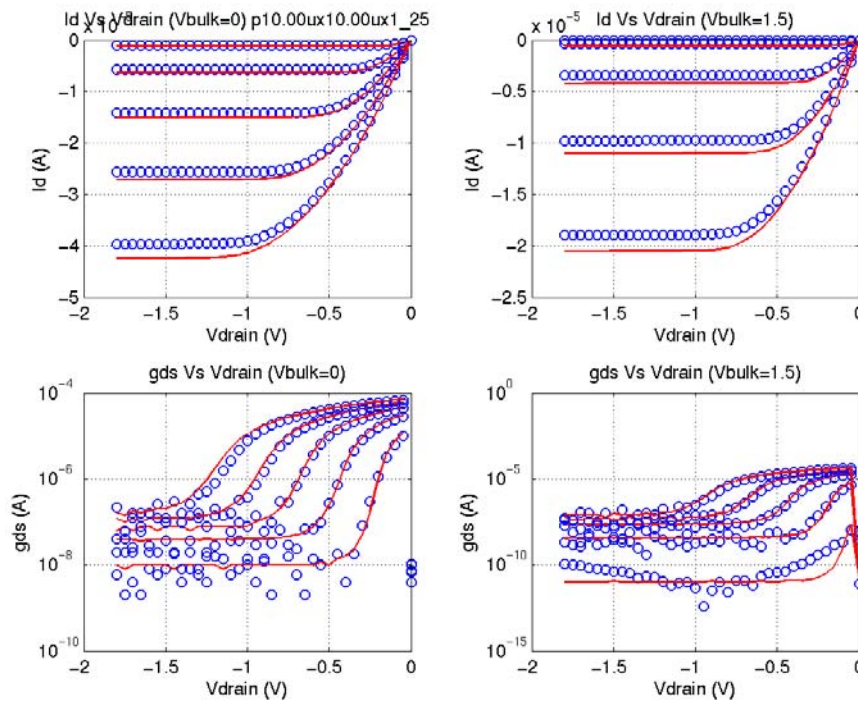


FIGURE 2.26 1p8v_PFET_10x0p18_idvg_25C

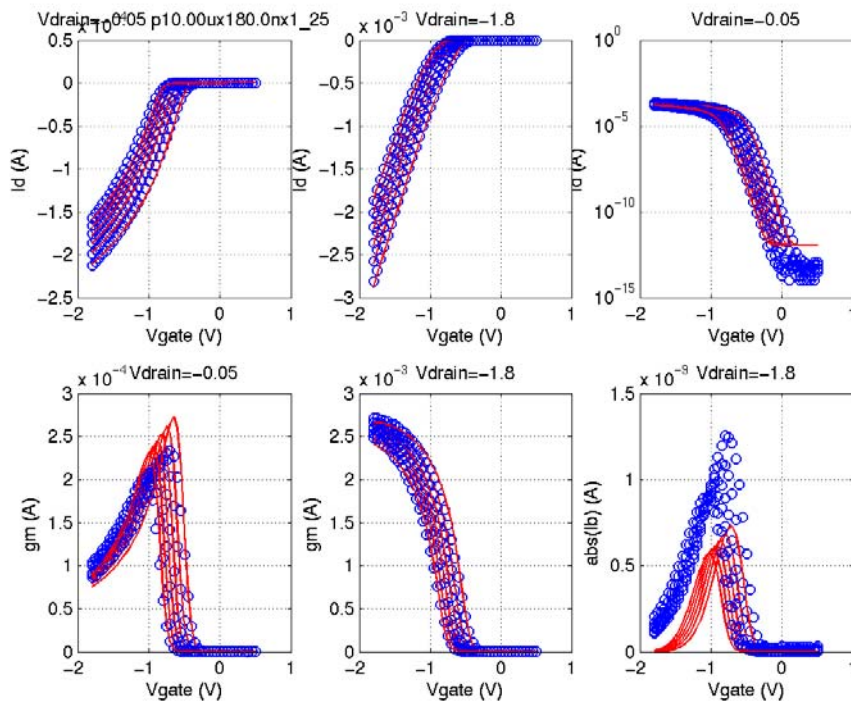


FIGURE 2.27 1p8v_PFET_10x0p18_idvd_25C

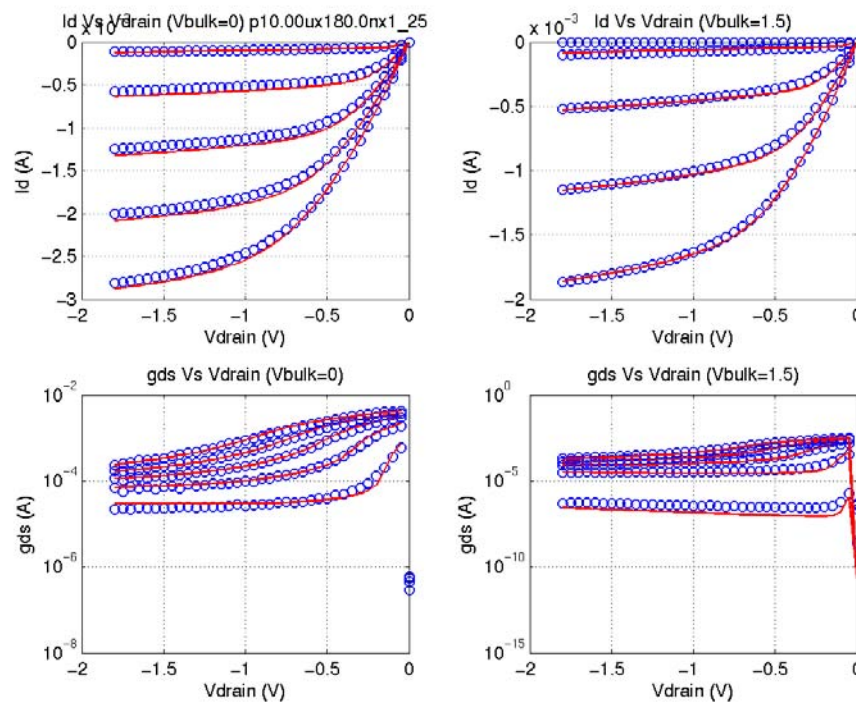


FIGURE 2.28 1p8v_PFET_0p22x10_idvg_25C

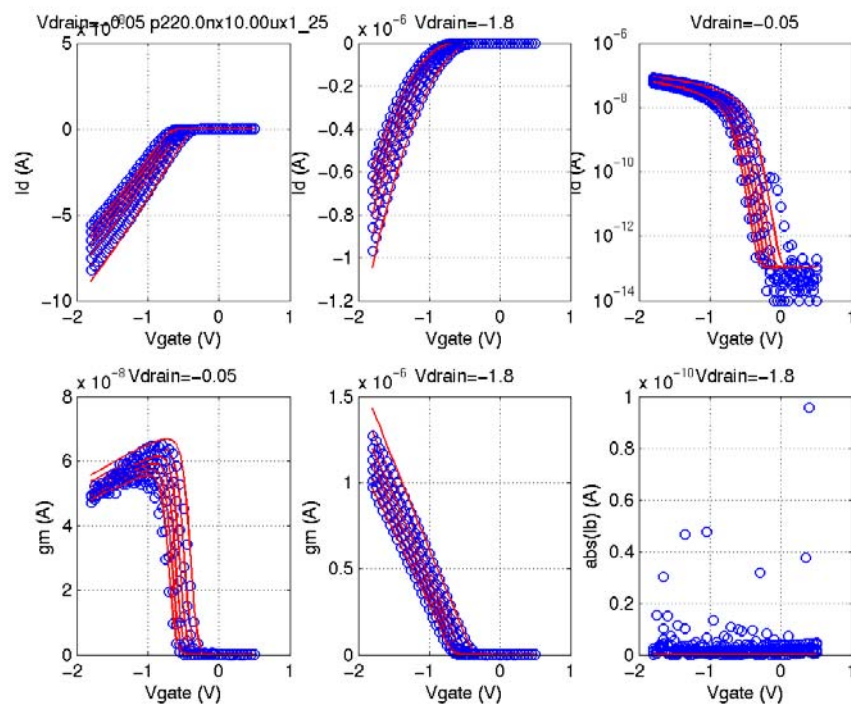


FIGURE 2.29 1p8v_PFET_0p22x10_idvd_25C

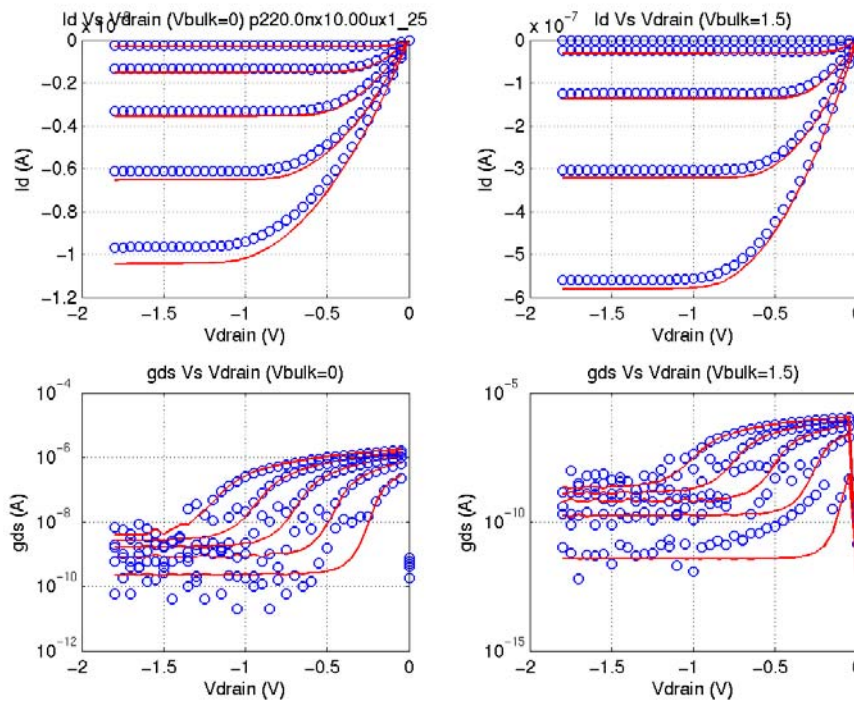


FIGURE 2.30 1p8v_PFET_0p22x0p18_idvg_25C - isolated “non-dogbonned” structure

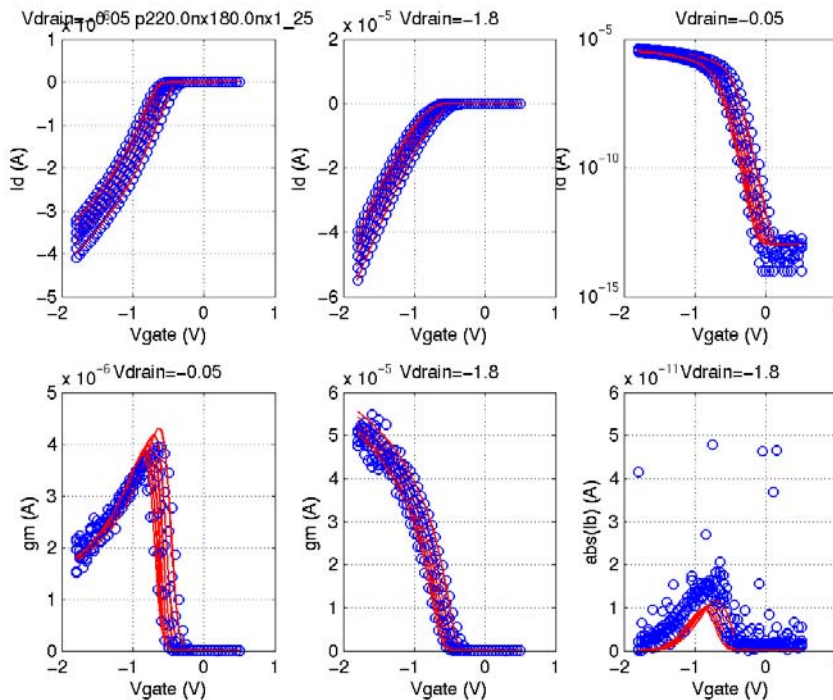


FIGURE 2.31 1p8v_PFET_0p22x0p18_idvd_25C - isolated “non-dogbonned” structure

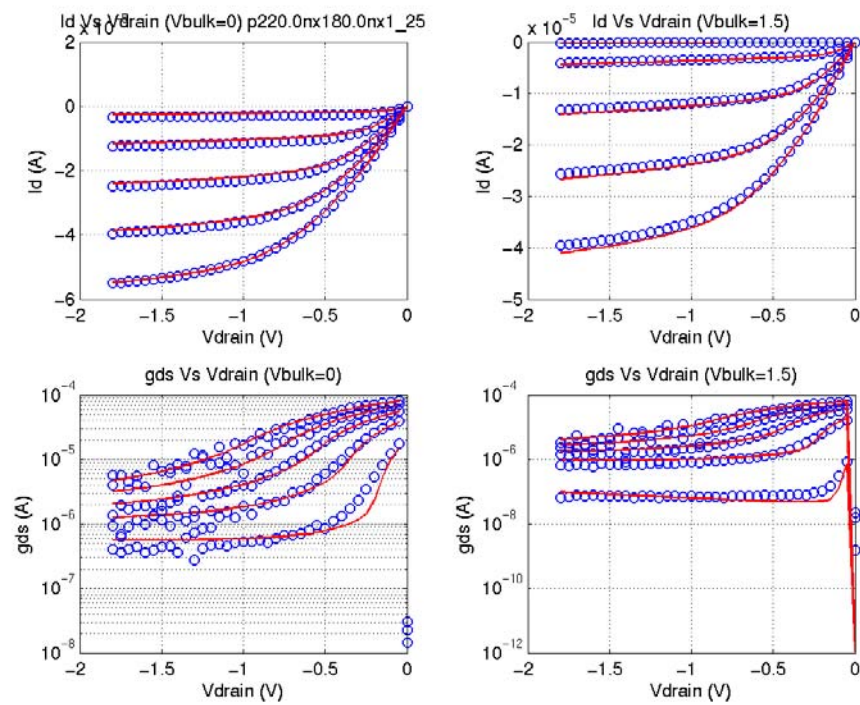


FIGURE 2.32 1p8v_PFET_0p4x0p18_idvg_25C

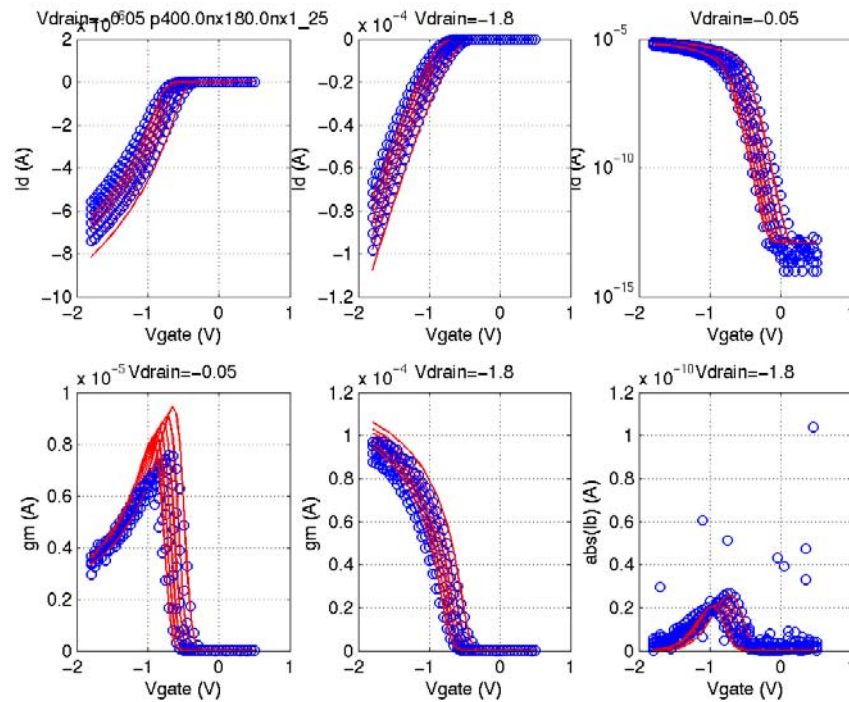


FIGURE 2.33 1p8v_PFET_0p4x0p18_idvd_25C

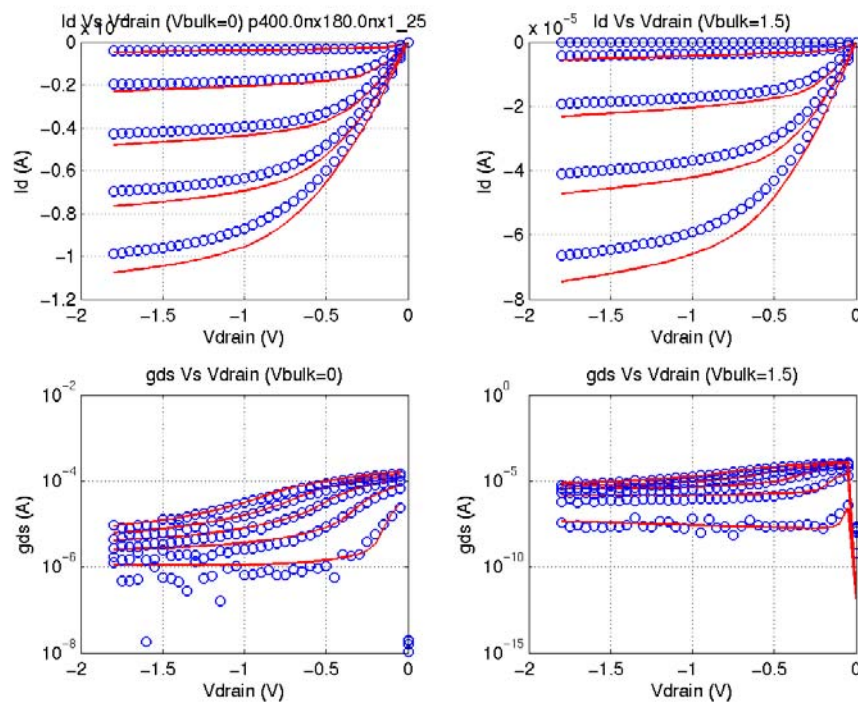


FIGURE 2.34 1p8v_PFET_10x0p25_idvg_25C

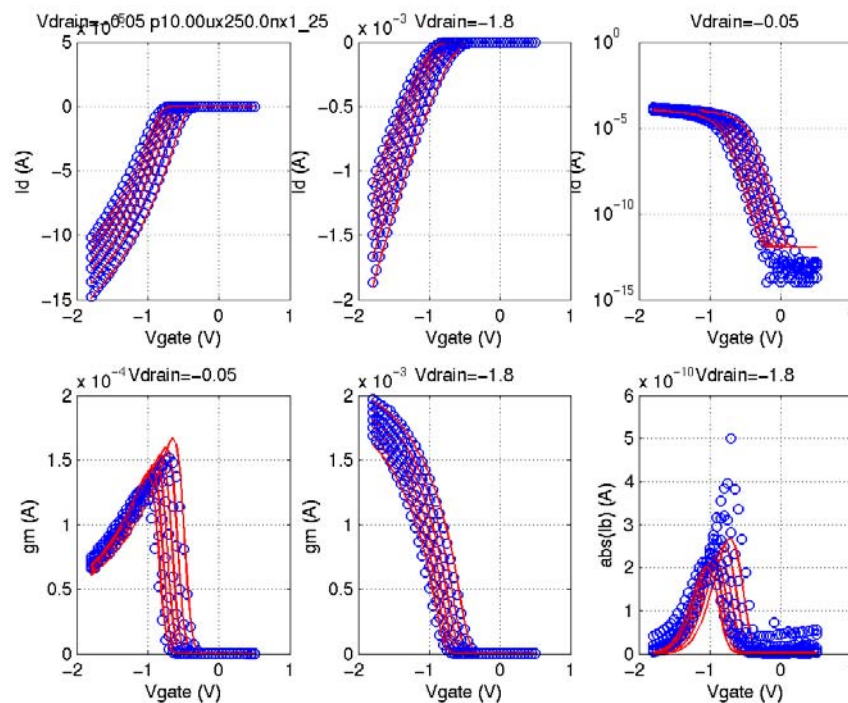


FIGURE 2.35 1p8v_PFET_10x0p25_idvd_25C

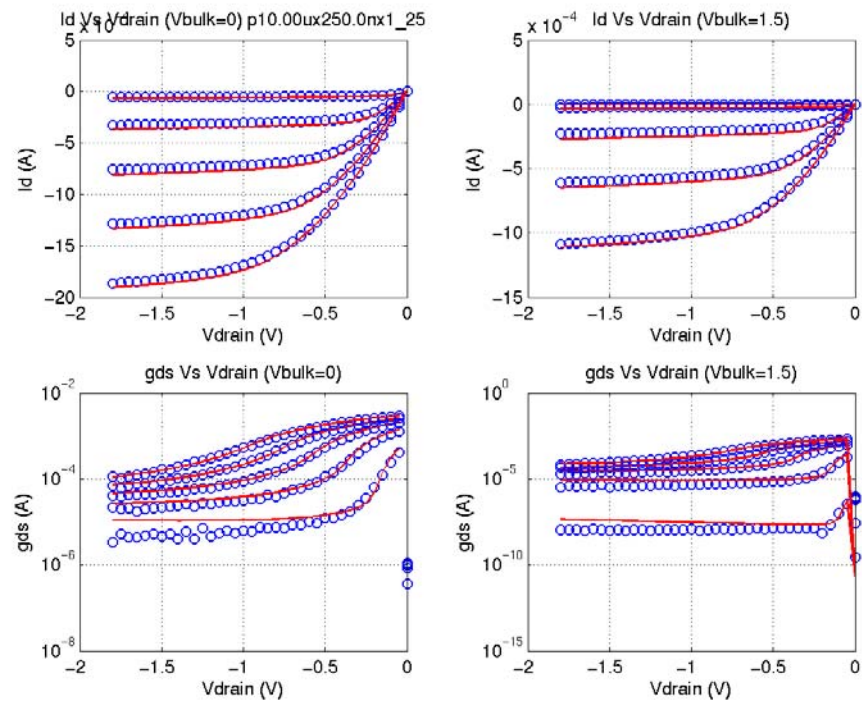


FIGURE 2.36 1p8v_PFET_10x0p18_idvg_-40C

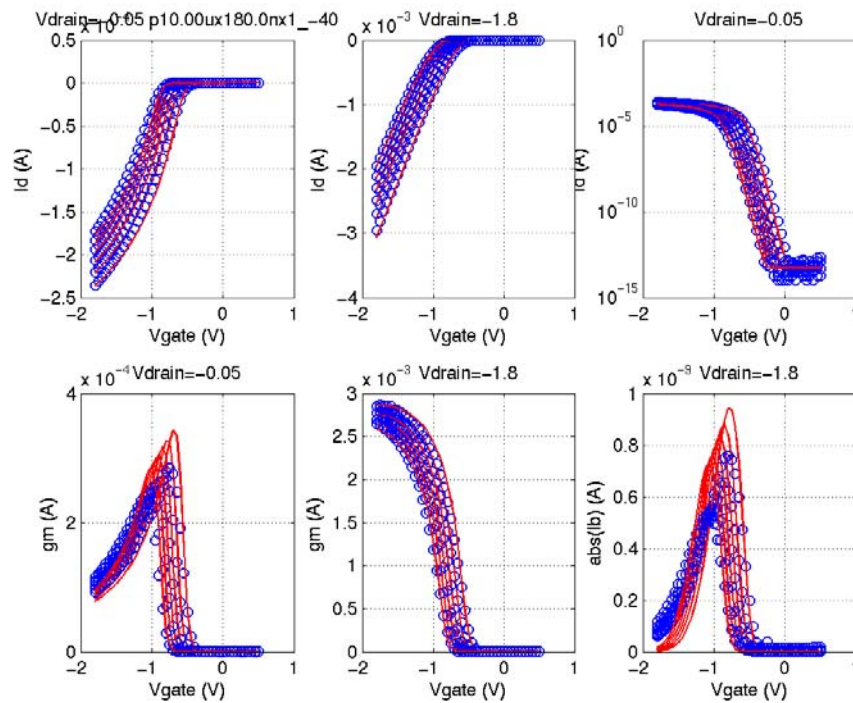


FIGURE 2.37 1p8v_PFET_10x0p18_idvd_-40C

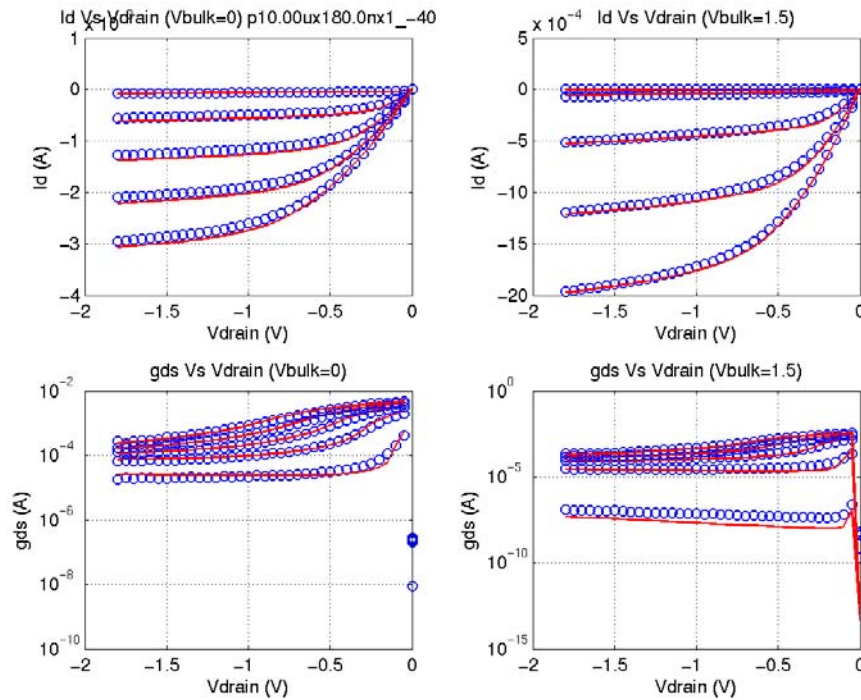


FIGURE 2.38 1p8v_PFET_10x0p18_idvg_125C

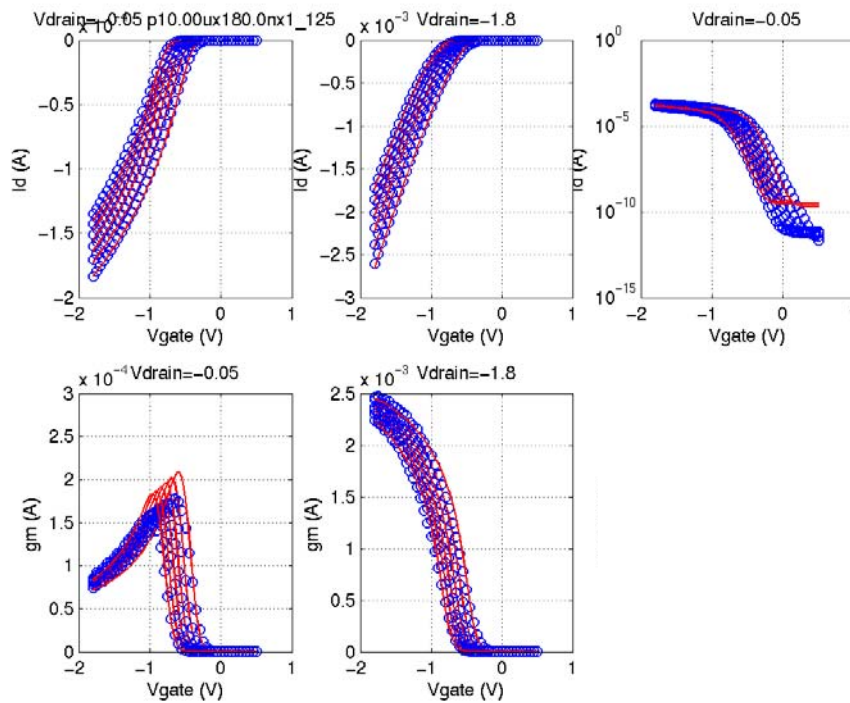


FIGURE 2.39 1p8v_PFET_10x0p18_idvd_125C

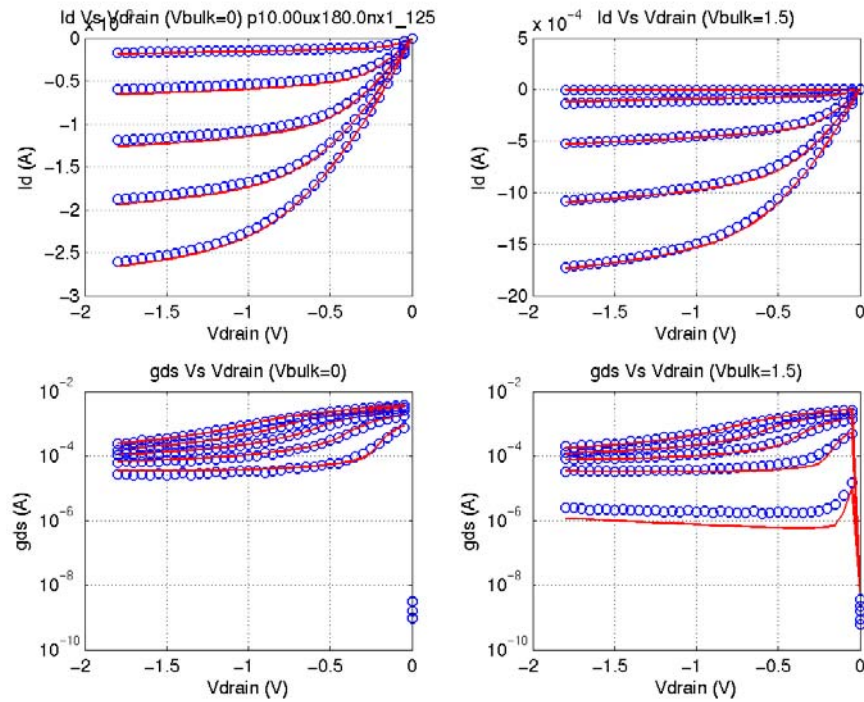


FIGURE 2.40 3p3_NFET_cv_25C

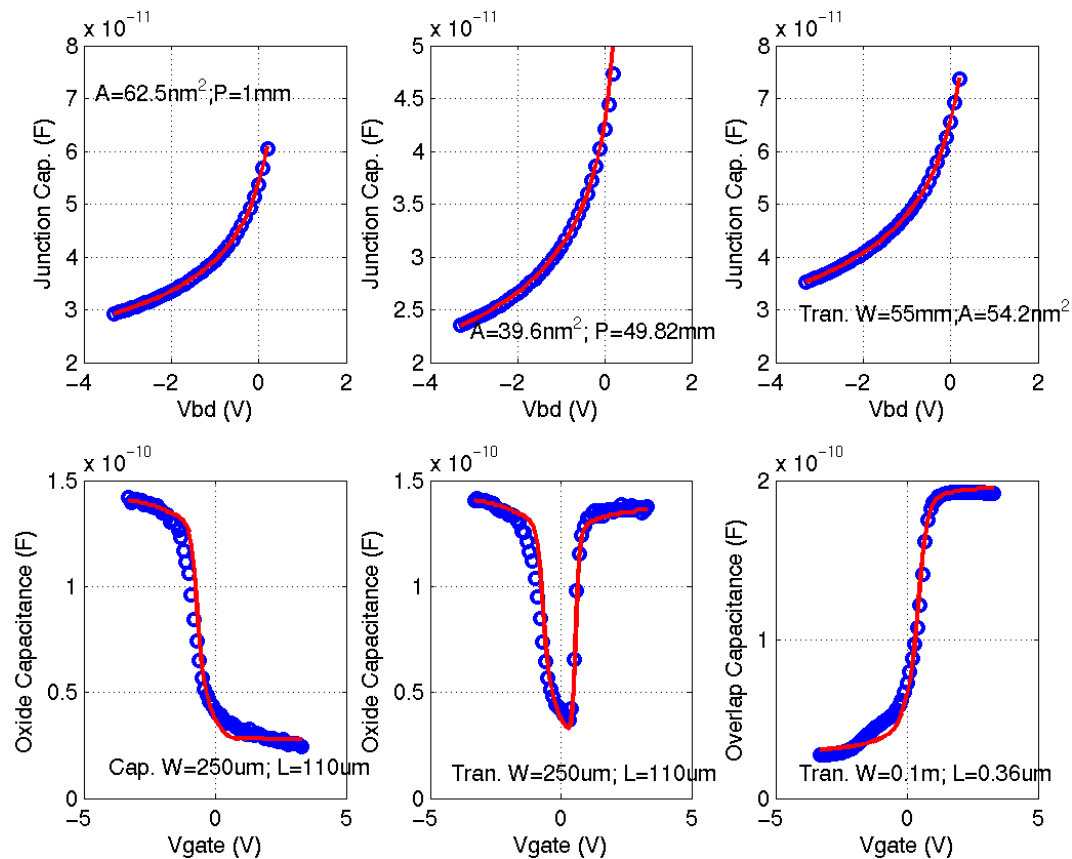


FIGURE 2.41 3p3v_NFET_vtVsL_25C

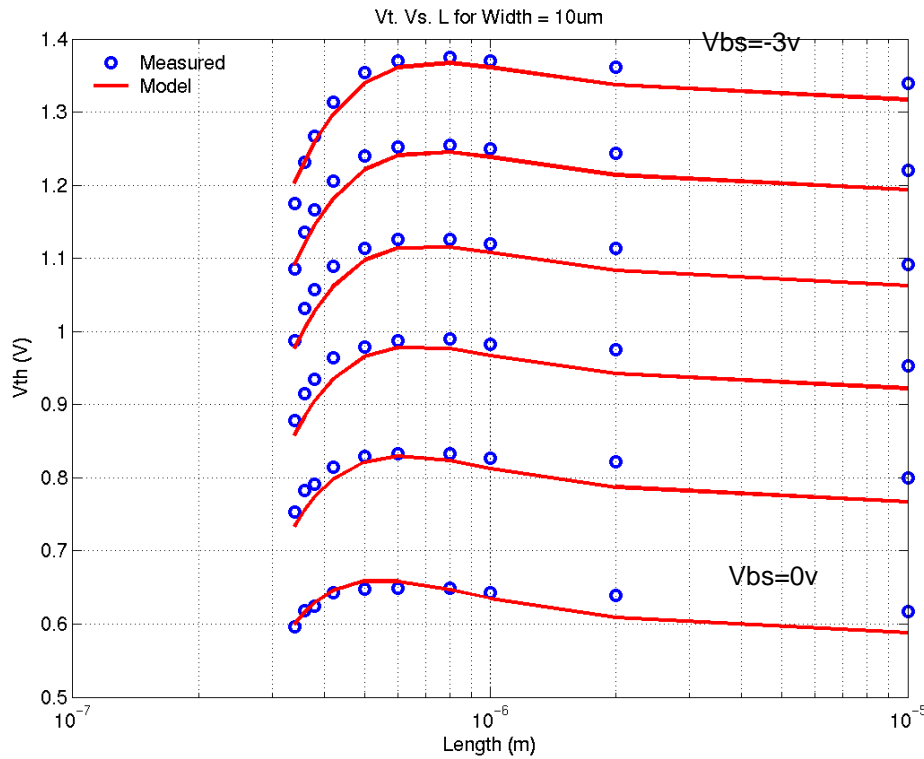


FIGURE 2.42 3p3v_NFET_vtVsW_25C

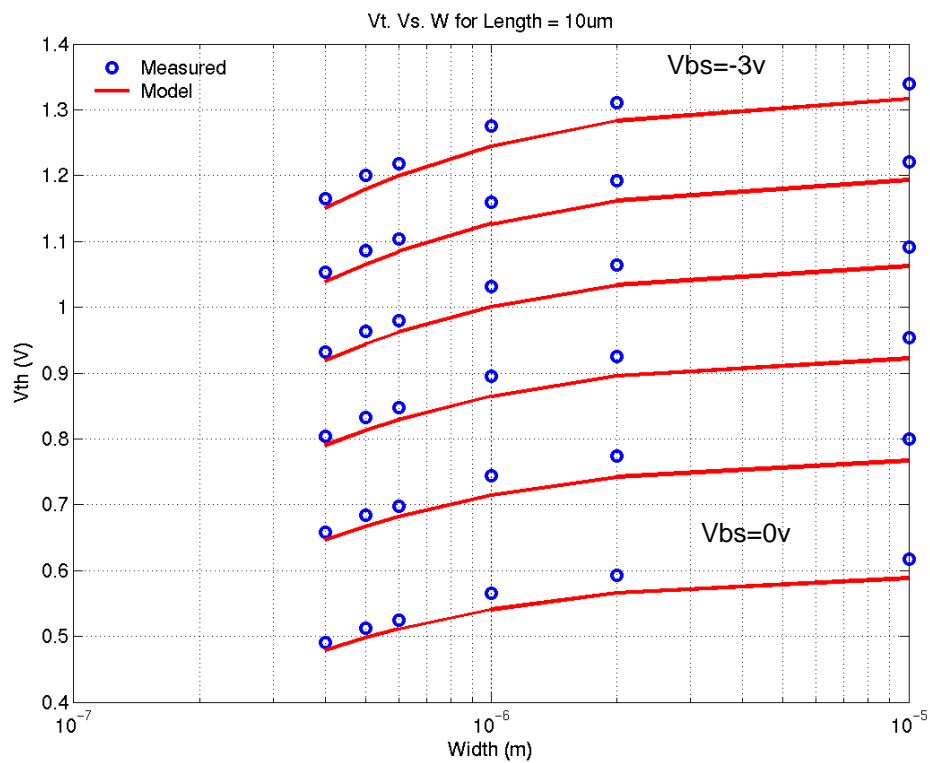


FIGURE 2.43 3p3v_NFET_10x10_idvg_25C

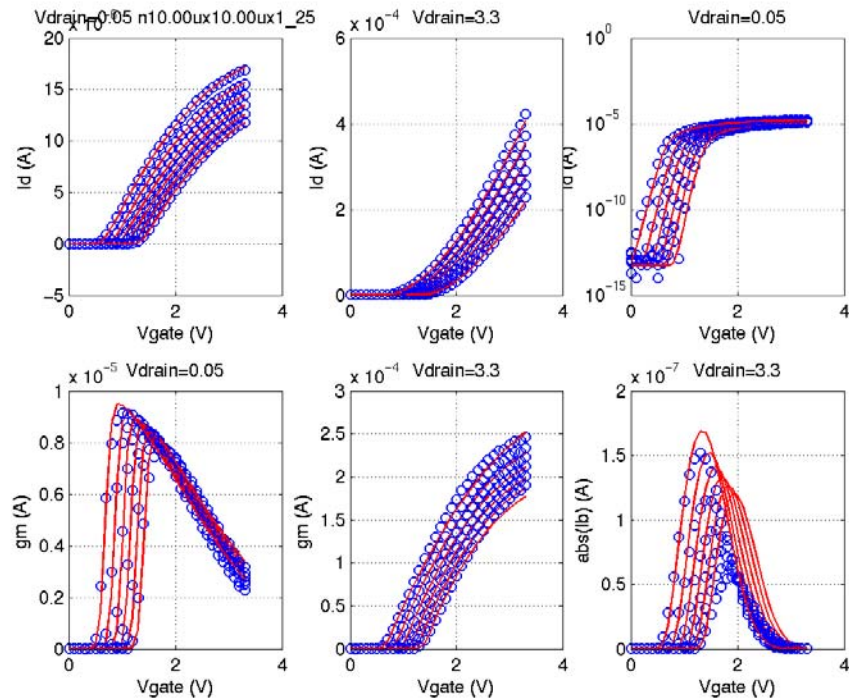


FIGURE 2.44 3p3v_NFET_10x10_idvd_25C

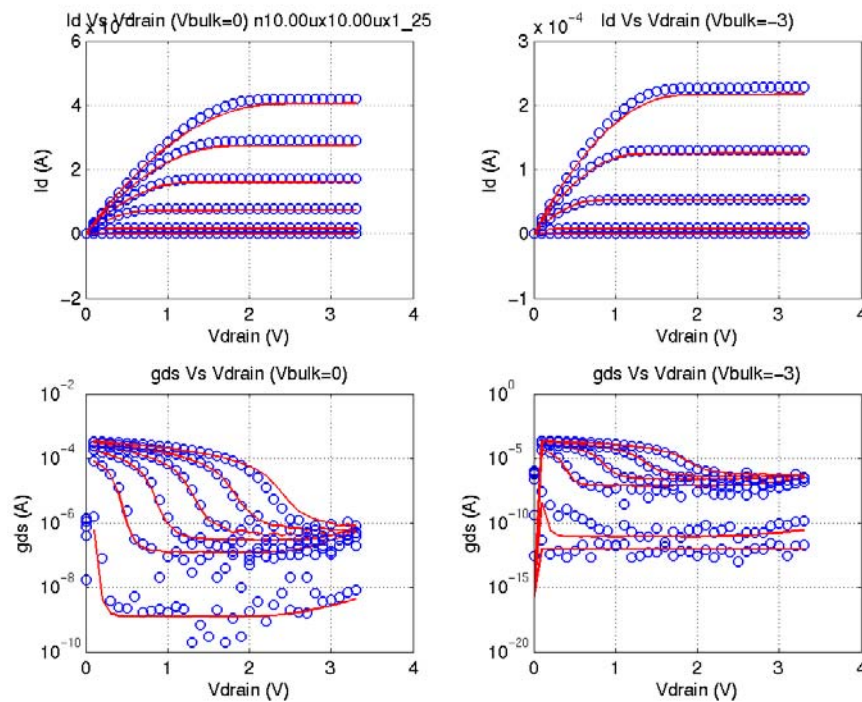


FIGURE 2.45 3p3v_NFET_10x0p36_idvg_25C

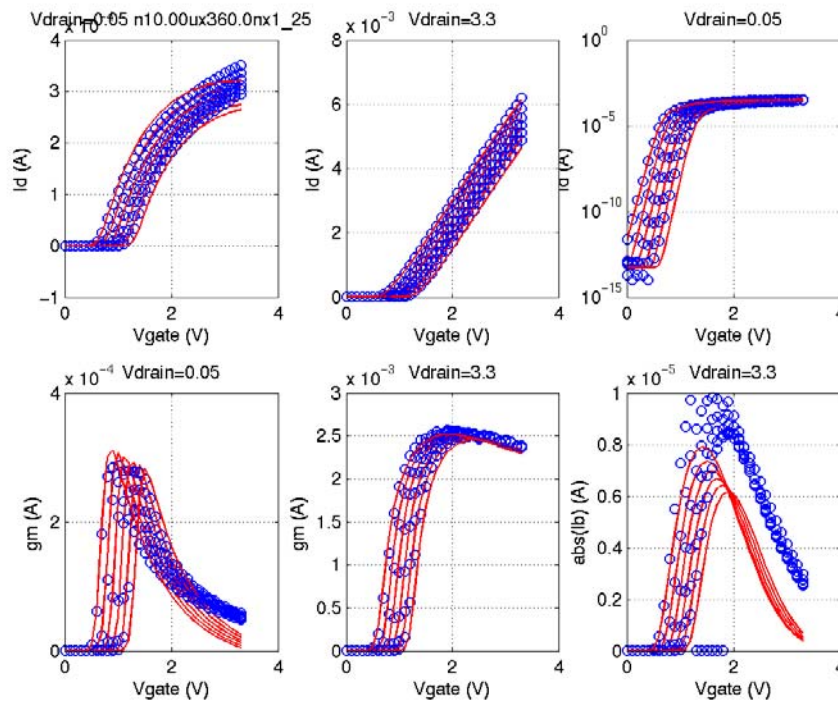


FIGURE 2.46 3p3v_NFET_10x0p36_idvd_25C

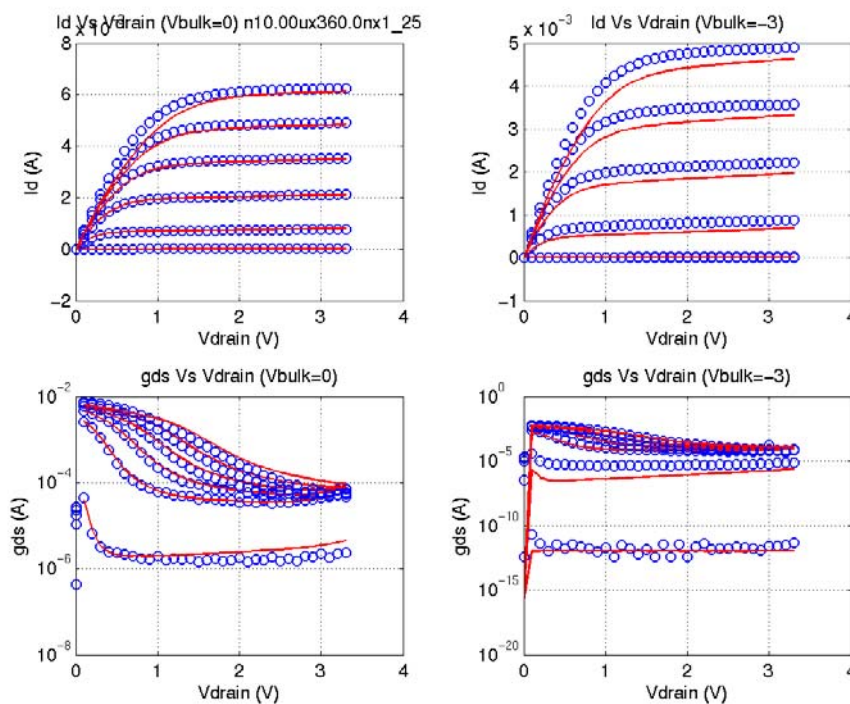


FIGURE 2.47 3p3v_NFET_0p4x10_idvg_25C

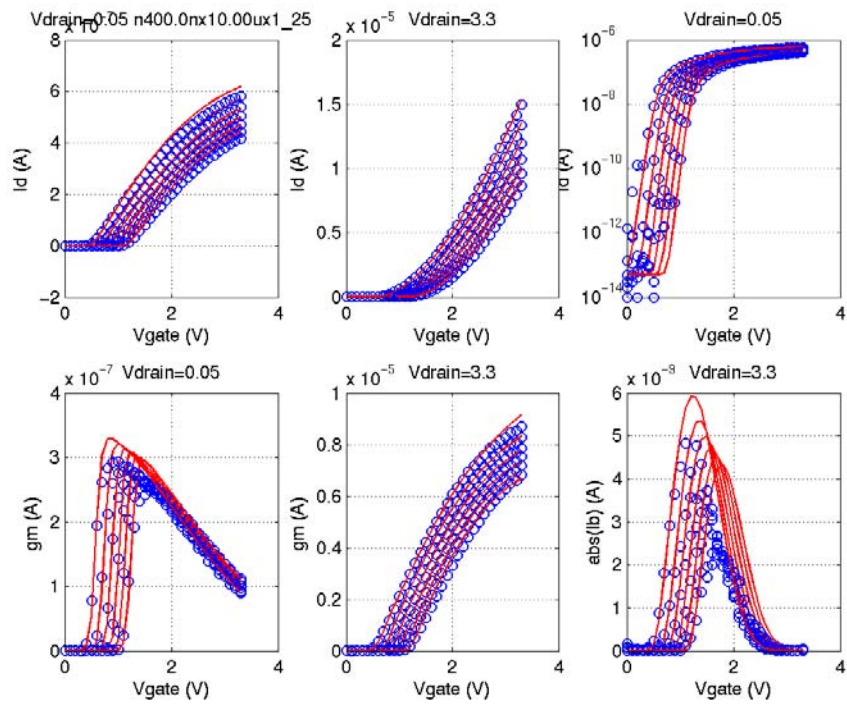


FIGURE 2.48 3p3v_NFET_0p4x10_idvd_25C

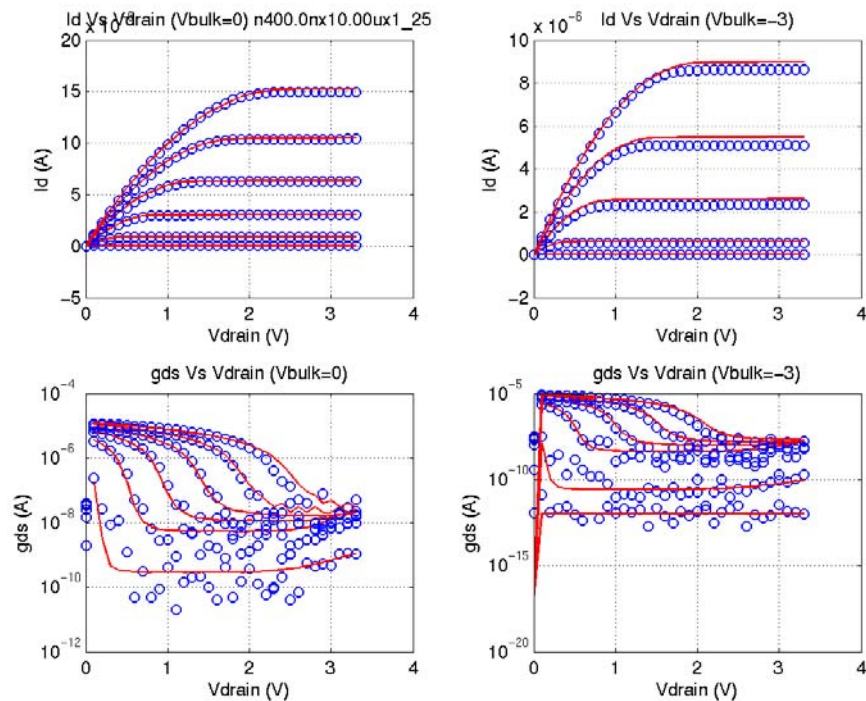


FIGURE 2.49 3p3v_NFET_0p4x0p36_idvg_25C

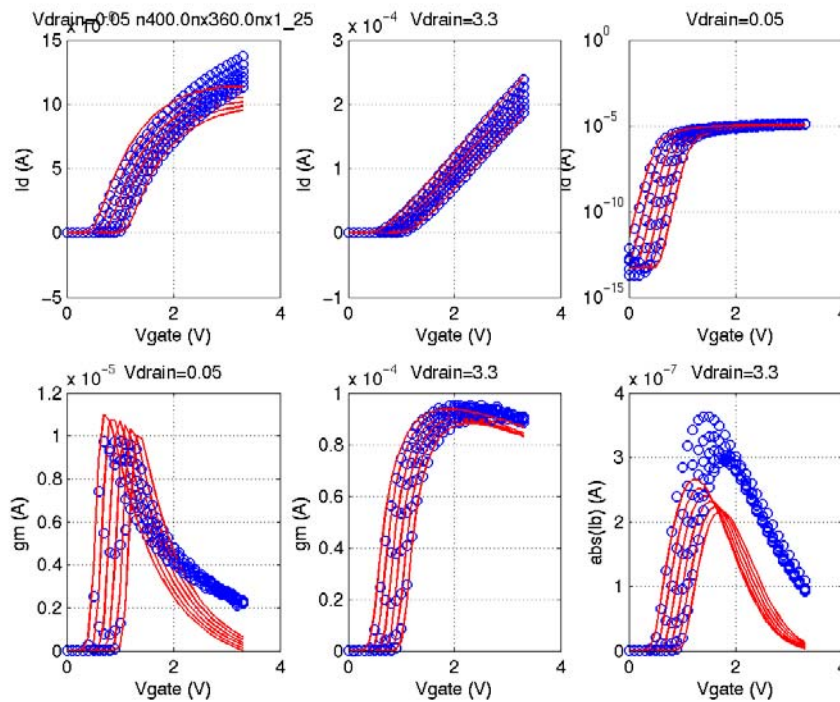


FIGURE 2.50 3p3v_NFET_0p4x0p36_idvd_25C

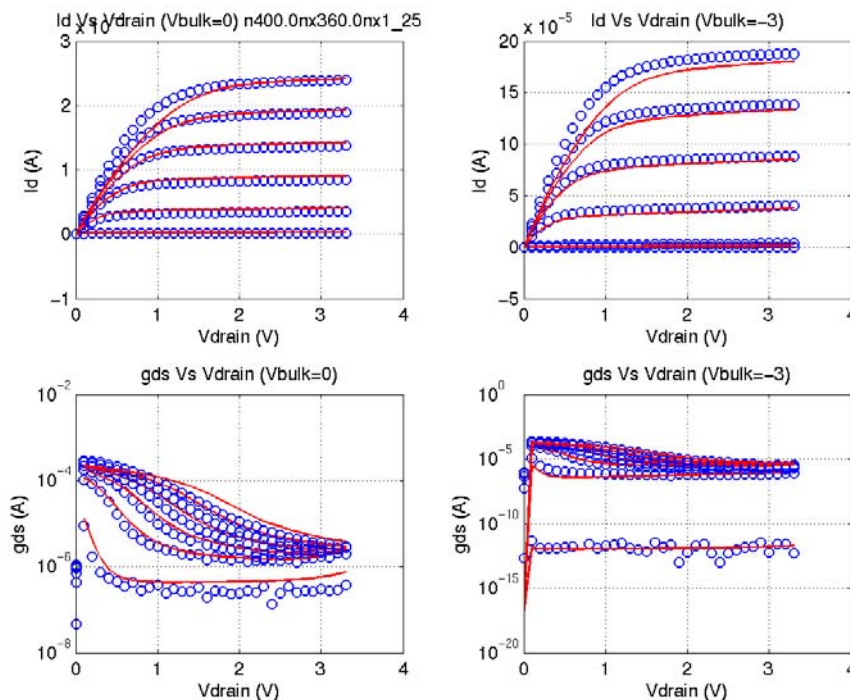


FIGURE 2.51 3p3v_NFET_0p6x0p36_idvg_25C

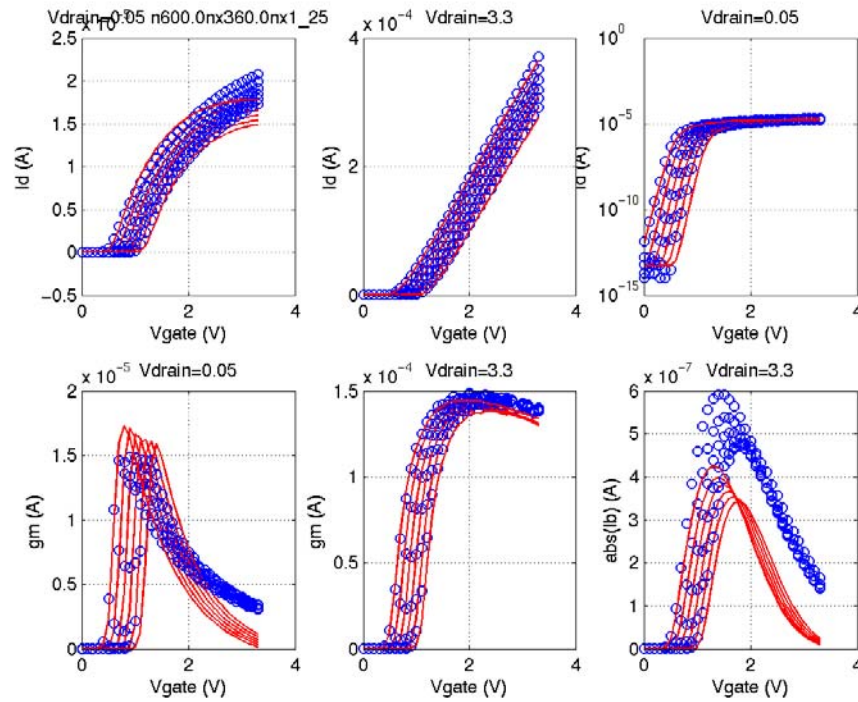


FIGURE 2.52 3p3v_NFET_0p6x0p36_idvd_25C

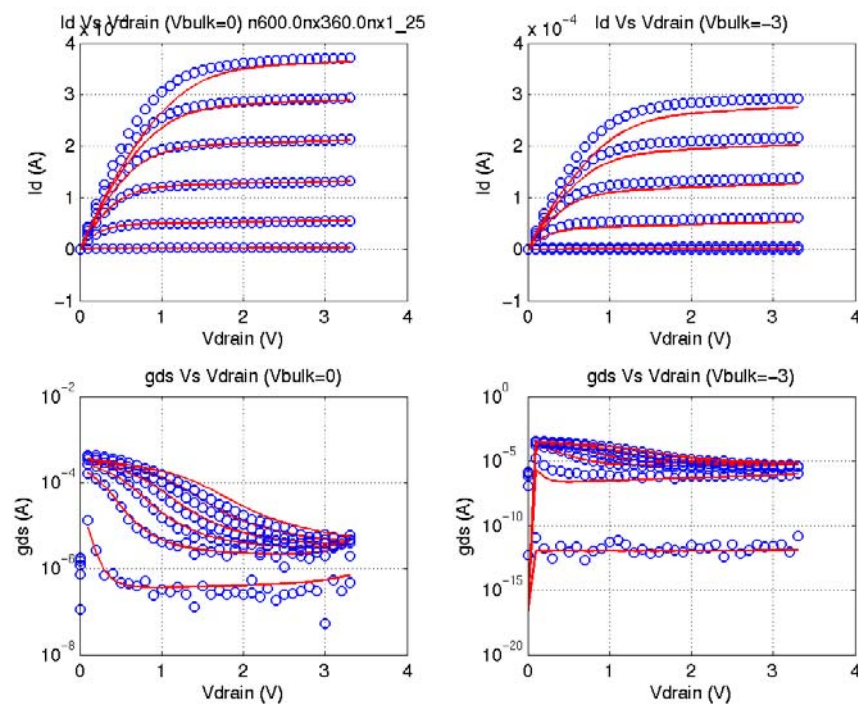


FIGURE 2.53 3p3v_NFET_10x0p6_idvg_25C

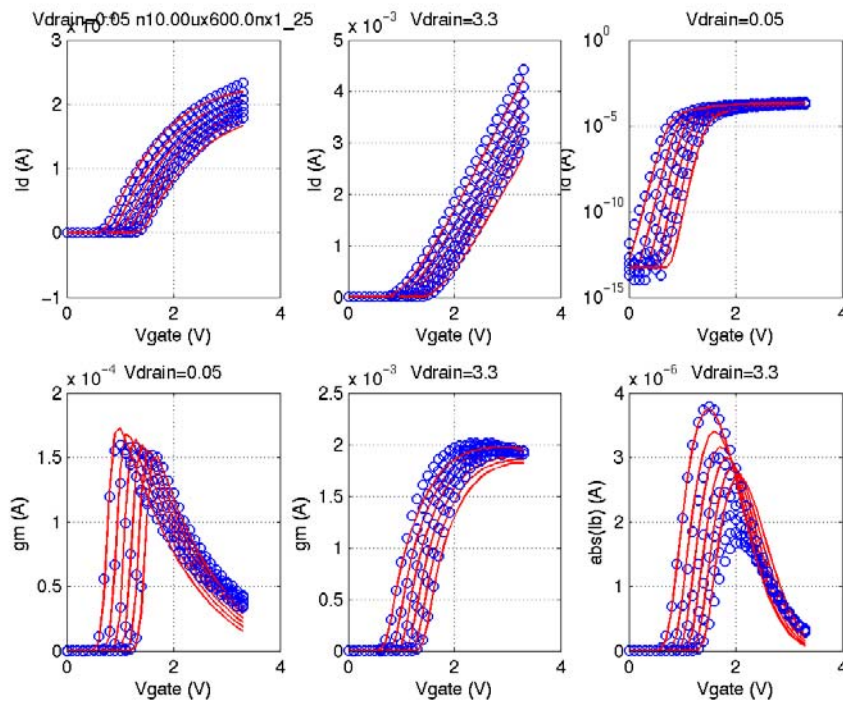


FIGURE 2.54 3p3v_NFET_10x0p6_idvd_25C

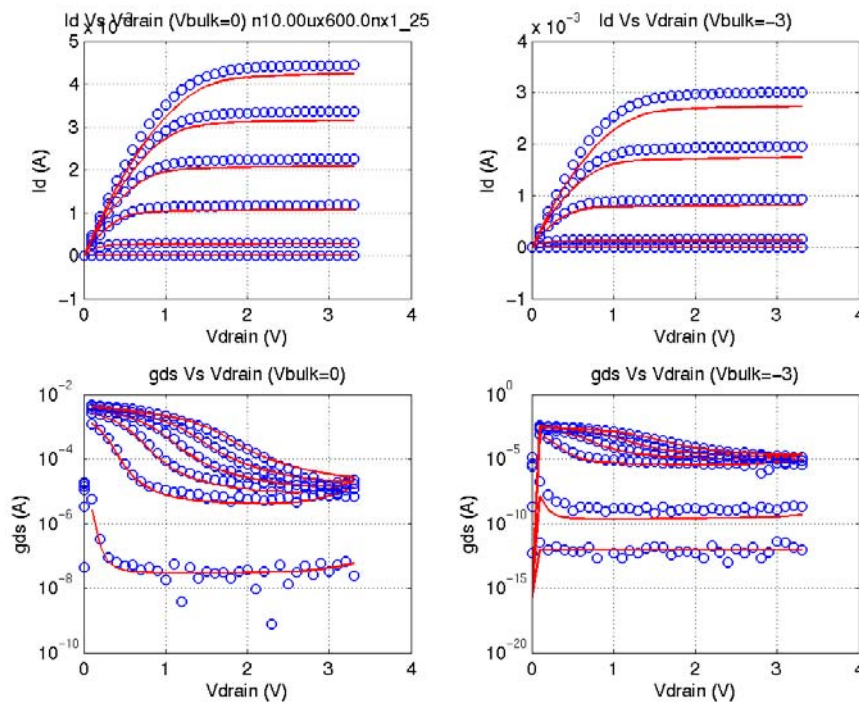


FIGURE 2.55 3p3v_NFET_10x0p36_idvg_-40C

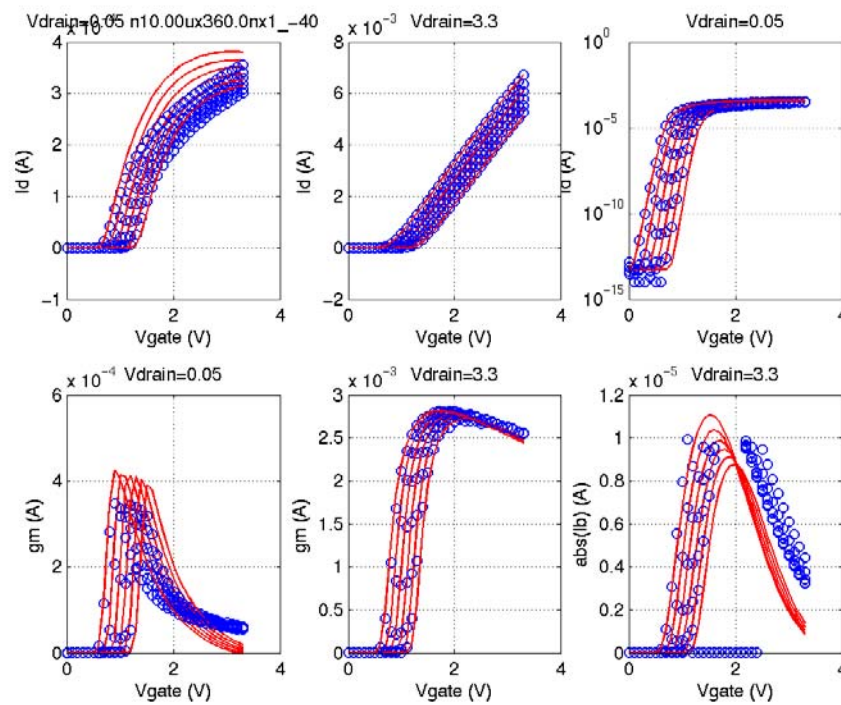


FIGURE 2.56 3p3v_NFET_10x0p36_idvd_-40C

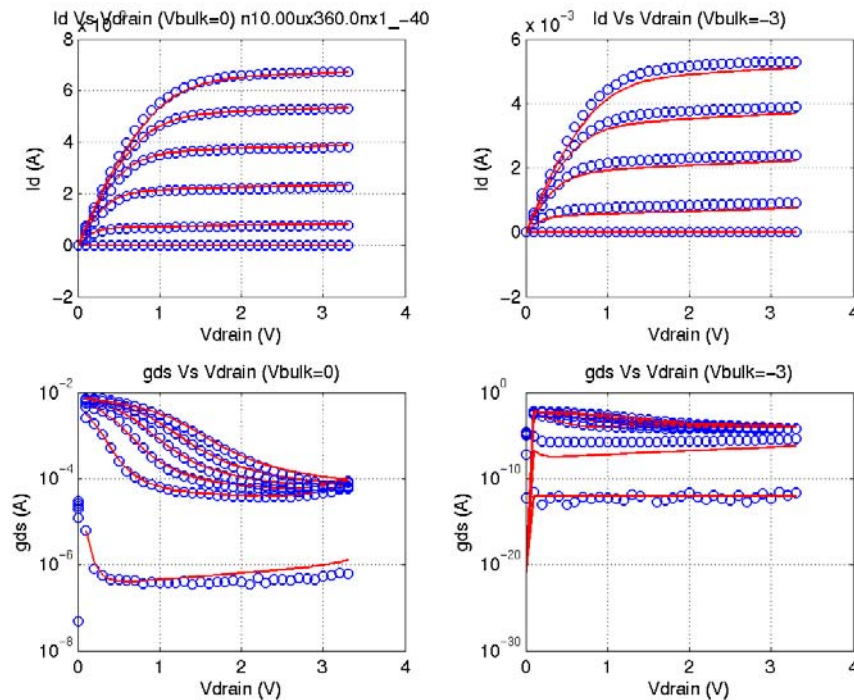


FIGURE 2.57 3p3v_NFET_10x0p36_idvg_125C

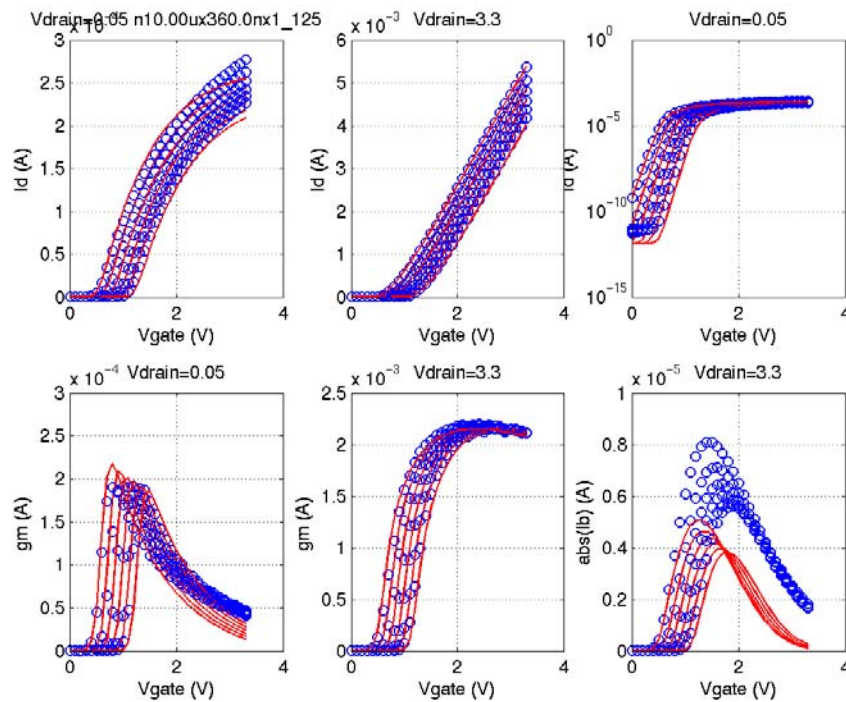


FIGURE 2.58 3p3v_NFET_10x0p36_idvd_125C

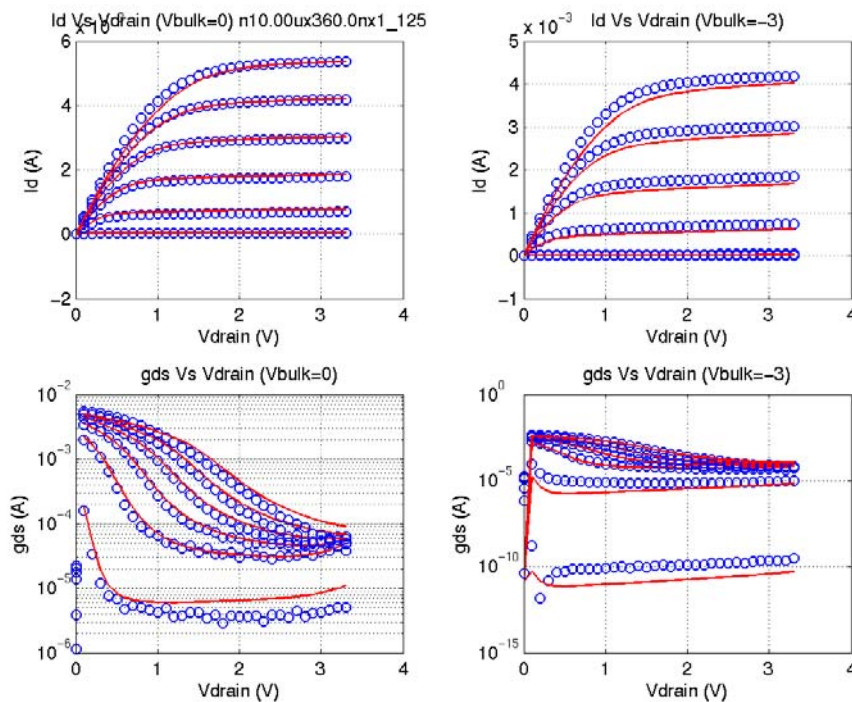
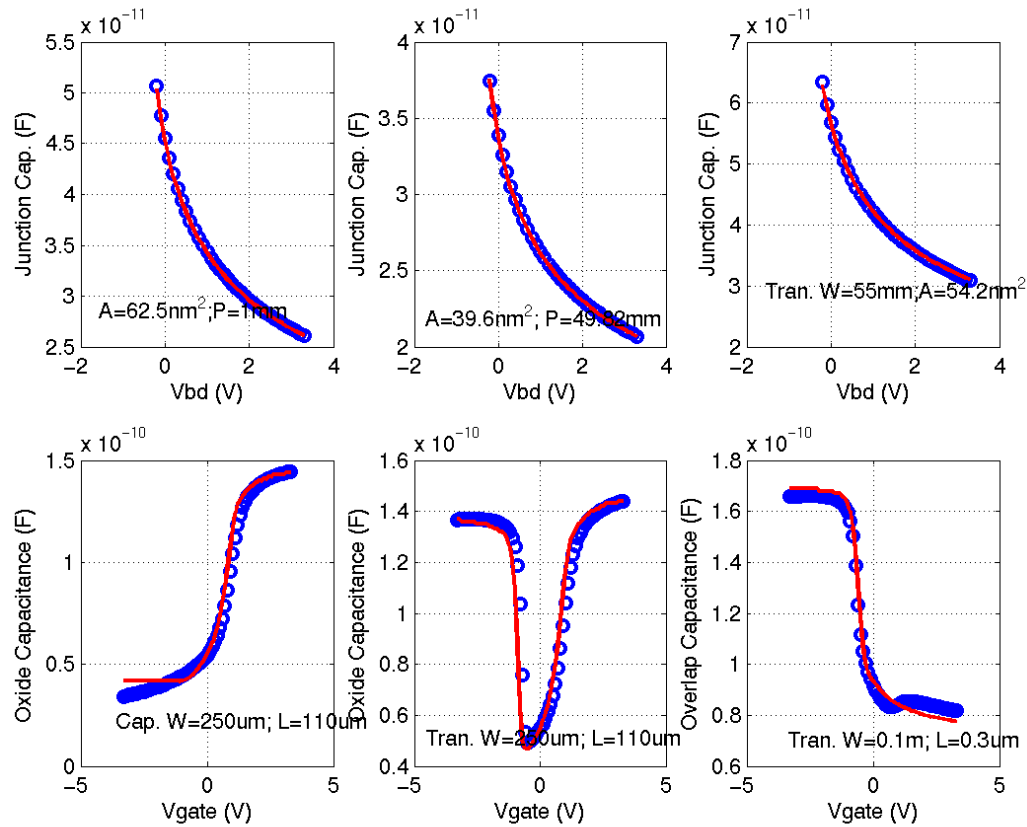
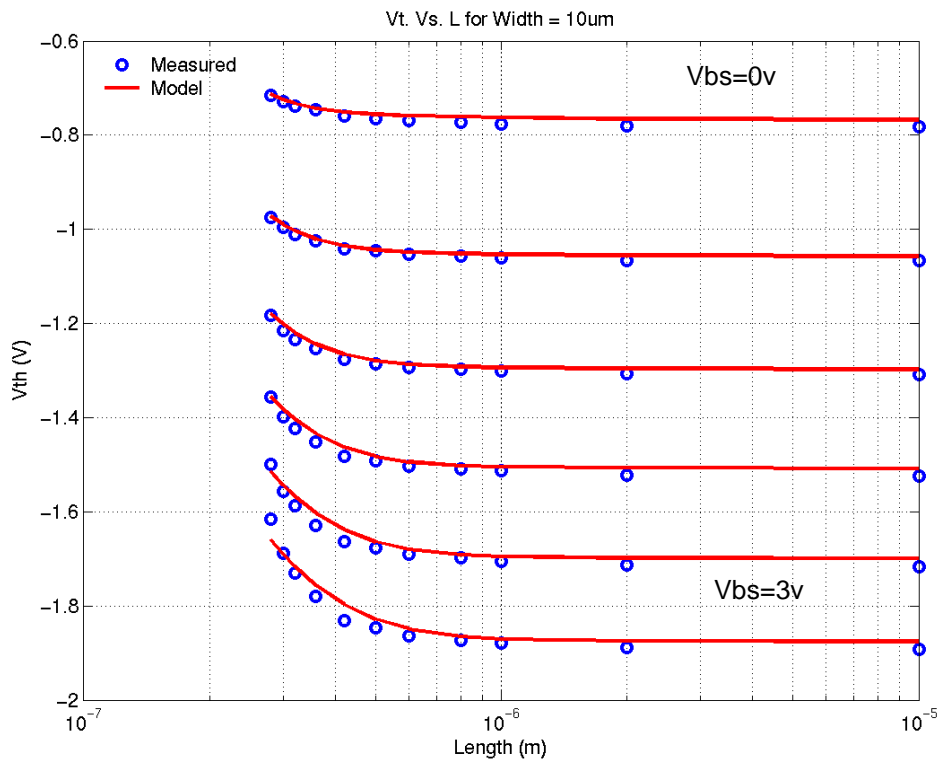


FIGURE 2.59 3p3_PFET_cv_25C



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FIGURE 2.60 3p3v_PFET_vtVsL_25C



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FIGURE 2.61 3p3v_PFET_vtVsW_25C

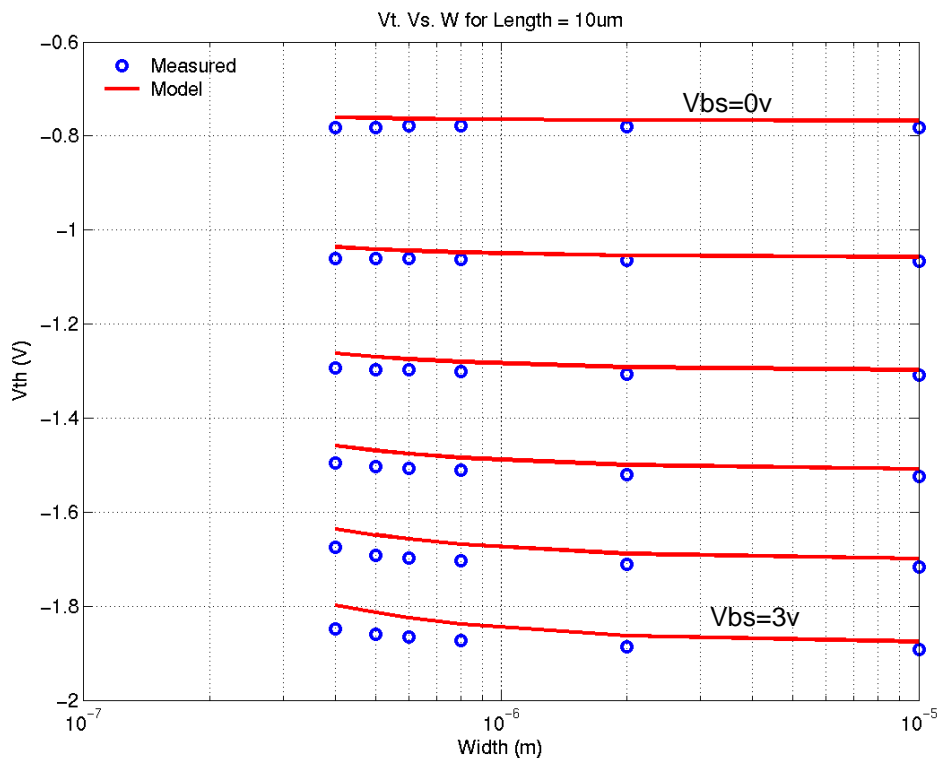


FIGURE 2.62 3p3v_PFET_10x10_idvg_25C

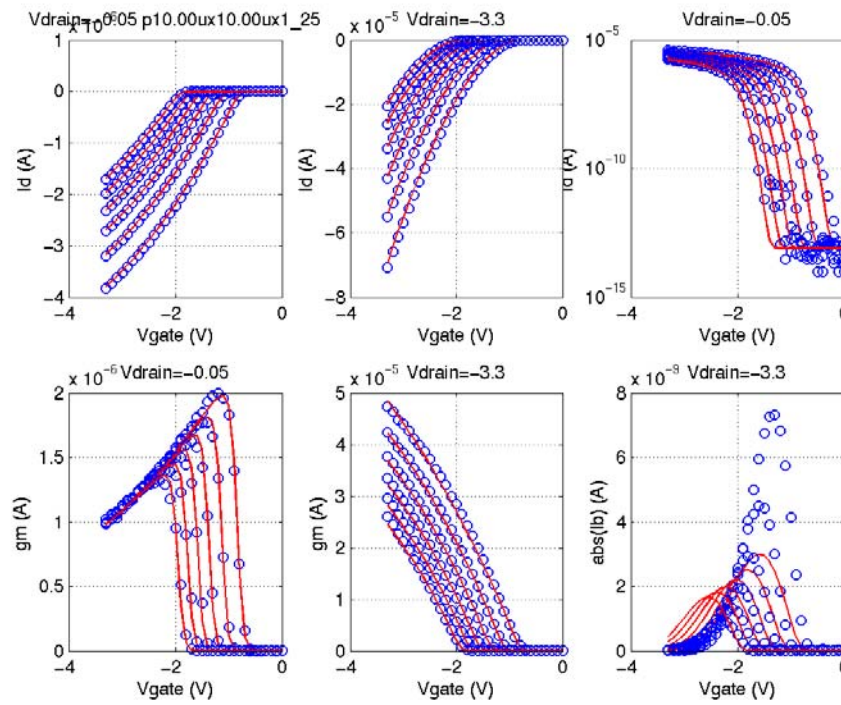


FIGURE 2.63 3p3v_PFET_10x10_idvd_25C

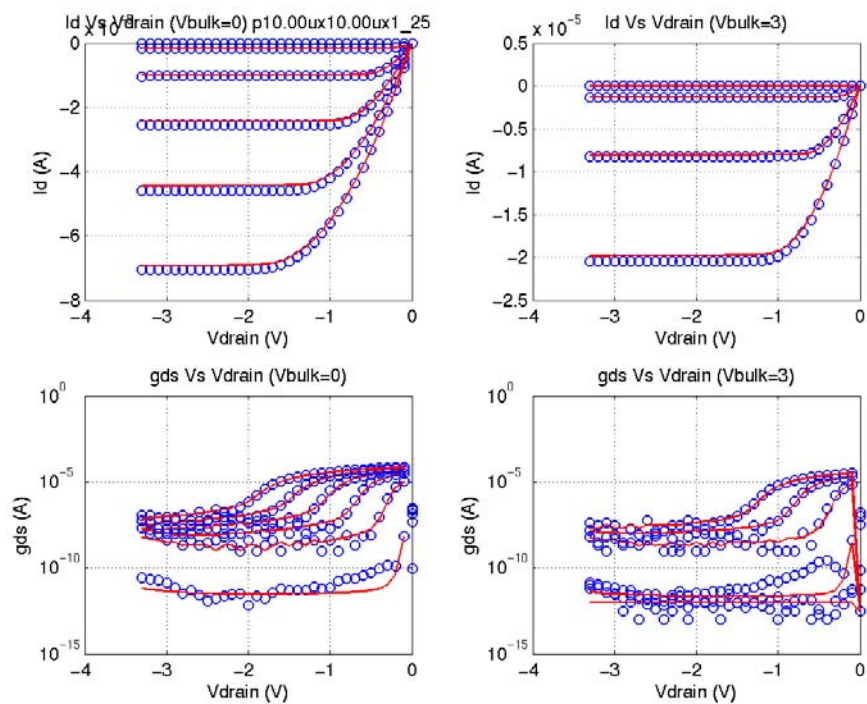


FIGURE 2.64 3p3v_PFET_10x0p3_idvg_25C

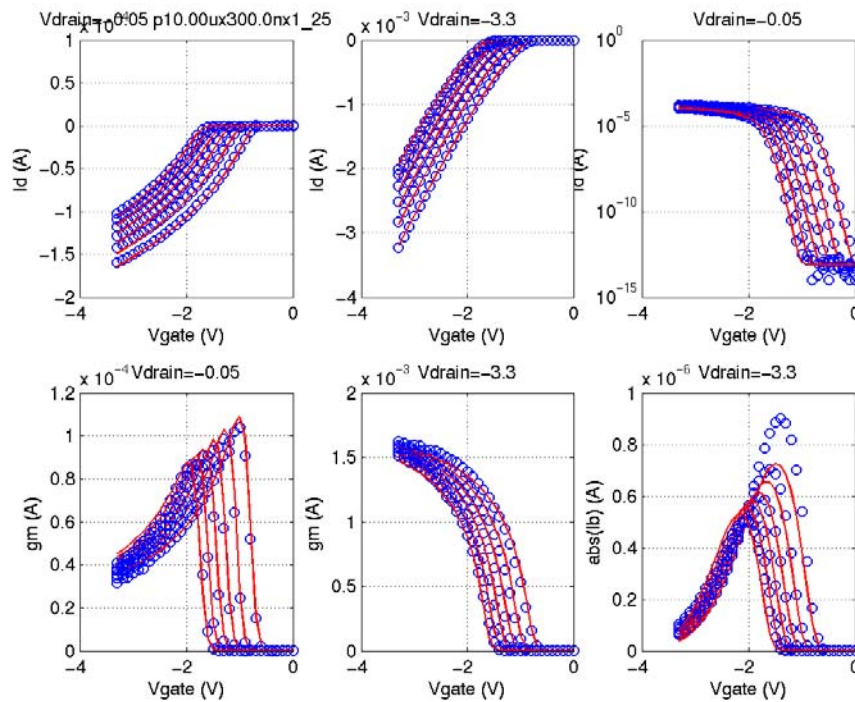


FIGURE 2.65 3p3v_PFET_10x0p3_idvd_25C

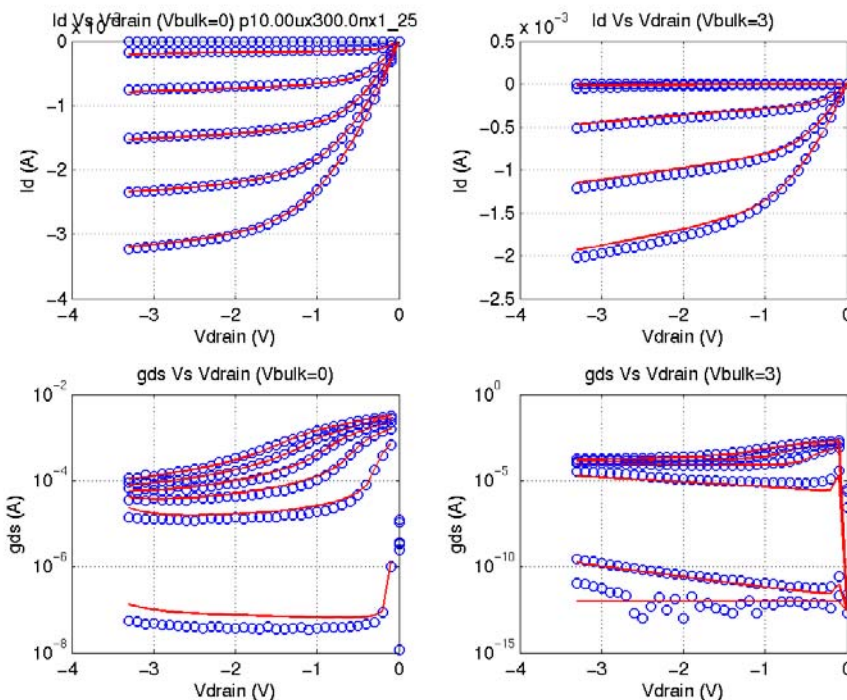


FIGURE 2.66 3p3v_PFET_0p4x10_idvg_25C

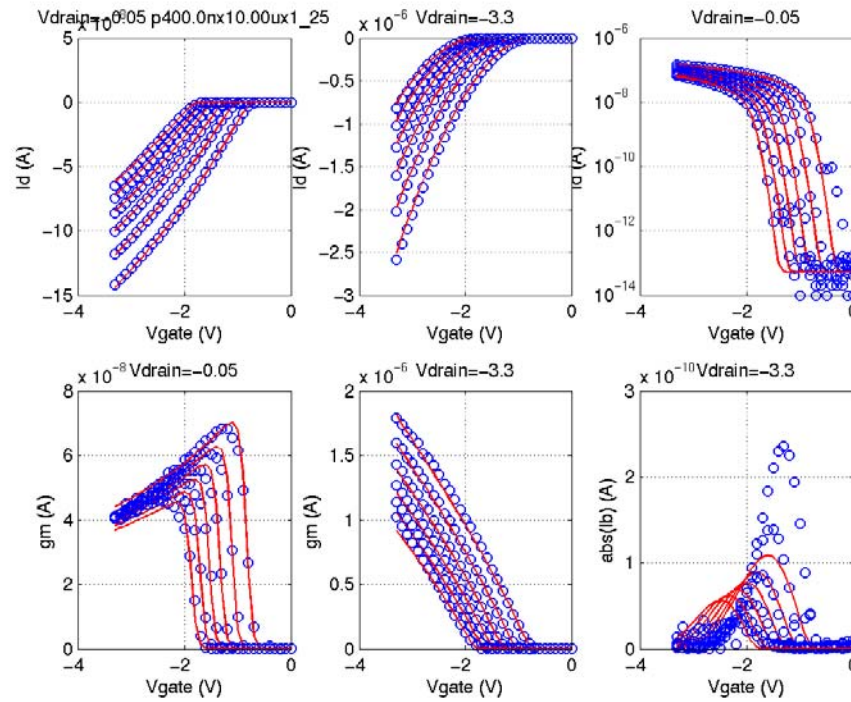


FIGURE 2.67 3p3v_PFET_0p4x10_idvd_25C

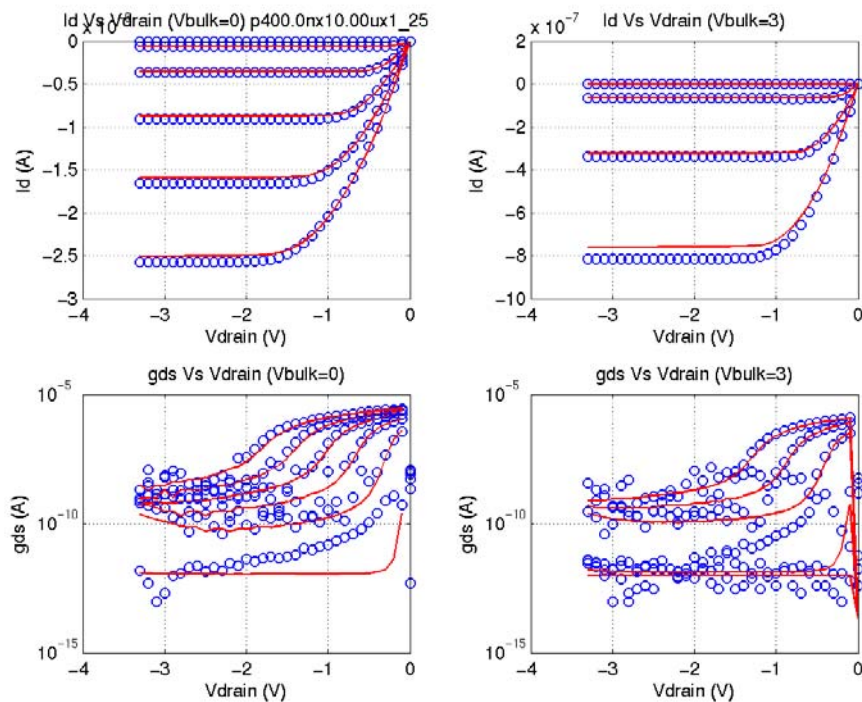


FIGURE 2.68 3p3v_PFET_0p4x0p3_idvg_25C

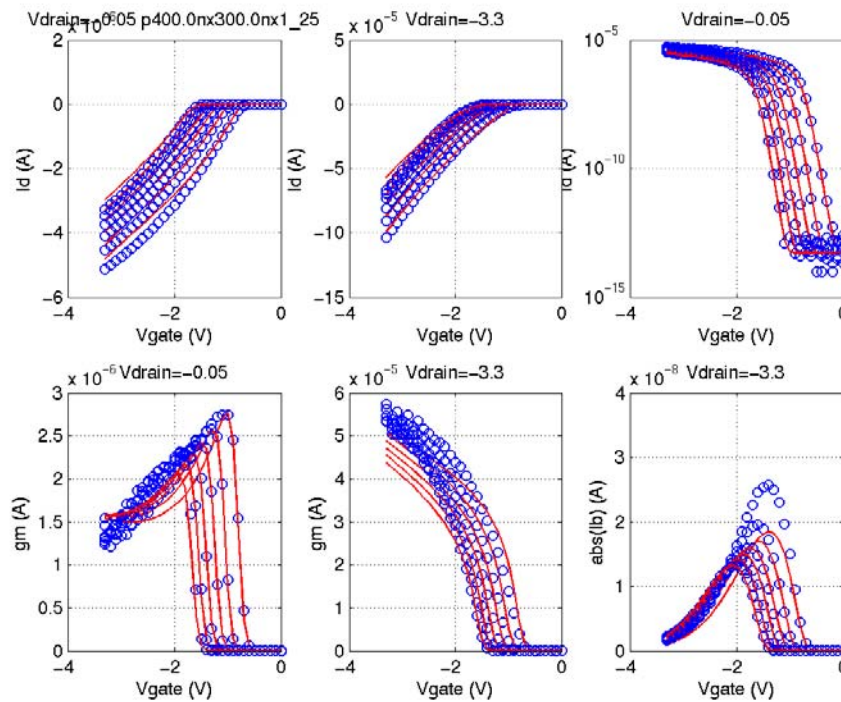


FIGURE 2.69 3p3v_PFET_0p4x0p3_idvd_25C

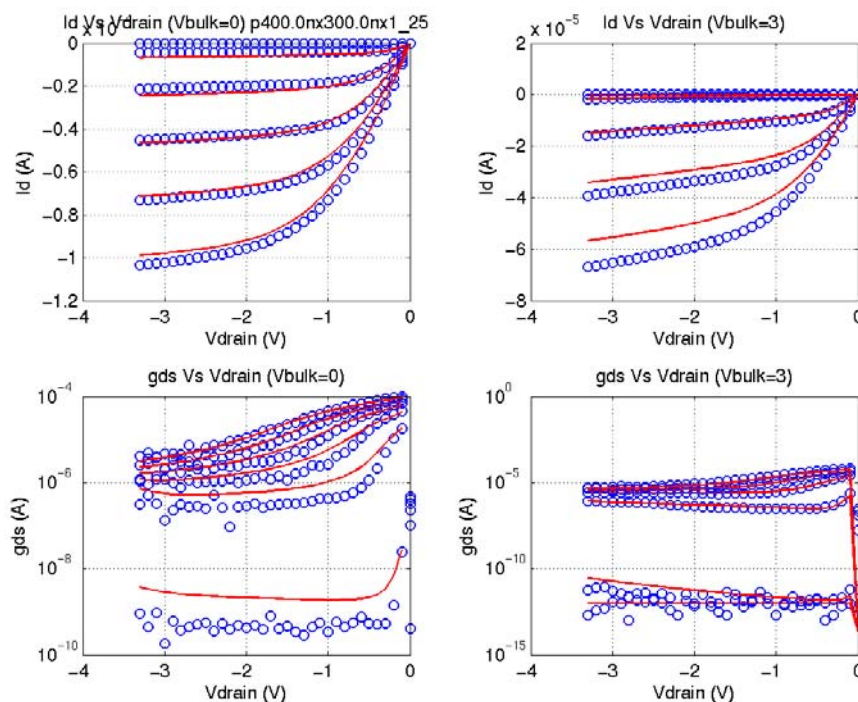


FIGURE 2.70 3p3v_PFET_0p6x0p3_idvg_25C

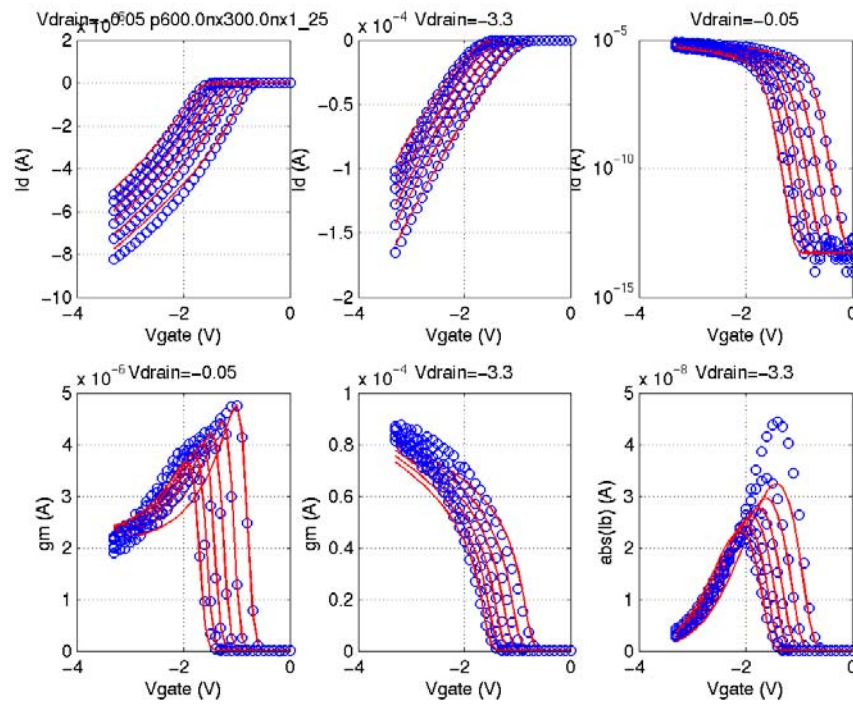


FIGURE 2.71 3p3v_PFET_0p6x0p3_idvd_25C

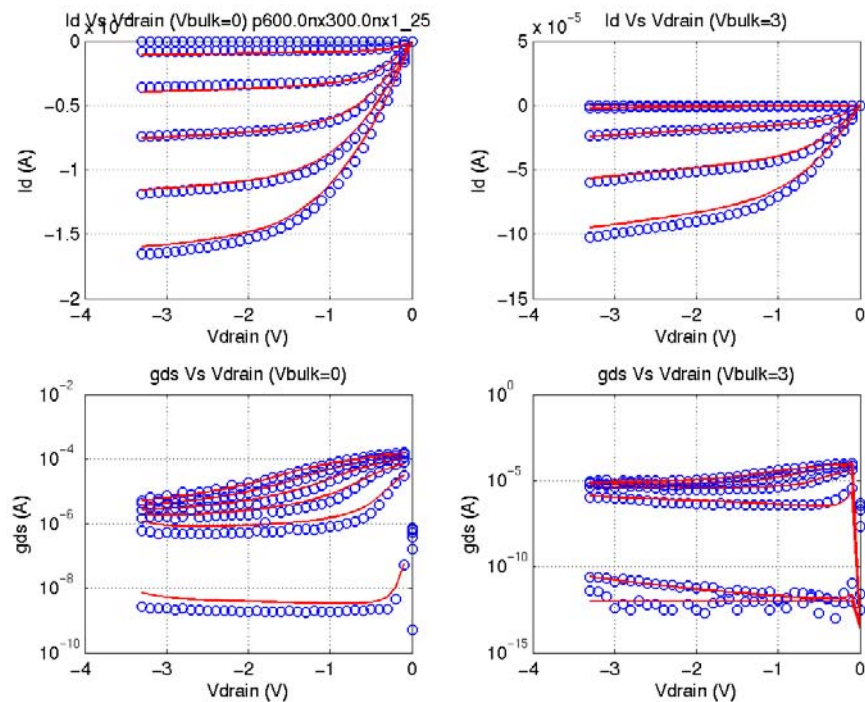


FIGURE 2.72 3p3v_PFET_10x0p6_idvg_25C

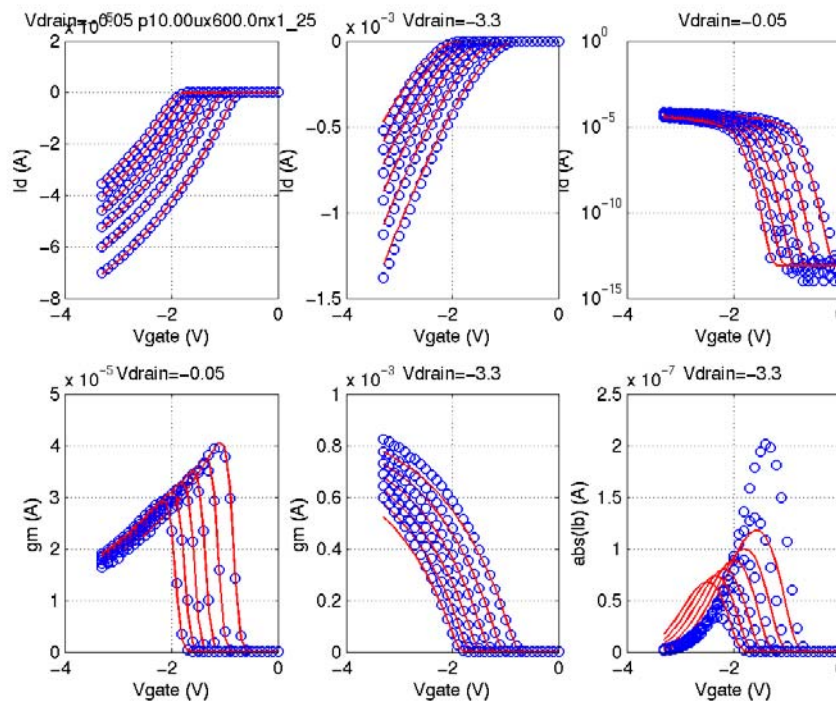


FIGURE 2.73 3p3v_PFET_10x0p6_idvd_25C

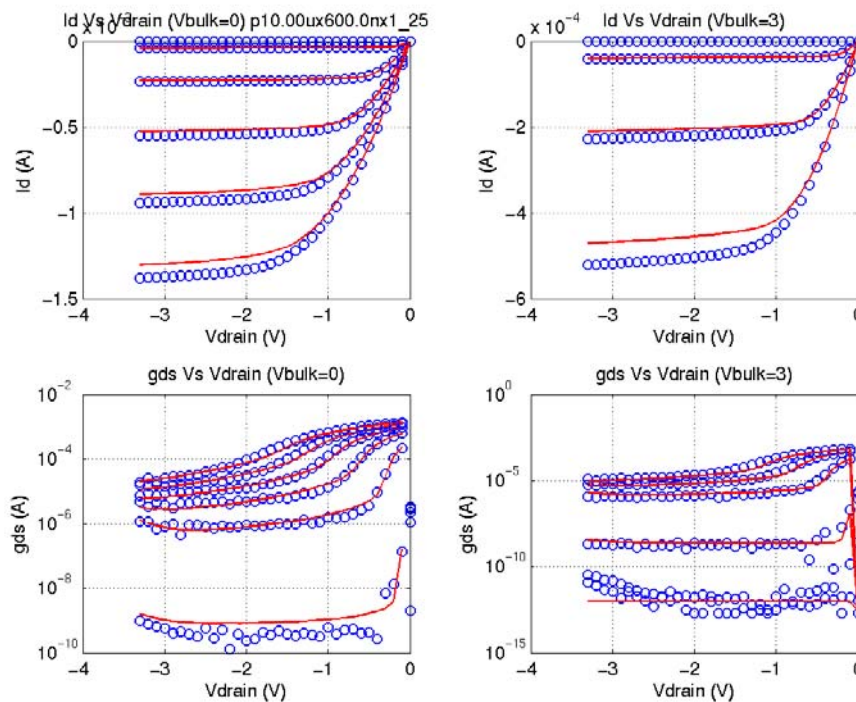


FIGURE 2.74 3p3v_PFET_10x0p3_idvg_-40C

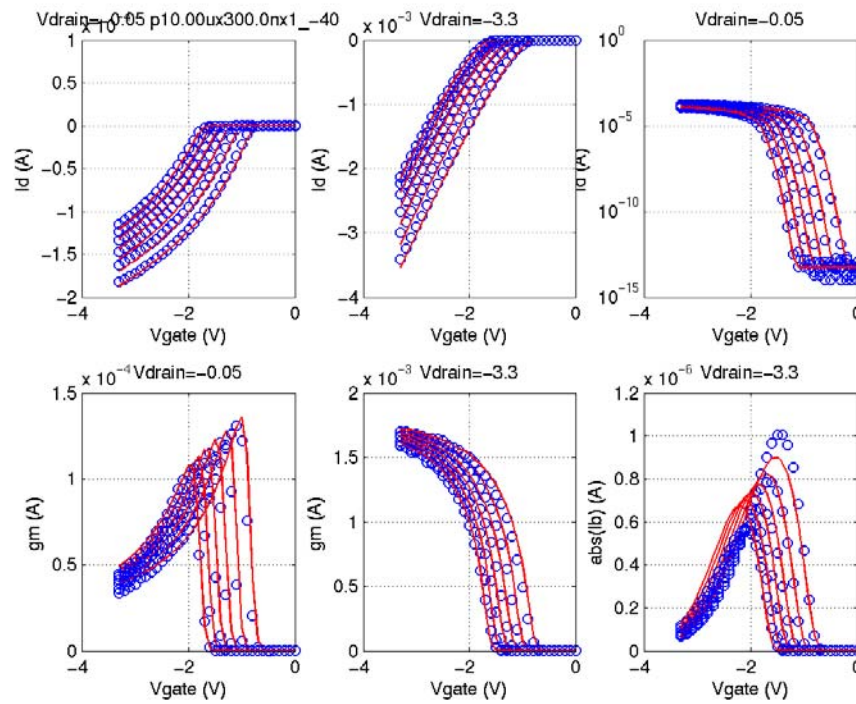


FIGURE 2.75 3p3v_PFET_10x0p3_idvd_-40C

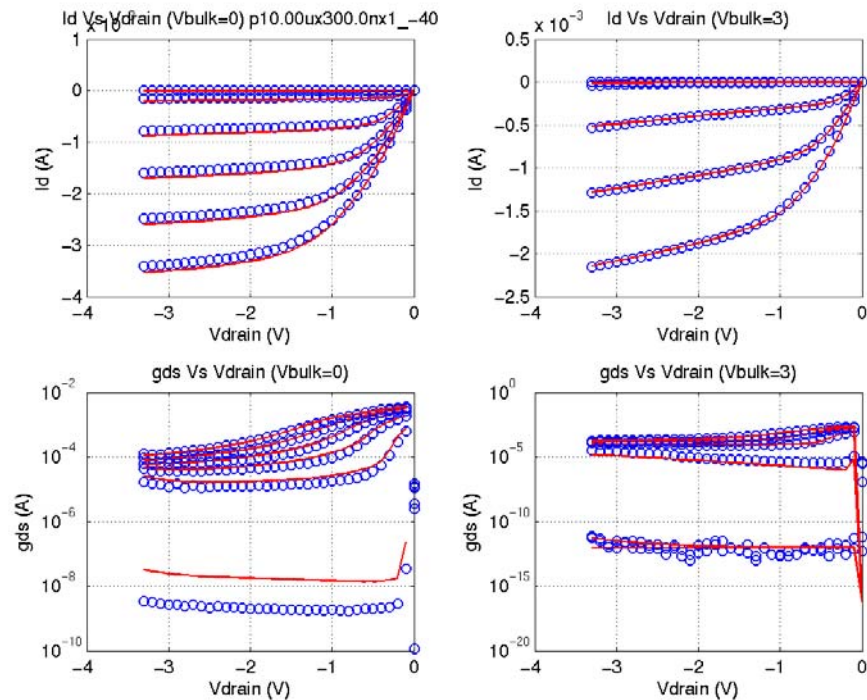


FIGURE 2.76 3p3v_PFET_10x0p3_idvg_125C

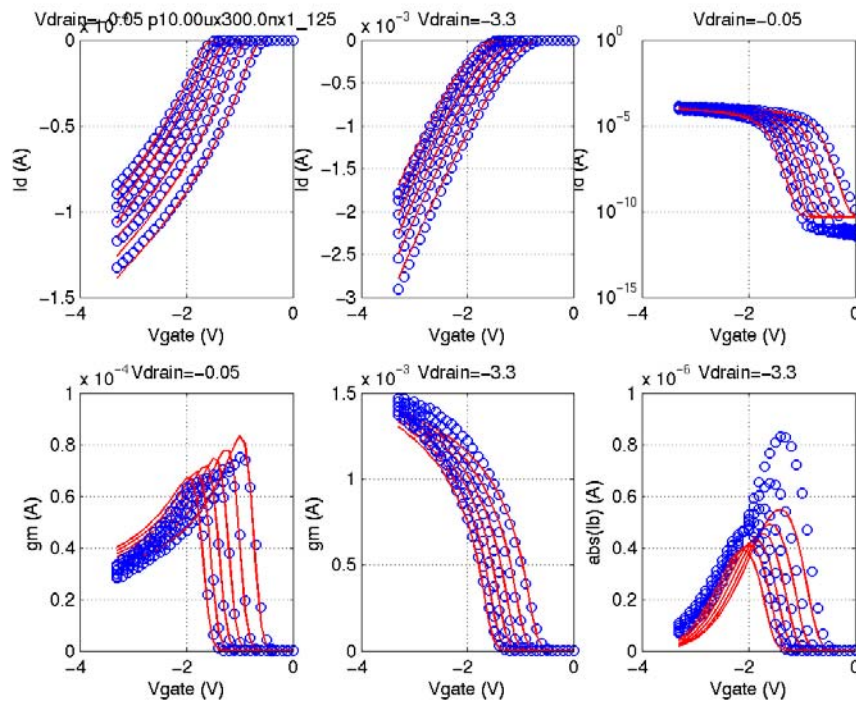


FIGURE 2.77 3p3v_PFET_10x0p3_idvd_125C

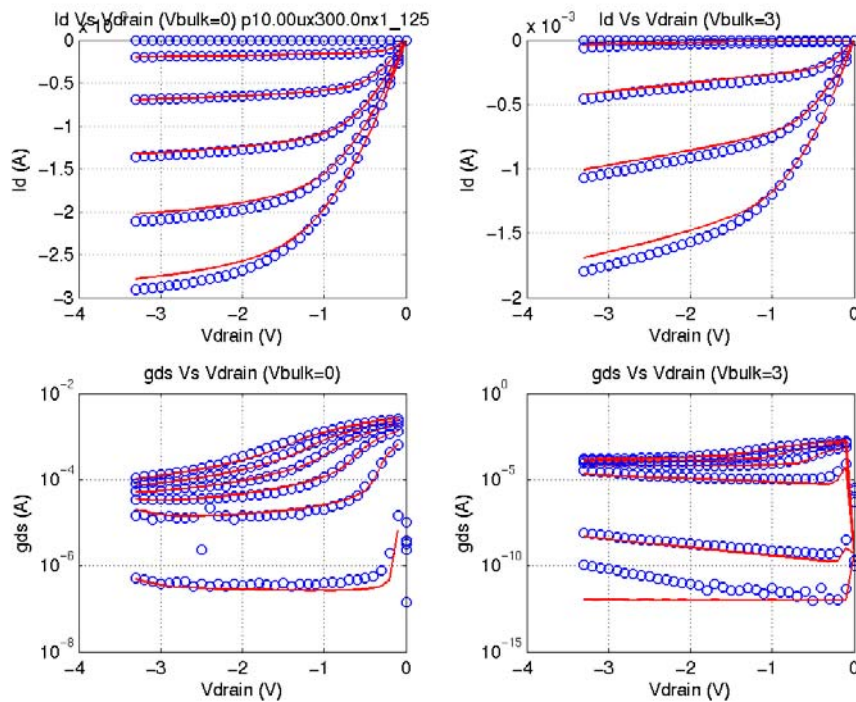
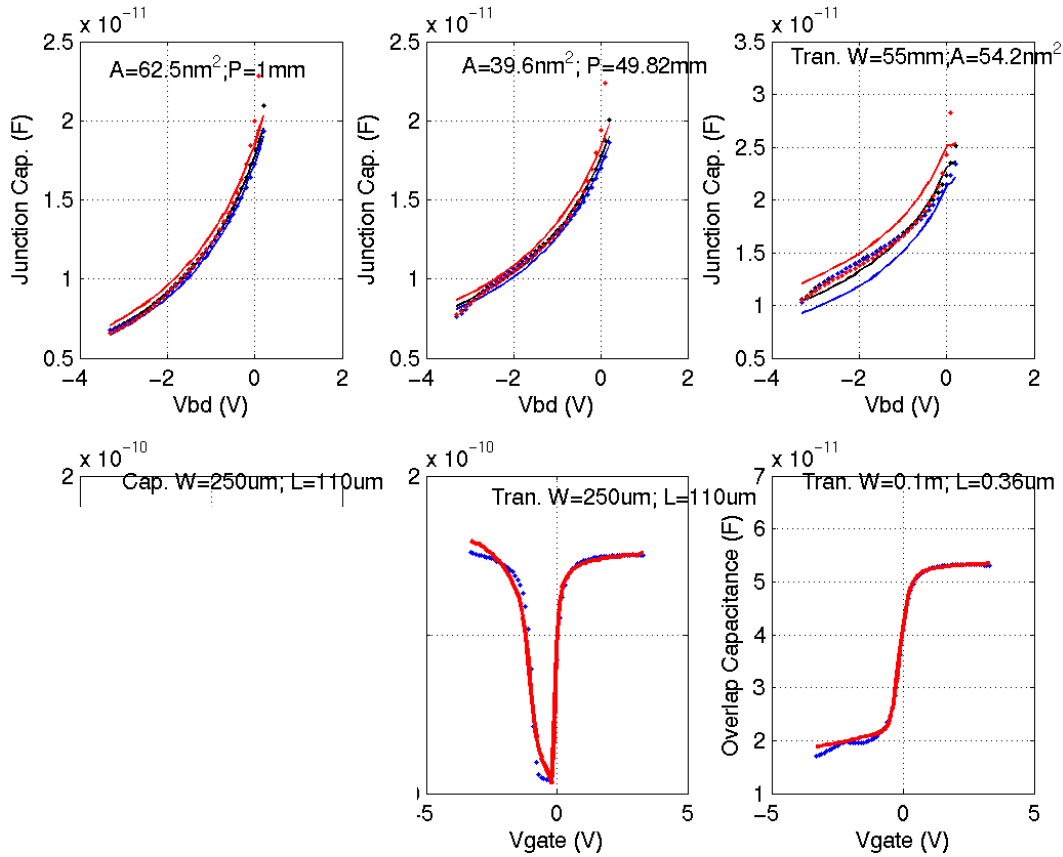


FIGURE 2.78 3p3_native_NFET_cv_25C



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FIGURE 2.79 3p3v_native_NFET_vtVsL_25C

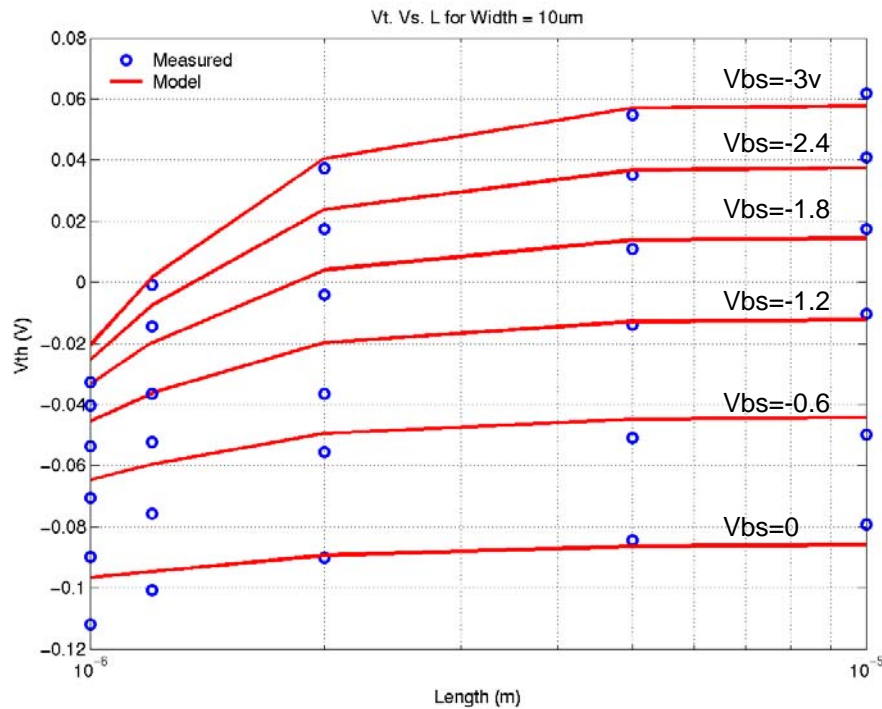


FIGURE 2.80 3p3v_native_NFET_vtVsW_25C

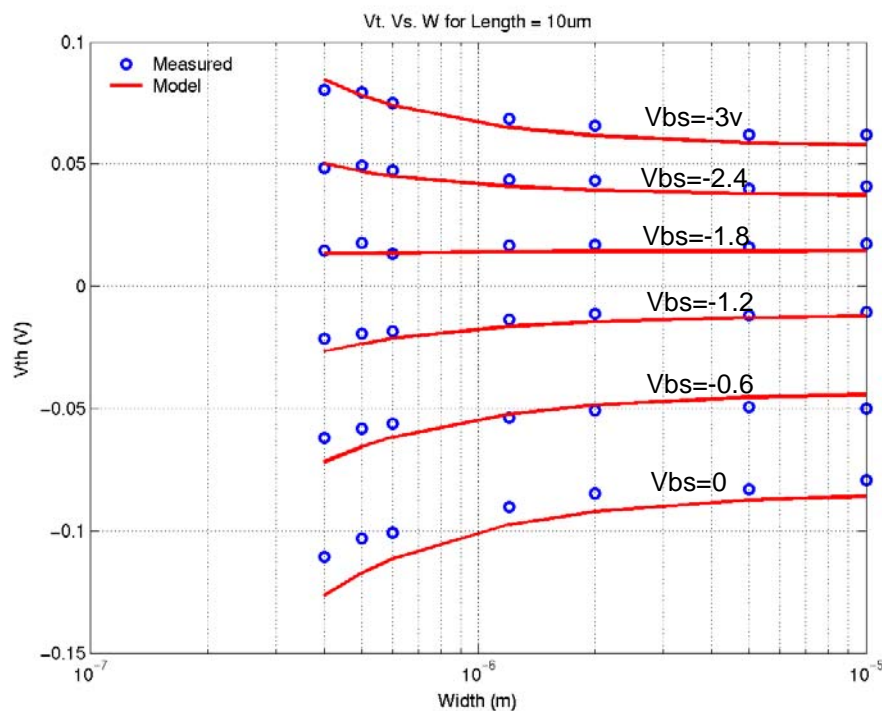


FIGURE 2.81 3p3v_native_NFET_10x10_idvg_25C

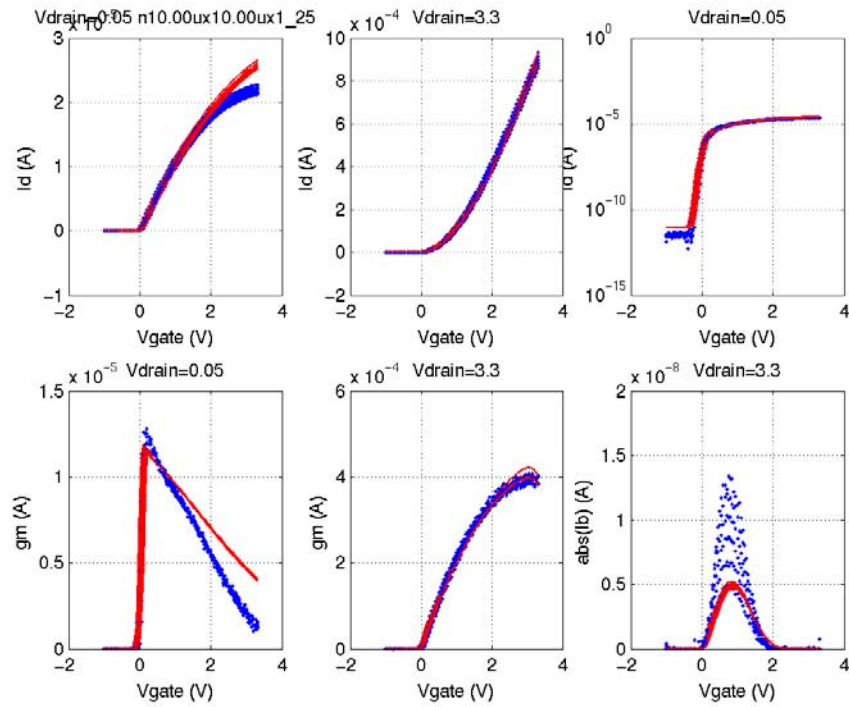


FIGURE 2.82 3p3v_native_NFET_10x10_idvd_25C

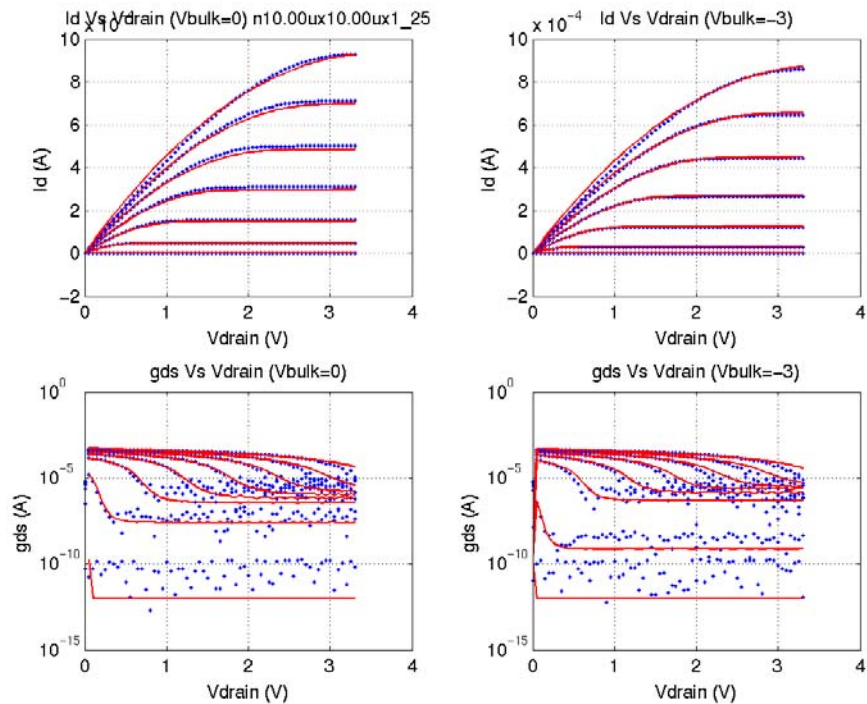


FIGURE 2.83 3p3v_native_NFET_10x1_idvg_25C

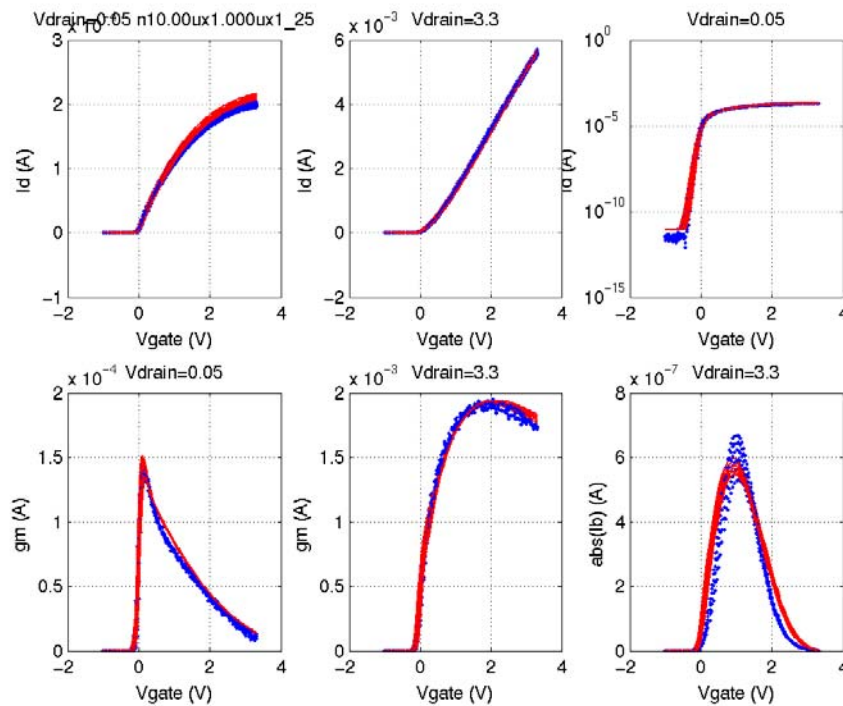


FIGURE 2.84 3p3v_native_NFET_10x1_idvd_25C

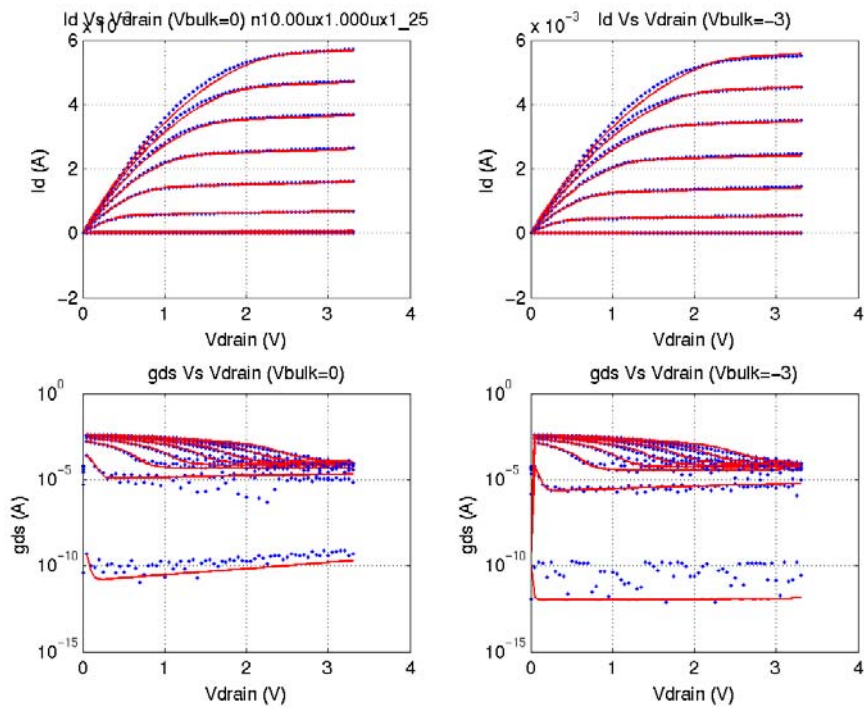


FIGURE 2.85 3p3v_native_NFET_0p4x10_idvg_25C

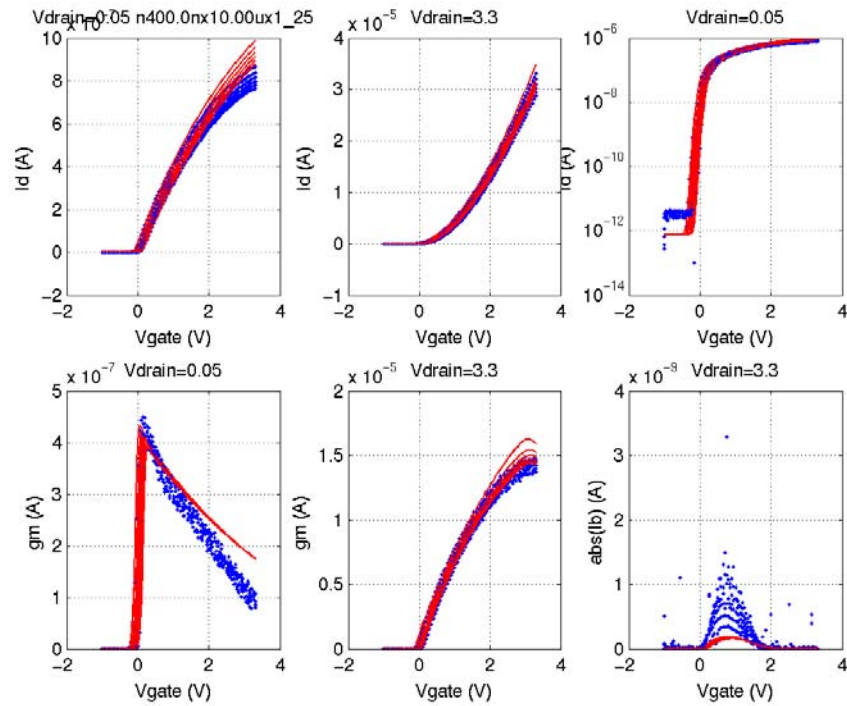


FIGURE 2.86 3p3v_native_NFET_0p4x10_idvd_25C

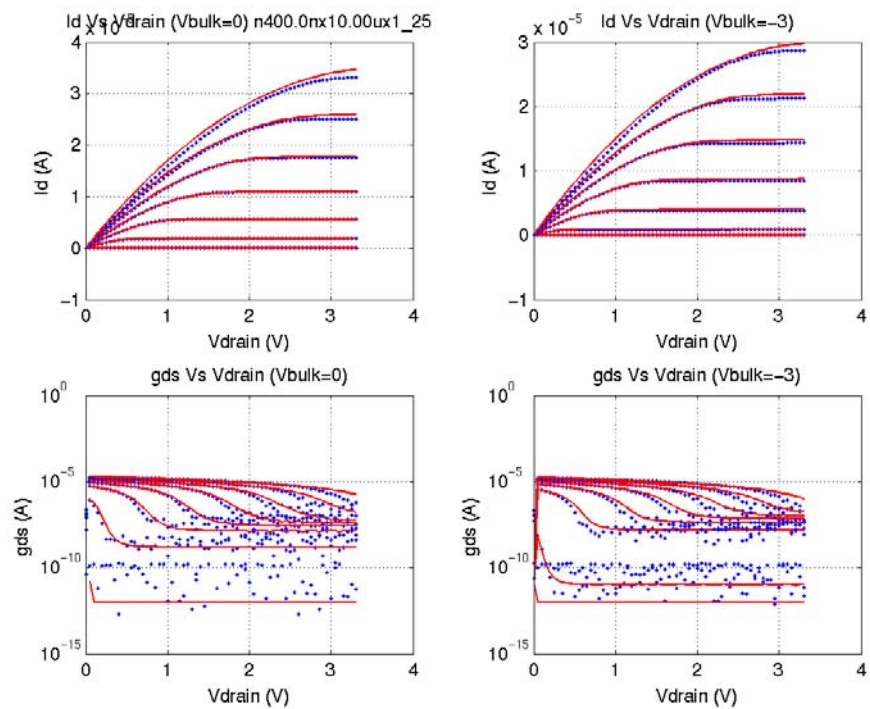


FIGURE 2.87 3p3v_native_NFET_0p4x1p2_idvg_25C

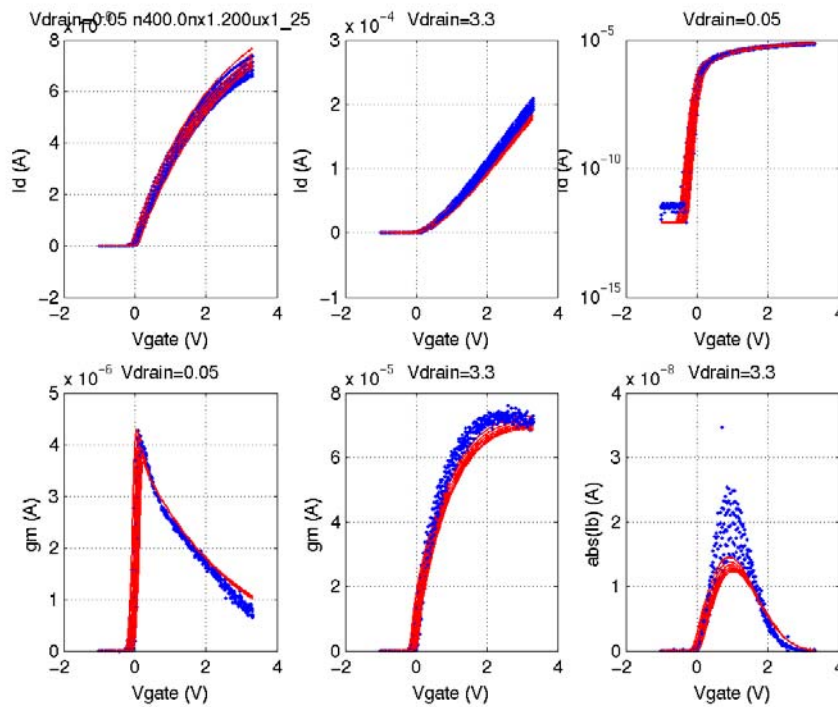


FIGURE 2.88 3p3v_native_NFET_0p4x1p2_idvd_25C

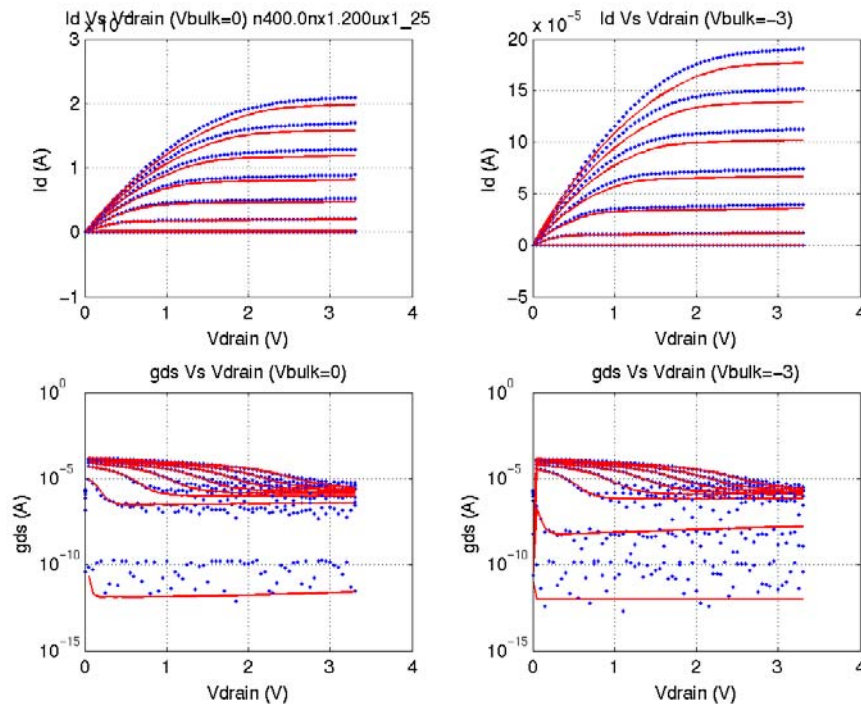


FIGURE 2.89 3p3v_native_NFET_0p6x1p2_idvg_25C

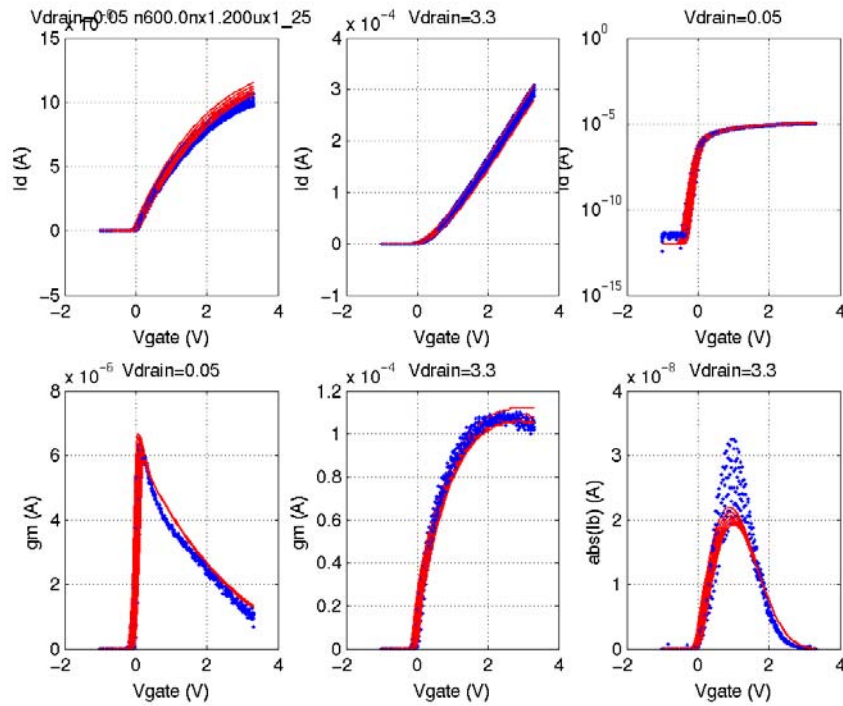


FIGURE 2.90 3p3v_native_NFET_0p6x1p2_idvd_25C

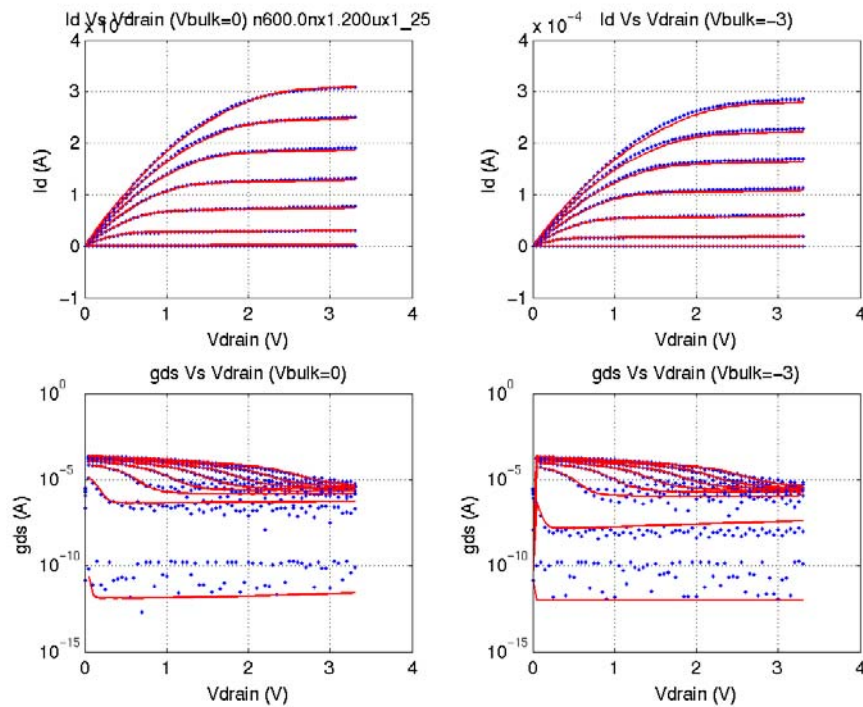


FIGURE 2.91 3p3v_native_NFET_10x1p2_idvg_25C

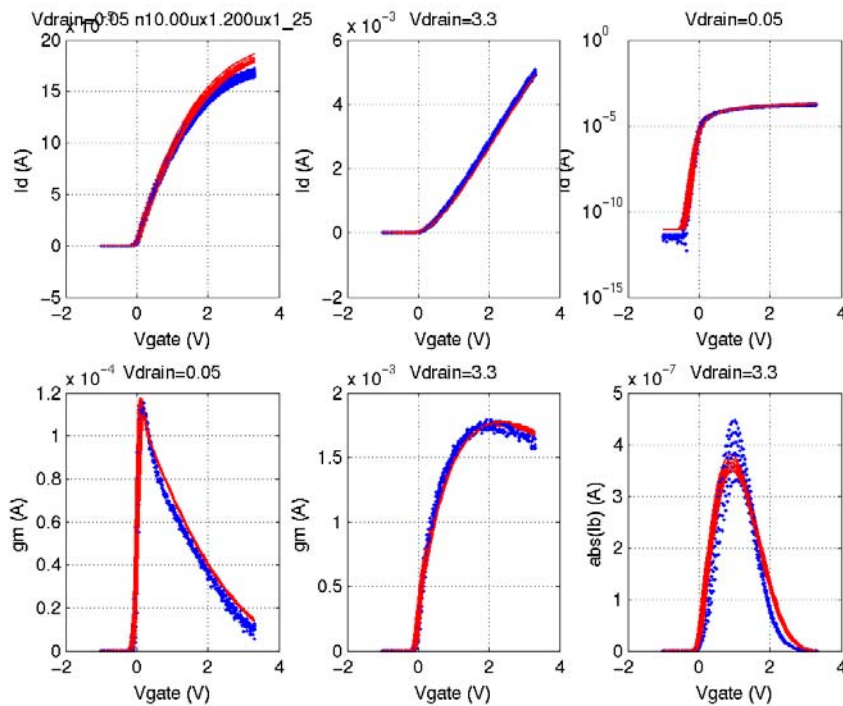


FIGURE 2.92 3p3v_native_NFET_10x1p2_idvd_25C

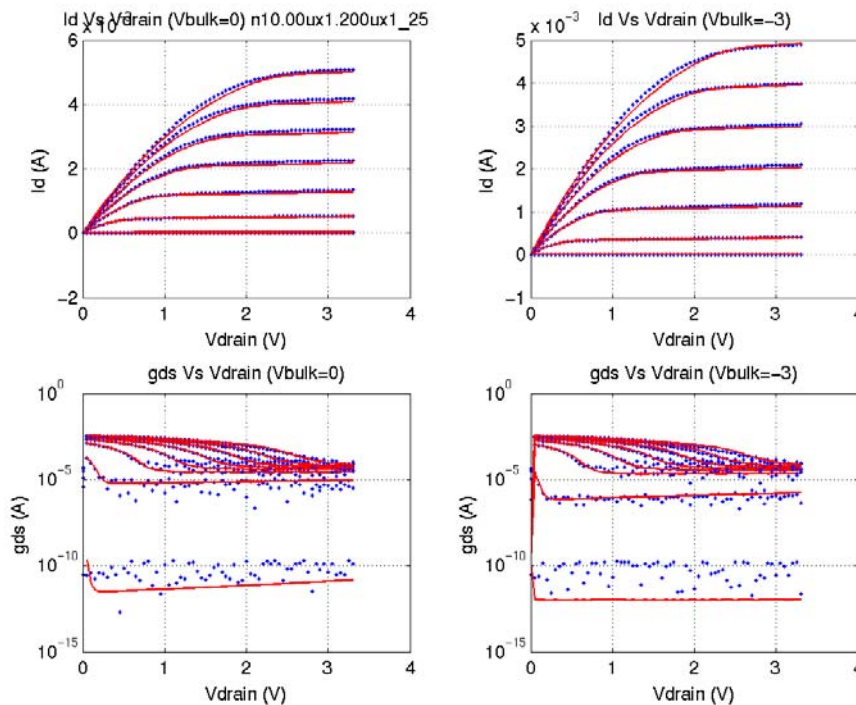


FIGURE 2.93 3p3v_native_NFET_10x1_idvg_-40C

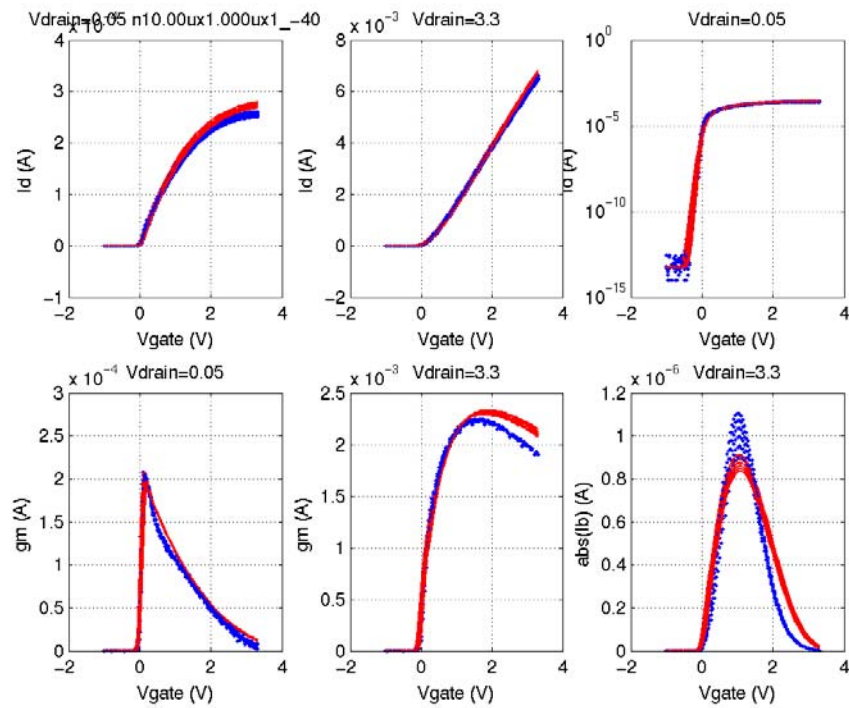


FIGURE 2.94 3p3v_native_NFET_10x1_idvd_-40C

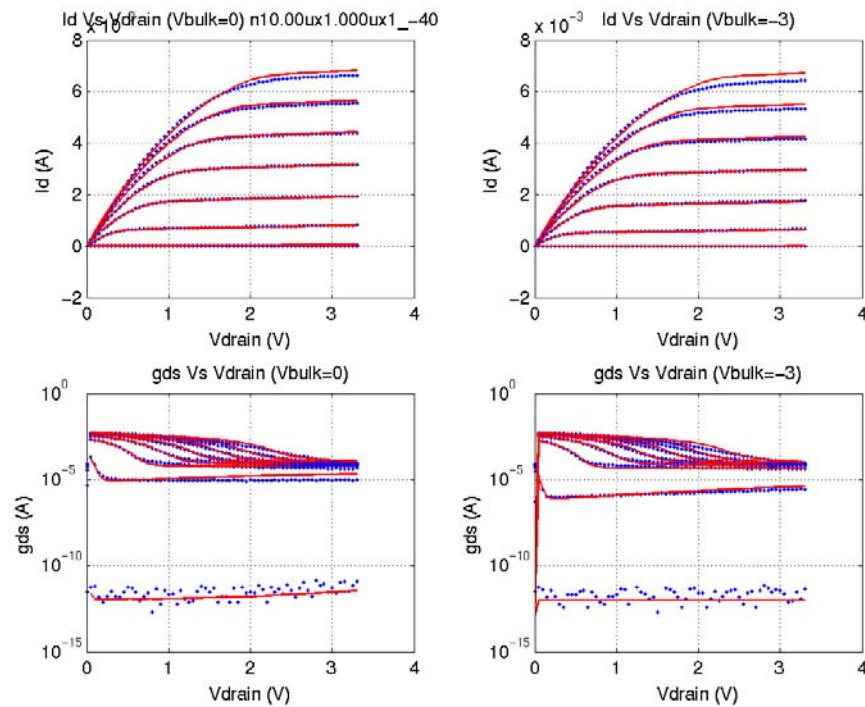


FIGURE 2.95 3p3v_native_NFET_10x1_idvg_125C

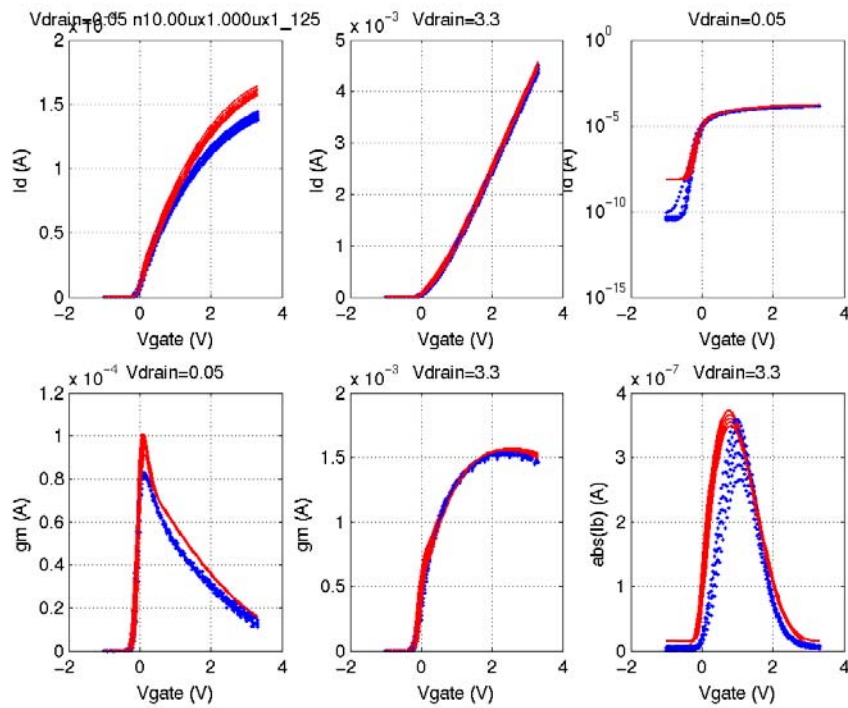


FIGURE 2.96 3p3v_native_NFET_10x1_idvd_125C

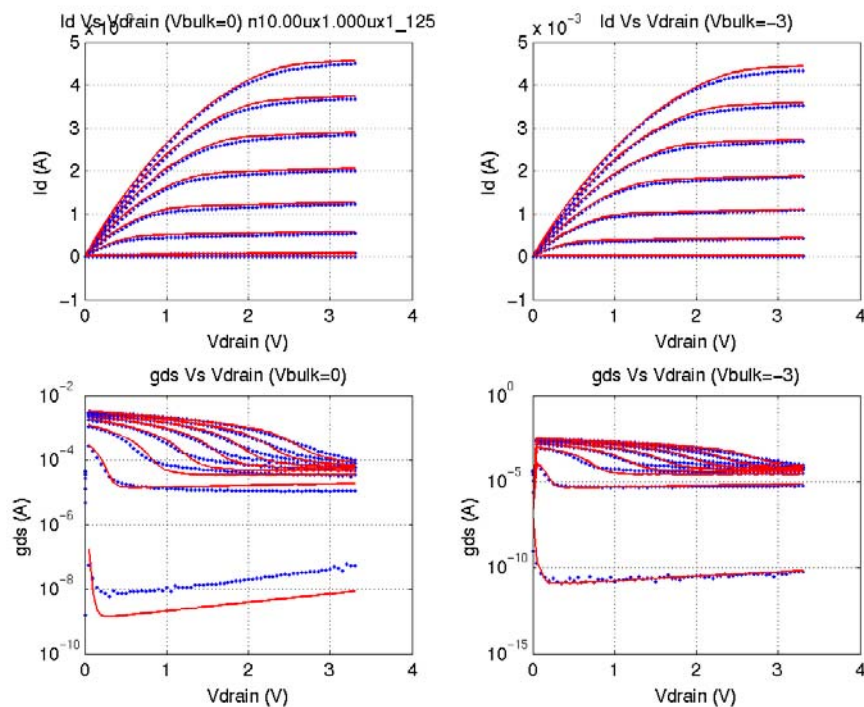


FIGURE 2.97 5p0_NFET_cv

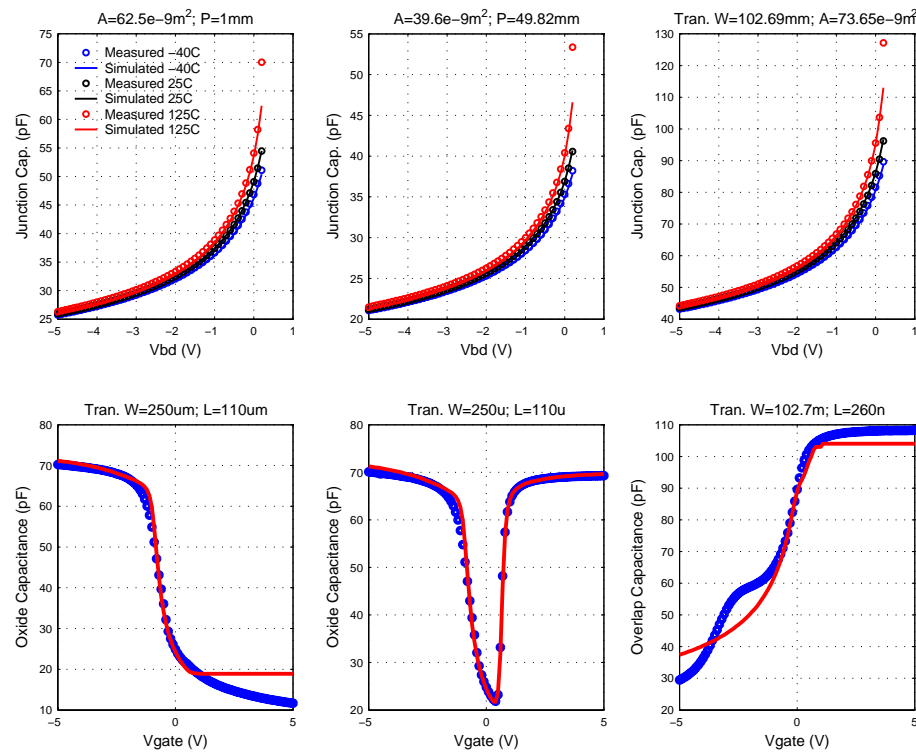


FIGURE 2.98 5p0_NFET_vtVsL_25C

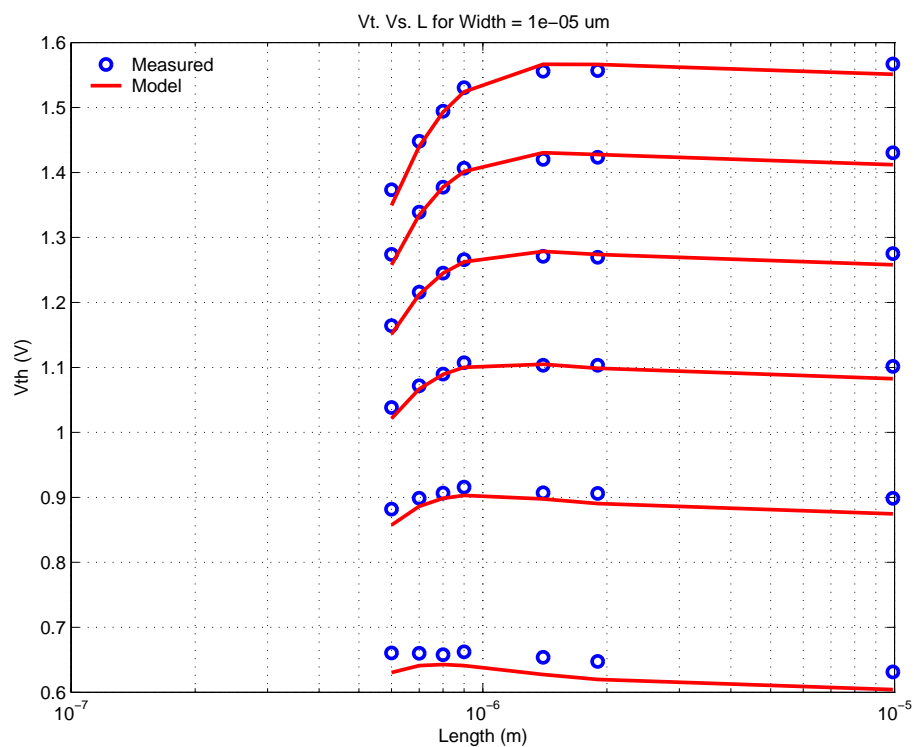


FIGURE 2.99 5p0_NFET_vtVsW_25C

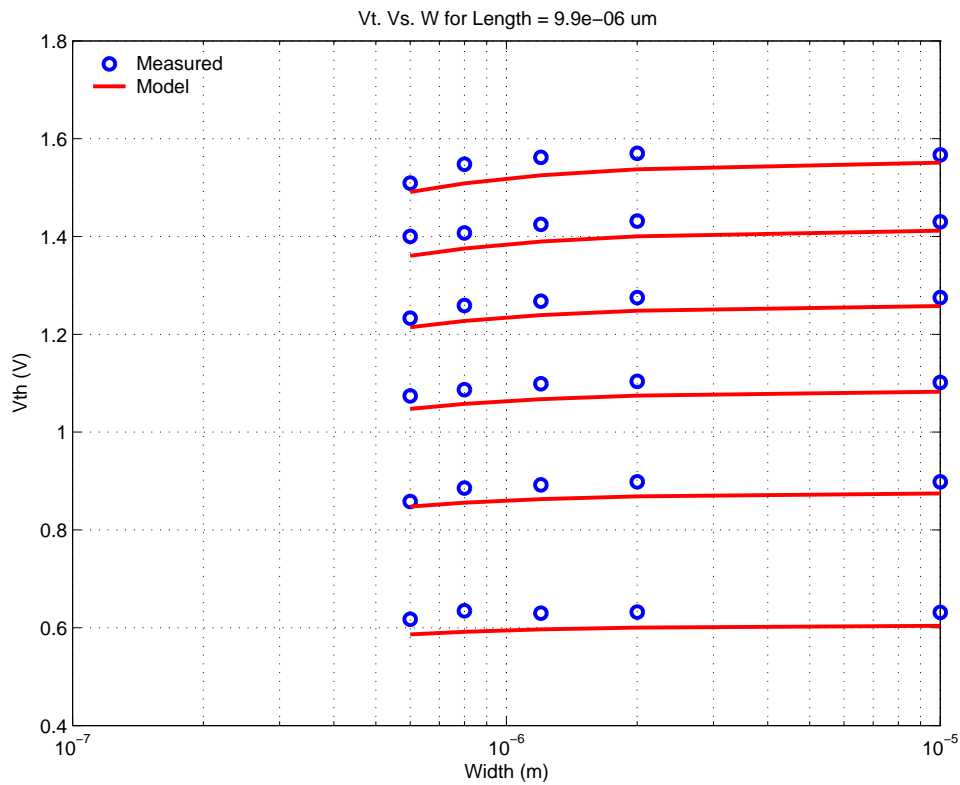


FIGURE 2.100 5p0_NFET_10x9p9_idvd_25C

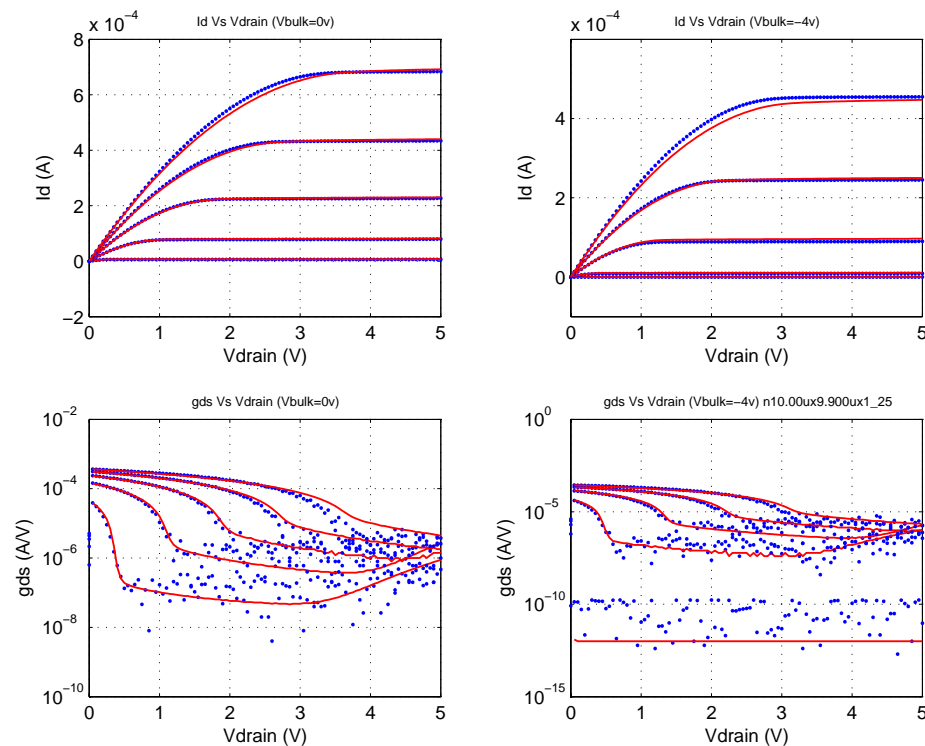


FIGURE 2.101 5p0_NFET_10x9p9_idvg_25C

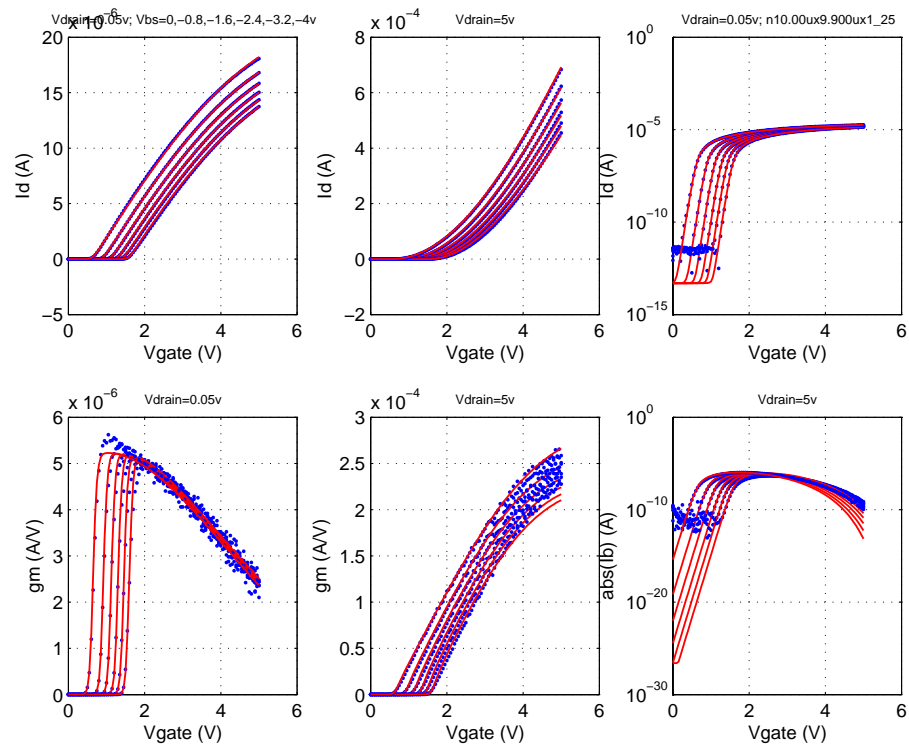


FIGURE 2.102 5p0_NFET_10x0p6_idvd_25C

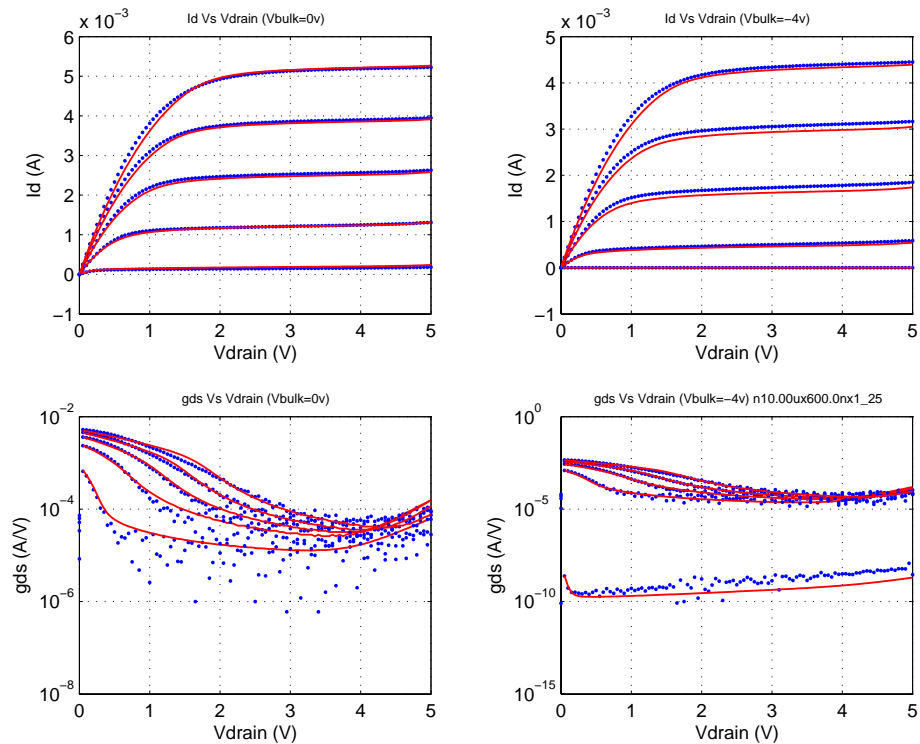


FIGURE 2.103 5p0_NFET_10x0p6_idvg_25C

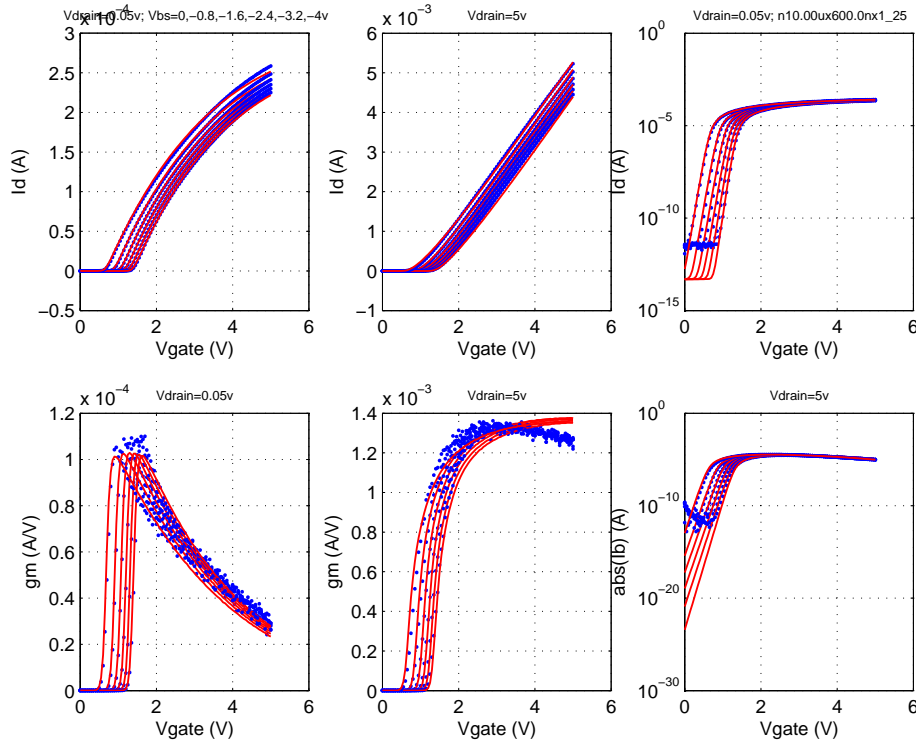


FIGURE 2.104 5p0_NFET_0p6x9p9_idvd_25C

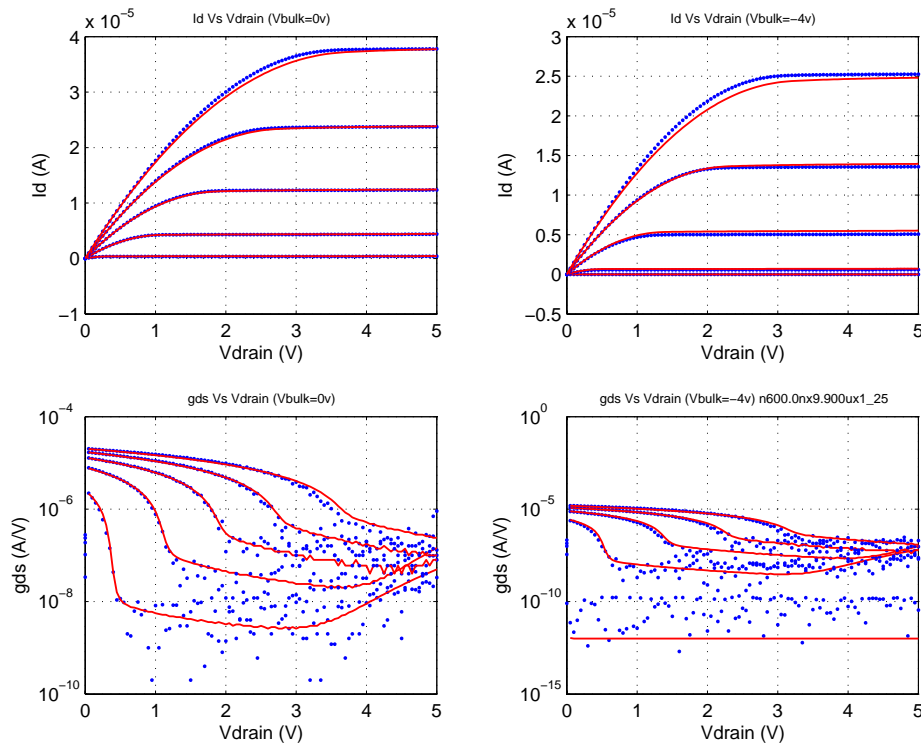


FIGURE 2.105 5p0_NFET_0p6x9p9_idvg_25C

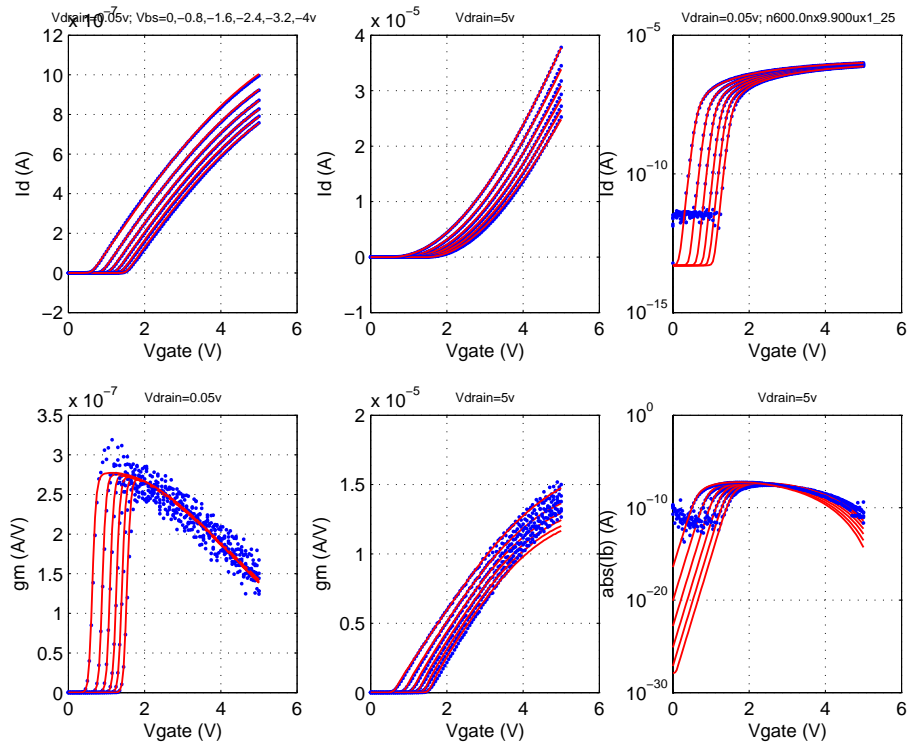


FIGURE 2.106 5p0_NFET_0p6x0p7_idvd_25C

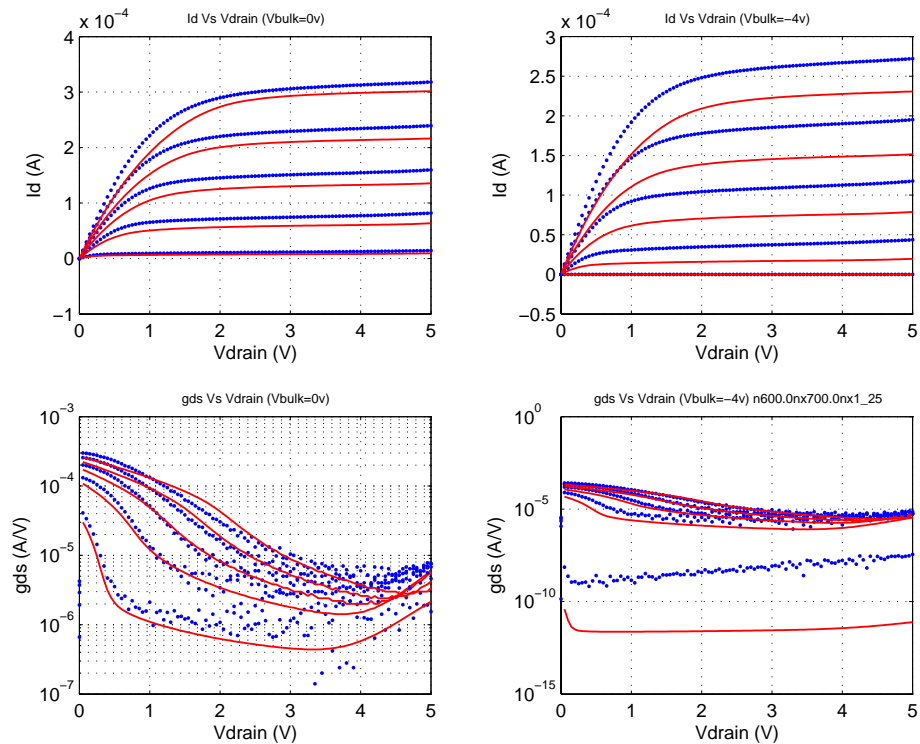


FIGURE 2.107 5p0_NFET_0p6x0p7_idvg_25C

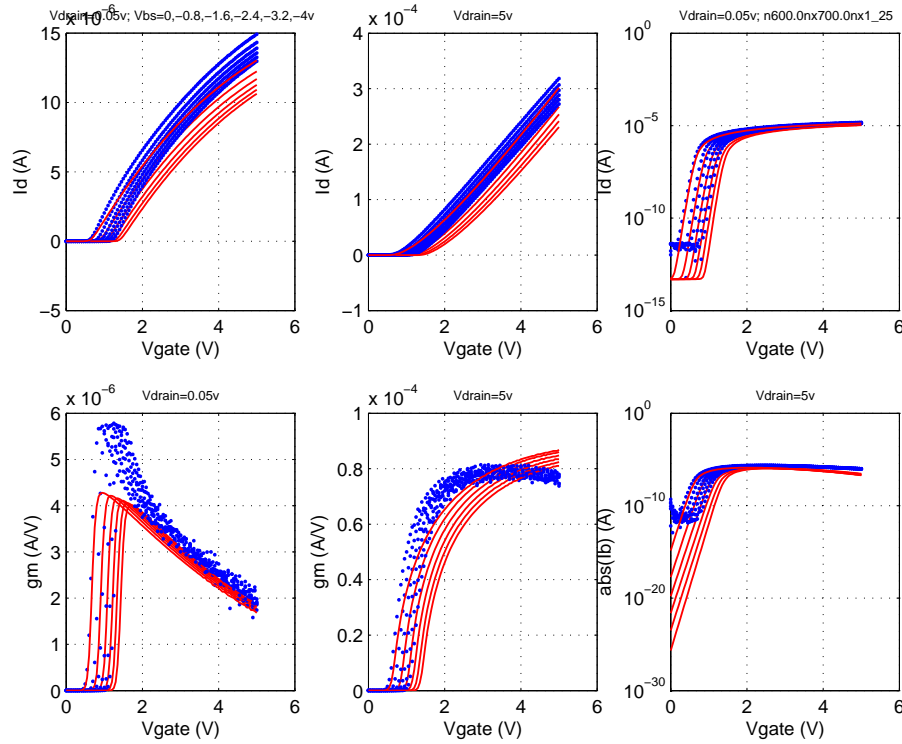


FIGURE 2.108 5p0_NFET_0p7x0p7_idvd_25C

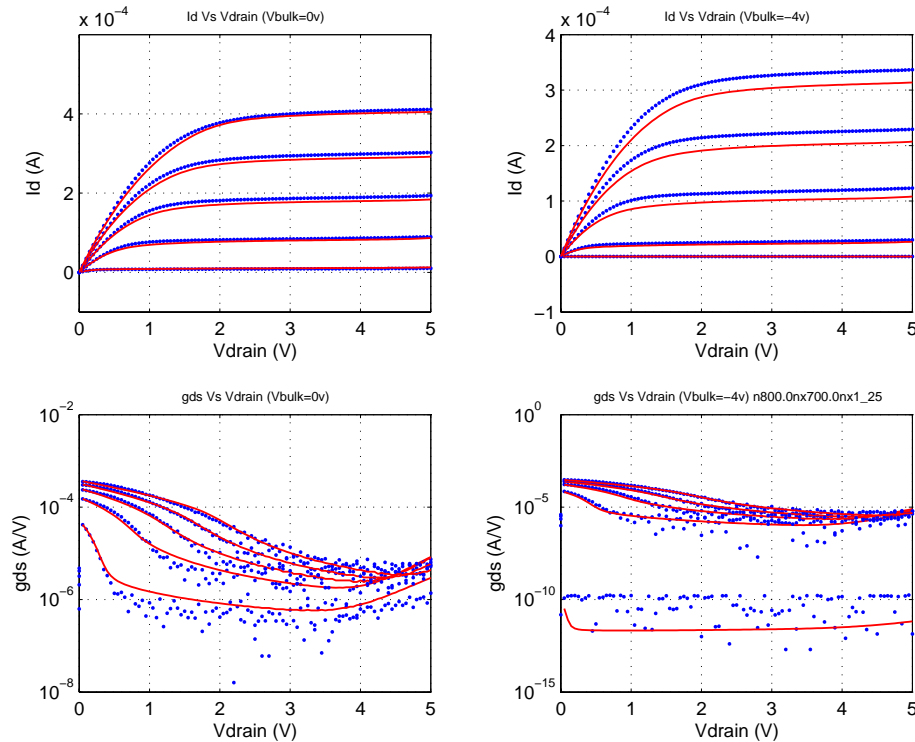


FIGURE 2.109 5p0_NFET_0p7x0p7_idvg_25C

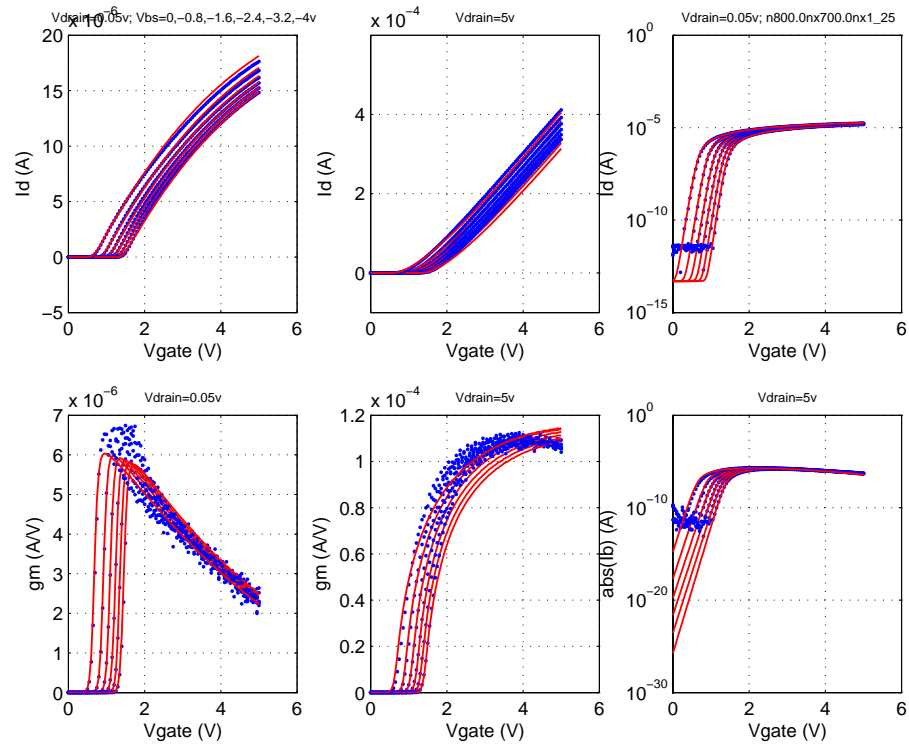


FIGURE 2.110 5p0_NFET_10x0p8_idvd_25C

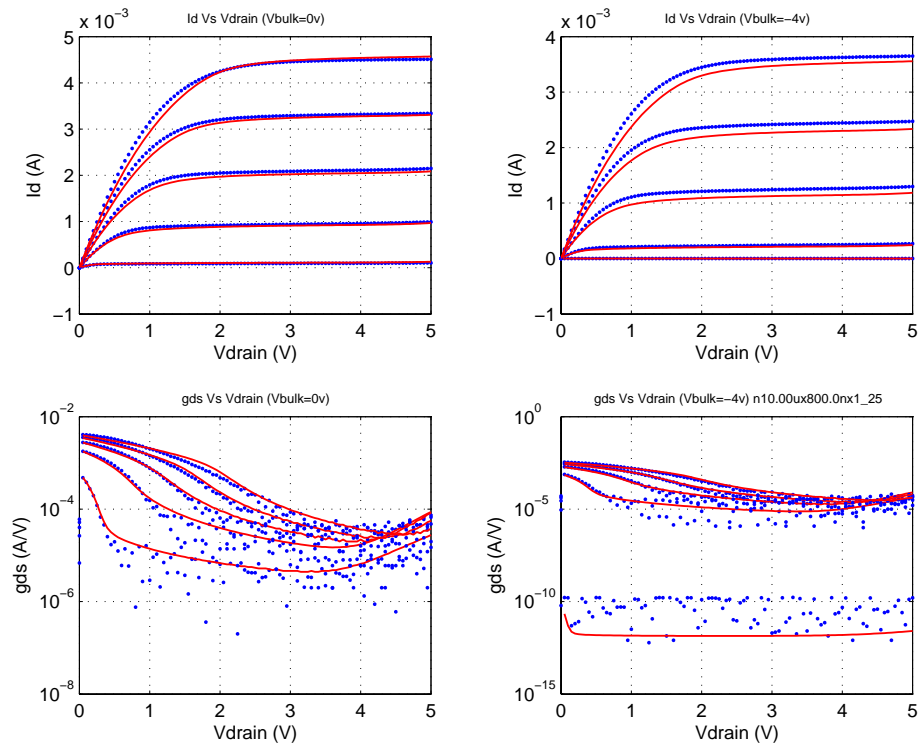


FIGURE 2.111 5p0_NFET_10x0p8_idvg_25C

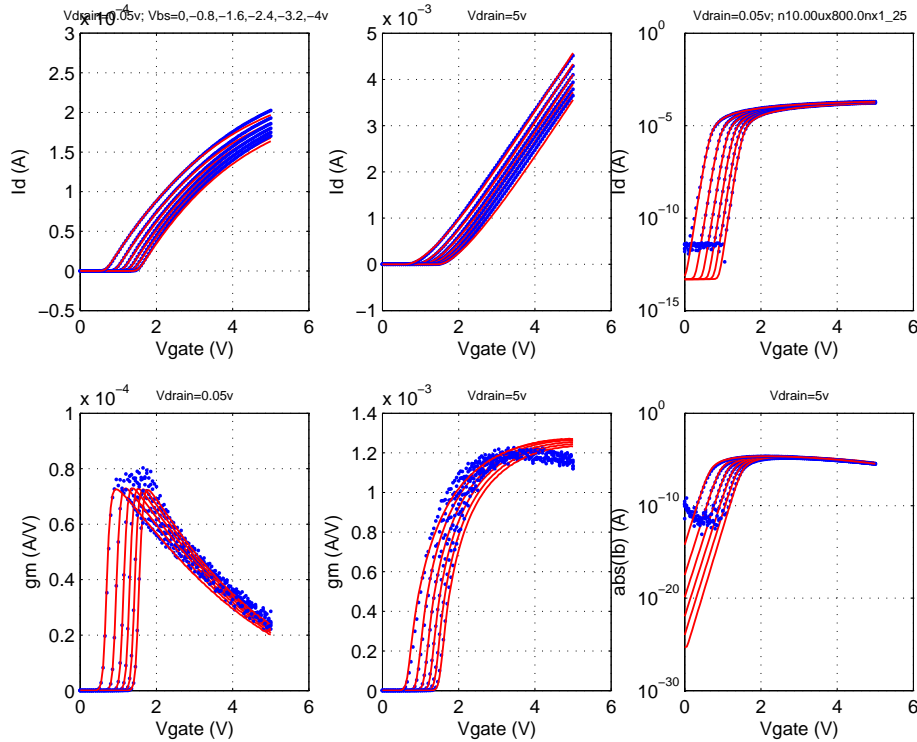


FIGURE 2.112 5p0_NFET_10x0p6_idvd_-40C

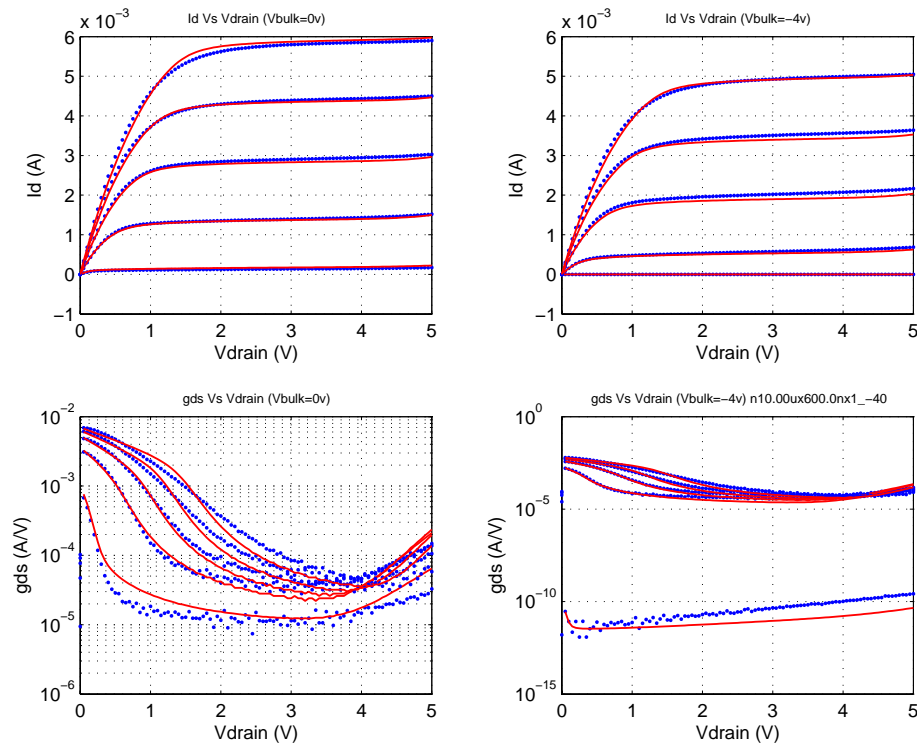


FIGURE 2.113 5p0_NFET_10x0p6_idvg_-40C

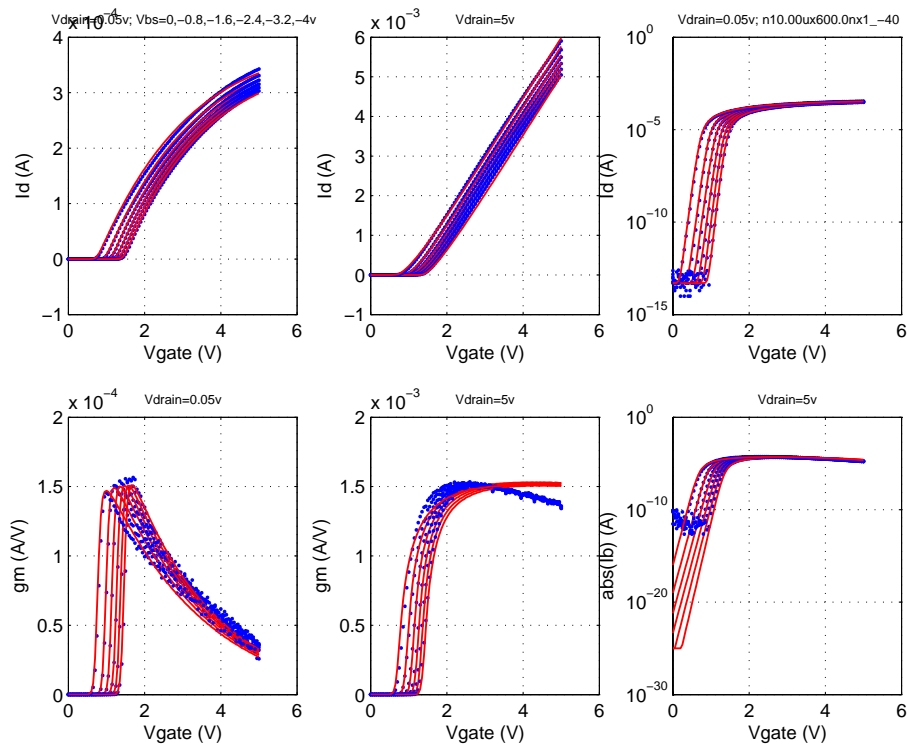


FIGURE 2.114 5p0_NFET_10x0p6_idvd_125C

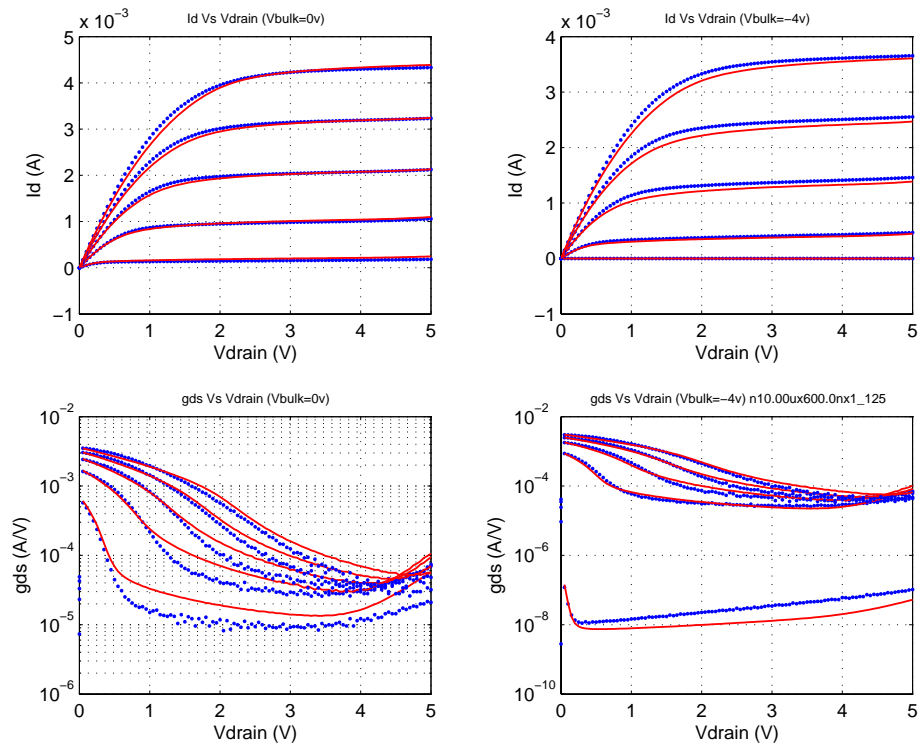


FIGURE 2.115 5p0_NFET_10x0p6_idvg_125C

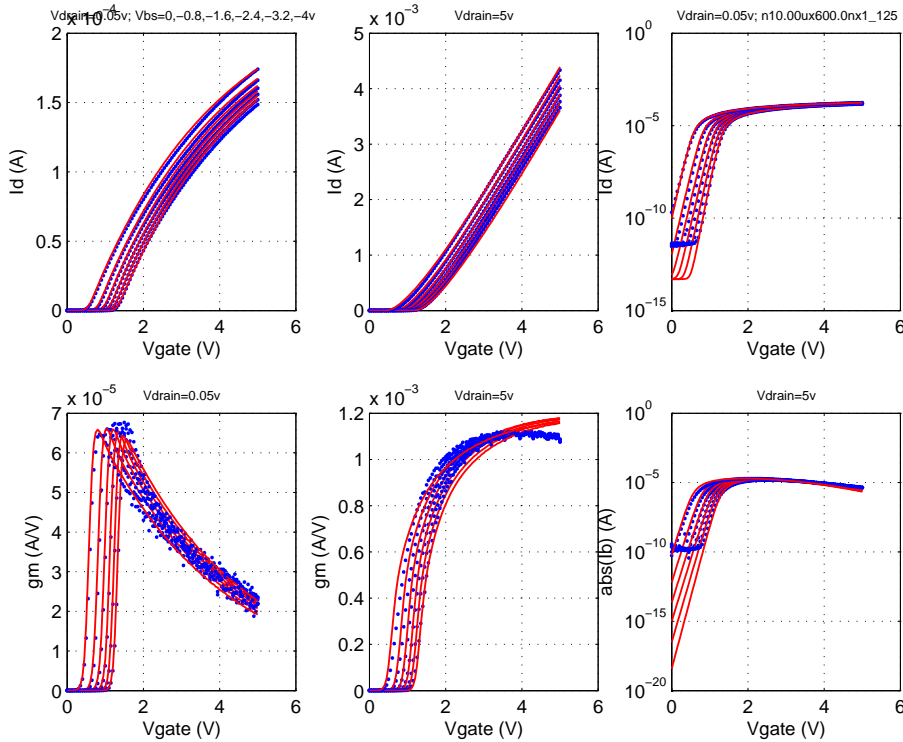


FIGURE 2.116 5p0_PFET_cv

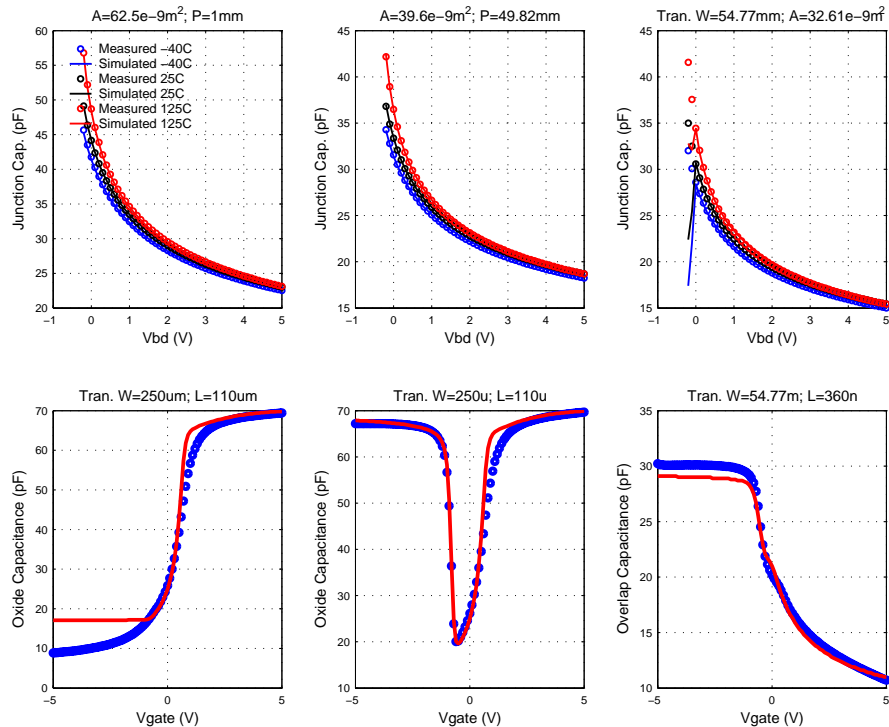


FIGURE 2.117 5p0_PFET_vtVsL_25C

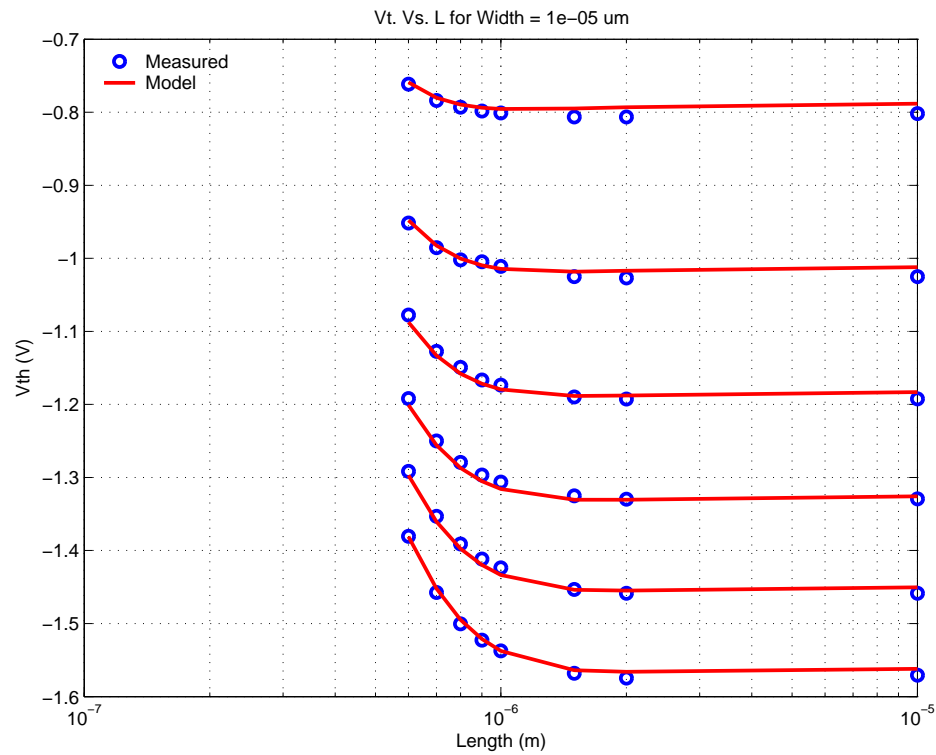


FIGURE 2.118 5p0_PFET_vtVsW_25C

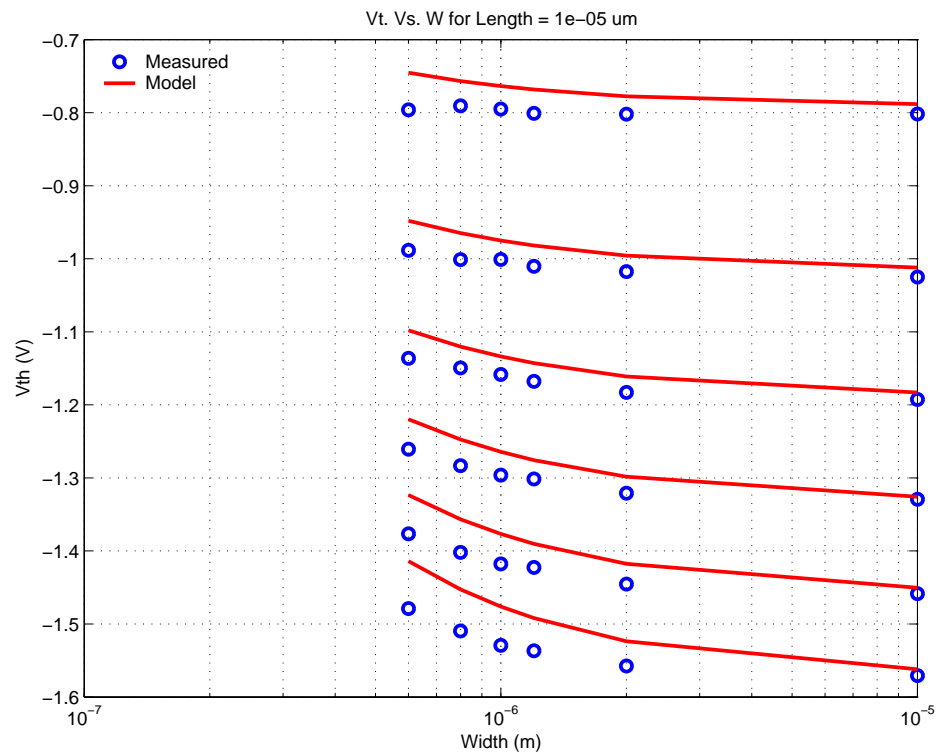


FIGURE 2.119 5p0_PFET_10x10_idvd_25C

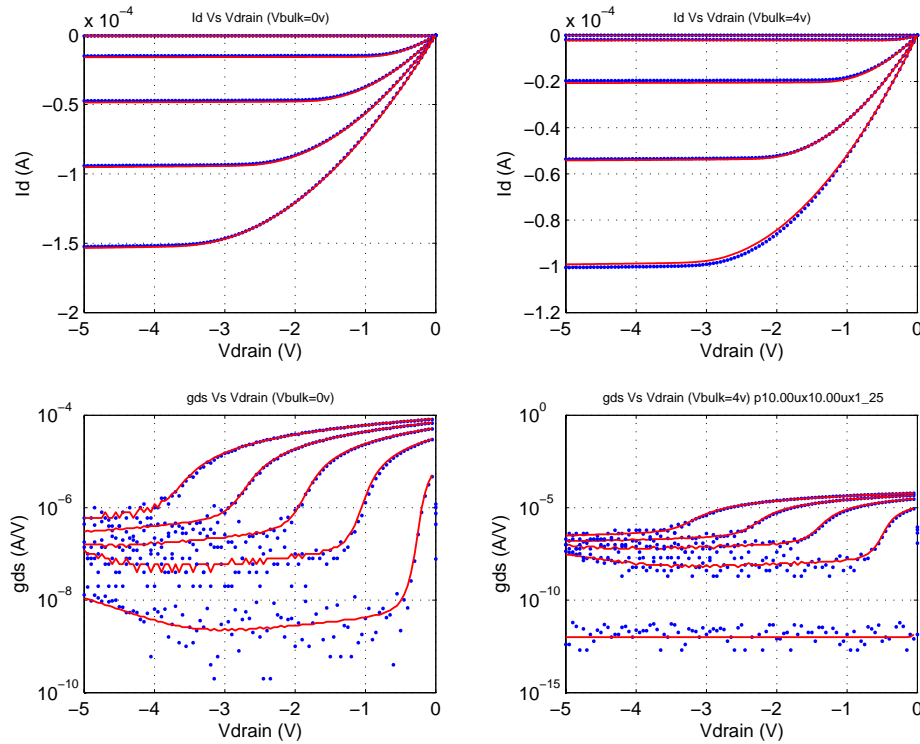


FIGURE 2.120 5p0_PFET_10x10_idvg_25C

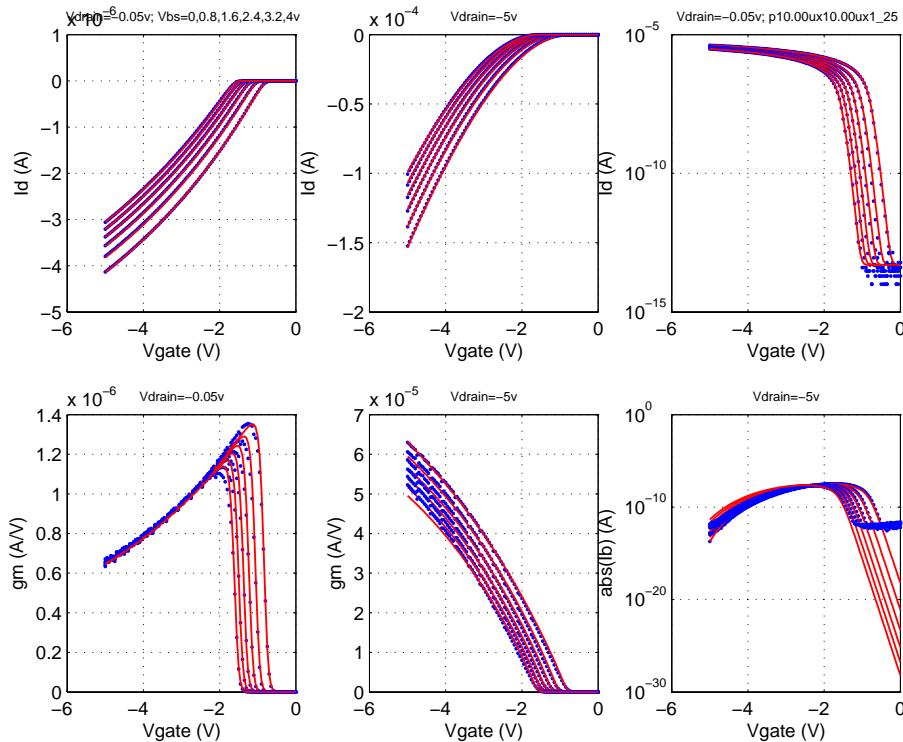


FIGURE 2.121 5p0_PFET_10x0p6_idvd_25C

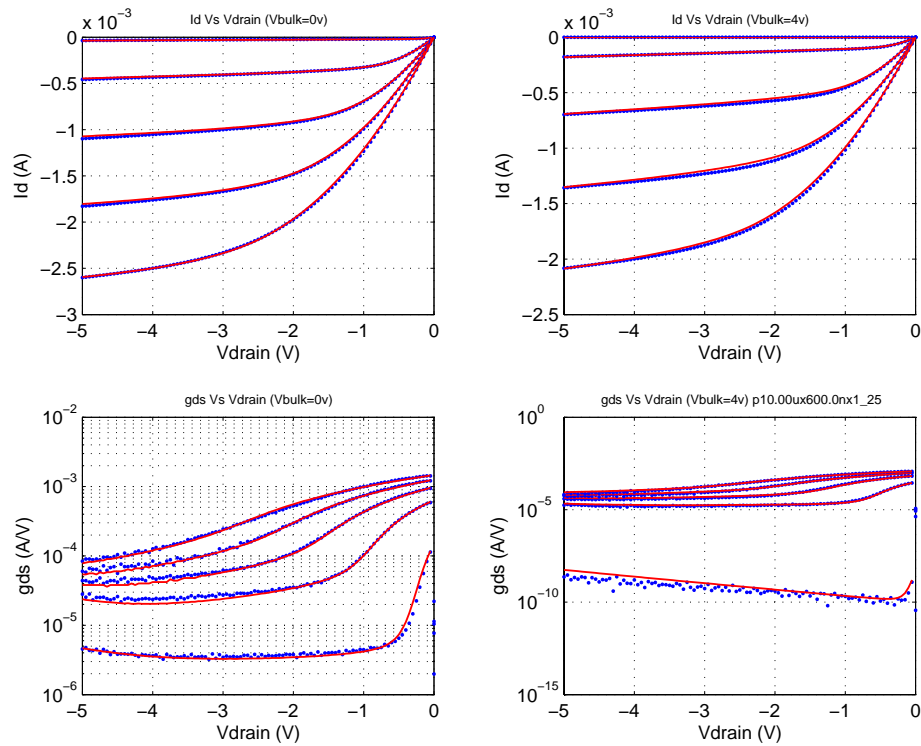


FIGURE 2.122 5p0_PFET_10x0p6_idvg_25C

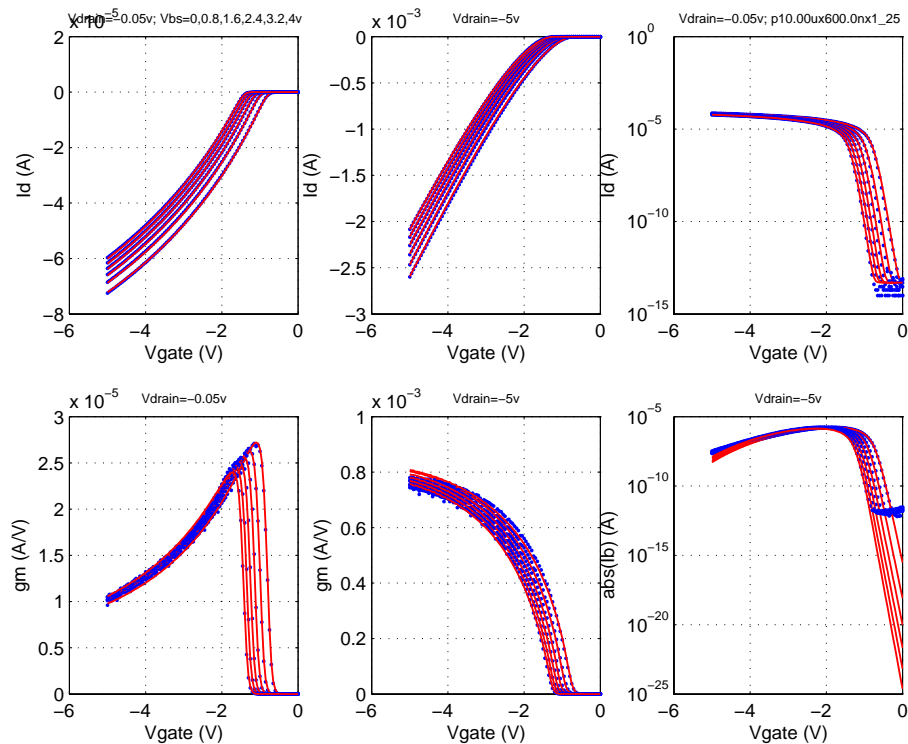


FIGURE 2.123 5p0_PFET_0p6x10_idvd_25C

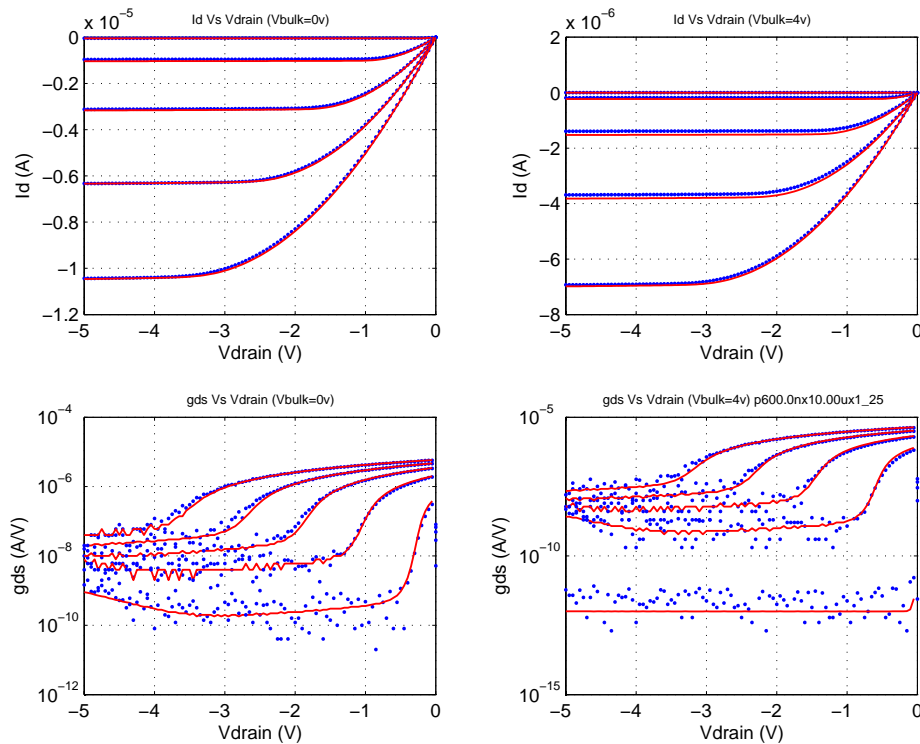


FIGURE 2.124 5p0_PFET_0p6x10_idvg_25C

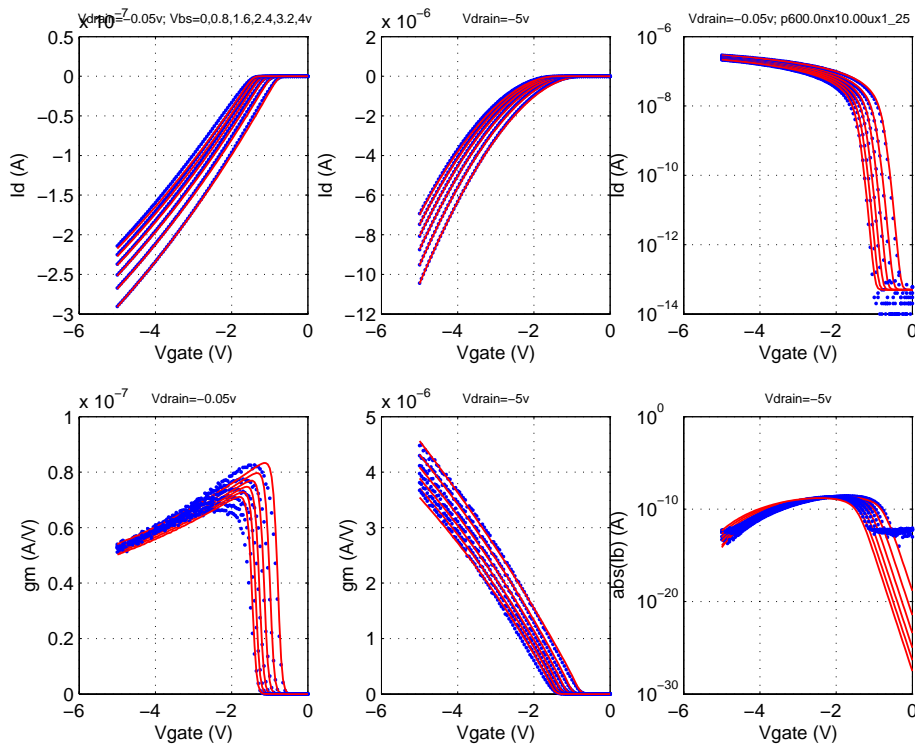


FIGURE 2.125 5p0_PFET_0p6x0p6_idvd_25C

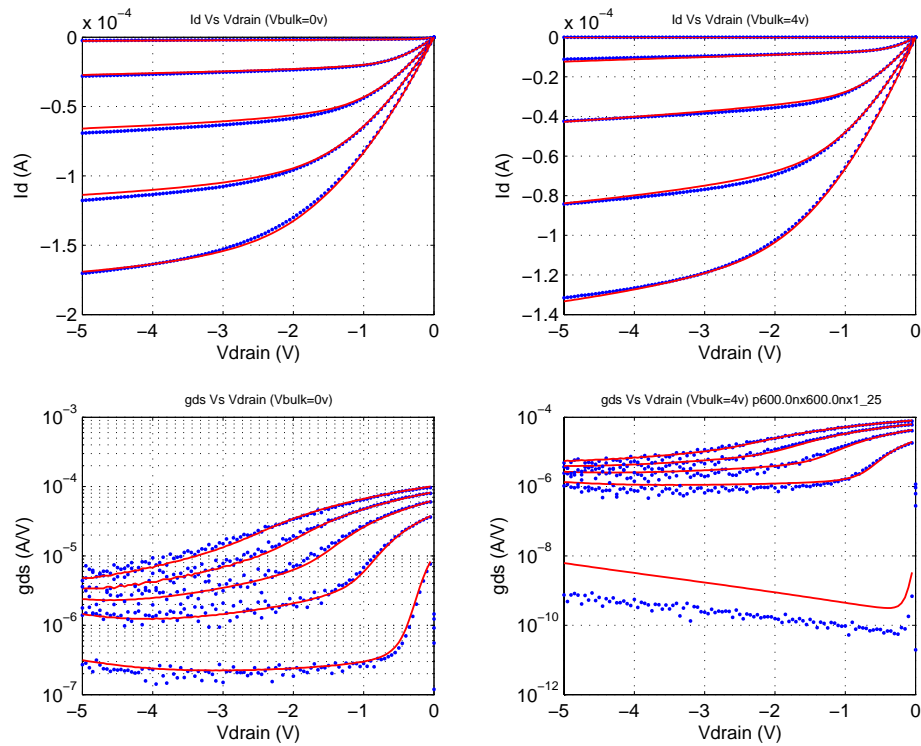


FIGURE 2.126 5p0_PFET_0p6x0p6_idvg_25C

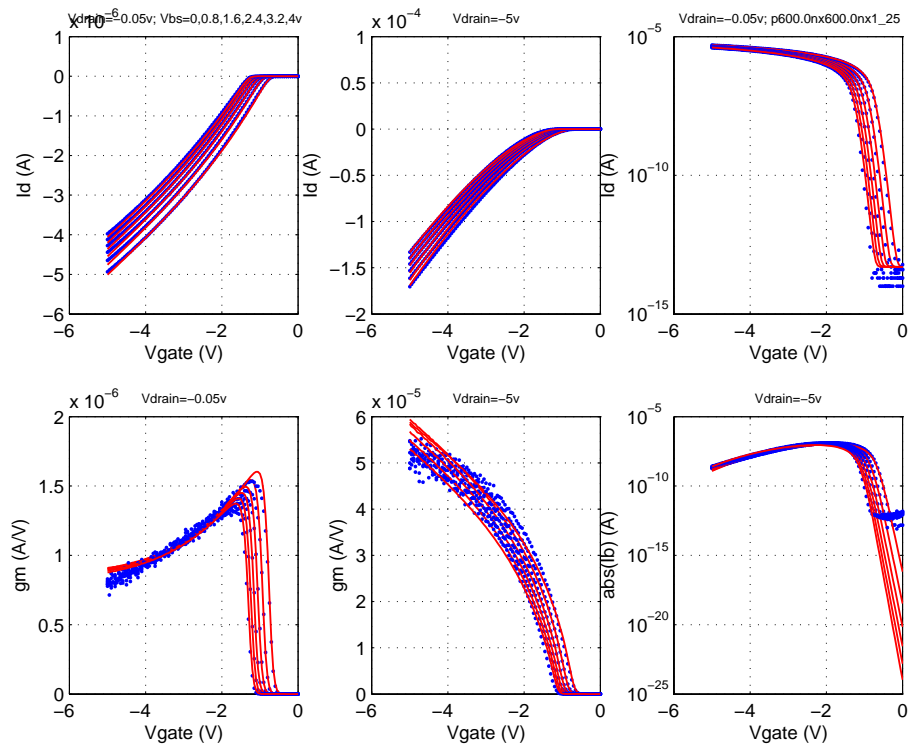


FIGURE 2.127 5p0_PFET_0p7x0p8_idvd_25C

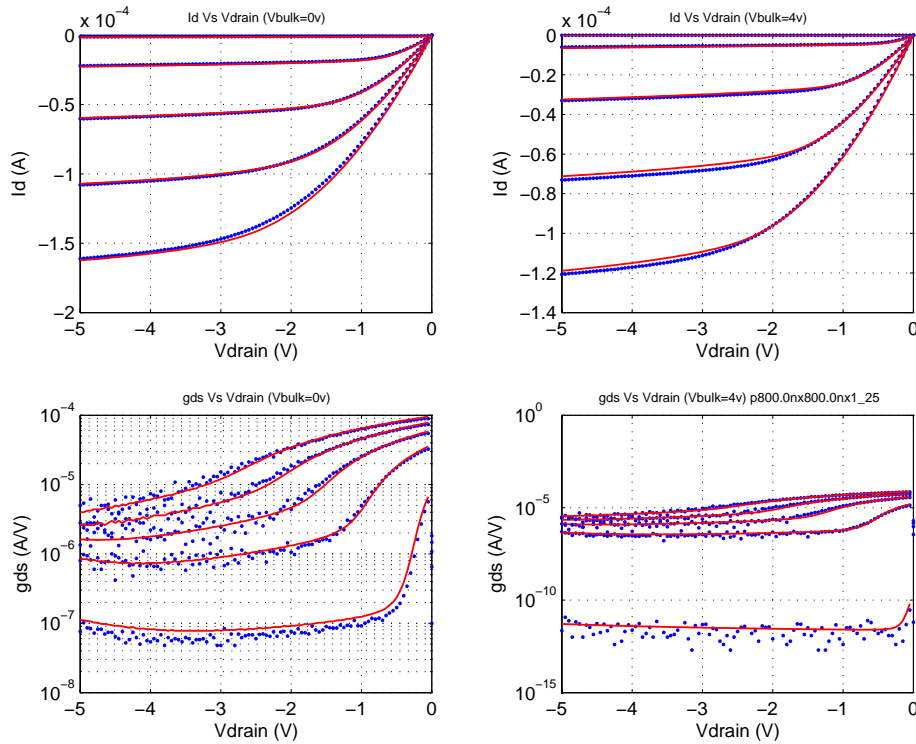


FIGURE 2.128 5p0_PFET_0p7x0p8_idvg_25C

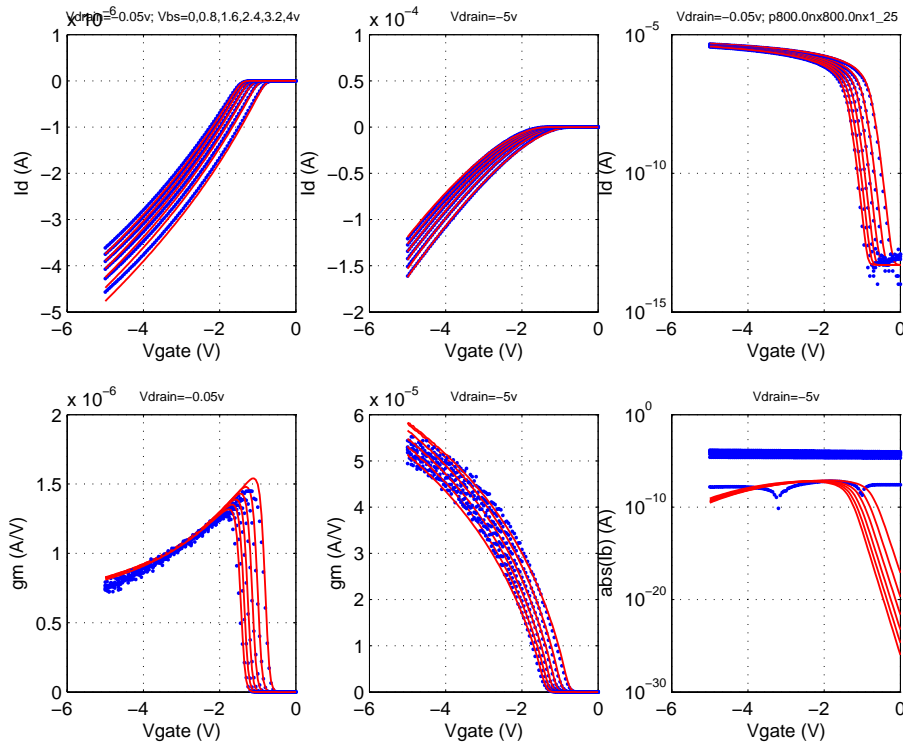


FIGURE 2.129 5p0_PFET_10x0p8_idvd_25C

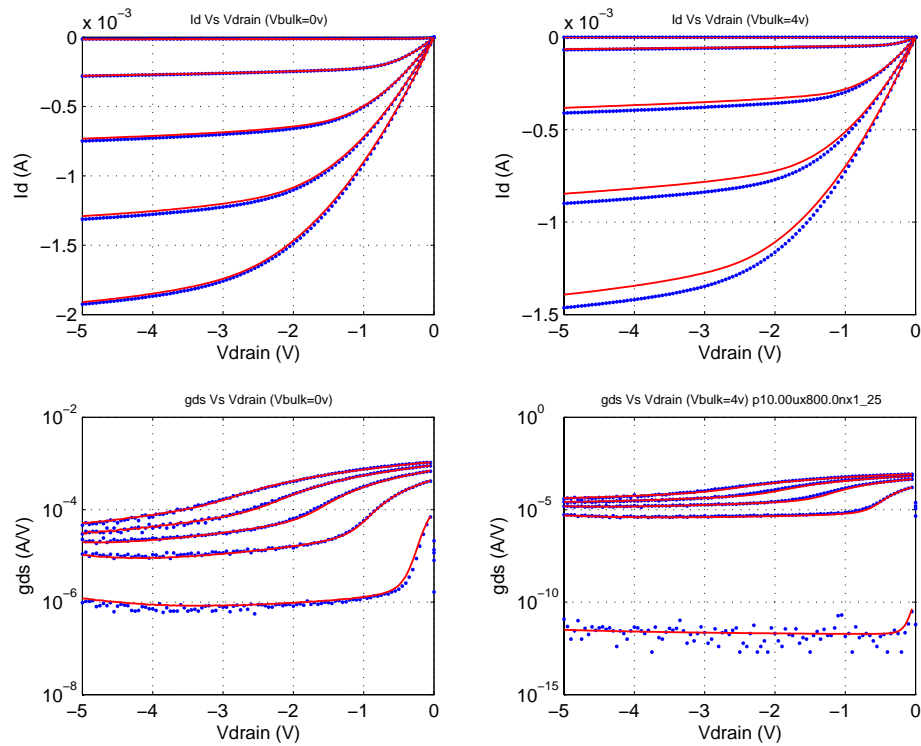


FIGURE 2.130 5p0_PFET_10x0p8_idvg_25C

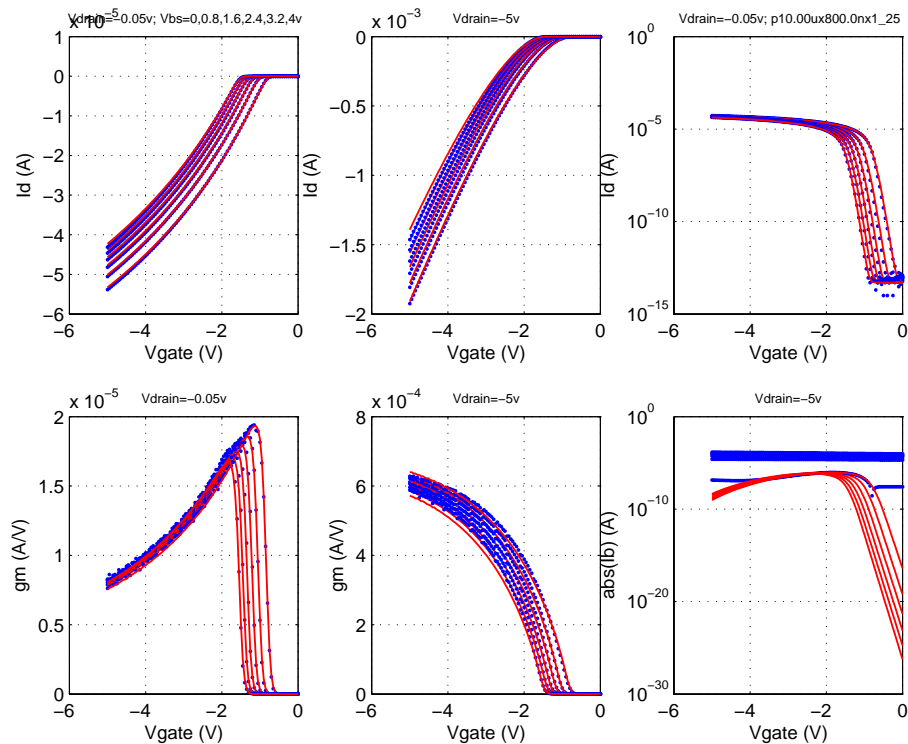


FIGURE 2.131 5p0_PFET_10x0p6_idvd_-40C

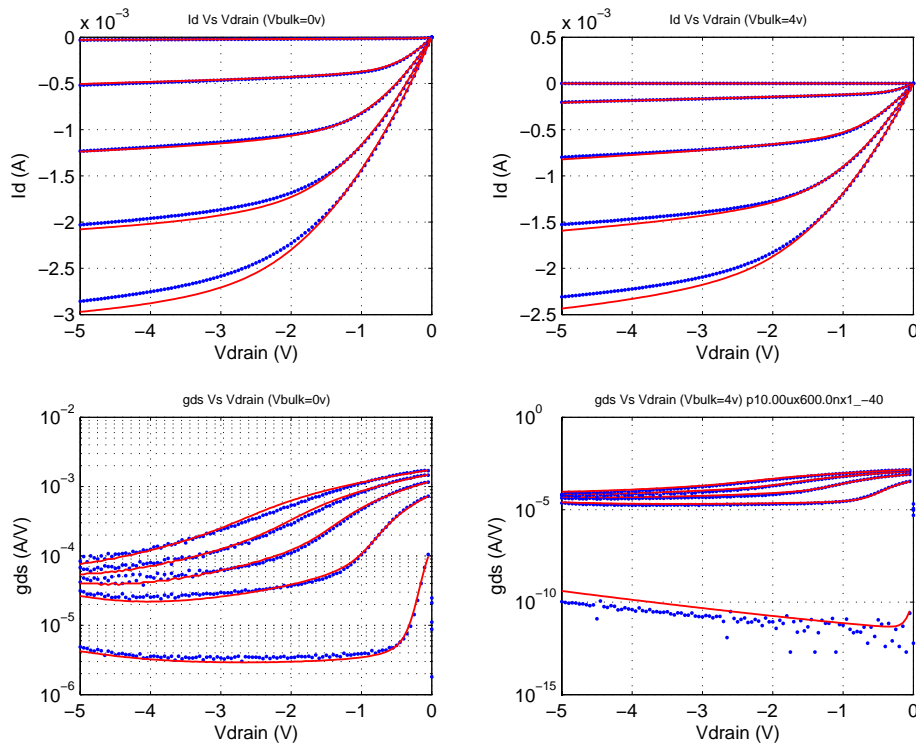


FIGURE 2.132 5p0_PFET_10x0p6_idvg_-40C

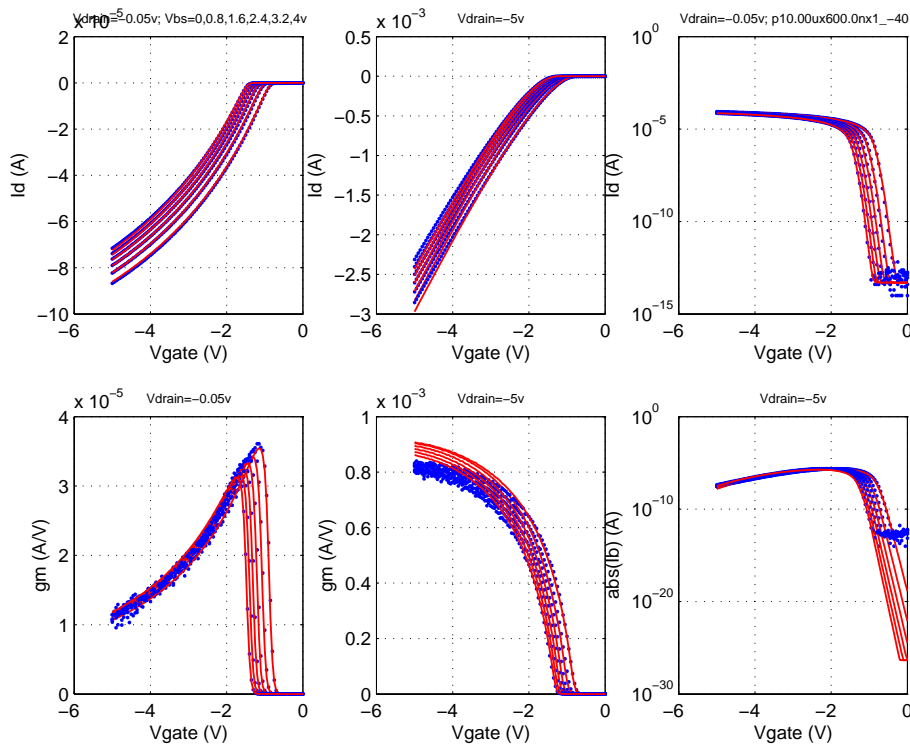


FIGURE 2.133 5p0_PFET_10x0p6_idvd_125C

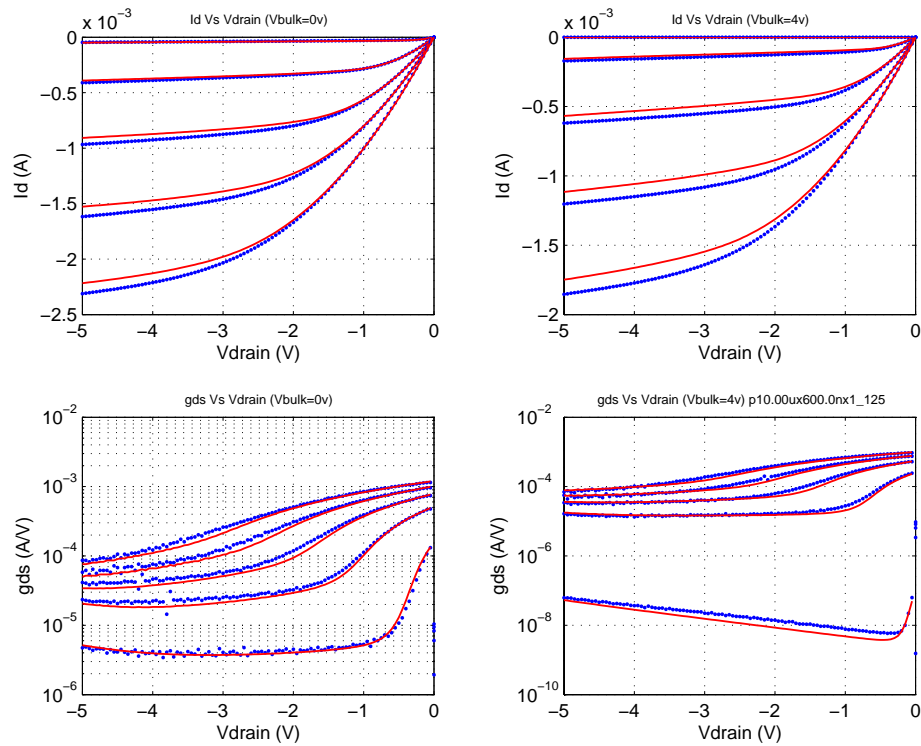


FIGURE 2.134 5p0_PFET_10x0p6_idvg_125C

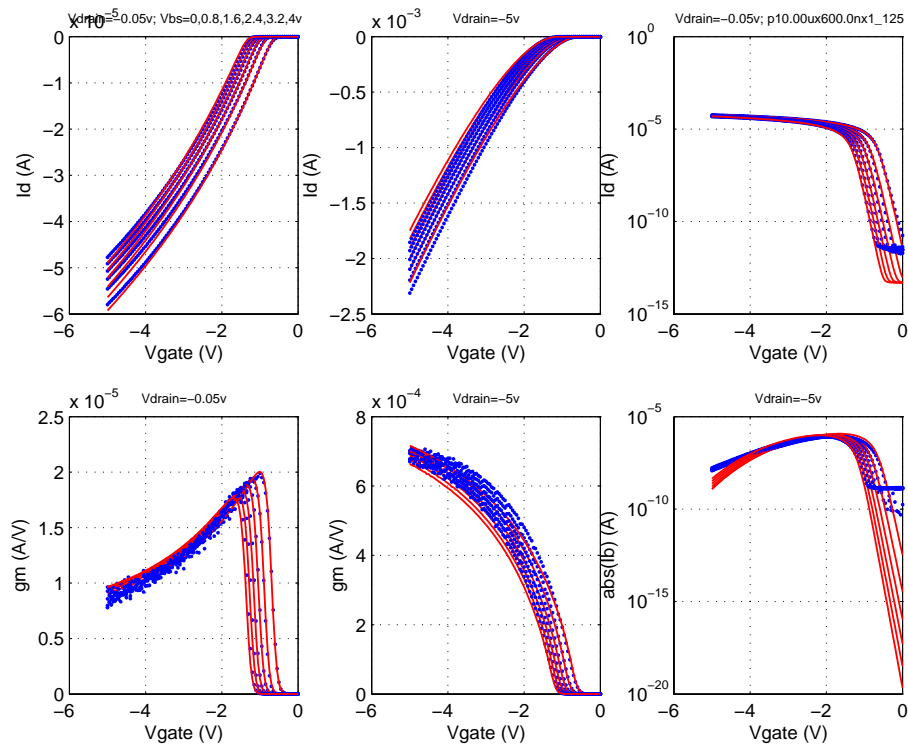


FIGURE 2.135 5p0_native_NFET_vtVsL_25C

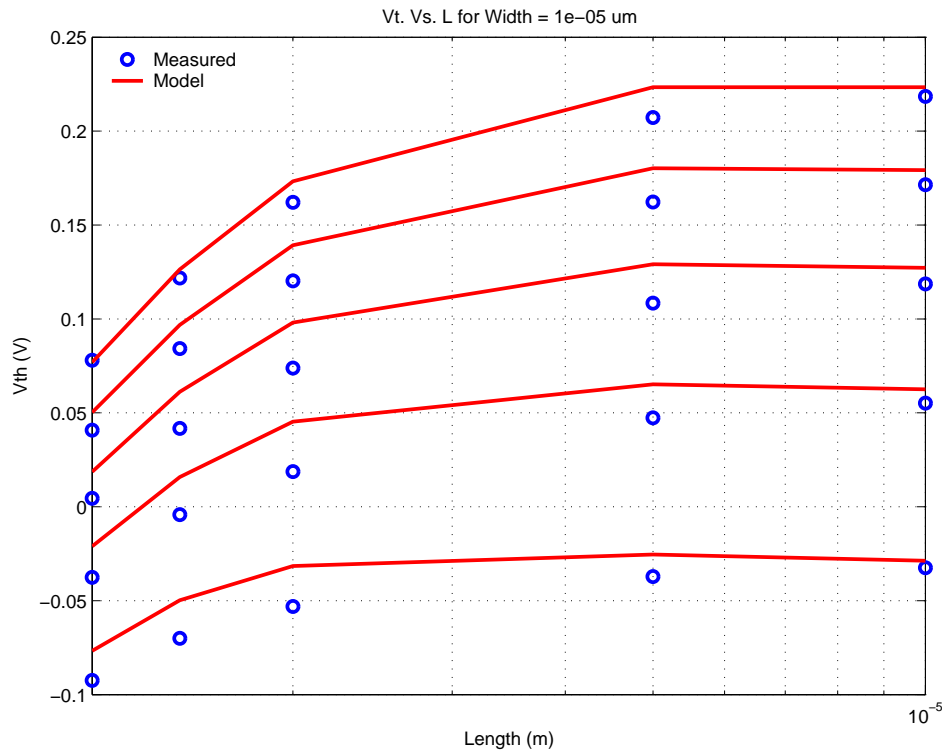


FIGURE 2.136 5p0_native_NFET_vtVsW_25C

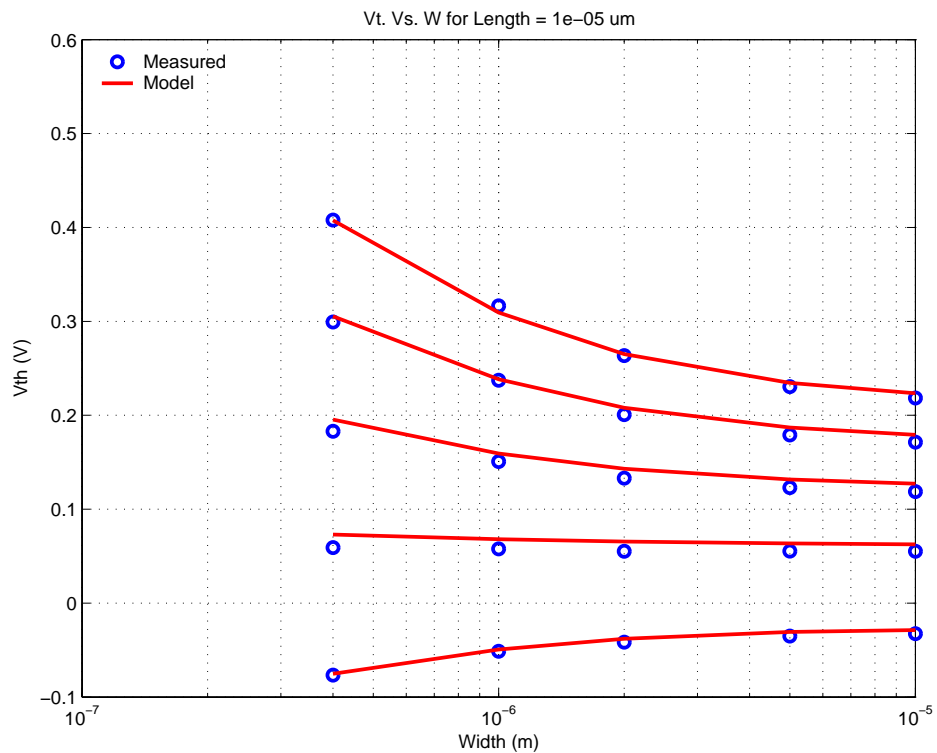


FIGURE 2.137 5p0_native_NFET_10x10_idvd_25C

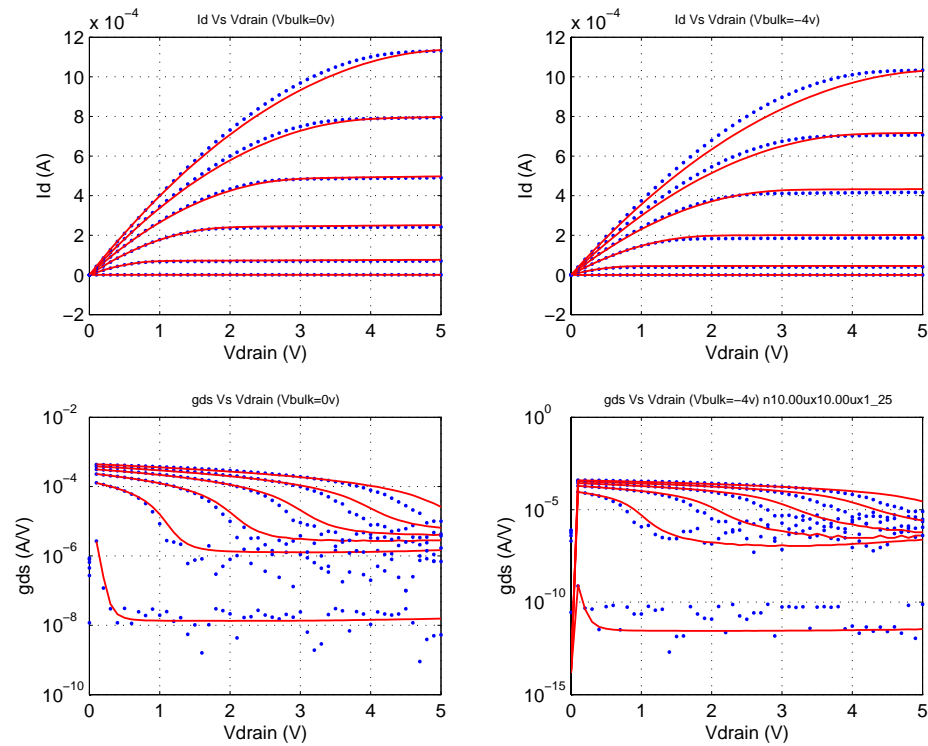


FIGURE 2.138 5p0_native_NFET_10x10_idvg_25C

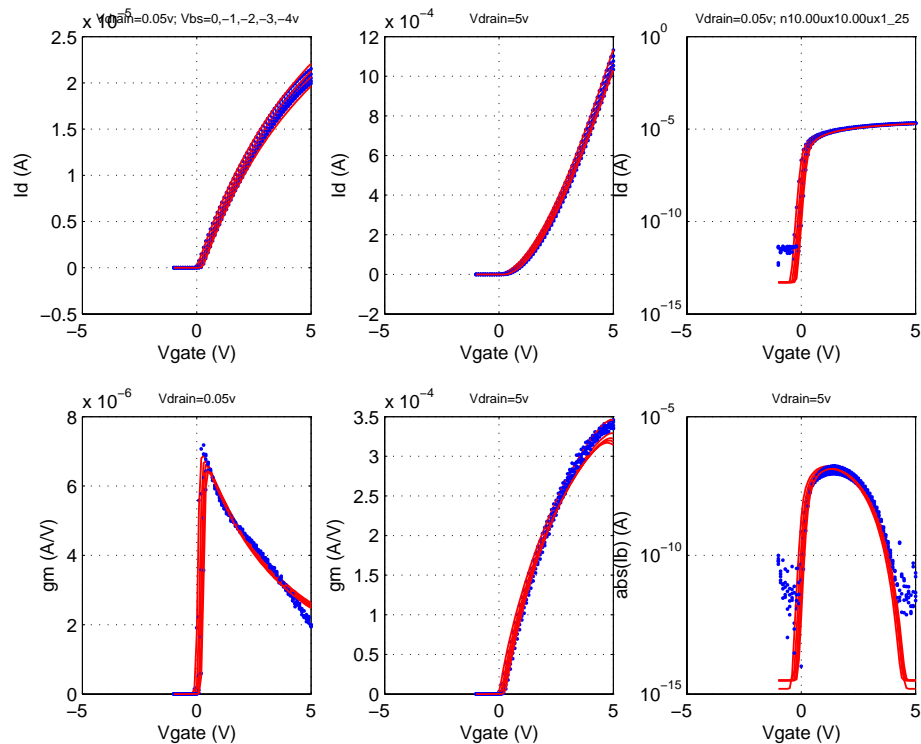


FIGURE 2.139 5p0_native_NFET_10x1p2_idvd_25C

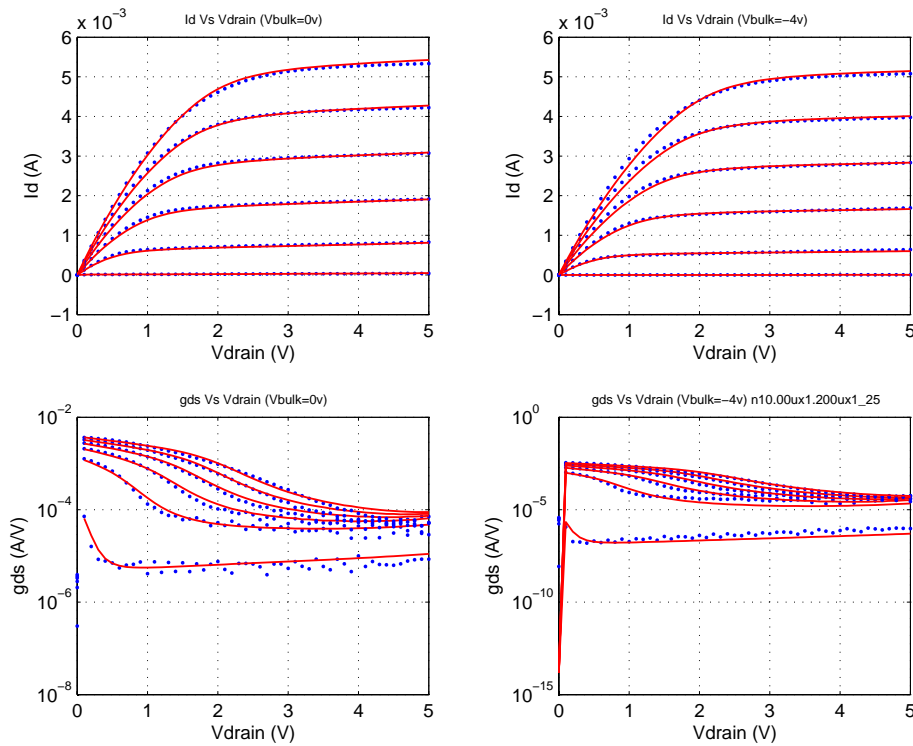


FIGURE 2.140 5p0_native_NFET_10x1p2_idvg_25C

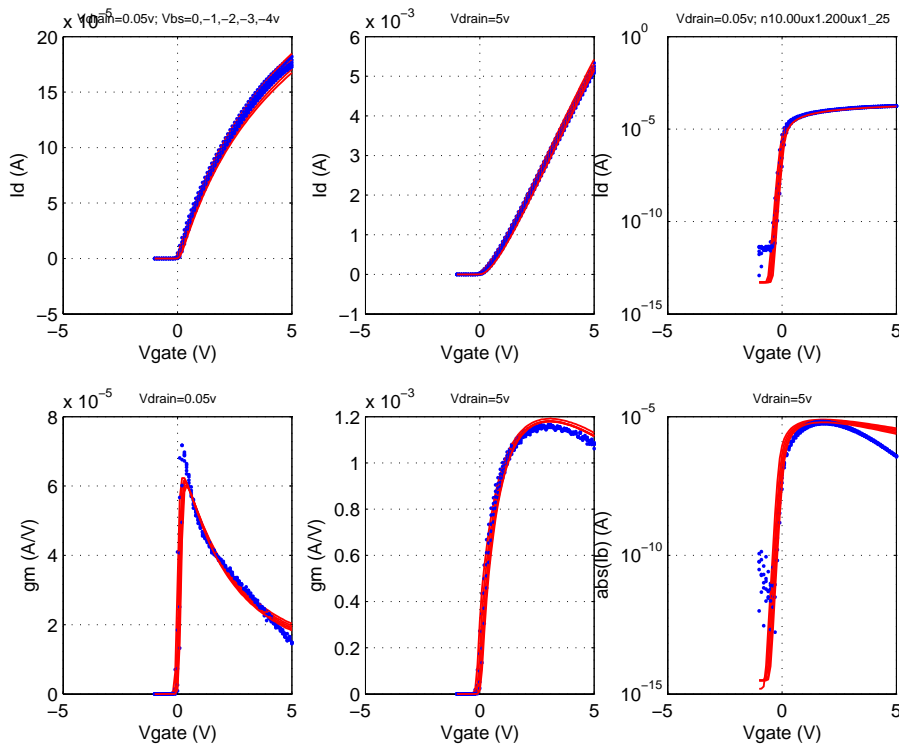


FIGURE 2.141 5p0_native_NFET_0p4x10_idvd_25C

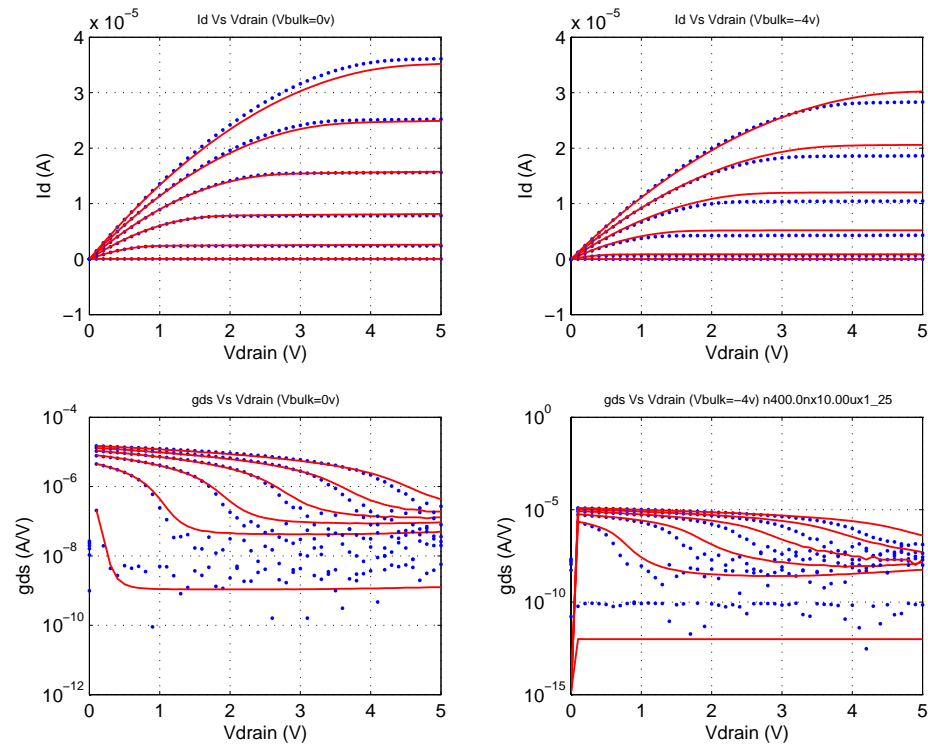


FIGURE 2.142 5p0_native_NFET_0p4x10_idvg_25C

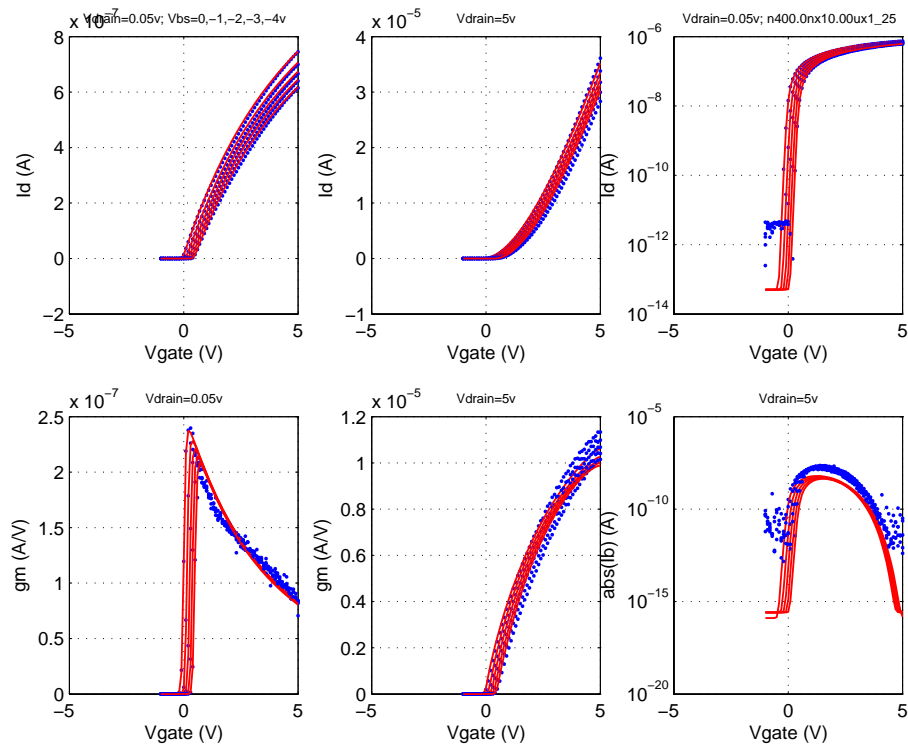


FIGURE 2.143 5p0_native_NFET_0p4x1_idvd_25C

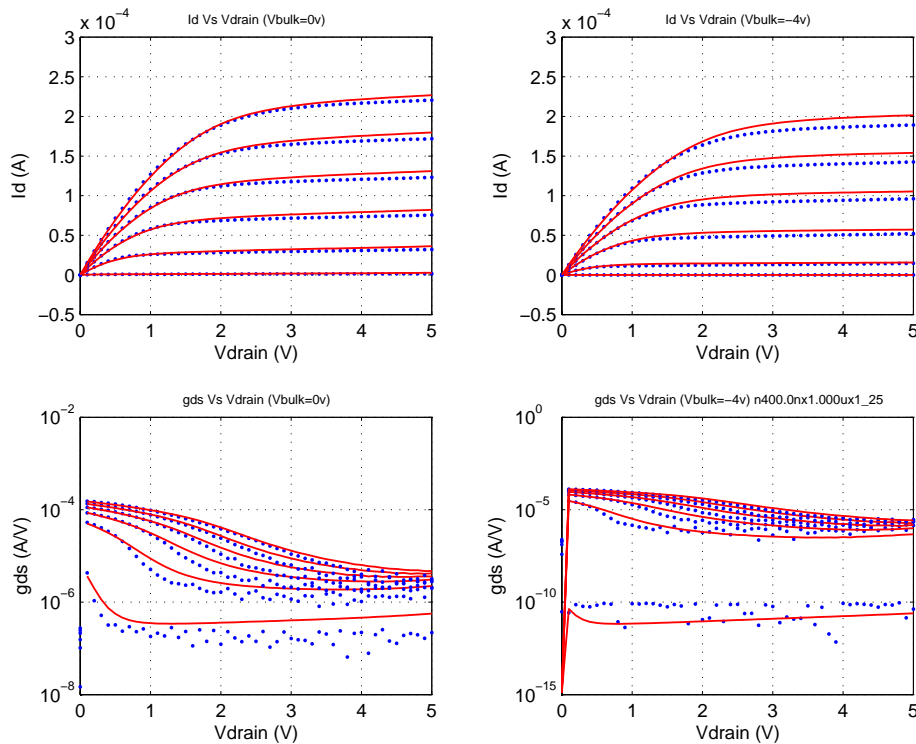


FIGURE 2.144 5p0_native_NFET_0p4x1_idvg_25C

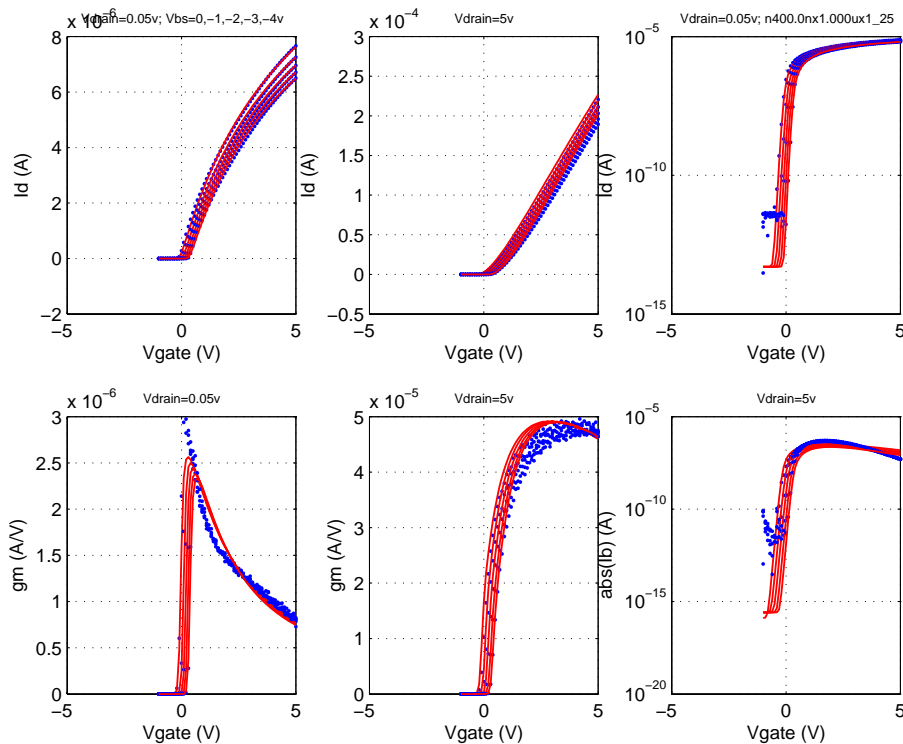


FIGURE 2.145 5p0_native_NFET_10x2_idvd_25C

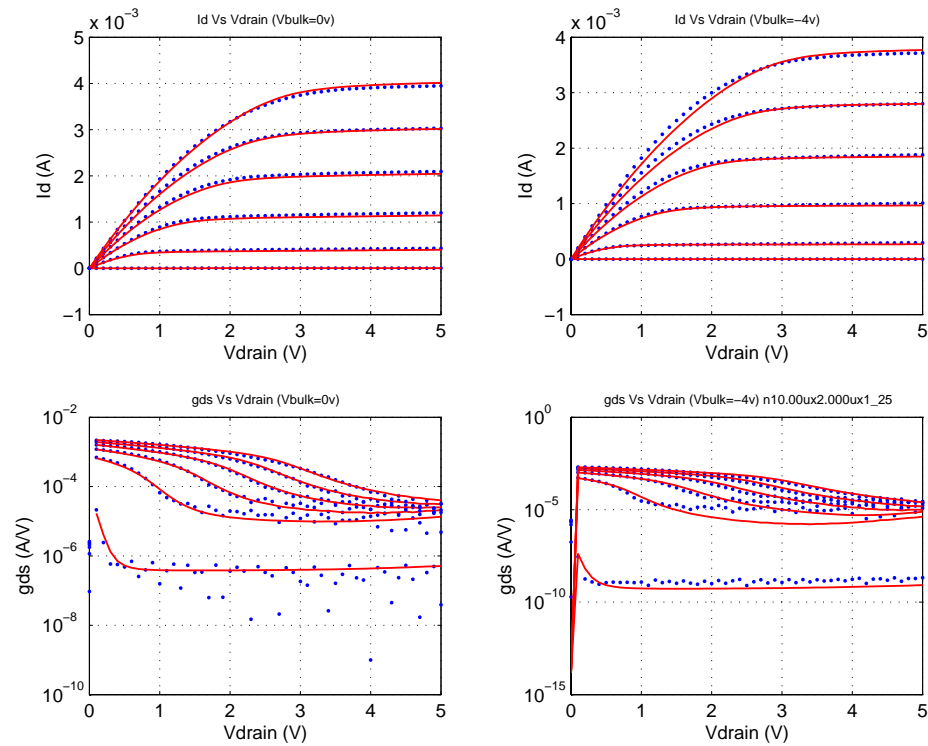
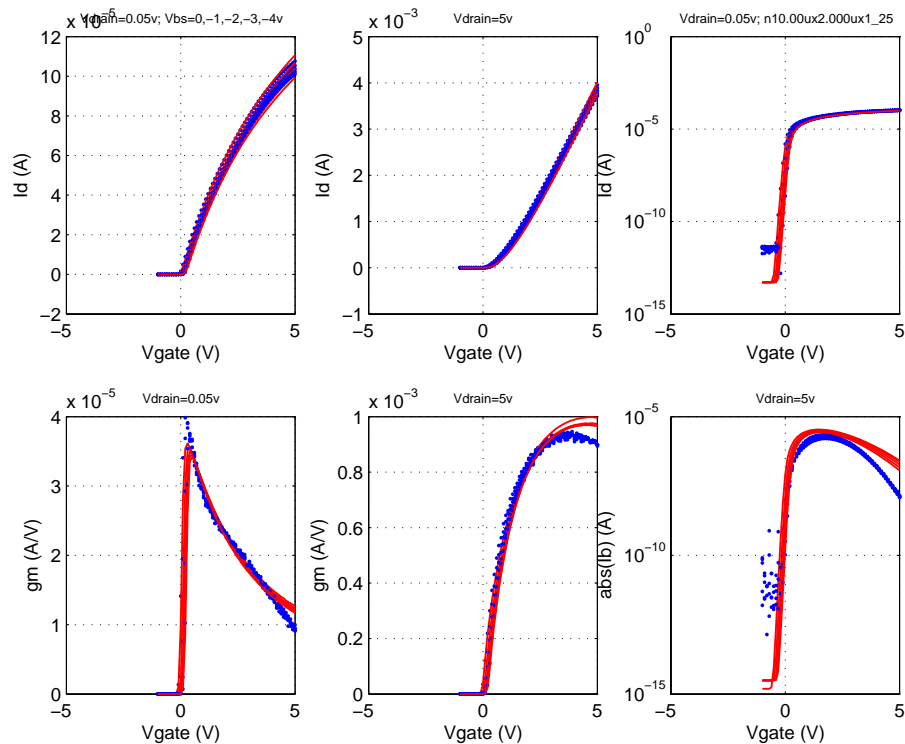


FIGURE 2.146 5p0_native_NFET_10x2_idvg_25C



2.5 Statistical and Corner Models

Statistical models are generated by specifying 1- σ variations of appropriate model parameters. These variances are generated via a physically based and robust mathematical approach called the “Backward Propagation of Variance (BPV). [3]” The BPV approach is defined by Eq. 3:

$$\sigma_{e_i}^2 = \sum_k \left(\frac{\partial e_i}{\partial p_k} \right)^2 \cdot \sigma_{p_k}^2 \quad (\text{EQ 3})$$

where σ_{e_i} is the standard deviation of the i^{th} Electrical Specification (E-spec), $\frac{\partial e_i}{\partial p_k}$ is the partial derivative of the E-spec w.r.t. to the k^{th} model parameter, and σ_{p_k} is the standard deviation of the model parameter that being solved for. The E-specs for this technology are extracted from Process Control Monitoring (PCM) data and are defined in Jazz document NPB-PS-0173 titled “Electrical Parameters of the CA18 Processes.” This process is termed as the backward propagation of variance, as it takes measurements in variances (E-specs) of important electrical quantities and then calculates the variances in the model process parameters that are necessary to fit the spread in the measured data, rather than taking the measured variations in the model process parameters and forward propagating them to predict the variations in σ_e . Conventional statistical modeling approaches are typically forward propagated, and do not guarantee consistency between model and E-spec corners and miss the real goal of statistical modeling.

The set of partial derivatives on the RHS of Eq. 3 represent the sensitivity matrix of the extracted model, and are directly evaluated using a circuit simulator such as Spectre. These derivatives can depend on the Δp_k values chosen to approximate δp_k . A global optimizer is used to minimize any error associated with the sensitivity matrix evaluation. The maximum deviation between the E-spec. and simulator prediction for the SLOW, NOM, and FAST corners is 1/2- σ , where 6- σ is the total range from the minimum to the maximum value of the E-spec. Typically, this corresponds to < 2% deviation of the model prediction w.r.t the E-spec. Statistical model predictions for the various flavors of FETs in this technology are shown in Table 2.19 through Table 2.26.

The statistical model allows un-correlated variations in oxide thickness, flat-band voltage (from oxide-charge and gate work-function), and channel doping as per Eq. 4 and Eq. 5 to impact threshold voltage (BSIM3v3 parameter VTH0). Additionally, the channel doping and oxide thickness are used for the body effect (BSIM3v3 parameter K1) evaluation as per Eq. 6 and Eq. 7.

$$VTH0 = VFB + 2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i} + \frac{T_{ox}}{E_{ox}} \sqrt{2q \cdot E_{si} \cdot N_{ch} \cdot 2 \frac{kT}{q} \ln \frac{N_{ch}}{n_i}} \quad (\text{EQ 4})$$

$$\Delta VTH0 = \Delta VFB + \frac{\partial}{\partial N_{ch}} VTH0 \cdot \Delta N_{ch} + \frac{\partial}{\partial T_{ox}} VTH0 \cdot \Delta T_{ox} \quad (\text{EQ 5})$$

$$K1 = \frac{T_{ox}}{E_{ox}} \cdot \sqrt{2q \cdot E_{si} \cdot N_{ch}} \quad (\text{EQ 6})$$

$$\Delta K1 = \frac{\partial}{\partial N_{ch}} K1 \cdot \Delta N_{ch} + \frac{\partial}{\partial T_{ox}} K1 \cdot \Delta T_{ox} \quad (\text{EQ 7})$$

The geometry dependence of the threshold voltage and body constant is captured by specifying un-correlated variations in the relevant BSIM3v3 parameters such as K3 (narrow width Vth), K3B (body effect in narrow device), DVT0 (short channel Vth), and DVT2 (body effect of short channel device).

The global variation in active dimensions (active_cd) is propagated into the W_{eff} calculation of FETs to be consistent with other active or passive devices in the circuit. Similarly, global process variations in the gate poly length (poly_cd) are propagated into L_{eff} calculations. Additionally, the L_{eff} depends on the variation in the lateral spread of the LDD (Lightly Doped Drain) under the gate. Oxide thickness and L_{eff} variations are physically propagated into overlap capacitance variation.

The extraction of statistical variations of model parameters is preceded by “Centering” process of the “measured” case. This is described in Section 2.5.1.

2.5.1 Centering

The measured case was “centered” to the E-specs of threshold voltage, body constant, and saturation currents for the devices listed in the E-specs. This is an important part of the model release methodology and generates a nominal model that is aligned to the nominal E-specs of the technology.

The centering is performed using the statistical modeling approach defined in Section 2.5 by modifying Eq. 3 as:

$$\Delta e_i = \sum_k \frac{\partial e_i}{\partial p_k} \cdot \Delta p_k \quad (\text{EQ 8})$$

where Δe_i is the difference between the measured case prediction of the E-spec and nominal E-spec, $\frac{\partial e_i}{\partial p_k}$ is the partial derivative of the e-spec w.r.t the relevant model parameter, and Δp_k is the shift in the model parameter needed to center the measured case to the E-spec. Typical shift in model parameters required to center the measured case are less than 1%, and represent a statistically valid and unique set of shifts in model parameters that are perfectly aligned with the “nominal” process targets of the Fab. It should be noted that these E-specs are targets that the fab continually tries to match, with the results being regularly reported as CPK charts.

2.5.2 Corner model generation

Corner models are generated via an approach identical to the centering model methodology described in Section 2.5.1 on page 102. The E-spec corners are used to calculate the E-spec delta on the LHS of Eq. 8, which is then solved for the required model parameter shift on the RHS. The maximum allowable deviation between the E-spec. and the model prediction is $1/2\text{-}\sigma$, where $6\text{-}\sigma$ is the total range from the minimum to the

maximum value of the E-spec. Typically, this corresponds to < 2% deviation of the model prediction w.r.t the E-spec.

The variation in junction area capacitance C_J is +/-5% in corner cases. The junction sidewall capacitance C_{JSW} and gate edge sidewall capacitance C_{JSWG} are skewed for the corner cases by +/- 10% for both FET and diode models.

Conventional corner modeling approaches are typically forward propagated, where measured model parameter deltas (Δp_k in Eq. 8) are used to predict spreads in key electrical properties of the FETs and do not guarantee consistency between corner models and E-spec corners. The extracted corner model parameters for the various fets thin and thick oxide FETs are shown from Table 2.14 to Table 2.18, respectively.

TABLE 2.14 Corner model parameters for 1.8V thin-oxide FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
tox (m)	Oxide thickness	3.95e-09	3.85e-09	3.75e-09	3.86e-09	3.76e-09	3.66e-09
vth0 (V)	Long channel threshold	4.22e-01	3.63e-01	3.03e-01	-4.96e-01	-4.18e-01	-3.40e-01
cgs1 (F/m)	High Vgs G-S ovlp.	2.65e-10	2.99e-10	3.29e-10	1.41e-10	1.50e-10	1.59e-10
cgd1 (F/m)	High Vgs D-S ovlp.	2.65e-10	2.99e-10	3.29e-10	1.41e-10	1.50e-10	1.59e-10
cgso (F/m)	G-S ovlp. cap.	1.08e-10	1.22e-10	1.34e-10	2.07e-10	2.20e-10	2.33e-10
cgdo (F/m)	G-D ovlp. cap.	1.08e-10	1.22e-10	1.34e-10	2.07e-10	2.20e-10	2.33e-10
nlx (m)	Short channel V_t	1.92e-07	2.17e-07	2.25e-07	3.12e-08	3.32e-08	3.71e-08
lint (m)	ΔL	1.33e-08	1.47e-08	1.57e-08	3.73e-08	3.86e-08	3.97e-08
k1 ($V^{1/2}$)	Body constant	4.66e-01	3.86e-01	3.30e-01	5.99e-01	5.31e-01	4.62e-01
k3	Narrow width co-efficient	-1.09e+01	-1.40e+01	-1.74e+01	-1.87e+00	-3.28e+00	-4.34e+00
k3b (1/V)	Body effect of K3	1.75e+00	2.92e+00	4.96e+00	1.11e+00	2.43e+00	3.91e+00
cjsw (F/m)	Sidewall junc. cap.	2.21e-10	2.01e-10	1.80e-10	6.60e-11	6.00e-11	5.40e-11
cjswg (F/m)	Sidewall under gate junc. cap.	6.17e-10	5.61e-10	5.05e-10	5.28e-10	4.80e-10	4.32e-10
cj (F/m ²)	Bottom junc. cap	1.11e-03	1.06e-03	1.01e-03	9.00e-04	8.57e-04	8.14e-04
u0 (cm ² /Vs)	Low field mobility	2.84e+02	2.98e+02	3.10e+02	8.82e+01	9.18e+01	9.49e+01
rdsw ($\Omega\text{-}\mu\text{m}$)	Drain/source series resistance	4.00e+01	3.80e+01	3.61e+01	1.14e+03	1.09e+03	1.04e+03
wint (m)	ΔW	5.38e-08	3.73e-08	2.52e-08	3.20e-08	1.32e-08	-1.64e-09
dvt2 (1/V)	Body effect in short channel	2.17e-02	-8.50e-02	-3.30e-01	-1.66e-01	-3.00e-01	-5.24e-01

TABLE 2.15 Corner model parameters for 3.3V thick-oxide FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
tox (m)	Oxide thickness	6.89e-09	6.71e-09	6.53e-09	6.89e-09	6.71e-09	6.53e-09
vth0 (V)	Long channel threshold	6.84e-01	6.06e-01	5.28e-01	-8.95e-01	-7.99e-01	-7.00e-01
cgs1 (F/m)	High Vgs G-S ovlp.	1.65e-10	2.10e-10	2.93e-10	1.05e-10	1.12e-10	1.16e-10
cgd1 (F/m)	High Vgs D-S ovlp.	1.65e-10	2.10e-10	2.93e-10	1.05e-10	1.12e-10	1.16e-10
cgso (F/m)	G-S ovlp. cap.	8.27e-11	1.05e-10	1.47e-10	2.38e-10	2.55e-10	2.64e-10
cgdo (F/m)	G-D ovlp. cap.	8.27e-11	1.05e-10	1.47e-10	2.38e-10	2.55e-10	2.64e-10
lint (m)	ΔL	5.36e-08	6.62e-08	8.99e-08	6.40e-08	6.67e-08	6.73e-08
k1 ($V^{1/2}$)	Body constant	5.84e-01	5.05e-01	4.25e-01	1.05e+00	9.37e-01	8.24e-01

TABLE 2.15 Corner model parameters for 3.3V thick-oxide FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
cjsw (F/m)	Sidewall junc. cap.	1.89e-10	1.72e-10	1.55e-10	1.14e-10	1.03e-10	9.31e-11
cjswg (F/m)	Sidewall under gate junc. cap.	3.81e-10	3.47e-10	3.12e-10	3.51e-10	3.19e-10	2.87e-10
cj (F/m ²)	Bottom junc. cap	9.02e-04	8.59e-04	8.16e-04	7.60e-04	7.24e-04	6.88e-04
u0 (cm ² /Vs)	Low field mobility	3.64e+02	3.84e+02	4.01e+02	9.27e+01	9.94e+01	1.08e+02
rdsw (Ω - μ m)	Drain/source series resistance	6.53e+02	6.22e+02	5.91e+02	2.19e+03	2.08e+03	1.98e+03
dvt0	Short channel Vt	6.81e+00	5.90e+00	4.14e+00	2.71e+00	2.44e+00	2.57e+00
wint (m)	ΔW	5.60e-08	3.11e-08	2.34e-08	7.92e-09	-2.44e-08	-8.02e-08
dvt2 (1/V)	Body effect in short channel	9.54e-02	7.00e-02	4.04e-02	-6.84e-02	-8.25e-02	-7.46e-02

TABLE 2.16 Corner model parameters for 3.3V thick-oxide native FETs

BSIM3v3 Parameter	Description	NFET		
		SLOW	NOM	FAST
tox (m)	Oxide thickness	6.28e-09	6.10e-09	5.92e-09
vth0 (V)	Long channel threshold	-1.19e-02	-1.08e-01	-2.11e-01
cgs1 (F/m)	High Vgs G-S ovlp.	1.63e-10	2.82e-10	3.87e-10
cgd1 (F/m)	High Vgs D-S ovlp.	1.63e-10	2.82e-10	3.87e-10
cgso (F/m)	G-S ovlp. cap.	6.88e-11	1.19e-10	1.63e-10
cgdo (F/m)	G-D ovlp. cap.	6.88e-11	1.19e-10	1.63e-10
lint (m)	ΔL	5.63e-08	9.43e-08	1.26e-07
k1 (V ^{1/2})	Body constant	1.86e-01	1.71e-01	1.54e-01
cjsw (F/m)	Sidewall junc. cap.	1.41e-10	1.28e-10	1.16e-10
cjswg (F/m)	Sidewall under gate junc. cap.	7.70e-11	7.00e-11	6.30e-11
cj (F/m ²)	Bottom junc. cap	2.97e-04	2.82e-04	2.68e-04
u0 (cm ² /Vs)	Low field mobility	3.77e+02	4.07e+02	4.33e+02
rdsw (Ω - μ m)	Drain/source series resistance	2.97e+02	2.83e+02	2.69e+02
wint (m)	ΔW	3.47e-08	1.66e-08	-6.69e-10

TABLE 2.17 Corner model parameters for 5V thick-oxide FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
tox (m)	Oxide thickness	1.42E-08	1.34E-08	1.26E-08	1.45E-08	1.37E-08	1.29E-08
vth0 (V)	Long channel threshold	7.28E-01	6.31E-01	5.33E-01	-9.09E-01	-8.12E-01	-7.15E-01
cgs1 (F/m)	High Vgs G-S ovlp.	4.00E-10	4.00E-10	4.00E-10	1.52E-10	1.52E-10	1.52E-10
cgd1 (F/m)	High Vgs D-S ovlp.	4.00E-10	4.00E-10	4.00E-10	1.52E-10	1.52E-10	1.52E-10
cgso (F/m)	G-S ovlp. cap.	4.93E-11	4.93E-11	4.93E-11	4.50E-11	4.50E-11	4.50E-11
cgdo (F/m)	G-D ovlp. cap.	4.93E-11	4.93E-11	4.93E-11	4.50E-11	4.50E-11	4.50E-11
nlx (m)	Short channel Vt	8.87E-08	8.87E-08	8.87E-08	2.32E-10	2.32E-10	2.32E-10
lint (m)	ΔL	3.27E-08	7.13E-08	1.04E-07	7.37E-08	8.75E-08	9.98E-08
k1 (V ^{1/2})	Body constant	8.61E-01	7.52E-01	6.44E-01	7.50E-01	6.40E-01	5.30E-01
k3	Narrow width co-efficient	-2.35	-2.73	-2.96	-1.14	-1.23	-1.34
k3b (1/V)	Body effect of K3	5.37E-01	5.74E-01	6.66	1.55	1.72	1.94

TABLE 2.17 Corner model parameters for 5V thick-oxide FETs

BSIM3v3 Parameter	Description	NFET			PFET		
		SLOW	NOM	FAST	SLOW	NOM	FAST
cjsw (F/m)	Sidewall junc. cap.	1.29E-10	1.18E-10	1.06E-10	1.21E-10	1.10E-10	9.86E-11
cjswg (F/m)	Sidewall under gate junc. cap.	3.03E-10	2.75E-10	2.48E-10	1.53E-10	1.39E-10	1.25E-10
cj (F/m ²)	Bottom junc. cap	8.62E-04	7.83E-04	7.05E-04	7.75E-04	7.05E-04	6.34E-04
u0 (cm ² /Vs)	Low field mobility	3.79E+02	3.98E+02	4.12E+02	1.20E+02	1.31E+02	1.41E+02
rdsw (Ω - μ m)	Drain/source series resistance	4.42E+02	4.42E+02	4.42E+02	1.89E+03	1.89E+03	1.89E+03
wint (m)	ΔW	6.46E-08	3.81E-08	2.54E-08	2.12E-08	1.48E-09	-2.11E-08
dvt2 (1/V)	Body effect in short channel	-1.27E-02	-4.42E-02	-1.04E-01	4.32E-02	-2.46E-02	-9.27E-02

TABLE 2.18 Corner model parameters for 5V thick-oxide Native NFETs

BSIM3v3 Parameter	Description	NFET		
		SLOW	NOM	FAST
tox (m)	Oxide thickness	1.42e-08	1.34e-08	1.26e-08
vth0 (V)	Long channel threshold	6.61e-02	-2.34e-02	-1.13e-01
cgs1 (F/m)	High Vgs G-S ovlp.	1.97e-10	4.00e-10	5.64e-10
cgd1 (F/m)	High Vgs D-S ovlp.	1.97e-10	4.00e-10	5.64e-10
cgso (F/m)	G-S ovlp. cap.	2.43e-11	4.93e-11	6.95e-11
cgdo (F/m)	G-D ovlp. cap.	2.43e-11	4.93e-11	6.95e-11
lint (m)	ΔL	5.17e-08	1.25e-07	1.79e-07
k1 (V ^{1/2})	Body constant	3.04e+02	2.28e+02	1.57e+02
cjsw (F/m)	Sidewall junc. cap.	1.62e-10	1.29e-10	9.42e-11
cjswg (F/m)	Sidewall under gate junc. cap.	8.83e-11	7.00e-11	5.13e-11
cj (F/m ²)	Bottom junc. cap	3.56e-04	2.82e-04	2.07e-04
u0 (cm ² /Vs)	Low field mobility	5.68e+02	5.70e+02	5.73e+02
rdsw (Ω - μ m)	Drain/source series resistance	9.17e+02	6.20e+02	4.18e+02
wint (m)	ΔW	4.64e-08	3.00e-08	1.35e-08

2.5.3 Statistical model usage guidelines

In contrast to the corner models, the statistical models allow “multi-directional” variability in model parameters. For a sufficient number of monte-carlo runs these simulation results converge to the measured (E-spec.) 3- σ variation in key MOSFET device properties (such as I_{dsat} , V_{th}) and in most cases represent a more accurate prediction (over corner models) of expected impact of process variations on circuit-level figures of merit. The statistical model is currently supported only in Spectre, which provides the needed framework for statistical modeling. The “process-only” variation option should be selected when setting up statistical model run. This represents the expected functional yield (non-defect related) that can be expected for the particular design split. The “numruns” (number of runs) in monte-carlo analysis is an important parameter that controls the accuracy of the statistical model prediction. For single transistor level simulations of V_{th} , I_{dsat} , and body constant a value of a 100 runs gives reasonably stable results. The user should check the mean value of the circuit-level figure of merit that is being simulated and compare it to nominal simulation and decide whether to increase or decrease this value.

2.5.4 Statistical and corner model tables

TABLE 2.19 1.8V thin-oxide NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
narrow	0.22x10	$kb^2 (V^{0.5})$	0.370	0.372	0.368	0.280	0.284	0.283	0.190	0.205	0.199
narrow	0.22x10	$vt^1 (V)$	0.300	0.302	0.305	0.230	0.230	0.231	0.160	0.157	0.156
large	10x10	$\beta^3 (\mu\text{A}/V^2)$	126.00	133.90	134.2	140.00	147.00	146.8	156.00	159.90	159.5
large	10x10	$kb^2 (V^{0.5})$	0.410	0.410	0.396	0.350	0.340	0.342	0.290	0.290	0.287
large	10x10	$vt^1 (V)$	0.420	0.420	0.417	0.360	0.360	0.362	0.300	0.300	0.307
small	0.22x0.18	$idsat^5 (mA)$	0.095	0.096	0.095	0.140	0.141	0.139	0.185	0.186	0.183
small	0.22x0.18	$kb^2 (V^{0.5})$	0.380	0.391	0.389	0.280	0.281	0.282	0.180	0.165	0.176
small	0.22x0.18	$vt^1 (V)$	0.530	0.535	0.533	0.430	0.428	0.433	0.330	0.326	0.333
short	10x0.18	$idsat^1 (mA)$	5.100	5.139	5.173	6.000	6.001	5.975	6.900	6.914	6.778
short	10x0.18	$kb^2 (V^{0.5})$	0.400	0.400	0.402	0.310	0.315	0.318	0.220	0.233	0.233
short	10x0.18	$vt^1 (V)$	0.600	0.596	0.609	0.520	0.520	0.523	0.440	0.439	0.437

TABLE 2.20 1.8V thin-oxide PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
narrow	0.22x10	$kb^2 (V^{0.5})$	0.580	0.569	0.564	0.480	0.478	0.476	0.380	0.389	0.388
narrow	0.22x10	$vt^1 (V)$	-0.460	-0.469	-0.461	-0.370	-0.370	-0.369	-0.280	-0.281	-0.277
large	10x10	$\beta^4 (\mu\text{A}/V^2)$	29.000	29.050	29.10	32.000	31.990	32.10	35.00	35.050	35.10
large	10x10	$kb^2 (V^{0.5})$	0.590	0.590	0.589	0.530	0.530	0.529	0.470	0.470	0.469
large	10x10	$vt^1 (V)$	-0.490	-0.490	-0.483	-0.410	-0.410	-0.409	-0.330	-0.330	-0.335
small	0.22x0.18	$idsat^6 (mA)$	-0.040	-0.040	-0.040	-0.060	-0.060	-0.060	-0.080	-0.082	-0.081
small	0.22x0.18	$kb^2 (V^{0.5})$	0.530	0.543	0.540	0.430	0.433	0.431	0.330	0.318	0.322
small	0.22x0.18	$vt^1 (V)$	-0.490	-0.495	-0.495	-0.390	-0.394	-0.392	-0.290	-0.305	-0.289
short	10x0.18	$idsat^1 (mA)$	-2.100	-2.117	-2.100	-2.550	-2.550	-2.560	-3.000	-3.018	-3.020
short	10x0.18	$kb^2 (V^{0.5})$	0.600	0.590	0.602	0.510	0.514	0.513	0.420	0.429	0.424
short	10x0.18	$vt^1 (V)$	-0.520	-0.524	-0.523	-0.440	-0.440	-0.439	-0.360	-0.359	-0.355

TABLE 2.21 3.3V thick-oxide NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10	$\beta^2 (\mu\text{A}/V^2)$	77.00	86.03	84.90	86.00	95.02	95.20	95.0	104.00	105.5
large	10x10	$kb^2 (V^{0.5})$	0.670	0.670	0.667	0.600	0.600	0.599	0.530	0.530	0.531
large	10x10	$vt^2 (V)$	0.690	0.690	0.677	0.610	0.610	0.609	0.530	0.530	0.541
small	0.6x0.36	$idsat^2 (mA)$	0.285	0.289	0.288	0.360	0.362	0.363	0.435	0.437	0.438
short	10x0.36	$idsat^1 (mA)$	5.000	5.014	4.930	6.000	5.876	5.900	7.000	7.018	6.880
short	10x0.36	$kb^2 (V^{0.5})$	0.620	0.620	0.618	0.520	0.520	0.519	0.420	0.423	0.420
short	10x0.36	$vt^1 (V)$	0.720	0.719	0.736	0.620	0.617	0.620	0.520	0.521	0.504

TABLE 2.22 3.3V thick-oxide PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10	β^2 (μA/V ²)	16.00	17.45	17.00	19.00	19.72	19.90	22.00	22.67	22.80
large	10x10	k_b^2 (V ^{0.5})	1.020	1.020	1.020	0.920	0.920	0.917	0.820	0.820	0.817
large	10x10	v_t^2 (V)	-0.900	-0.900	-0.902	-0.800	-0.801	-0.799	-0.700	-0.700	-0.696
small	0.6x0.3	i_{dsat}^2 (mA)	-0.130	-0.133	-0.122	-0.180	-0.173	-0.173	-0.230	-0.235	-0.224
short	10x0.3	i_{dsat}^1 (mA)	-2.400	-2.514	-2.500	-2.9	-2.987	-3.000	-3.400	-3.512	-3.500
short	10x0.3	k_b^2 (V ^{0.5})	0.940	0.941	0.939	0.840	0.841	0.837	0.740	0.740	0.735
short	10x0.3	v_t^1 (V)	-0.840	-0.840	-0.846	-0.740	-0.743	-0.741	-0.640	-0.640	-0.636

TABLE 2.23 3.3V Thick-oxide native NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
short	10x1	v_t^2 (V)	-0.010	-0.010	-0.008	-0.110	-0.106	-0.104	-0.210	-0.210	-0.200
short	10x1	i_{dsat}^2 (mA)	4.800	4.827	4.910	5.700	5.703	5.700	6.600	6.623	6.490

TABLE 2.24 5V Thick-oxide NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10 ¹	β^2 (μA/V ²)	47	47.02	47.1	53	53.08	53.2	59	59	59.4
large	10x10 ¹	k_b^2 (V ^{0.5})	0.77	0.77	0.766	0.67	0.669	0.668	0.57	0.57	0.57
large	10x10 ¹	v_t^2 (V)	0.74	0.74	0.735	0.64	0.64	0.64	0.54	0.54	0.545
small	0.6x0.7	i_{dsat}^2 (mA)	0.25	0.251	0.248	0.33	0.333	0.334	0.41	0.413	0.42
short	10x0.6	i_{dsat}^1 (mA)	4.4	4.417	4.47	5.2	5.199	5.21	6	6.014	5.95
short	10x0.6	k_b^2 (V ^{0.5})	0.64	0.641	0.65	0.52	0.519	0.515	0.4	0.402	0.38
short	10x0.6	v_t^1 (V)	0.75	0.755	0.756	0.65	0.652	0.649	0.55	0.555	0.542

TABLE 2.25 5V Thick-oxide PFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10	β^2 (μA/V ²)	11	11.05	11	13	13	13	15	15.06	15
large	10x10	k_b^2 (V ^{0.5})	0.64	0.64	0.641	0.54	0.54	0.54	0.44	0.44	0.439
large	10x10	v_t^2 (V)	-0.91	-0.91	-0.912	-0.81	-0.81	-0.811	-0.71	-0.71	-0.711
small	0.6x0.6	i_{dsat}^2 (mA)	-0.125	-0.127	-0.122	-0.17	-0.168	-0.168	-0.215	-0.218	-0.215
short	10x0.6	i_{dsat}^1 (mA)	-2.1	-2.118	-2.08	-2.6	-2.601	-2.6	-3.1	-3.117	-3.12
short	10x0.6	k_b^2 (V ^{0.5})	0.59	0.591	0.585	0.44	0.44	0.437	0.29	0.29	0.289
short	10x0.6	v_t^1 (V)	-0.87	-0.869	-0.874	-0.77	-0.77	-0.77	-0.67	-0.67	-0.666

TABLE 2.26 5V Thick-oxide native NFET corner and statistical model predictions

Device	WxL(μm)	Espec Name (unit)	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
large	10x10	β^2 (μA/V ²)	62.000	62.550	62.83	69.00	69.10	69.26	76.00	76.630	75.681
large	10x10	k_b^2 (V ^{0.5})	0.255	0.258	0.252	0.185	0.186	0.185	0.115	0.118	0.118
large	10x10	v_t^2 (V)	0.061	0.061	0.069	-0.029	-0.029	-0.031	-0.119	-0.119	-0.131
small	0.4x1	i_{dsat}^2 (mA)	0.150	0.148	0.144	0.200	0.198	0.197	0.250	0.257	0.250
short	10x1.2	i_{dsat}^1 (mA)	4.550	4.616	4.544	5.400	5.426	5.429	6.250	6.296	6.314
short	10x1.2	k_b^2 (V ^{0.5})	0.190	0.193	0.180	0.110	0.114	0.110	0.030	0.041	0.041
short	10x1.2	v_t^1 (V)	0.023	0.024	0.024	-0.077	-0.077	-0.079	-0.177	-0.177	-0.182

PCM notes:

1. PCM and ESPEC share the same limits
 2. There is no PCM monitoring
 3. K' (Beta) NOM model is not centered to E-spec
 4. i_{dsat} PCM limits for 0.22x0.18 thin oxide NFET are 0.12-0.28 mA
 5. i_{dsat} PCM limits for 0.22x0.18 thin oxide PFET are 0.05-0.1 mA
- PCM limits in notes 4-5 will be changed to match the ESPECs

TABLE 2.27 TOX Variation in Corner and Statistical Models

	3-σ Corner		3-σ Stat	
	Espec	Model	Espec	Model
1.8V thin tox	+/- 1A	+/- 1A	+/- 1.5A	+/- 1.5A
3.3V thick tox	+/- 1.8A	+/- 1.8A	+/- 3A	+/- 3A
5V thick tox	+/- 8A	+/- 8A	+/- 10A	+/- 10A

2.6 Mismatch Models

2.6.1 Measurements

The measurement setup is composed of a HP4156 Semiconductor Parameter Analyzer, Keithley 707 switch matrix with 7172 low current matrix cards, and Signatone S485 semi-automatic prober with hot chuck. The test is a two step process. In the first step, the average thresholds of the two transistors in the FET pair are measured via the maximum transconductance method. In the second step, the gate is biased at $V_{gs} = V_{gst} = V_t + 0.1, 0.3, 0.5$ and the currents in each transistor measured for multiple drain biases ($V_{ds} = 0.2, 0.6, 1.4$). The mismatch current is then evaluated via Eq. 9:

$$\Delta I_d = 100 \times \frac{I_{d2} - I_{d1}}{I_{d1}} \quad (\text{EQ 9})$$

The mismatch current represents the error between the currents in a simple current mirror. The transistors in the mismatch test-structures are typically ~10μm apart, representing a worst-case mismatch for most analog layouts, where the transistors in the matched pair can be laid-out in closer proximity to each other.

A detailed description of MOSFET mismatch characterization methodology and results are available in Jazz Semiconductor document NPB PS-0281 titled “Analog Characterization Report for CA18.”

2.6.2 Mismatch modeling

The mismatch between neighboring FETs is a representation of the local variation of process parameters such as oxide thickness, channel doping, oxide charge, gate work-function, channel length and width. The basic equations used to model such variations are identical to what was described in the section “Statistical and Corner Models” on page 101. To match the measured data, these variations are made geometry dependent as per Eq. 10:

$$\sigma_{local}(X) = \frac{\sigma_X}{\sqrt{W_{eff} \cdot L_{eff}}} \quad (\text{EQ 10})$$

where X is the channel doping N_{ch} , low field mobility U_0 , flat-band voltage V_{FB} , or oxide thickness T_{ox} . The impact of local lithographic variations is captured via Eq. 11 and Eq. 12:

$$\sigma_{local}(\Delta W) = \frac{\sigma(\Delta W)}{\sqrt{L_{eff}}} \quad (\text{EQ 11})$$

$$\sigma_{local}(\Delta L) = \frac{\sigma(\Delta L)}{\sqrt{W_{eff}}} \quad (\text{EQ 12})$$

whereby a narrower device can be expected to have larger channel length variations, and a shorter device can be expected to have larger channel width variations.

The local variation in these 6 parameters is extracted via a nonlinear least squares global optimization method to best fit the measured data.

2.6.3 Mismatch model usage guidelines

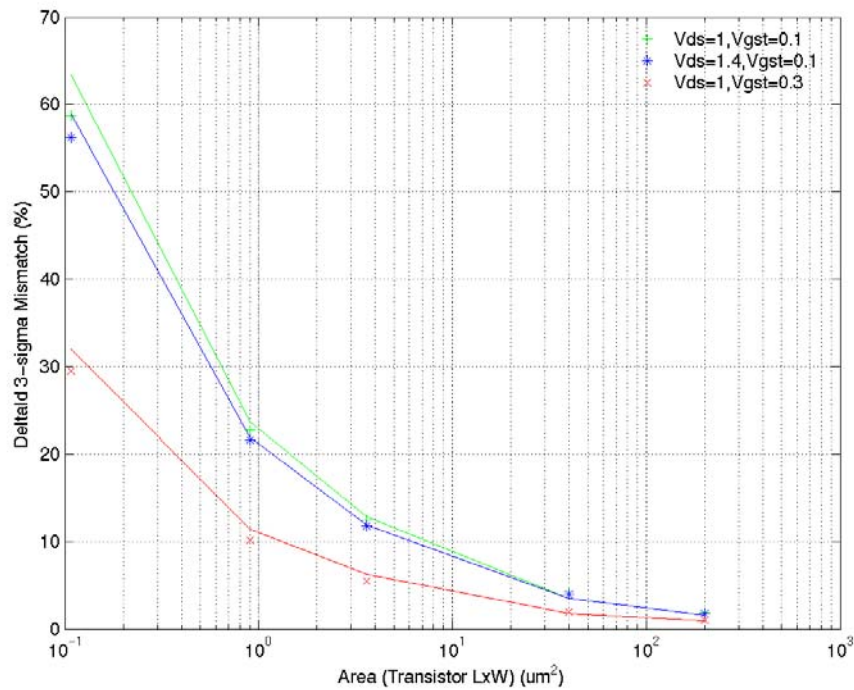
The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between transistors. It is implemented inside the “sub-circuit” definition of the FETs allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the FETs. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

2.6.4 Mismatch model comparison with measurements

Figure 2.147 through Figure 2.153 compare the mismatch model prediction with the measured data for the $3\text{-}\sigma$ ΔI_d mismatch between a pair of neighboring transistors for low and high voltage N and PFETs. The discrete points are the measured data, while the solid lines represent simulated data. The 3.3V native FET mismatch model is based on data from regular 3.3V FETs. Mismatch data for 5V FETs is not available. The model is

extracted from mismatch data available on similar 5V FETs in another technology. Mismatch models on 5V native FETs are not currently supported.

FIGURE 2.147 1p8_NFET mismatch model vs. measurements



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FIGURE 2.148 1p8_PFET mismatch model vs. measurements

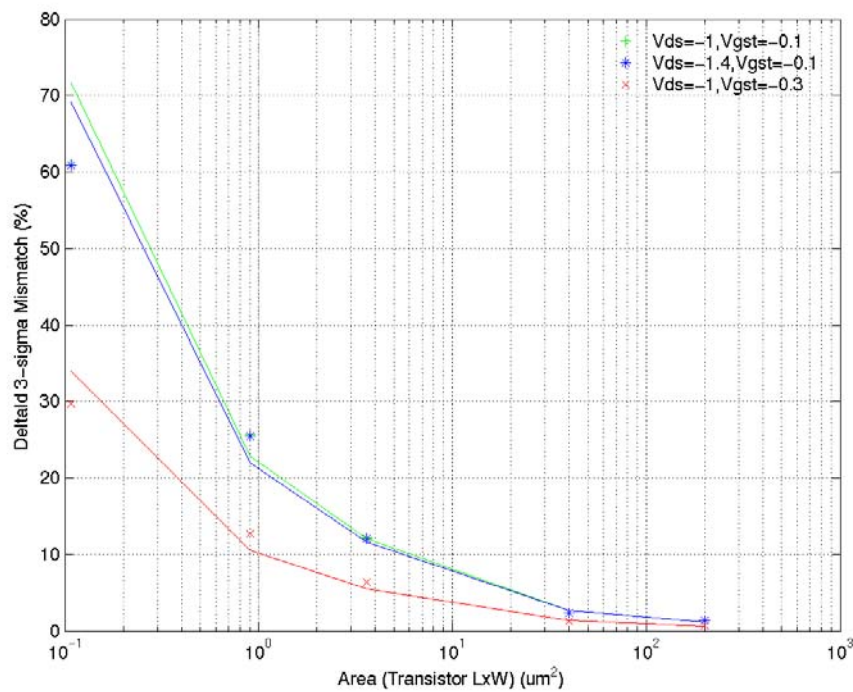


FIGURE 2.149 3p3_NFET mismatch model vs. measurements

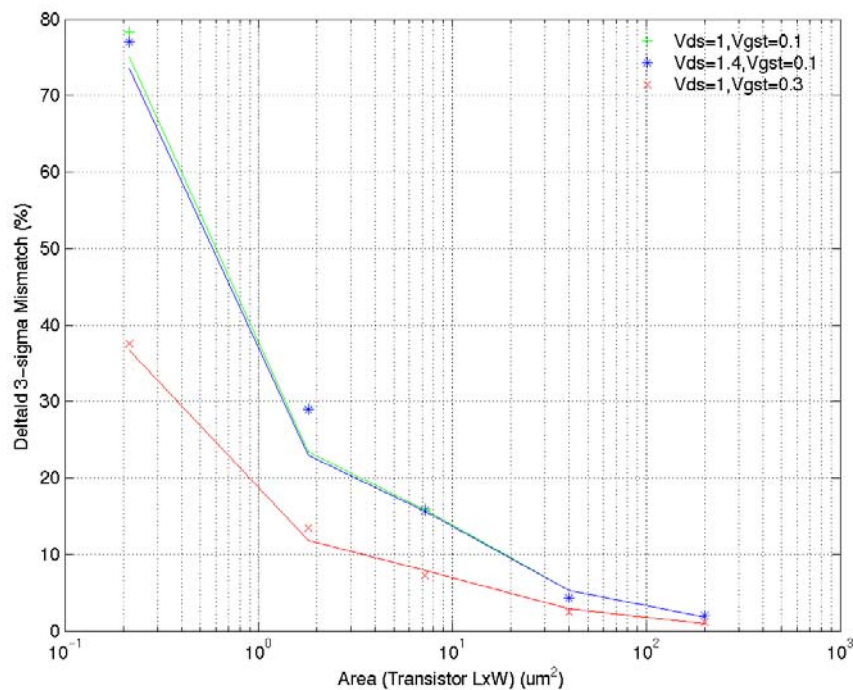


FIGURE 2.150 3p3_PFET mismatch model vs. measurements

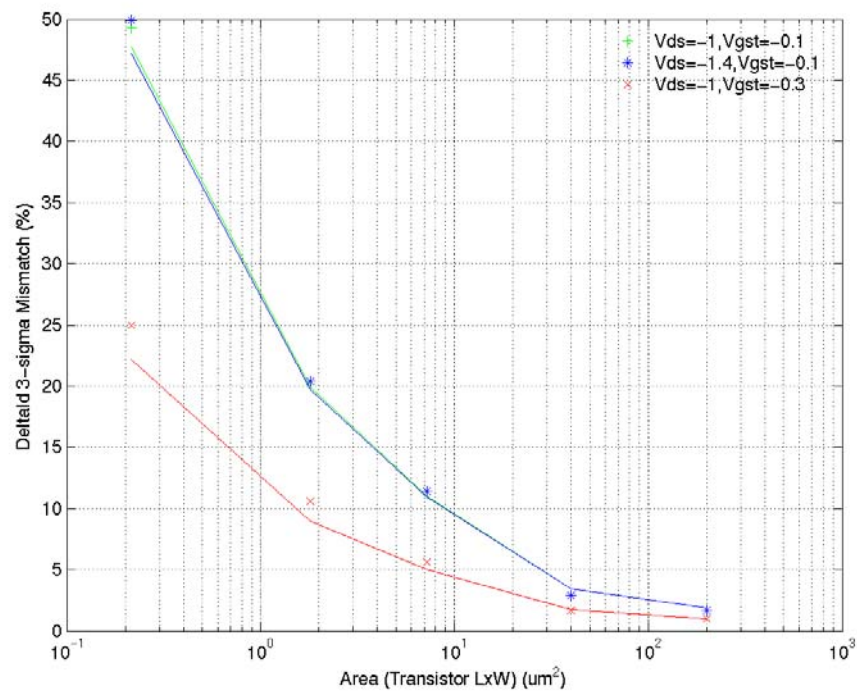


FIGURE 2.151 3p3_native_NFET mismatch model vs. measurements

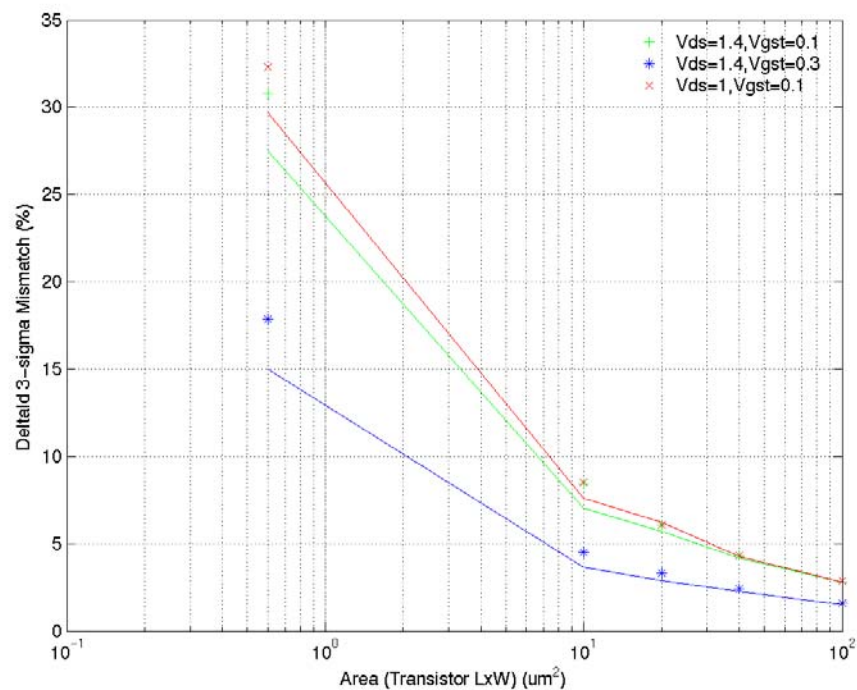


FIGURE 2.152 5V_NFET mismatch model vs. measurements

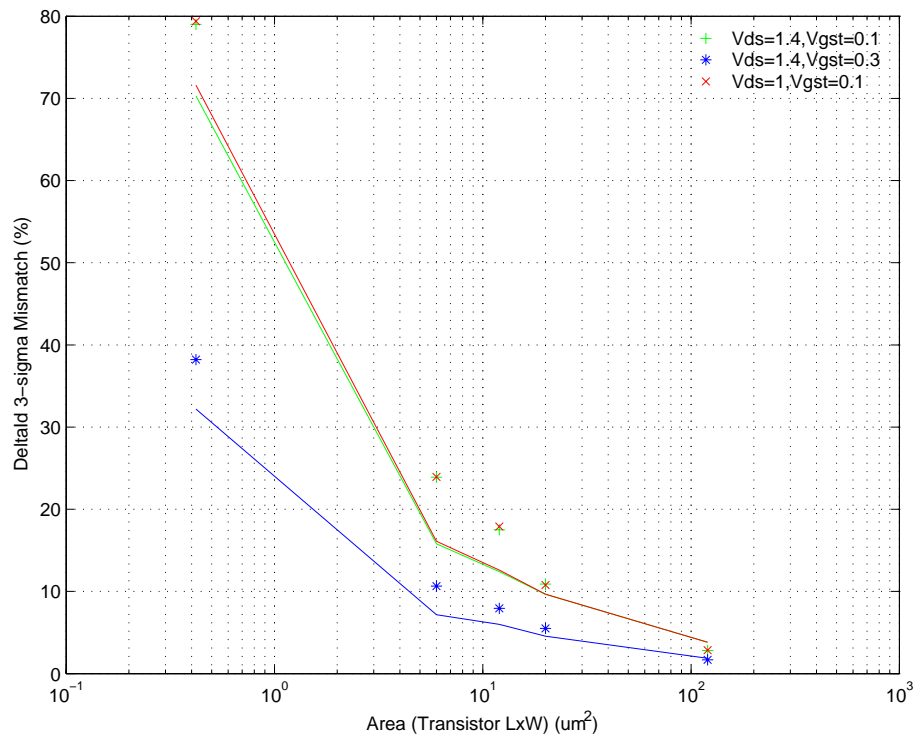
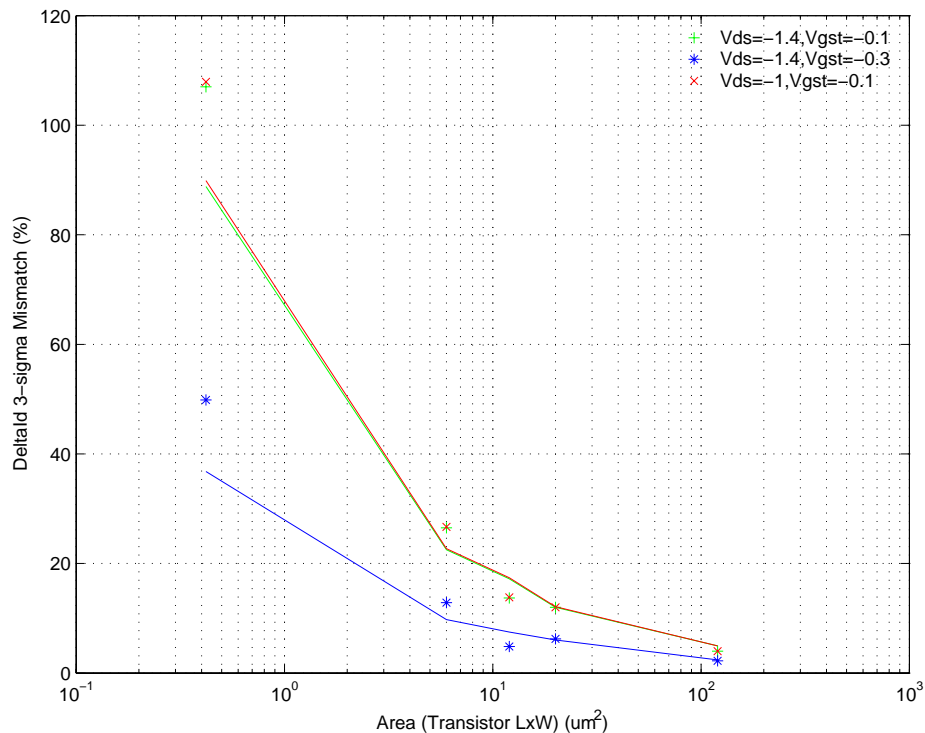


FIGURE 2.153 5V_PFET mismatch model vs. measurements

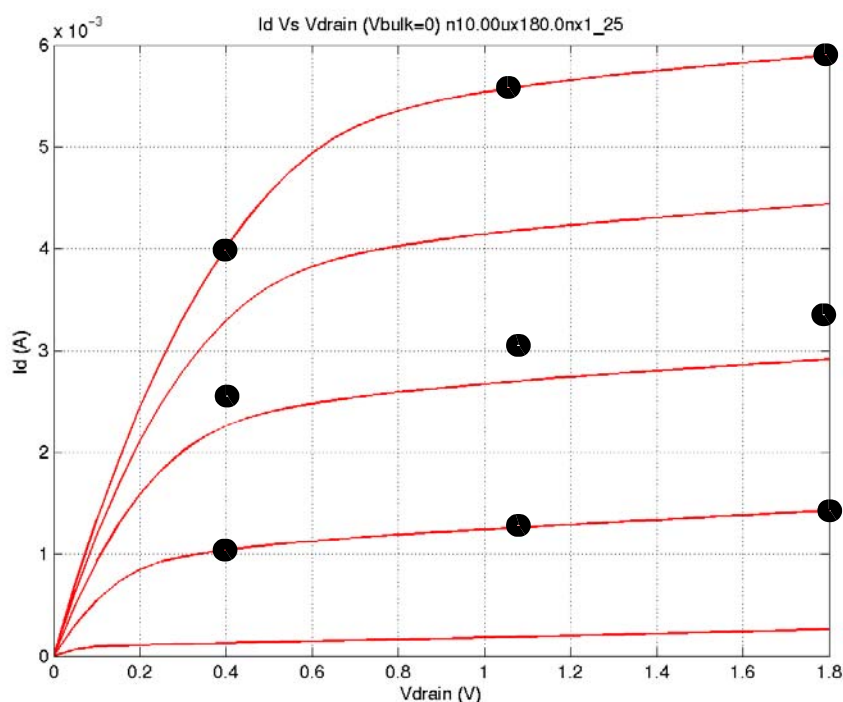


2.7 Flicker Noise

2.7.1 Measurement

Flicker noise ($1/f$ noise) was measured using the BTA9812A noise analyzer system in conjunction with the HP35670A dynamic signal analyzer using an on-wafer probe-station. BTA's Noisepro software was used to automate the measurements. Precautions were taken to electrically isolate the DUT and the RF-transistor (Ground-Signal-Ground) layouts were used to minimize on-wafer ground loops that can corrupt the measurements. Multi-die measurements with the MOSFET biased in saturation were performed to select the worst-case noise site. Measurements were then performed at 9 different biases. The list of biases encompassed both the linear and saturation regions of the FET and are illustrated in Figure 2.154.

FIGURE 2.154 Plot illustrating the bias points at which flicker noise measurements were performed



2.7.2 Flicker noise modeling

There are several flicker noise models available inside BSIM3v3. The BSIM3 flicker noise model has been found to give an accurate description of the bias and geometry dependence of flicker noise. This model is used whenever sufficient data with bias and geometry dependence is available. In addition, commercial circuit simulators such as Spectre, ADS, and HSPICE provide a “gm” based noise model with the correct area dependence. This model is available in Spectre by setting “flkmod=1”, and in ADS and HSPICE by setting “nlev=2.” Mathematically this model is expressed in Eq. 13:

$$S_{id}(f) = \frac{KF \cdot g_m^2}{f^{AF} \cdot C_{ox} \cdot W_{eff} \cdot L_{eff}} \quad (\text{EQ 13})$$

Model parameters KF and AF were extracted from measurements via a global optimization method across bias and geometries. Table 2.28 lists the flicker noise model used for the various FETs in CA18.

TABLE 2.28 Flicker noise model usage in CA18 MOSFETs

FET	Flicker Noise Model
1.8V N and PFETs	BSIM3
3.3V N and PFETs	BSIM3
3.3V Native NFET	gm-based
5V N and PFETs	gm-based
5V Native NFET	gm-based

2.7.3 Flicker noise model playbacks

FIGURE 2.155 1.8V NFET Flicker Noise; $NF \times W \times L = 1 \times 10 \mu\text{m} \times 0.18 \mu\text{m}$

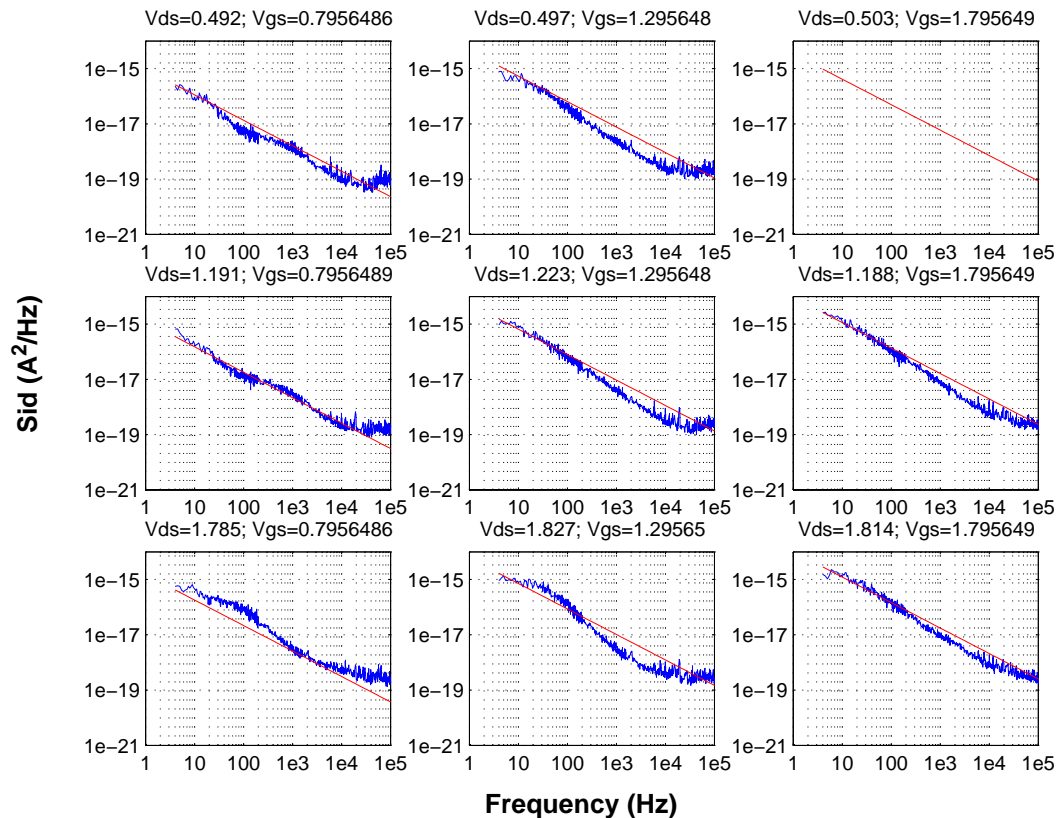


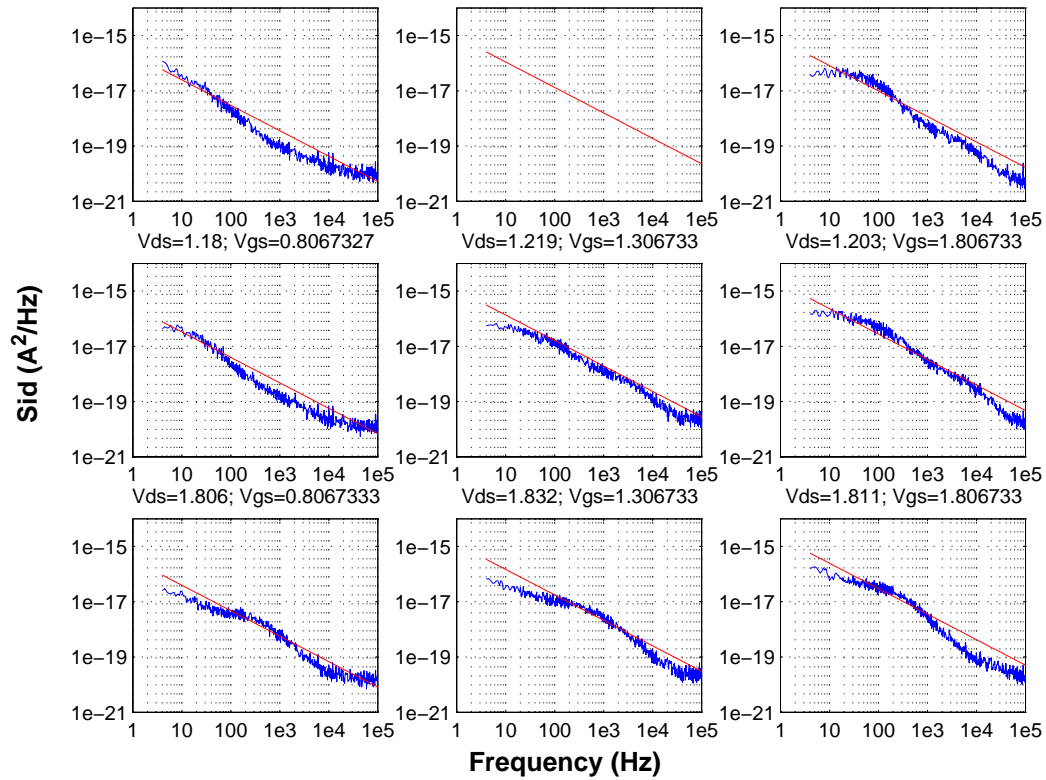
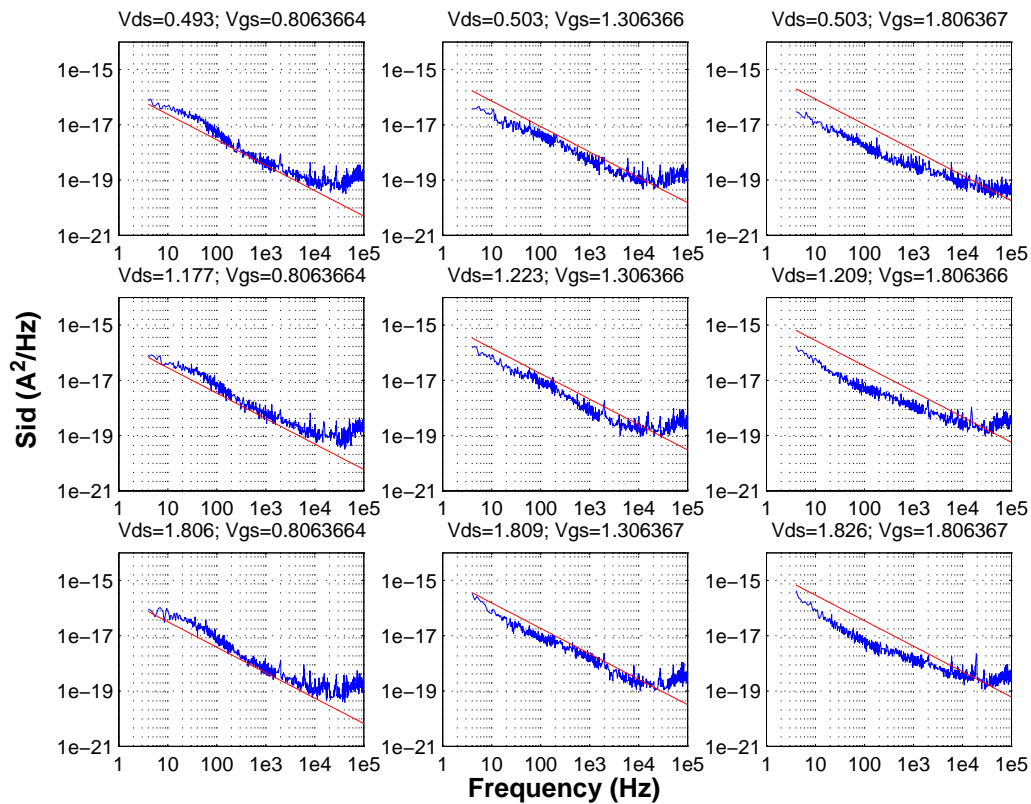
FIGURE 2.156 1.8V NFET Flicker Noise; NFxWxL = 1x2 μ m x 0.18 μ m**FIGURE 2.157 1.8V NFET Flicker Noise; NFxWxL = 1x10 μ m x 0.3 μ m**

FIGURE 2.158 1.8V1.8V PFET Flicker Noise; NFxWxL = 1x10 μ m x 0.18 μ m

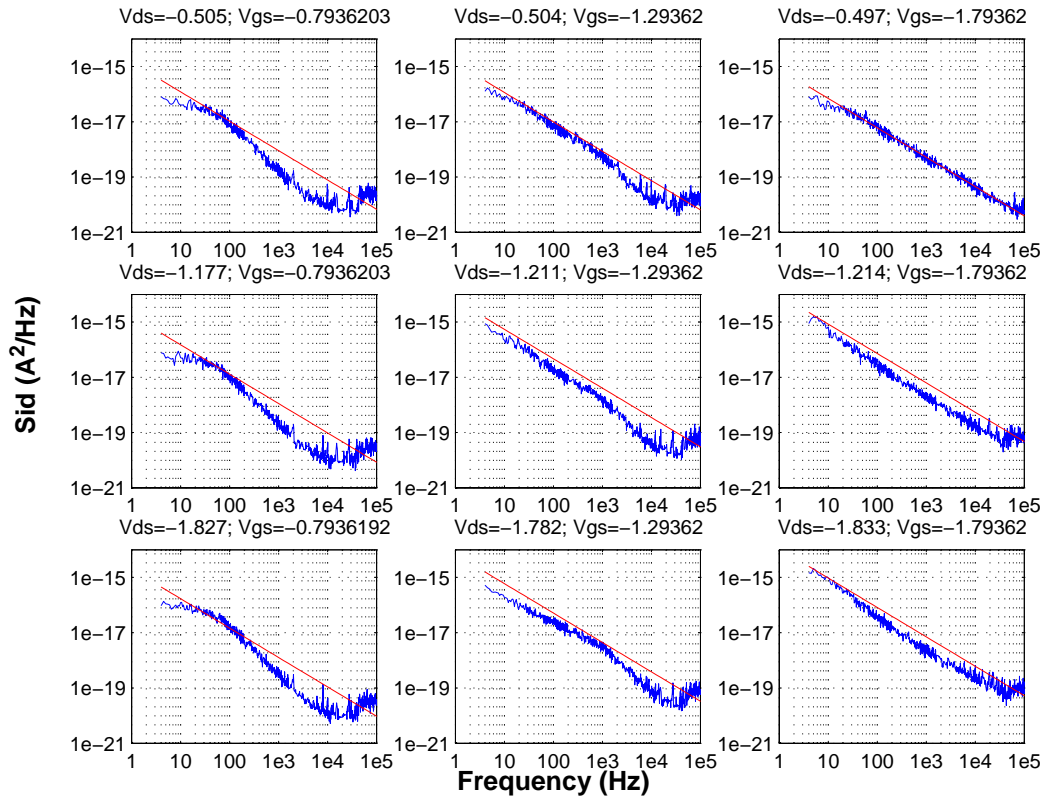


FIGURE 2.159 1.8V PFET Flicker Noise; NFxWxL = 1x2 μ m x 0.18 μ m

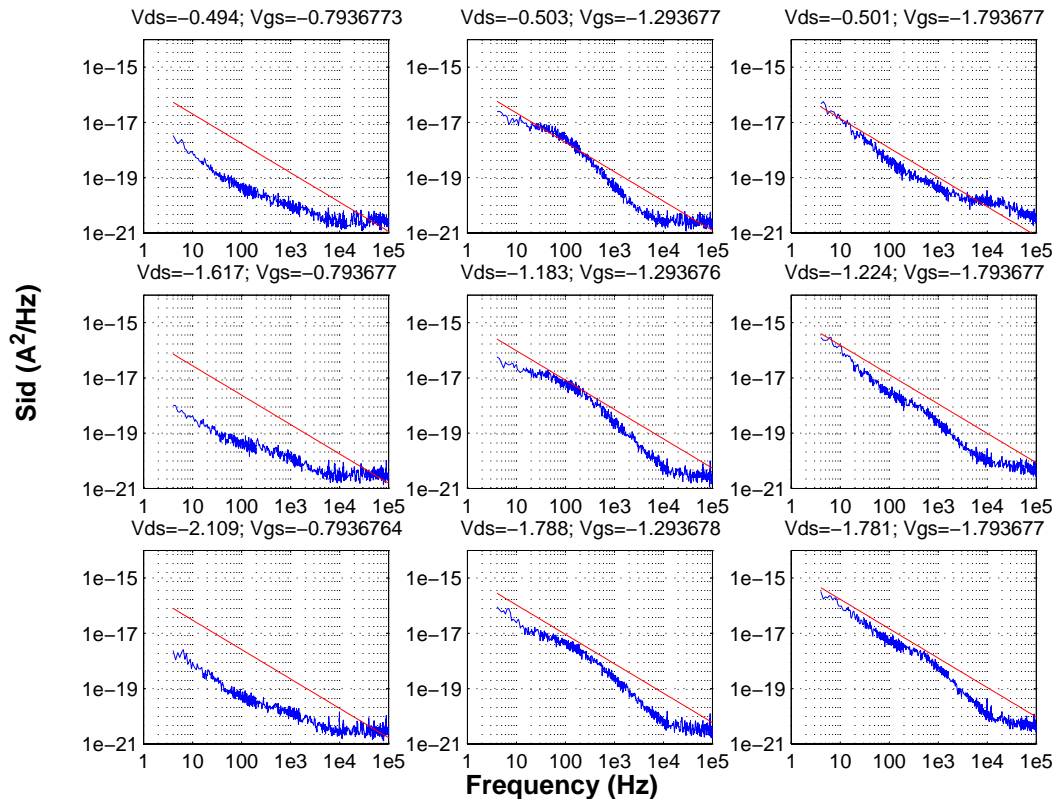


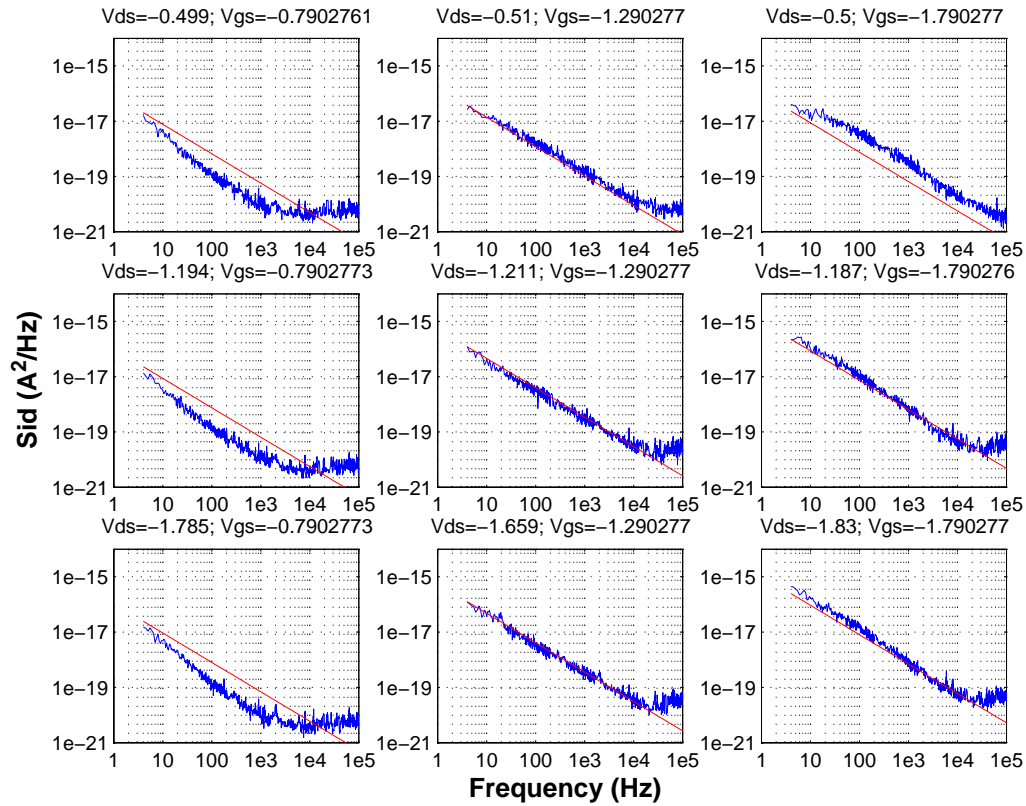
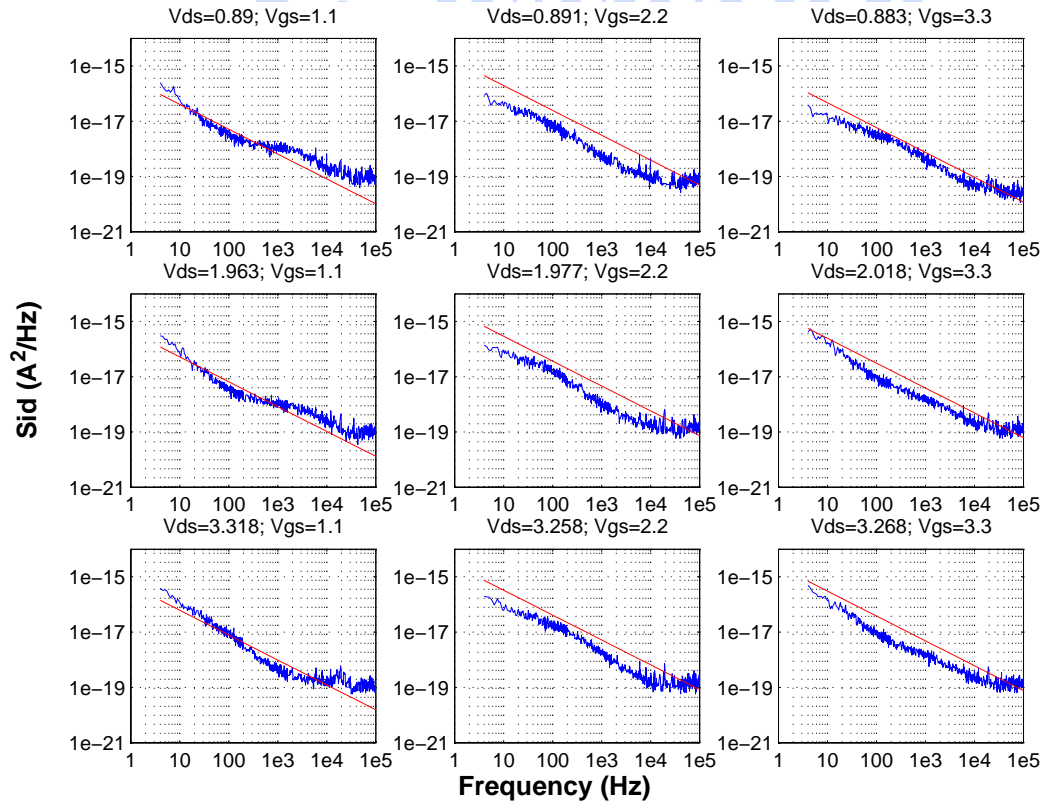
FIGURE 2.160 1.8V PFET Flicker Noise; NFxWxL = 1x10 μ m x 0.3 μ m**FIGURE 2.161 3.3V NFET Flicker Noise; NFxWxL = 1x10 μ m x 0.36 μ m**

FIGURE 2.162 3.3V NFET Flicker Noise; NFxWxL = 1x2 μ m x 0.36 μ m

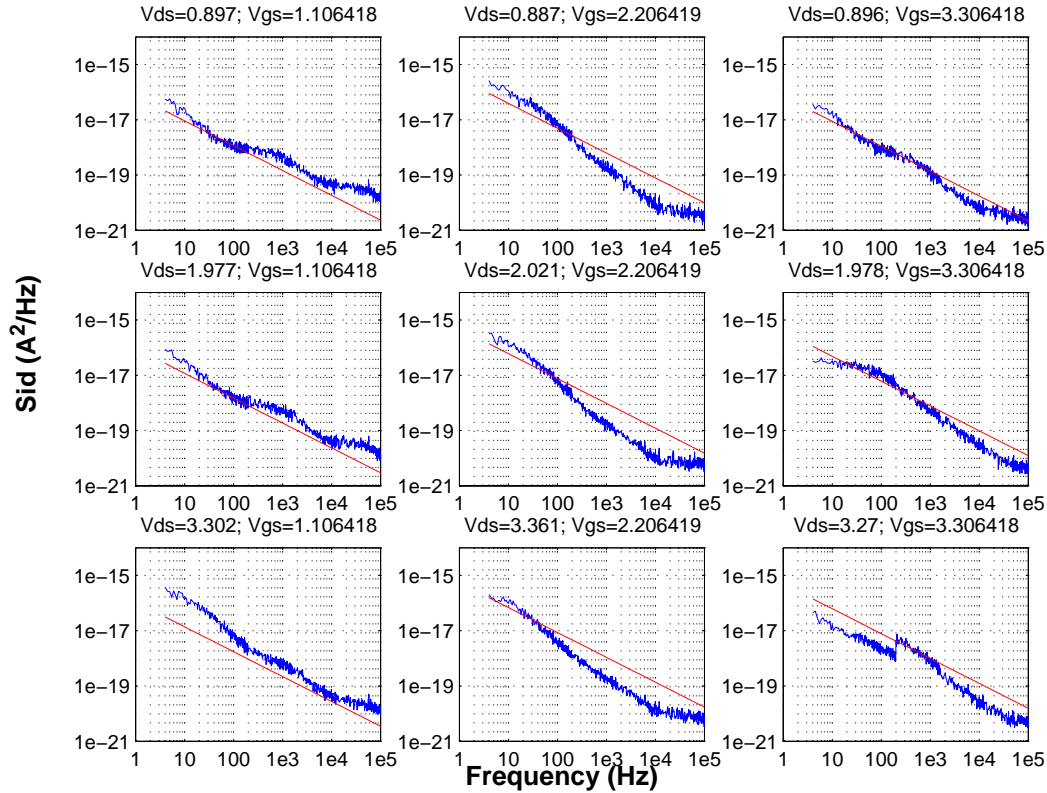


FIGURE 2.163 3.3V NFET Flicker Noise; NFxWxL = 1x10 μ m x 0.6 μ m

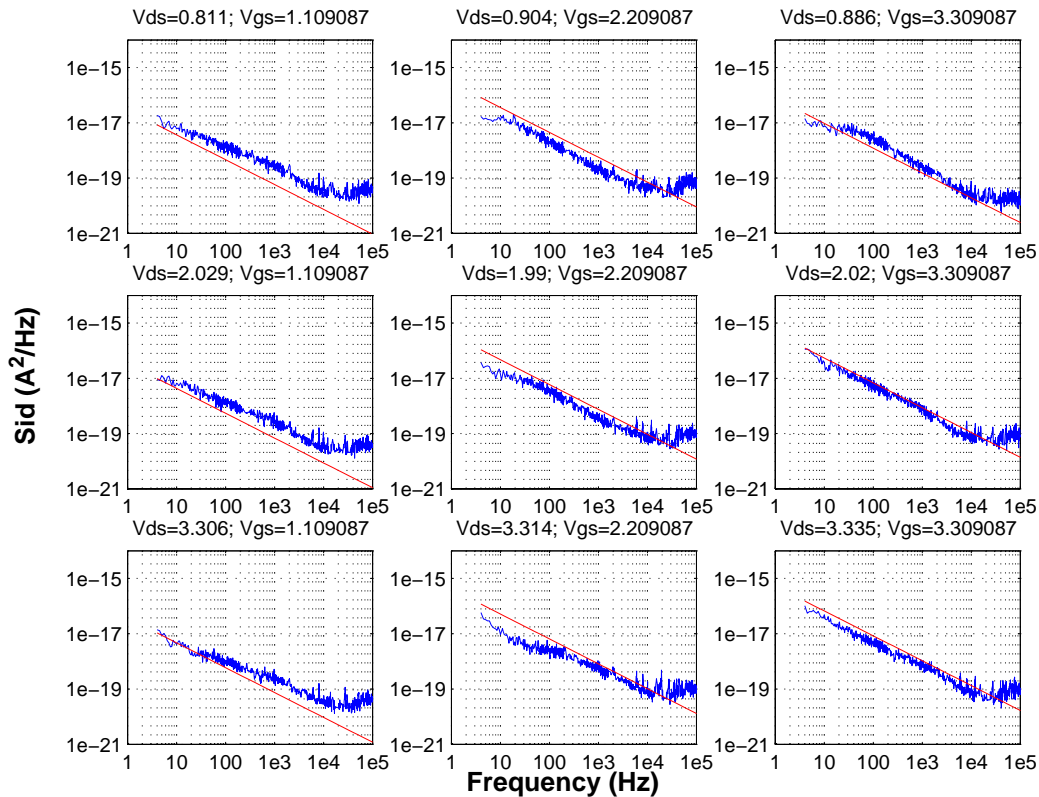


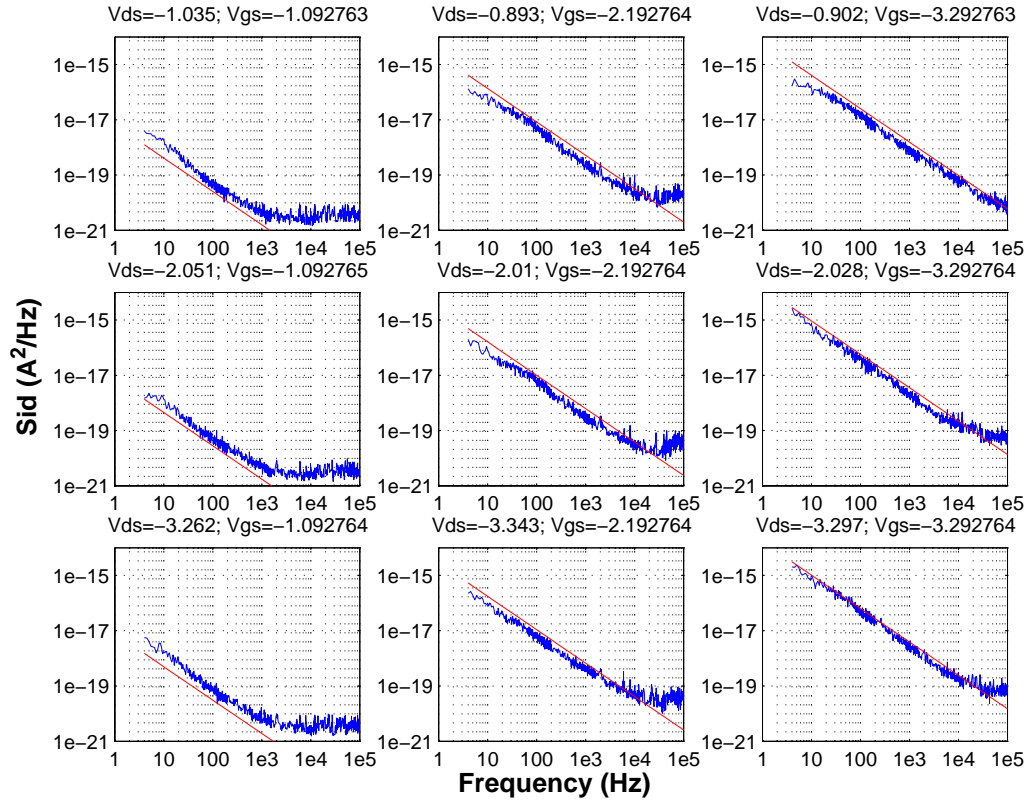
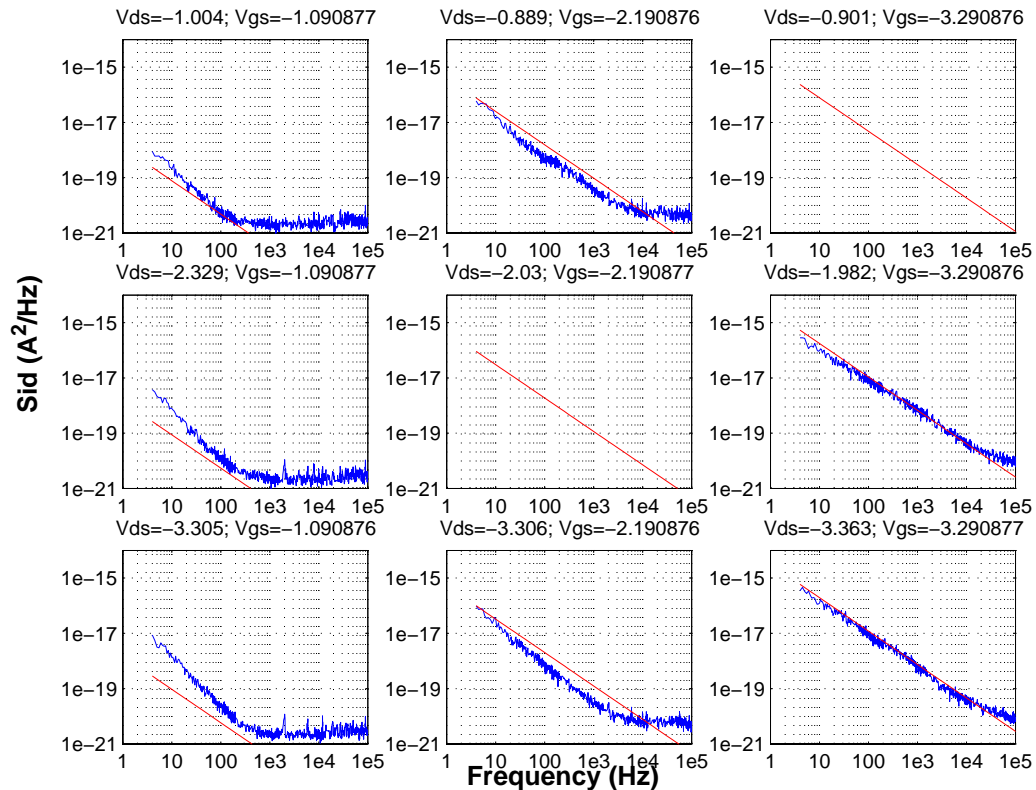
FIGURE 2.164 3.3V PFET Flicker Noise; NFxWxL = 1x10 μ m x 0.36 μ m**FIGURE 2.165 3.3V PFET Flicker Noise; NFxWxL = 1x2 μ m x 0.36 μ m**

FIGURE 2.166 3.3V PFET Flicker Noise; NFxWxL = 1x10 μ m x 0.6 μ m

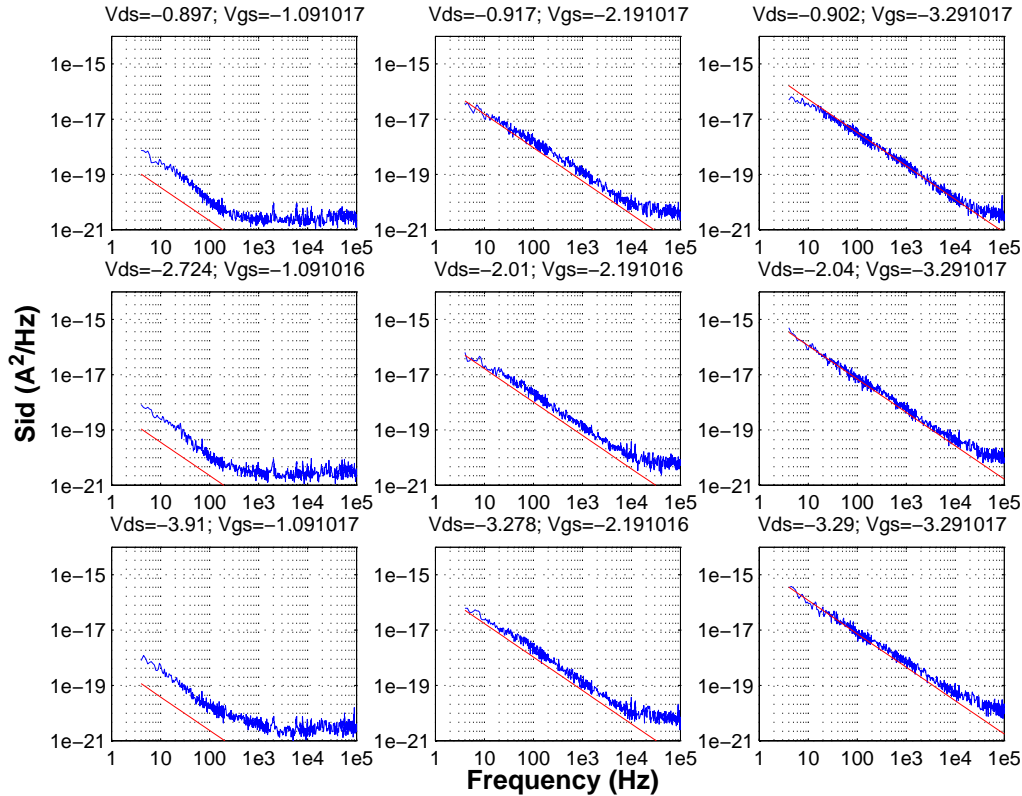


FIGURE 2.167 3.3V Native NFET Flicker Noise; NFxWxL = 10x4 μ m x 1.2 μ m

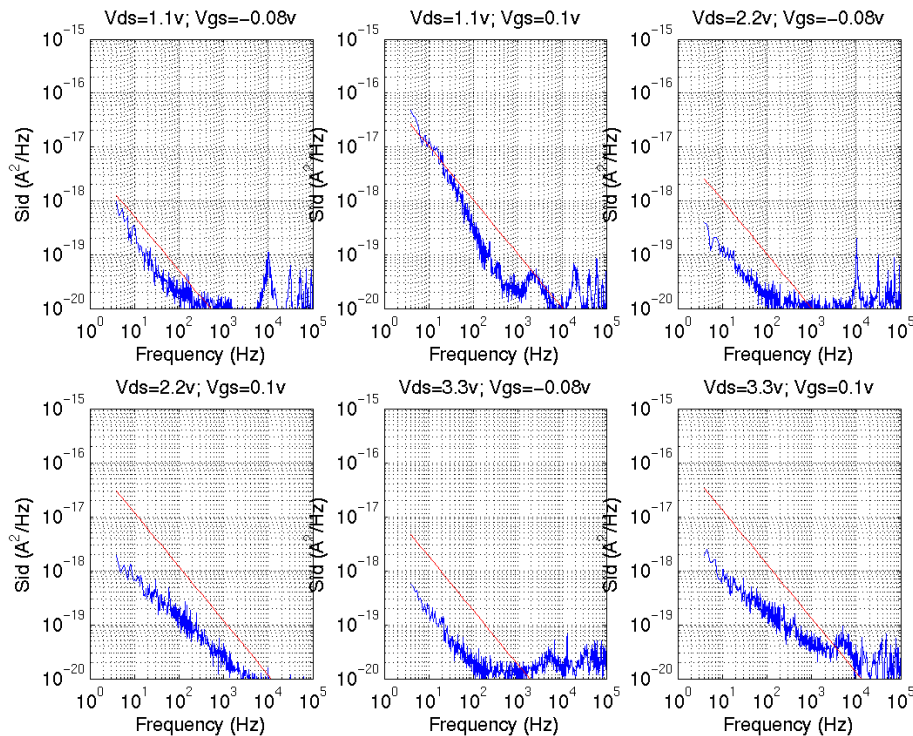
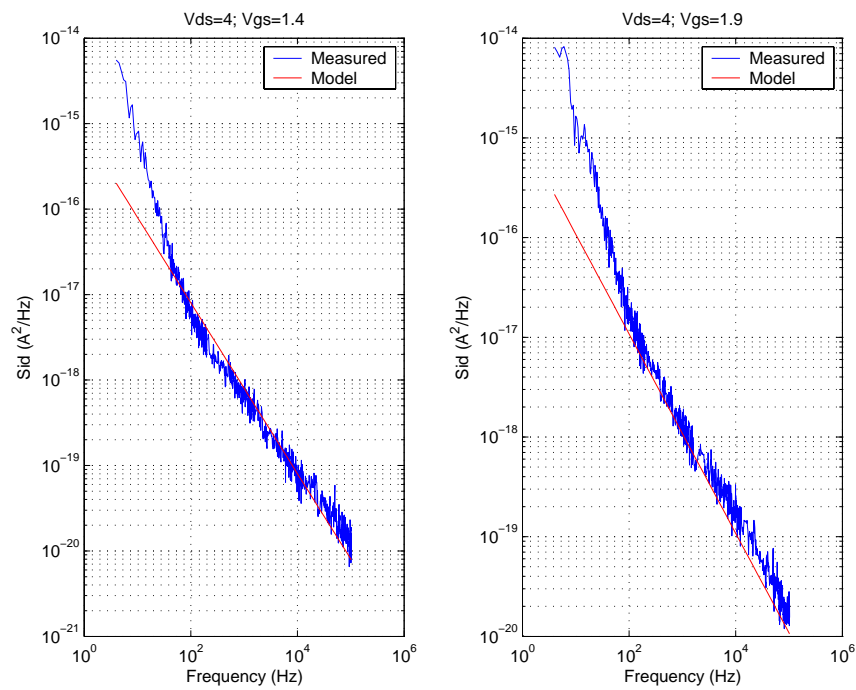
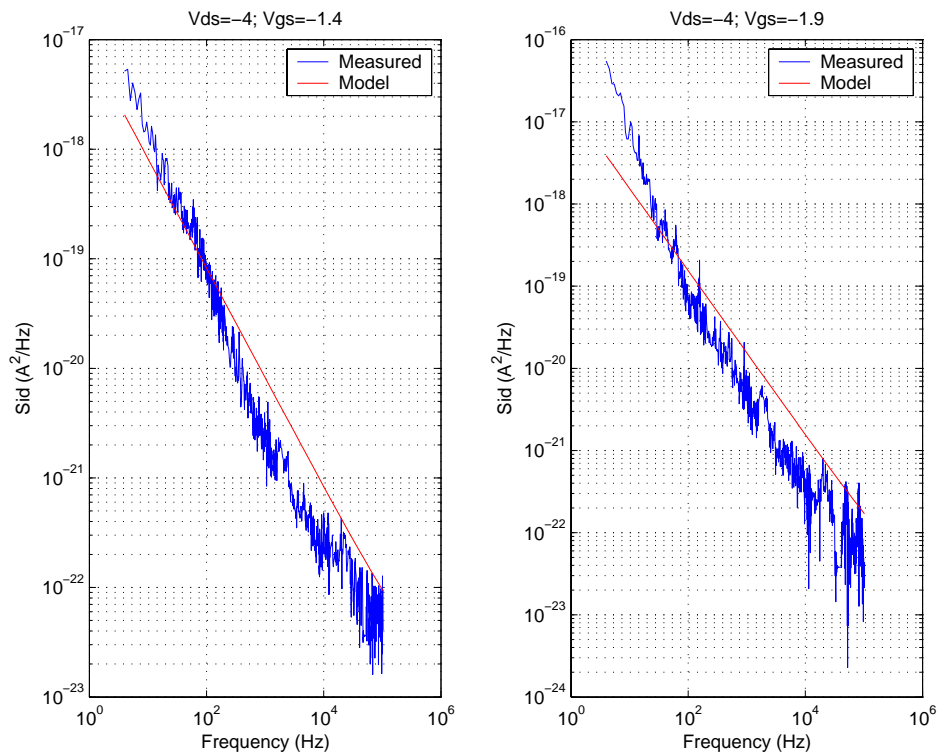


FIGURE 2.168 5V NFET Flicker Noise; NFxWxL = 1x25 μ m x 0.6 μ mFIGURE 2.169 5V PFET Flicker Noise; NFxWxL = 1x25 μ m x 0.6 μ m

2.8 Released model Quality Assurance (QA)

A rigorous QA procedure is executed before any new model release. The geometry dependence of 9 key device parameters is examined for any non-physical behavior for all 3 cases: Nominal, Fast, and Slow. These parameters are listed in Table 2.29 .

TABLE 2.29 MOSFET electrical parameters list examined as part of model release QA

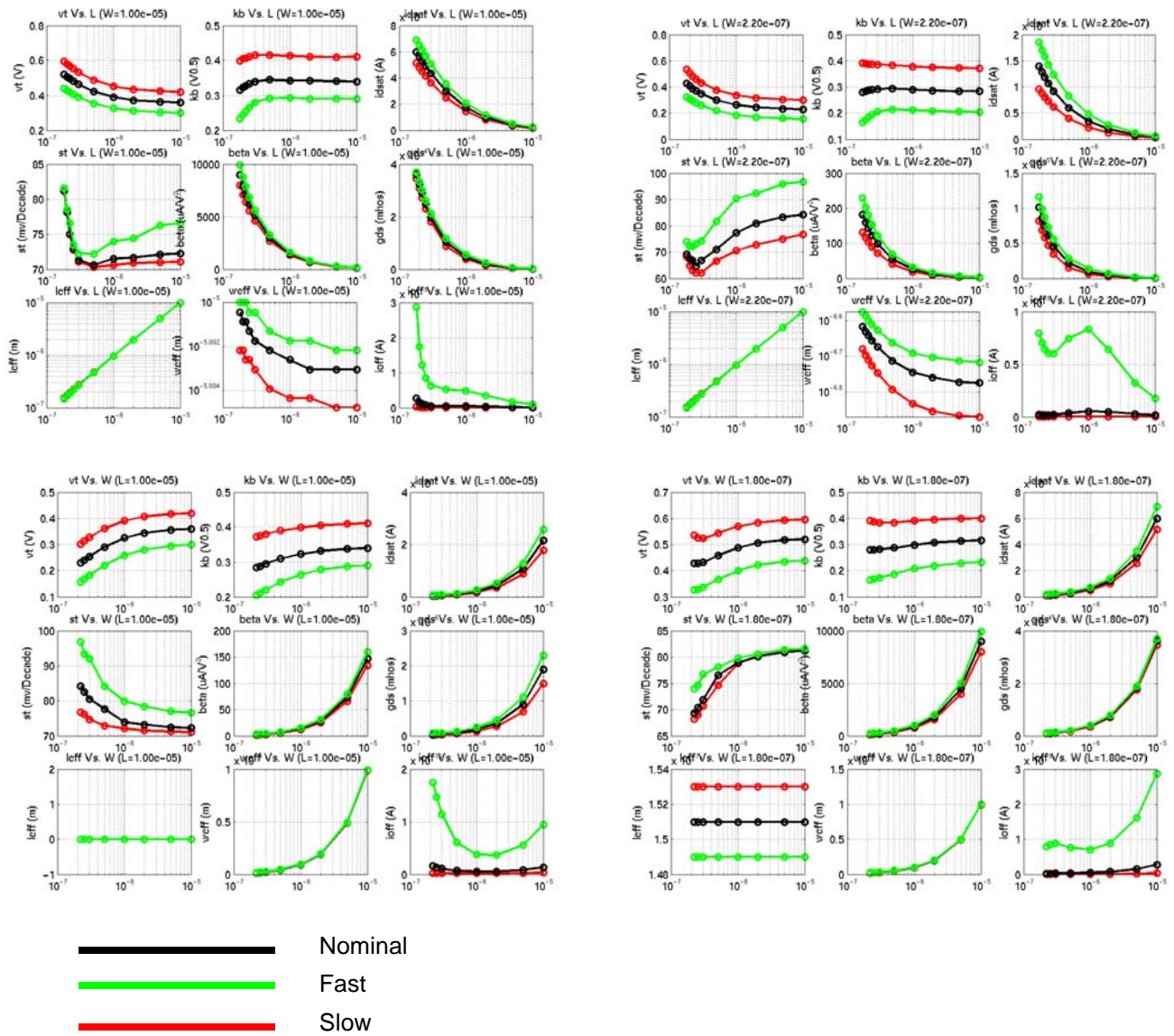
Parameter	Description
v_t (V)	Threshold voltage in the linear region
k_b ($V^{0.5}$)	Body constant
i_{dsat} (mA)	Drain current at $V_{gs}=V_{ds}=V_{dd}$
st (mV/dec.)	Sub-threshold slope in the linear region evaluated at $V_{gs}=V_t/5$
β ($\mu A/V^2$)	Extracted from the max. g_m as: $1e6 \cdot (g_{m_max}/2 \cdot \text{abs}(v_d))$, where $\text{abs}(v_d)=0.05$ V is the drain voltage to bias the trans. in the linear region
g_{ds} (mhos)	Output conductance in the saturation region evaluated at $V_{gs}=V_{ds}=V_{dd}$
L_{eff} (μm)	Electrical channel length
W_{eff} (μm)	Electrical channel width
i_{off} (A)	Off-state leakage current at $V_{gs}=0$, $V_{ds}=V_{dd}$

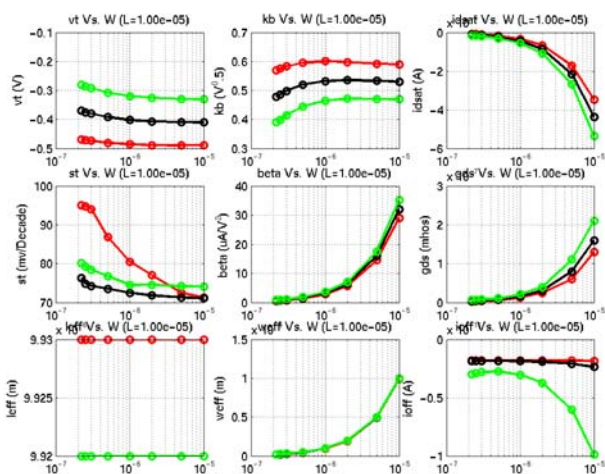
Figures 2.170 through 2.177 illustrate the geometry dependence of these 9 parameters for the 1.8V thin-, 3.3V thick- and 5V thick-oxide N and P-FETs. For each devices 4 plots are generated as per Table 2.30 . The right-hand most column in the table references the location of the plot. For e.g. the 1.8V thin oxide NFET, electrical parameter vs. channel length for the $10\mu m$ wide device is on the top-right of Figure 2.170.




TABLE 2.30 MOSFET channel lengths and widths included as part of QA procedure

Variable dimension	Fixed dimension	Location on plots (Figure 2.170 through Figure 2.173)
Channel length (min. design rule $< L < 10\mu m$)	Channel width = $10\mu m$	Top-left
Channel length (min. design rule $< L < 10\mu m$)	Channel width = Min. design rule	Top-right
Channel width (min. design rule $< W < 10\mu m$)	Channel length = $10\mu m$	Bottom-left
Channel width (min. design rule $< W < 10\mu m$)	Channel length = Min. design rule	Bottom-right

FIGURE 2.170 1p8_NFET_qa_plots





	Nominal
	Fast
	Slow

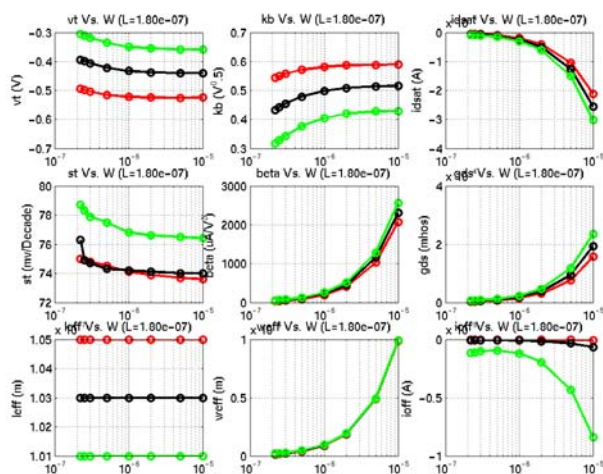
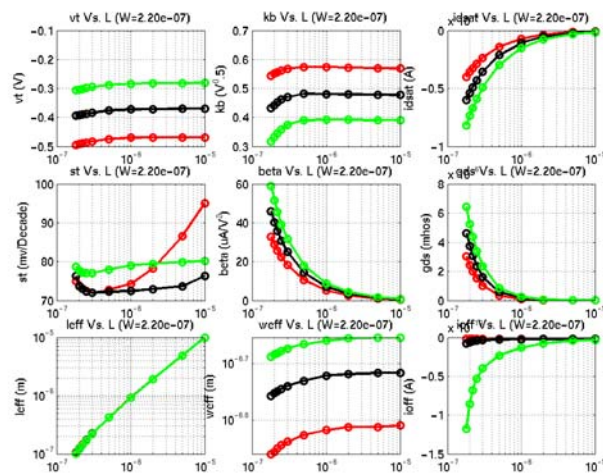


FIGURE 2.172 3p3_NFET_qa_plots

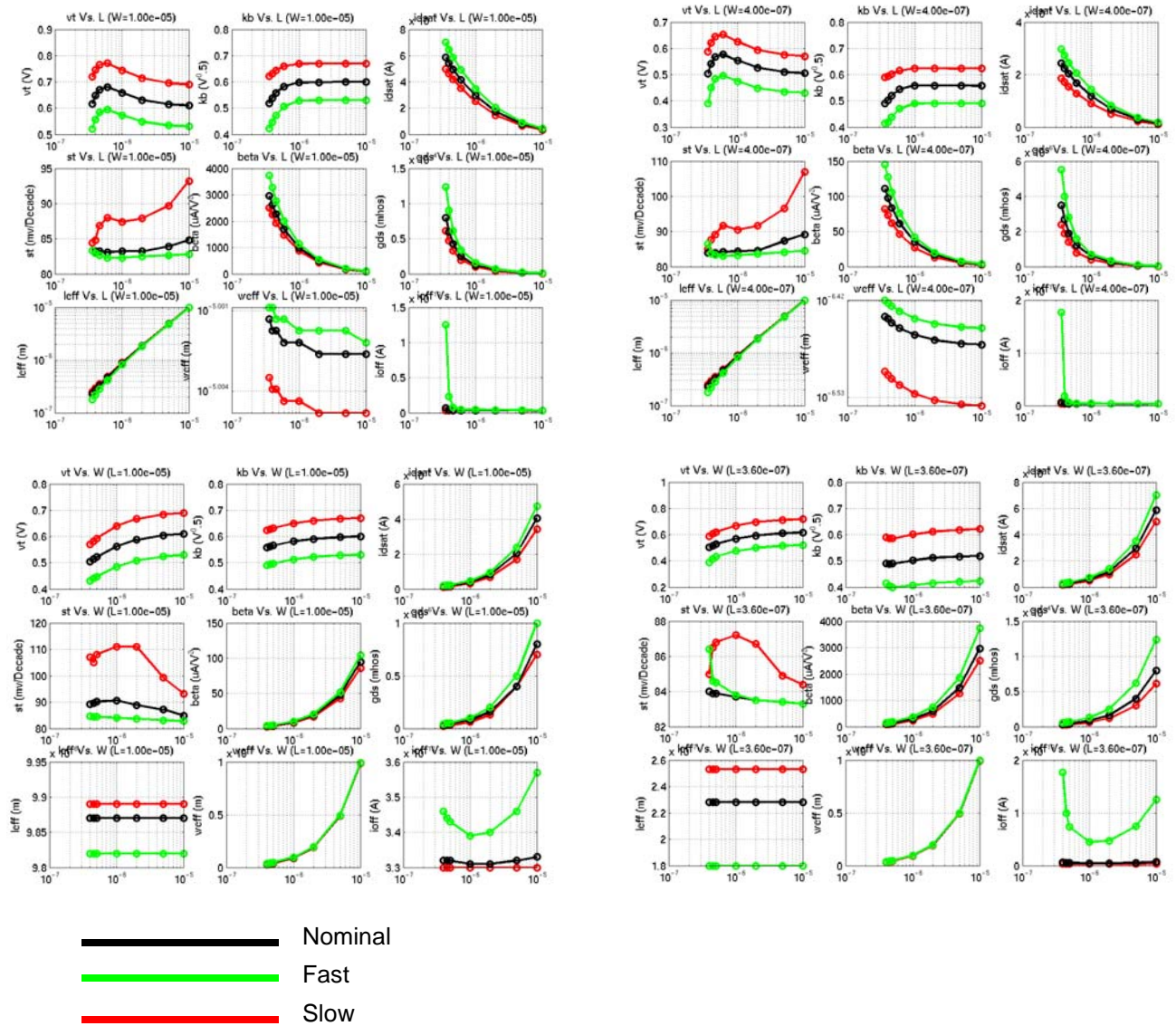


FIGURE 2.173 3p3_PFET_qa_plots

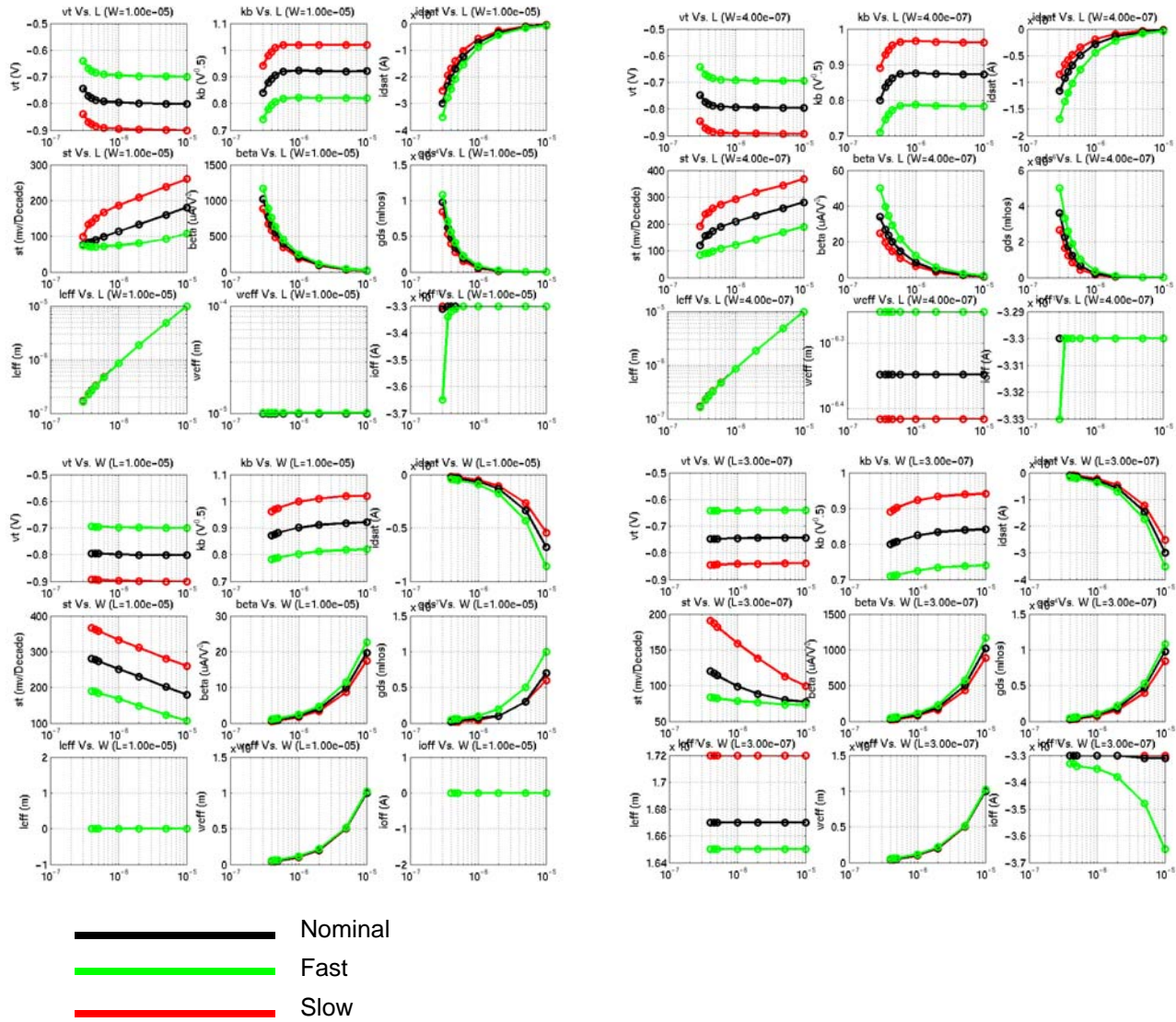


FIGURE 2.174 3p3_native_NFET_qa_plots

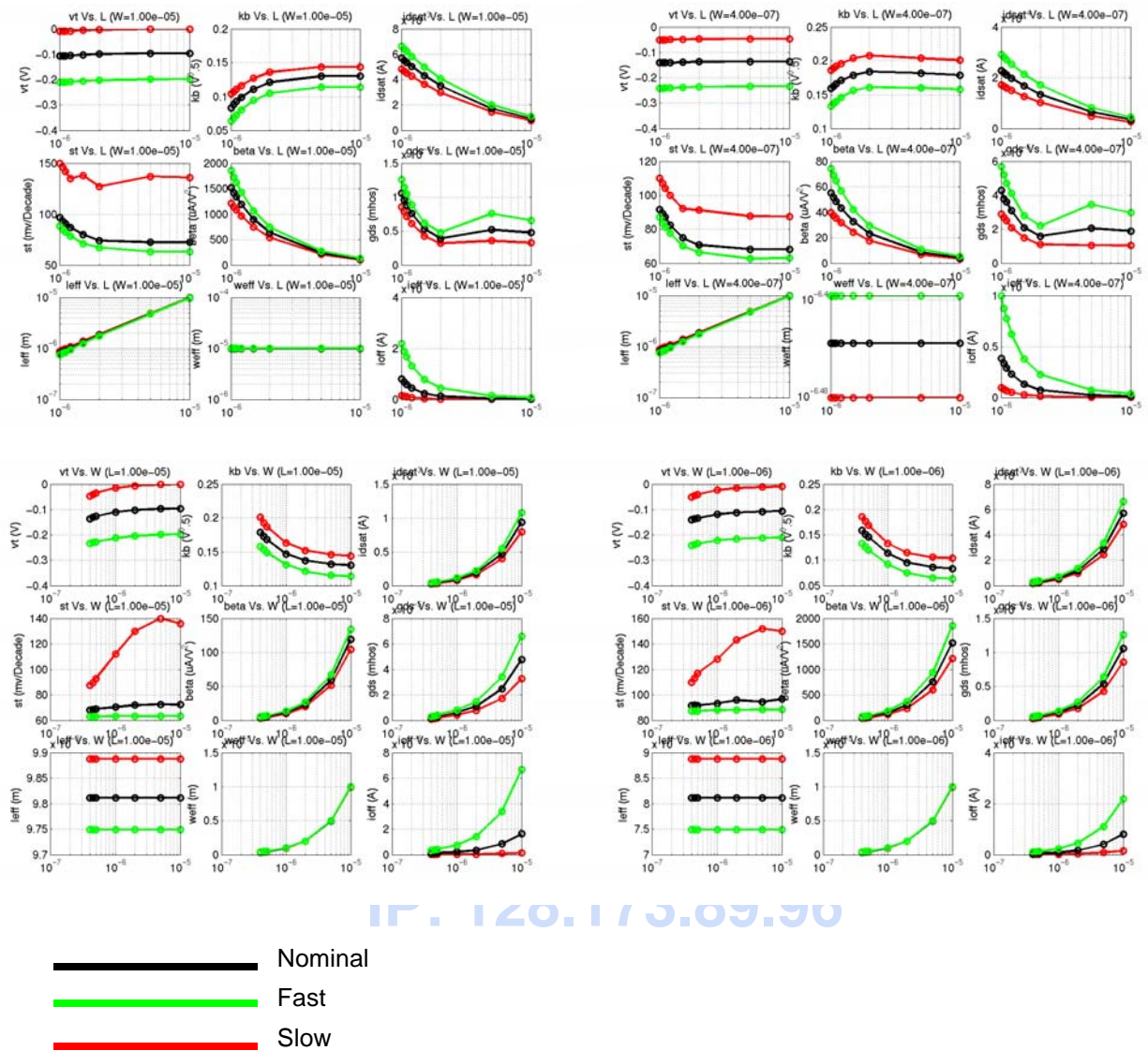


FIGURE 2.175 5V_NFET_qa_plots

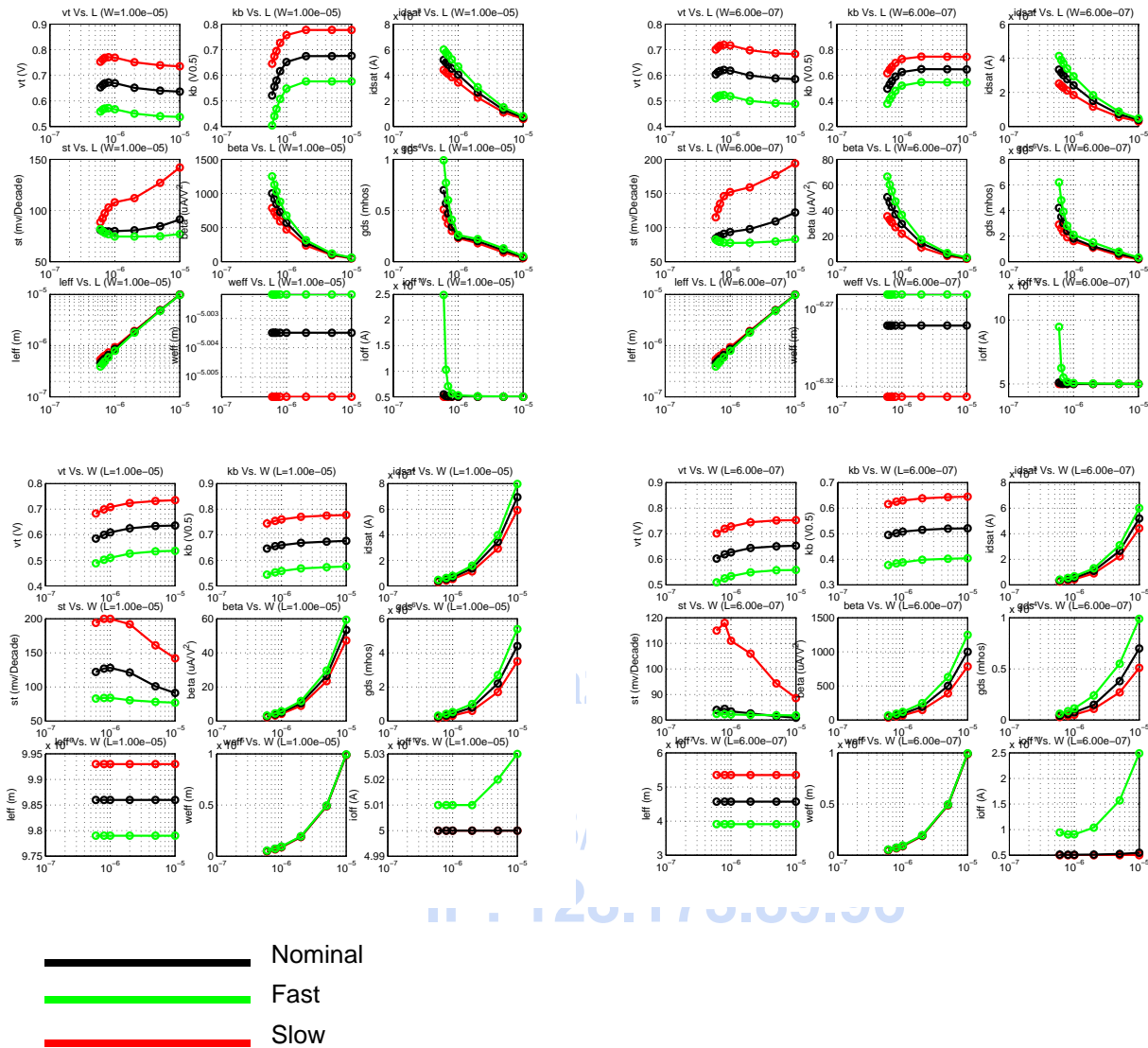
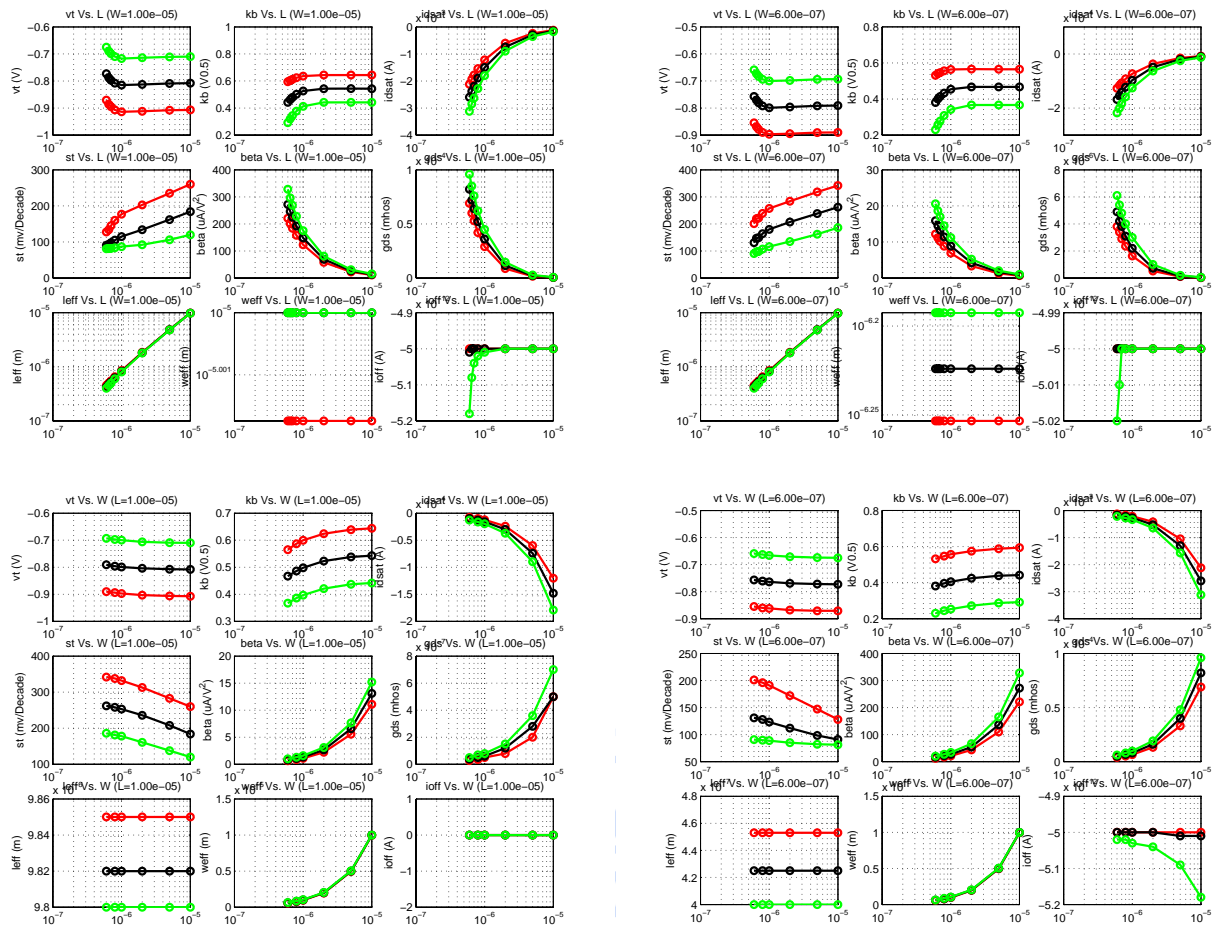
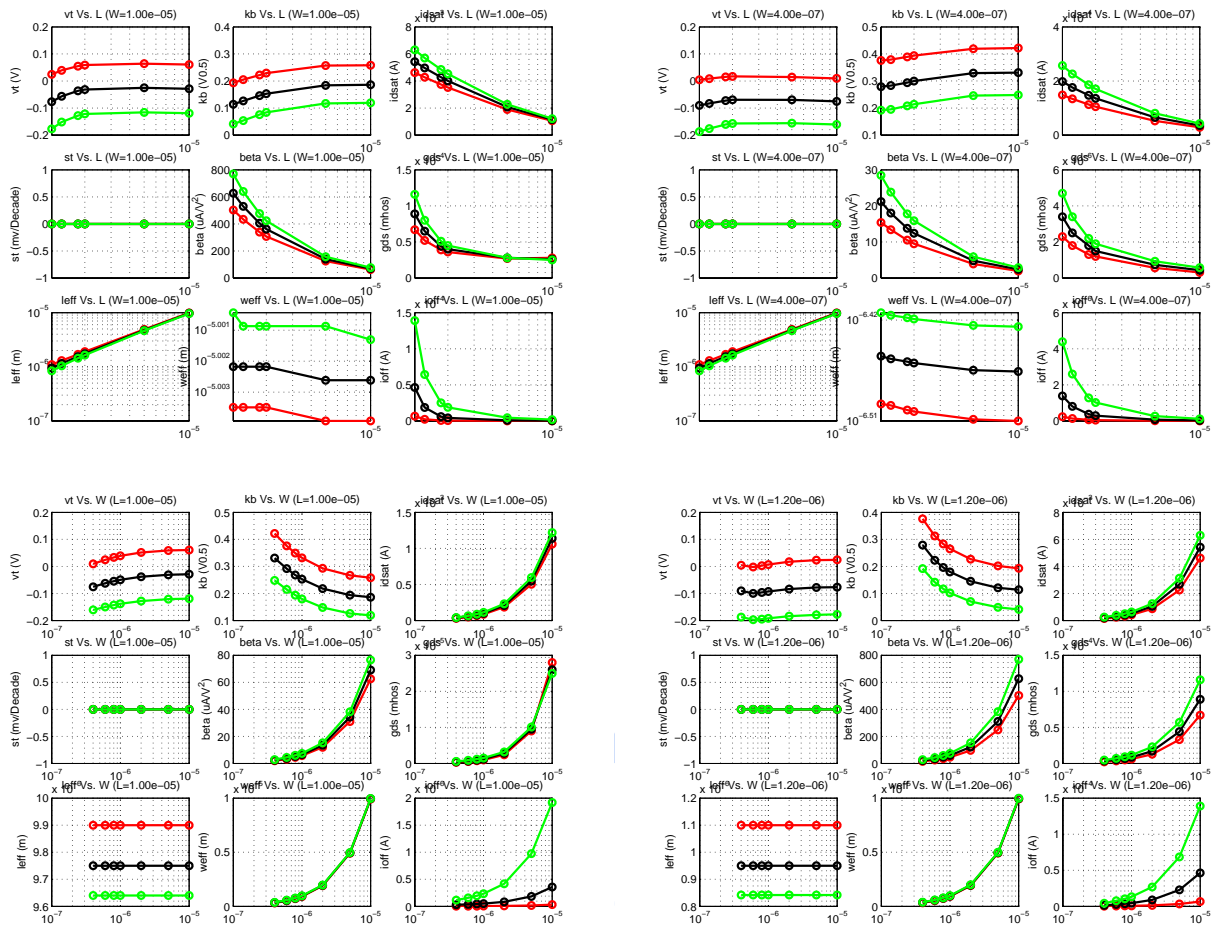


FIGURE 2.176 5V_PFET_qa_plots



— Nominal
 — Fast
 — Slow

FIGURE 2.177 5V_native_NFET_qa_plots



— Nominal
— Fast
— Slow

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2.9 Model Update History v3.2

TABLE 2.31 Mixed-signal model specific updates in model release version 3.2

v3.2 update	Devices	Reason	Impact on user
Noimod changed from 2 to 1	All 1.8V and 3.3V FETs	Better off-state prediction of RF thermal noise	Reduced (1/10 - 1/200x) noise for $V_g \sim 0V$. 10-20% change in the on-state ($V_g > V_t$)
Added parameter hdiff	All 1.8V and 3.3V FETs	Allows approximate calculation of as, ad, ps, pd (area and perimeter of source and drain) when primitive model (e.g. NFET) is used directly	No impact if as, ad, ps, pd are specified by user or if sub-circuit wrappers around primitives (NFETs, PFETs, ...) are used
Added ACM=12, CAP-CALCM=1 in HSPICE and ADS	All 1.8V and 3.3V FETs	Junction capacitance calculations are now compatible across simulators (Spectre, Hspice, ADS)	Increased junction capacitance for Hspice and ADS simulations in v3.2 (over v3.1)

2.9.1 v3.4

TABLE 2.32 Mixed-signal model specific updates in model release version 3.4

v3.4 update	Devices	Reason	Impact on user
Corner/Statistical model oxide thicknesses	All 1.8V and 3.3V FETs	Updated to match new E-spec. w/ tighter variation	No change in NOMINAL model. Reduced corner/statistical model variation in gate oxide capacitance: 1.8V FETs corner model: v3.3a +/- 1Å; v3.4 +/- 1Å 1.8V FETs stat. model: v3.3a +/- 3Å; v3.4 +/- 1.5Å 3.3V FETs corner model: v3.3a +/- 2Å; v3.4 +/- 1.8Å 3.3V FETs stat. model: v3.3a +/- 6Å; v3.4 +/- 3Å
Corner and stat. parameters added to model process variation on drain/source series resistance	All 1.8V and 3.3V FETs	More physical corner and statistical models	No change in NOMINAL model. Larger gm variation in corner and statistical models for short channel FETs
Corner and stat. parameters added to model process variation on gate-source and gate-drain overlap capacitances	All 1.8V and 3.3V FETs	Corner and statistical models for overlap capacitance in v3.2 did not capture oxide thickness and ΔL variation	No change in NOMINAL model. Larger gate-source and gate-drain overlap capacitance variation in corner and statistical models
Statistical correlation added to FASTSLOW and SLOW-FAST corners	All 1.8V and 3.3V FETs	Improved modeling of N and PFET correlation due to process variations	Reduced oxide thickness, ΔL , and ΔW variation when simulating with the FASTSLOW and SLOW-FAST corners

2.9.2 v3.7

TABLE 2.33 Mixed-signal model specific updates in model release version 3.7

v3.7 update	Devices	Reason	Impact on user
Reduced Idsat in narrow devices	1.8V n and pfet	PCM data running at SLOW corner	15-35% reduction in Idsat of narrow width ($W \sim 0.22\mu m$) devices.
Flicker noise model changed from gm-based to BSIM3	1.8V n and pfet 3.3V5V n and pfet	Improved modeling of bias dependent flicker noise	Reduced flicker noise at lower gate biases ($\sim V_t$) for most cases
Added new BSIM3 mixed-signal models for 5V native NFETs	5V FETs		
Add "multiplicity" to mismatch model	All FETs	Mismatch should improve with multiple devices	Correct modeling of transistor mismatch for $m > 1$

2.9.3 v4.0

TABLE 2.34 Mixed-signal model specific updates in model release version 4.0

v4.0 update	Devices	Reason	Impact on user
Added x-sigma support	1.8V3.3V and 3.3V FETs 3.3V Native FETs 5V FETs 5V Native FETs	Add capability to design to process corners other than +/- 3-sigma Isolate device causing failures in FAST/SLOW corner simulations	

2.9.4 v4.1

TABLE 2.35 RF FET model specific updates in model release version 4.1

v4.0 update	Devices	Reason	Impact on user
Flicker noise	3.3V PFET	New data on L=0.3 μ m device	Simulated flicker noise is now 2-3x higher for biases close to Vt

2.10 References

1. BSIM3 Modeling Package, Agilent 85194E, "http://www.admos.de/uploads/media/bsim3_datasheet_02.pdf"
2. T. Gneiting, "A Unified Environment for the Modeling of Ultra Deep Submicron MOS Transistors," Nanotech 2003 Conference
3. Colin C. McAndrew, "Statistical Circuit Modeling," SISPAD 98

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3.0 RF CMOS Model

3.1 Model List and Description

The CA18 process supports two different RF models. The first model relates to the thin gate-oxide FETs with a maximum operation voltage of 1.8v. The second model relates to the thick gate-oxide FETs with a maximum operation voltage of 3.3V.

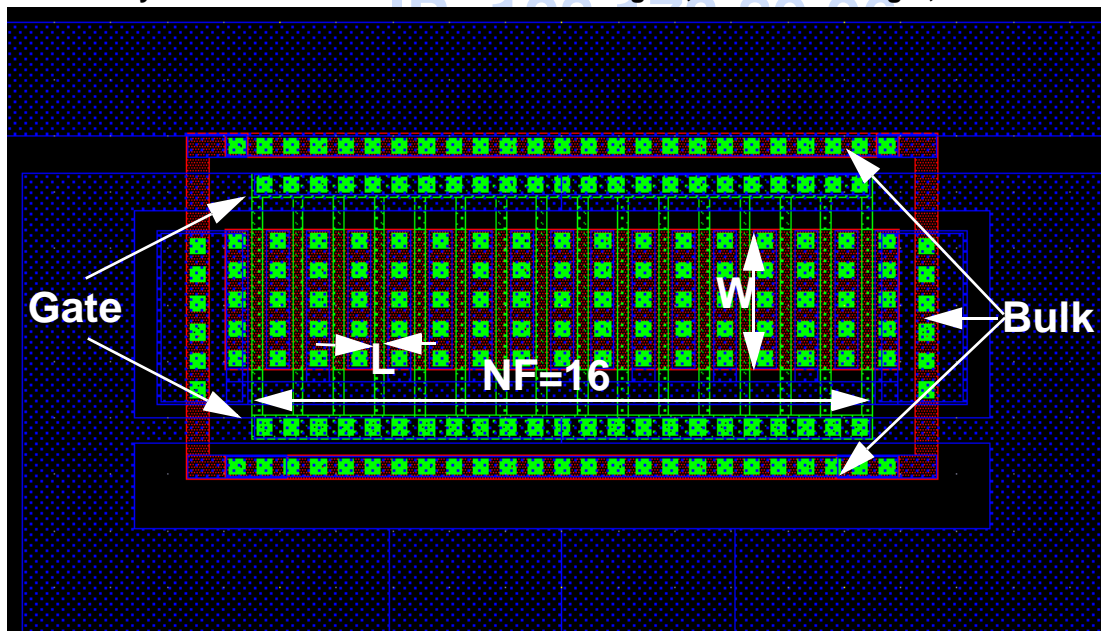
TABLE 3.1 Fet model summary for 1.8 and 3.3v FETs

Property	1.8v RF FETs	3.3v RF FETs
Model name	NFET_rf, PFET_rf	NFET3p3_rf, PFET3p3_rf
Temperature Range	25°C	25°C
Channel Length	$0.18\mu\text{m} \leq L \leq 0.5\mu\text{m}$	$0.36\mu\text{m} \leq L \leq 0.5\mu\text{m}$ NFET $0.3\mu\text{m} \leq L \leq 0.5\mu\text{m}$ PFET
Channel Width	$2\mu\text{m} \leq W \leq 10\mu\text{m}$	$2\mu\text{m} \leq W \leq 10\mu\text{m}$
No. of fingers	$1 \leq \text{NF} \leq 100$	$1 \leq \text{NF} \leq 100$
Bias Range	$ V_{gs} : 0 \sim 1.8\text{V}, V_{ds} : 0 \sim 1.8\text{V}, V_{bs} : 0 \sim 1.8\text{V}$	$ V_{gs} : 0 \sim 3.3\text{V}, V_{ds} : 0 \sim 3.3\text{V}, V_{bs} : 0 \sim 3\text{V}$

Using these models outside of the specified ranges may generate simulation errors. The RF model is based on the core MS model which has been validated over for temperatures valid from -40 to 125°C. Though no RF model validation is performed at temperatures other than 25°C, the RF model should provide a reasonable estimate of RF properties when simulated at temperatures in -40 to 125°C range.

3.2 Layout

FIGURE 3.1 Layout of RF MOSFET. NF= number of fingers, L= channel length, W = channel width



The top view of a RF MOSFET is shown in Figure 3.1 with the key design parameters (NF, L, and W). Note that the total width of the RF MOSFETs is equal to NF*W. RF transistors are typically laid out as multi-finger devices to minimize gate resistance and parasitic junction effects. These improvements translate into higher cutoff (f_t) and maximum oscillation frequencies (f_{max}), as well as lower device noise. The gate resistance R_g can further be improved by contacting the gate on multiple sides as per Eq. 1.

$$R_g = W \cdot \frac{R_{polySheet}}{NF \cdot 3 \cdot L \cdot N_{gc}^2} + \frac{\rho_c}{NF \cdot W \cdot L} \quad (EQ 1)$$

where $R_{polySheet}$ is the salicided poly sheet resistance, N_{gc} is the number of sides that the gate is contacted from, and ρ_c is the contact resistance per unit area between the salicide and the polysilicon gate, and represents an additional component of the gate resistance, dominant for narrow widths ($< 3\mu m$). The factor 3 is due to the distributed nature of this resistance at high frequencies. The p-cell N_{gc} defaults to a value of 1, consistent with the default “top-sided” gate connection. The user can, however, choose a double-sided gate contact by checking the “Both” option under the “**Gate Connection**” cdf variable, as shown in Figure 3.2. The reduced gate resistance might be useful in applications where a large f_{max} or low gate noise is desirable. The various components of the gate resistance in a RF FET are shown in Figure 3.3. The interconnect (metal wiring to the intrinsic FET) resistance is not shown in Figure 3.3. This can be an important component of the gate resistance, and should be included in the post-extraction simulation of the FETs.

Like the gate resistance, the substrate resistance is also layout dependent. The default model for both the 1.8v and 3.3v RF FETs is for a ring of substrate contacts around the active FET, and corresponds to the “**Detached**” Bodytie Type with “lbrt” Tap Style (Left, Right, Top, and Bottom), as shown in Figure 3.2. The 2-sided substrate model is also available corresponding to the “**Detached**” Bodytie Type and “lr” Tap Style (Left and Right). The use of a ringed substrate can significantly reduce the “roll-up” in drain-source conductance g_{ds} (or reduction of output resistance r_o) at high frequencies (Figure 3.4). One-sided contacts or two-sided contacts on the top and bottom are not supported in the model or in the p-cell schematic and layout.

FIGURE 3.2 CDF selection options for RF FETs

Gate Connection
☐ None ☒ Top ☐ Bottom ☐ Both ☐ Alternate

Style
☐ unconnected ☐ 1met ☐ 2met ☒ 2met(RF)

Current
 0 A

Number of Slices
 1

Simulation parameters update

High Frequency Noise Option 0

S/D Metal Width
 340n M

use ABLB overplots
☐

Bodytie Type
 Detached

Tap Style
 lbrt

Gate connection (Ngc in Eq. 1):
 Top: Ngc = 1(Default)
 Bottom: Ngc = 1
 Both: Ngc = 2
 Alternate: Ngc = 1

High frequency noise option (1.8v RF NFET only) is turned off by default. Set to "1" to simulate excess high frequency noise (Section 3.8).

Bodytie Type: Only detached option available with Tap style either "lbrt" (4-sided "ringed") or "lr" (2-sided left and right)

FIGURE 3.3 Components of the gate resistance in a RF-FET

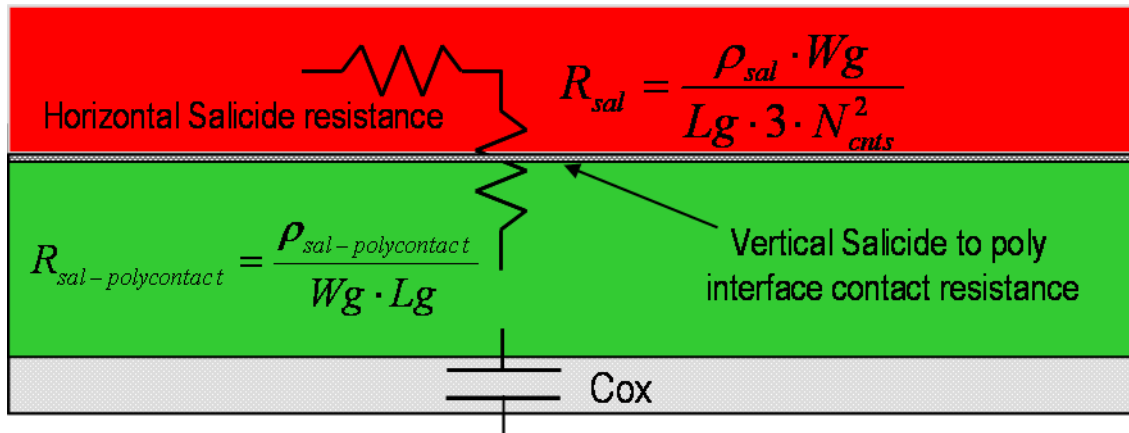
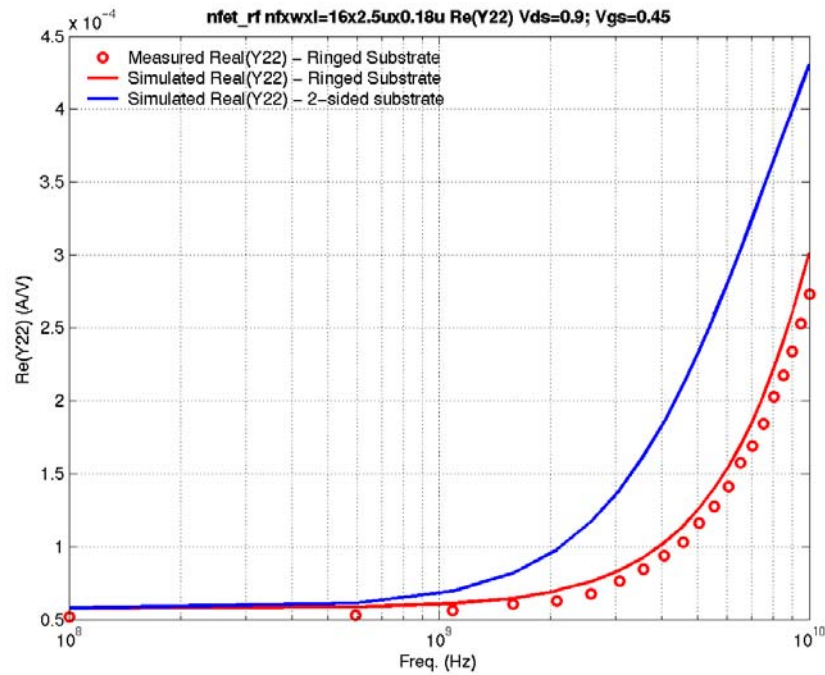


FIGURE 3.4 Impact of “ringed-substrate” on the output conductance



3.3 Measurements

Transistors with multiple widths, channel lengths and number of fingers were measured to extract a model that is scalable over the geometry space. Measurements were made on Ground-Signal-Ground test-structures with a 150 μ m pitch between the pads. The list of transistors measured for the thin and thick-oxide FETs is shown in Table 3.2 on page 138.

TABLE 3.2 List of devices measured for RF model extraction

Thin oxide (N and P FETs)			Thick oxide (N and P FETs)		
NF	W (μ m)	L (μ m)	NF	W (μ m)	L (μ m)
10	10	0.18, 0.22, 0.3, 0.38, 0.5	10	10	0.36, 0.42, 0.5, 0.6, 0.7
10	2.5	0.18	10	2.5	0.36
11,5,4,3,1	10	0.18	11,5,4,3,1	10	0.36
4,16,32,64*	2.5*	0.18, 0.22, 0.3, 0.8*	10	4	0.3 (PFET only)

*FETs have ringed substrate and double-sided gate contacts.

The s-parameters of the RF MOSFETs, were measured on HP 8510C network analyzer. The frequency was swept from 0.1 to 10GHz. The list of biases for the thin and thick-oxide FETs is shown in Table 3.3 on page 139.

TABLE 3.3 List of biases at which s-parameters were measured for the thin and thick-oxide FETs

Thin oxide		Thick oxide	
Vgs (V)	Vds (V)	Vgs (V)	Vds (V)
0	0,0.45,0.9,1.35,1.8	0	0,0.825,1.65,2.475,3.3
0.45	0,0.45,0.9,1.35,1.8	0.825	0,0.825,1.65,2.475,3.3
0.9	0,0.45,0.9,1.35,1.8	1.65	0,0.825,1.65,2.475,3.3
1.35	0,0.45,0.9,1.35,1.8	2.475	0,0.825,1.65,2.475,3.3
1.8	0,0.45,0.9,1.35,1.8	3.3	0,0.825,1.65,2.475,3.3

3.4 Modeling

The BSIM3v3 model described in the chapter “MOSFET Model” on page 19 is valid at low frequencies (< 200MHz). At higher frequencies, the coupling between the source and drain through the bulk and the distributed resistance and capacitance effects require the gate, substrate and source/drain coupling networks to be explicitly included. The core mixed-signal (MS) model can be extended for use at high frequencies by adding parasitic resistances and capacitances as shown in Figure 3.5. The gate resistance R_g is modeled via Eq. 1 and has a direct impact on the input admittance [1]:

$$Re(Y_{11}) \sim R_g \cdot Im(Y_{11})^2 \quad (\text{EQ 2})$$

where $Im(Y_{11}) \sim \omega \cdot C_{gate}$.

The substrate network includes 3 resistances in a T-network. R_{db} which models the drain-bulk coupling, and R_{sb} which models the source-bulk coupling are given by:

$$R_{sb} = R_{sbSheet} \times \frac{L}{(2 \times W \times NF)} \quad (\text{EQ 3})$$

$$R_{db} = R_{dbSheet} \times \frac{L}{(2 \times W \times NF)} \quad (\text{EQ 4})$$

where $R_{sbSheet} = R_{dbSheet}$, is the sheet resistance of the region that couples the ac signal from the source to the drain, and is fit to the measured data. The third resistor in the T-network represents the bulk resistance and is modeled by splitting it into 2 components given by Equations 5 and 6:

$$R_{dsbv} = R_{dsbSheet} \times \frac{(W/2 + W_{act2act} + W_{act2con})}{2 \times (L + 2 \times (W_{con2gate} + W_{con} + W_{act2con})) \times NF} \quad (\text{EQ 5})$$

where, R_{dsbv} is the vertical component of substrate resistance to the top and bottom taps, $R_{dsbSheet}$ is the sheet resistance of the well and is extracted from the measured s-parameter data, $W_{act2act}$ is the distance between the active regions of the FET and substrate contacts ($=1.59\mu\text{m}$), $W_{act2con}$ is the minimum design

rule for the active to contact ($=0.1\mu\text{m}$), $W_{con2gate}$ is the distance between contact and gate, and W_{con} is the width of the contact.

$$R_{dsbh} = R_{dsbSheet} \times \frac{(L/2 + W_{con2gate} + W_{con} + W_{act2con} + W_{sti} + W_{act2con})}{2 \times W} \quad (\text{EQ 6})$$

where R_{dsbh} is the horizontal component of the substrate resistance to the left and right taps, and W_{sti} is the width of the isolation. R_{dsbh} is calculated for the two outermost fingers of the RF FET, as the contribution from the inner fingers has negligible impact on this resistance for layouts with $NF > 4$. The substrate resistance of the RF FETs is either:

$$R_{dsb} = R_{dsbh} \quad (\text{EQ 7})$$

for a 2-sided substrate contact (corresponding to Tap Style “lr” in Figure 3.2), or

$$R_{dsb} = R_{dsbh} \parallel R_{dsbv} \quad (\text{EQ 8})$$

for a 4-sided “ringed” substrate contact (corresponding to Tap Style “lbrt” in Figure 3.2).

Collectively the substrate network (R_{sub}) impacts the output impedance:

$$R_{sub} \sim Re(Y_{22}) / (\omega^2 \cdot C_{db}) \quad (\text{EQ 9})$$

The transmission parameter from gate to drain:

$$Y_{12} \sim -j\omega C_{gd} - \omega^2 \cdot C_{gd} \cdot C_{gg} \cdot R_g \quad (\text{EQ 10})$$

where C_{gd} is the overlap capacitance extracted at low-frequency as described in Section 2.3.2 on page 25.

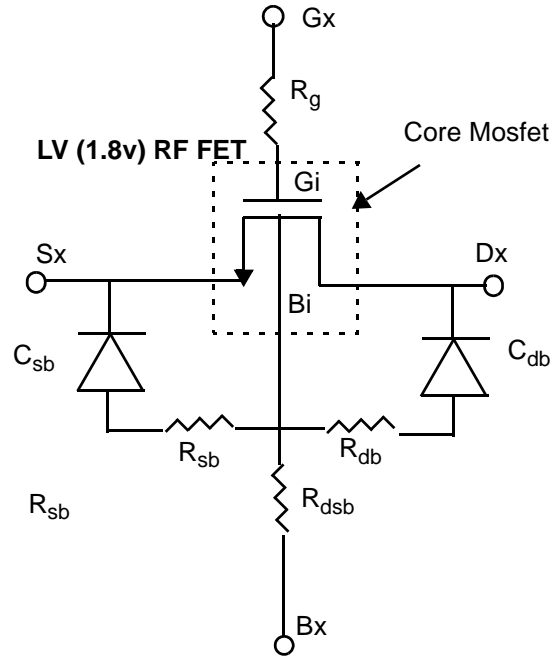
The drain resistance impacts the reverse transmission parameter from drain to gate:

$$Y_{21} \sim -j\omega C_{gd} - \omega^2 \cdot (C_{gd}^2 \cdot R_d + C_{gd} \cdot C_{gg} \cdot R_g) \quad (\text{EQ 11})$$

The drain and source resistances and their associated gate-bias dependencies are included in the core MS model and are not explicitly modeled in the sub-circuit. Modeling these resistors as extrinsic lumped elements in the sub-circuit results in inaccurate predictions of g_m and g_{ds} ; essential in both ac and noise simulations.

The area (C_j) and perimeter components (C_{jsw} , C_{jswg}) of the junction capacitance are pulled out (i.e. set to 0) from mixed-signal (DC) model and placed as external diodes in the sub-circuit (C_{db} , C_{sb}) to model the capacitive coupling of the drain-bulk and source-bulk junctions.

FIGURE 3.5 Illustration of the Sub-circuit of the 1.8v and 3.3v RF NFET model



3.5 Statistical and Corner Models

The core MS corner and statistical model parameters in the RF sub-circuit extension are identical to what was described in Section 2.5.2 on page 102 and Section 2.5 on page 101 respectively, and are valid at higher frequencies. In addition, the sheet resistance of the salicided poly and the contact resistivity of the salicide-polysilicon interface is changed by $\pm 24\%$ for the SLOW/FAST corner cases. Similarly, a $\pm 24\%$ variation is used to model the $3\text{-}\sigma$ variation of these parameter in the statistical models. The $3\text{-}\sigma$ variation of the salicided poly sheet resistance is consistent with E-specs specified for salicided poly resistors. The variation of the substrate resistance is modeled in a manner consistent with the channel doping variation in the statistical model.

3.6 Y-parameter playbacks

The simulated y-parameters and the cut-off frequency (f_t) of the various MOSFETs are compared with the measured data in Figures 3.6 through 3.28. The plots are for multiple biases which include the linear and saturation regimes. The device description is included in the figure caption using the notation:

max_operating_voltage_fetType_NFxWxL. Devices with 2 and 4-sided substrate contacts and with 1 or 2-sided gate contacts are shown.

Y-parameters are shown since they lend better meaning to the device performance than s-parameters.

FIGURE 3.6 1p8_NFET_16x2p5x0p18 (2-sided gate contact, 4-sided “ringed” substrate contact)

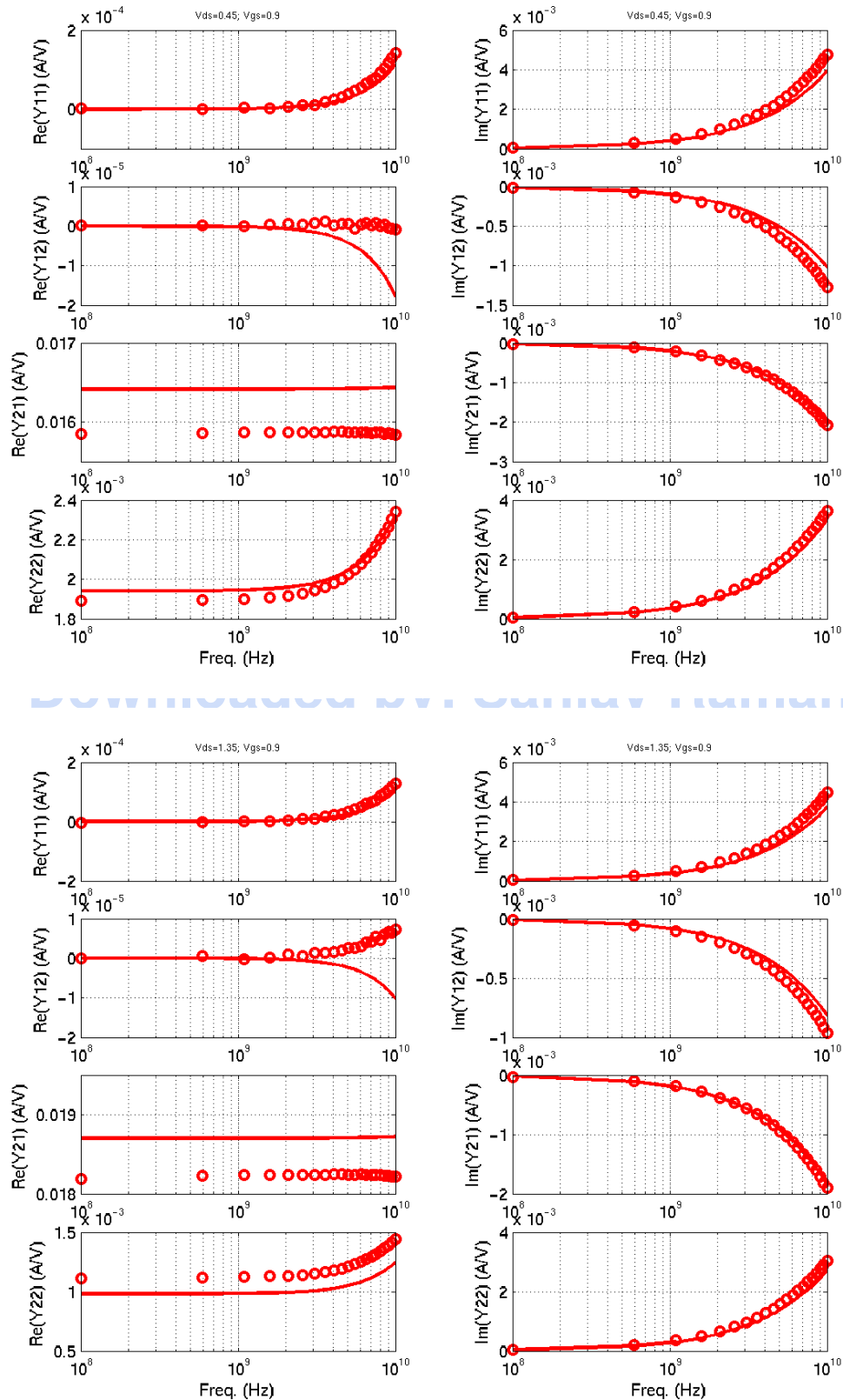


FIGURE 3.7 1p8_NFET_32x2p5x0p18 (2-sided gate contact, 4-sided “ringed” substrate contact)

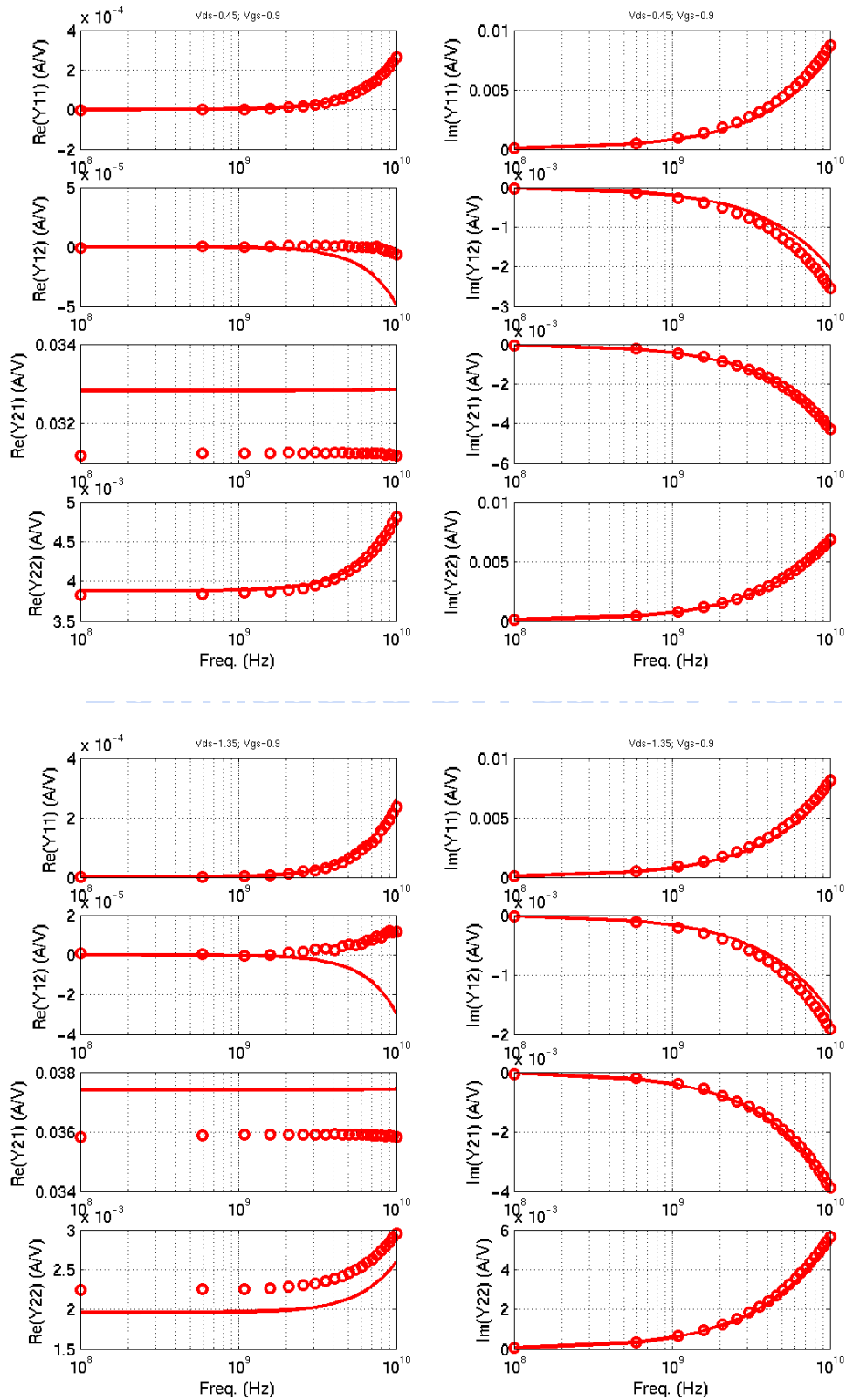


FIGURE 3.8 1p8_NFET_10x5x0p18 (1-sided gate contact, 2-sided substrate contact)

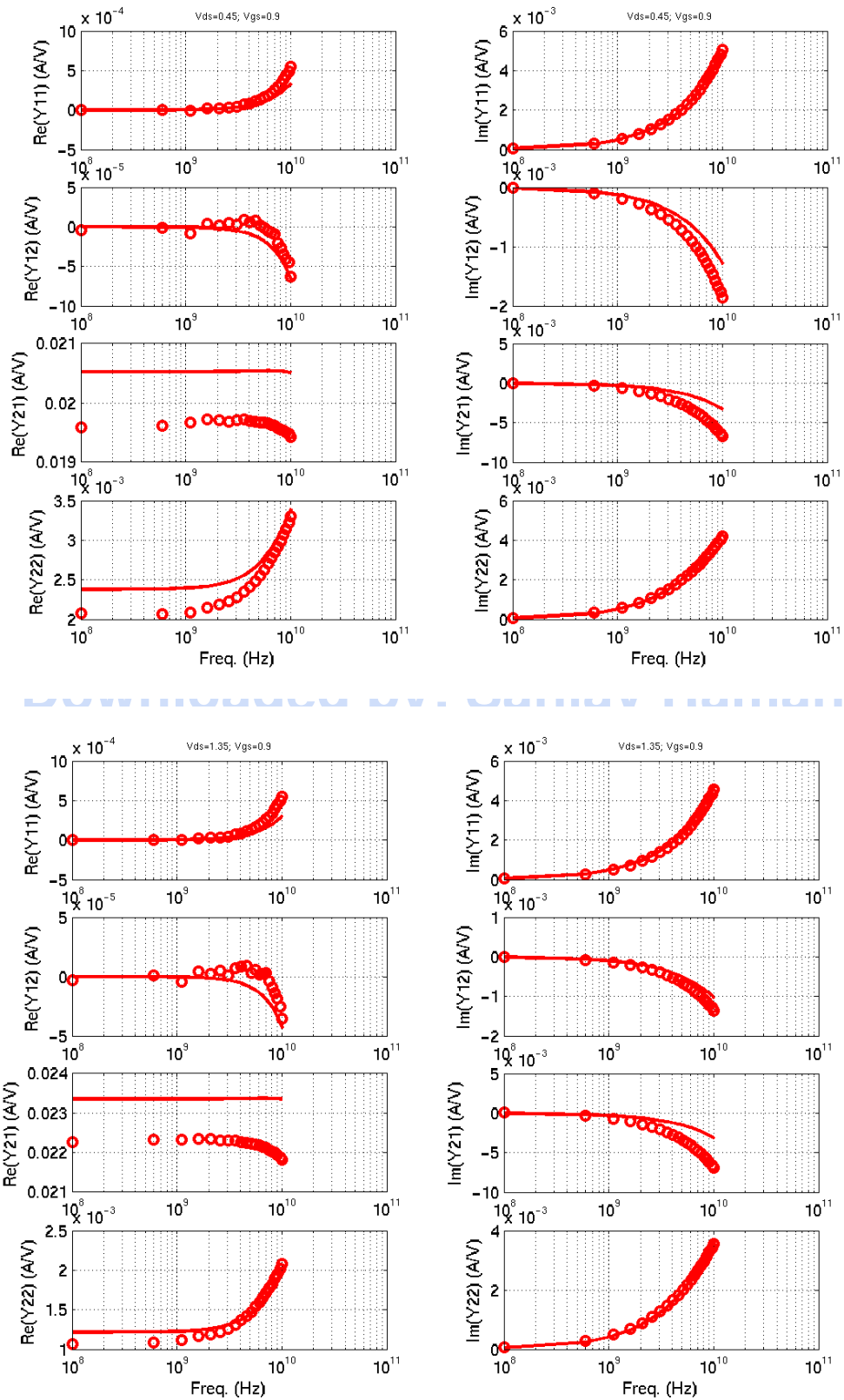


FIGURE 3.9 1p8_NFET_10x2x0p18 (1-sided gate contact, 2-sided substrate contact)

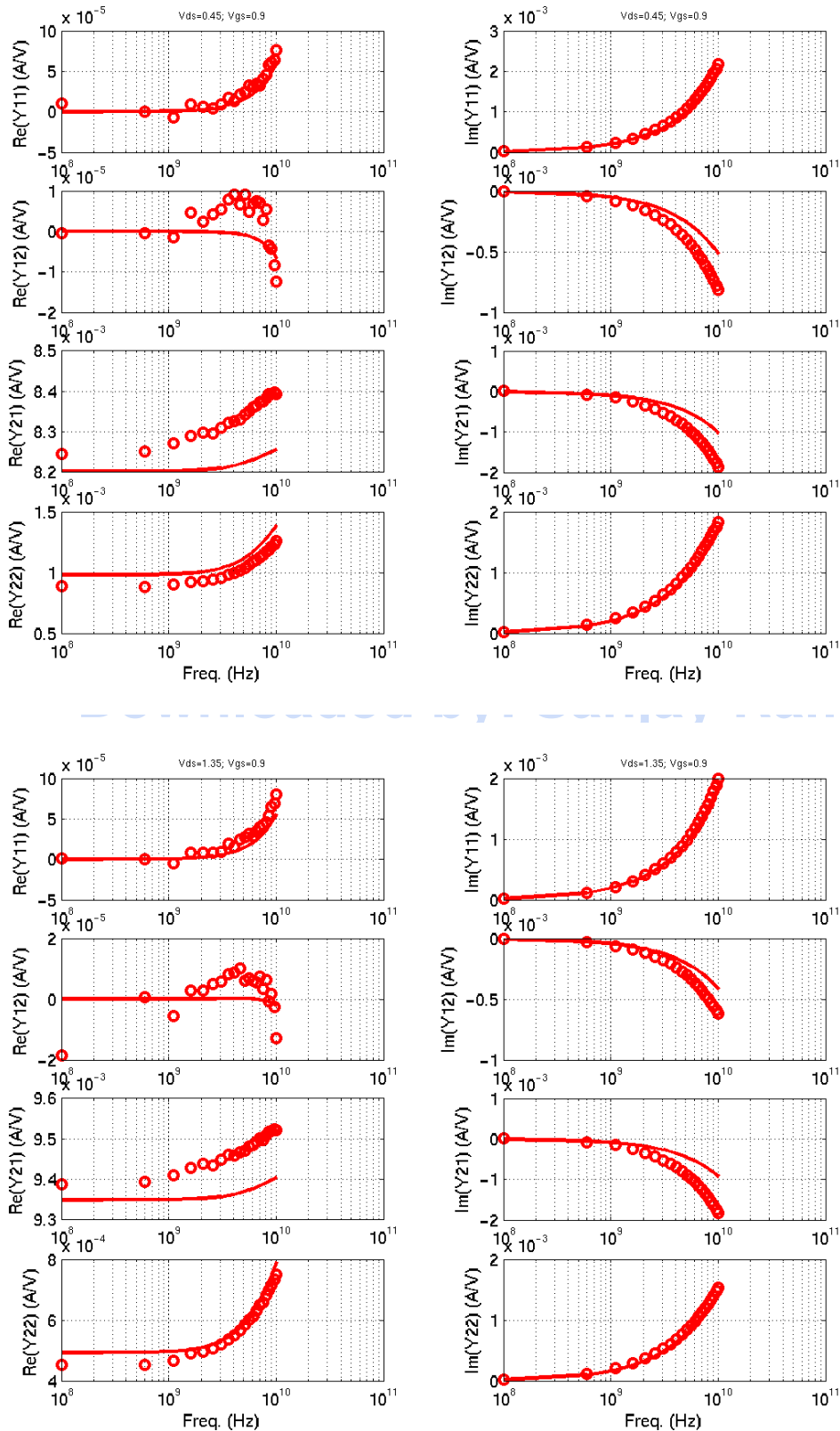


FIGURE 3.10 1p8_NFET_10x10x0p22 (1-sided gate contact, 2-sided substrate contact)

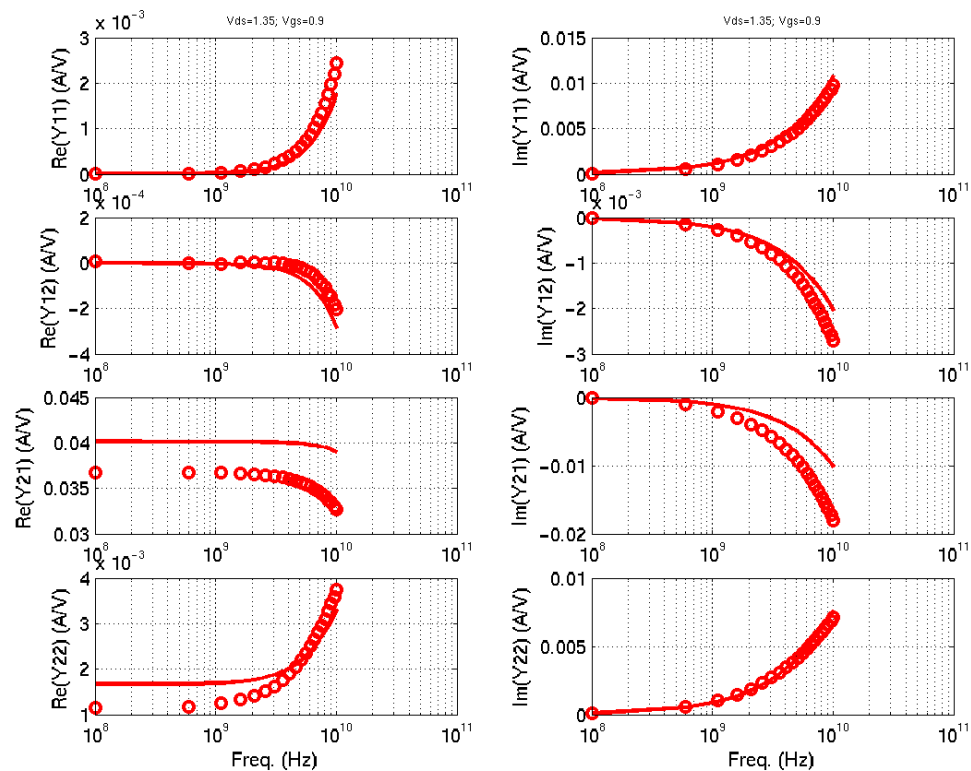
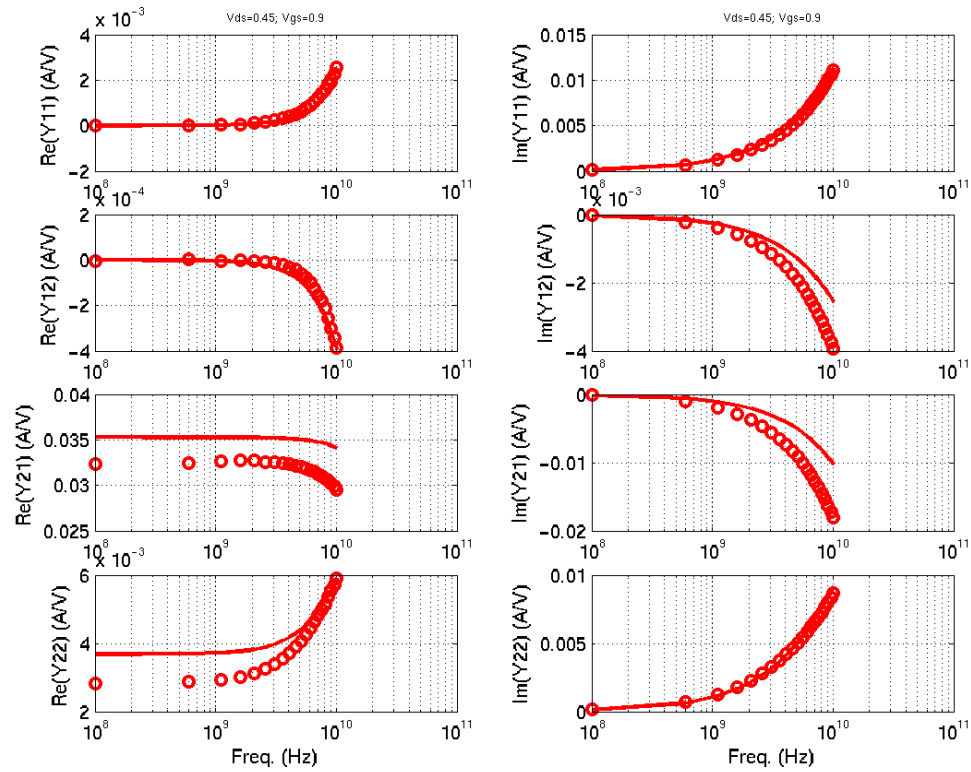


FIGURE 3.11 1p8_NFET_5x10x0p18 (1-sided gate contact, 2-sided substrate contact)

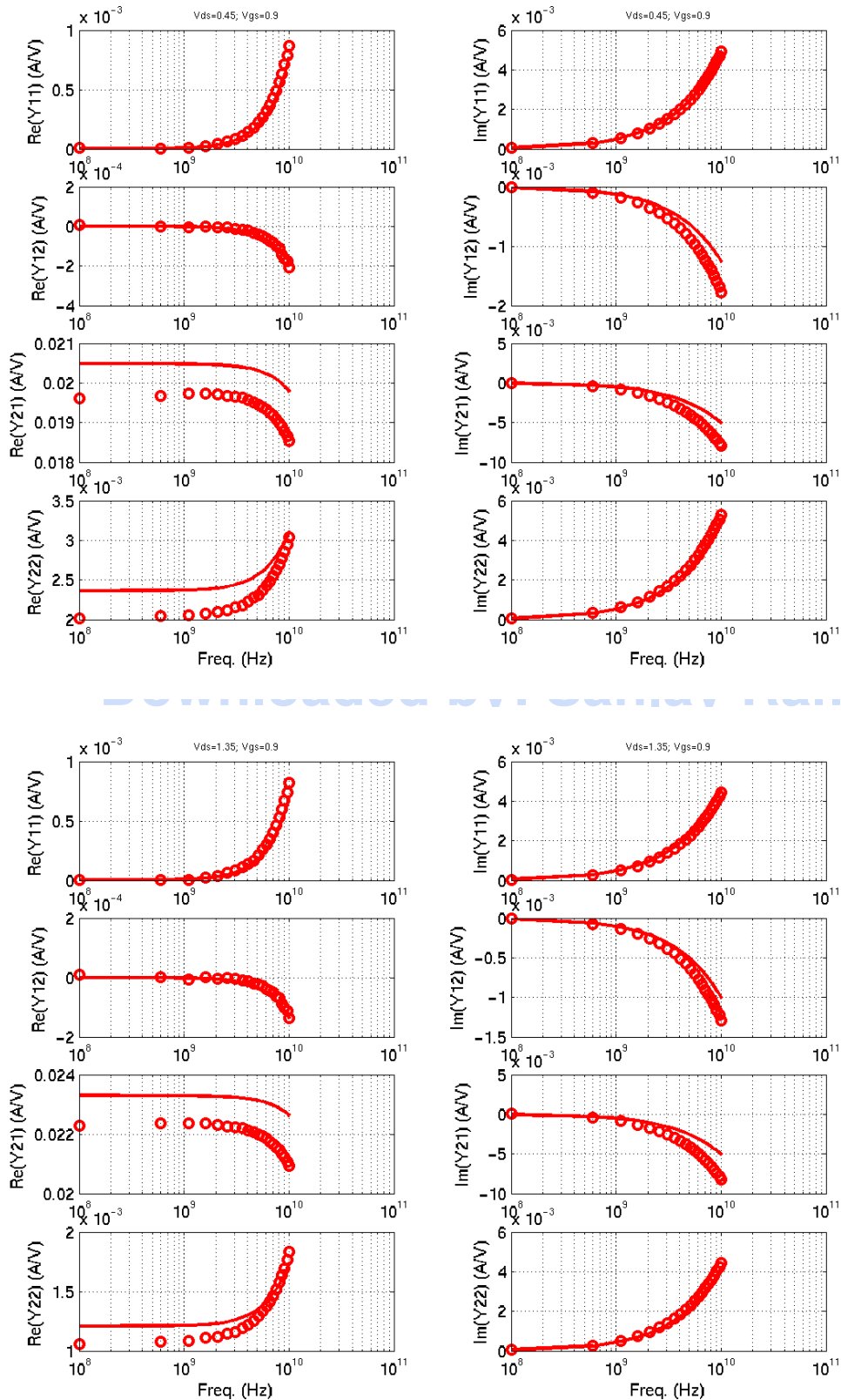
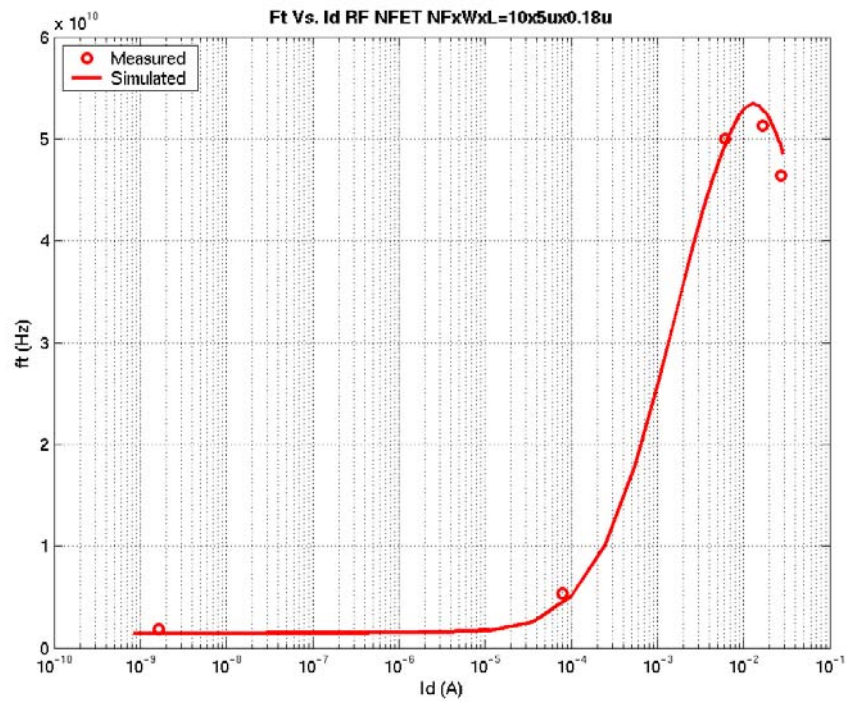


FIGURE 3.12 1p8_NFET_10x5x0p18_ftVsId_Vds_1.35v (Single gate contact, 2-sided sub.)



contact)1p8_PFET_10x5x0p18_ftVsId_Vds_-1.35 (1-sided gate contact, 2-sided sub. contact)

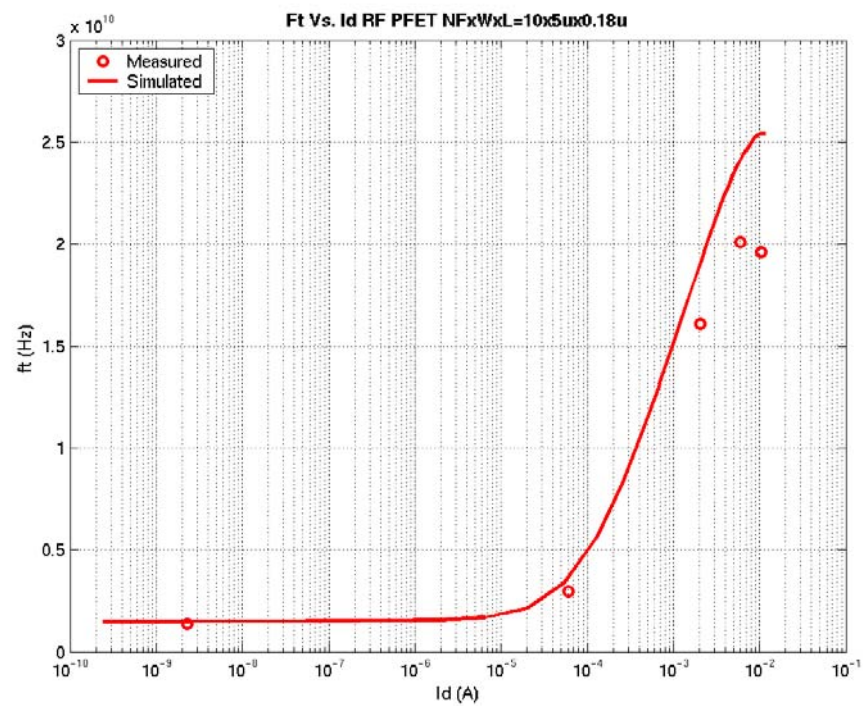


FIGURE 3.13 1p8_PFET_16x2p5x0p18 (2-sided gate contact, 4-sided “ringed” substrate contact)

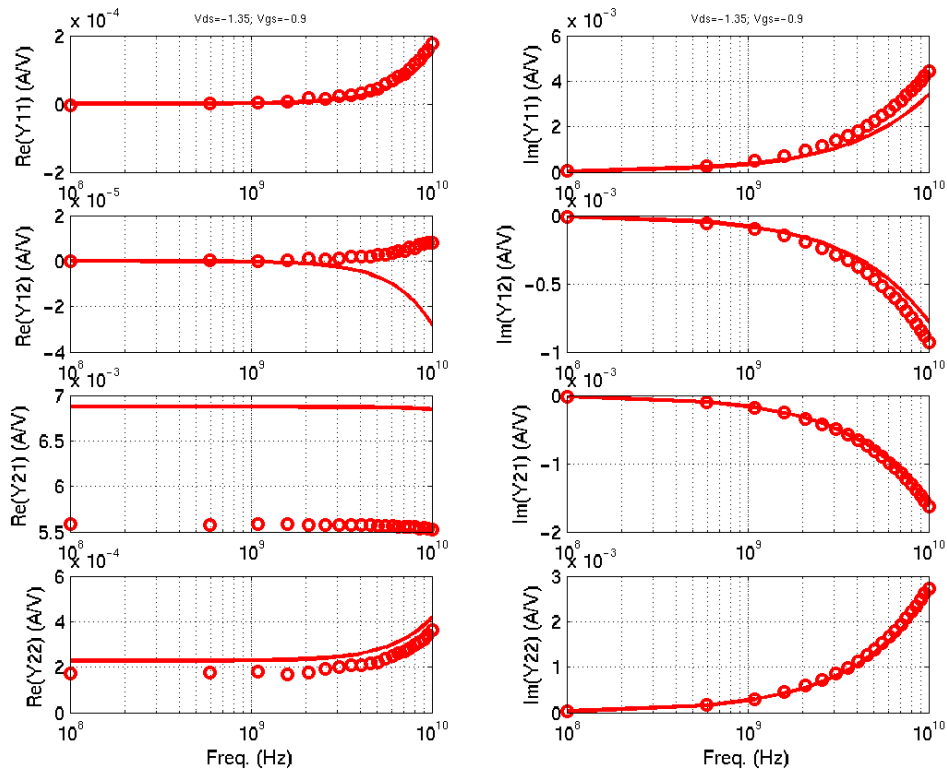
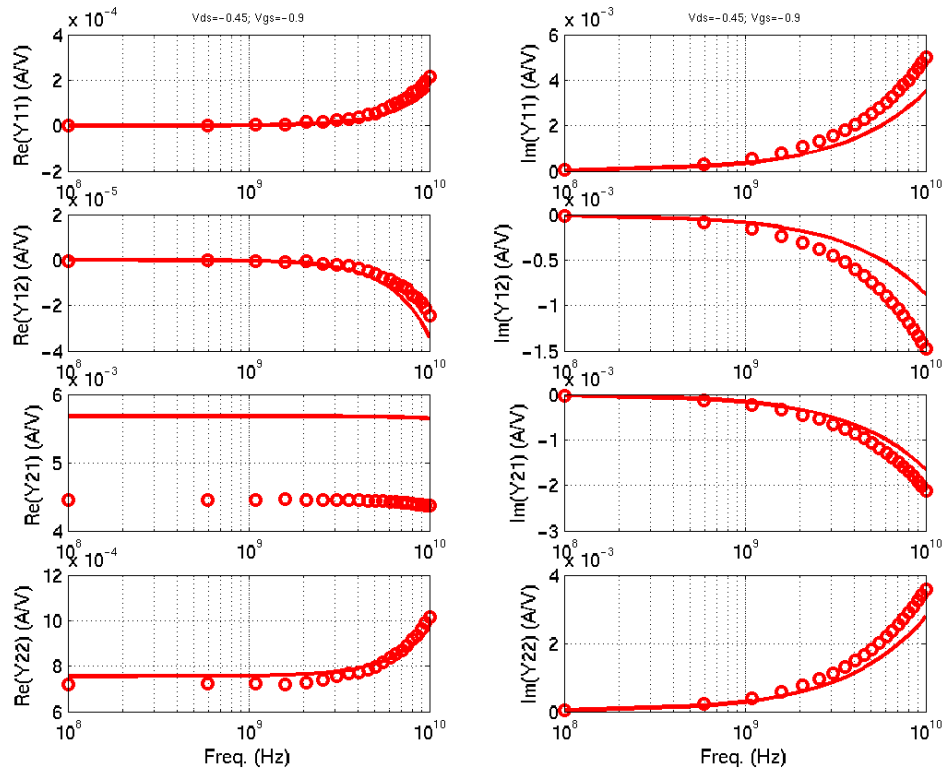


FIGURE 3.14 1p8_PFET_32x2p5x0p18 (2-sided gate contact, 4-sided “ringed” substrate contact)

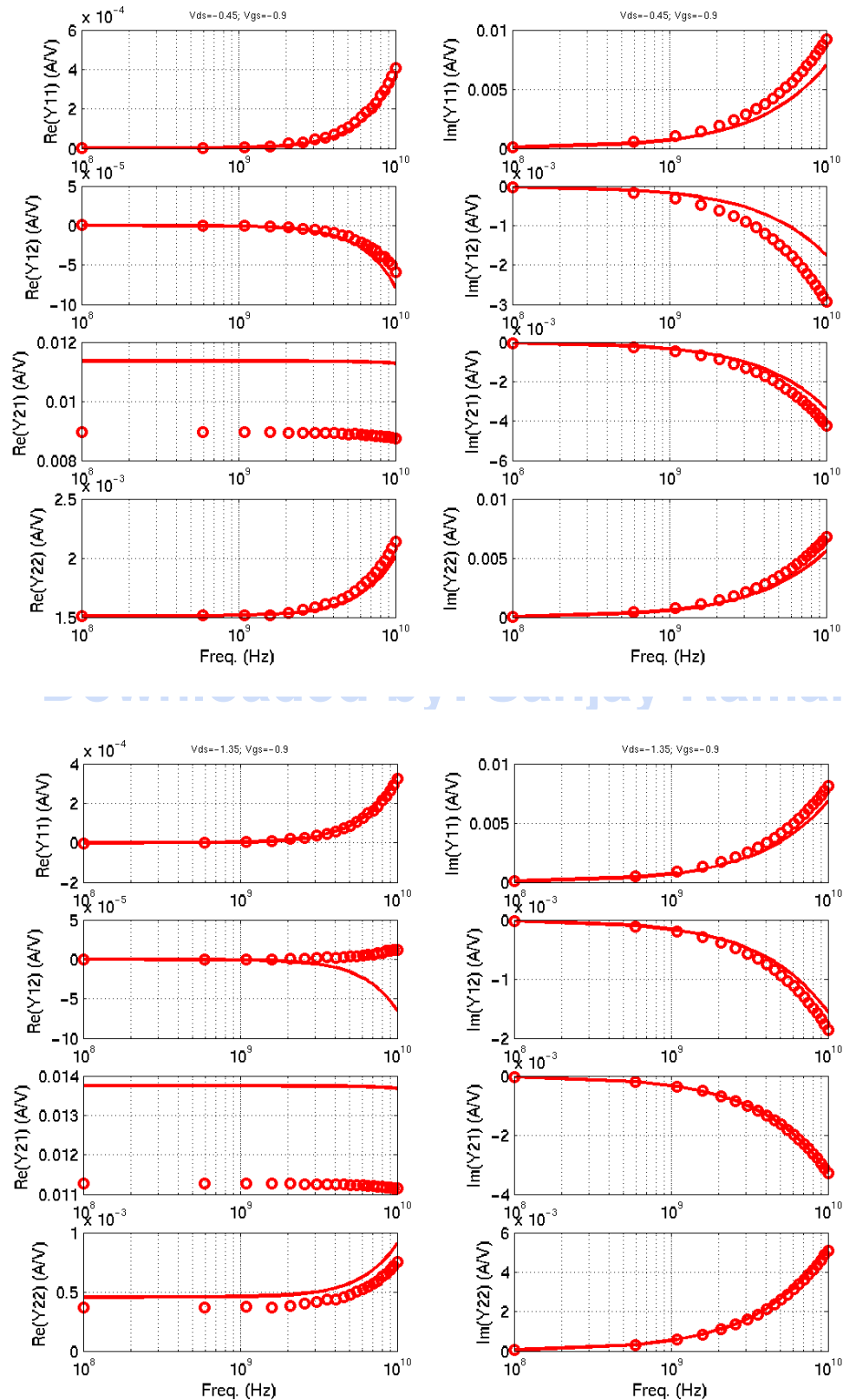


FIGURE 3.15 1p8_PFET_10x5x0p18 (1-sided gate contact, 2-sided substrate contact)

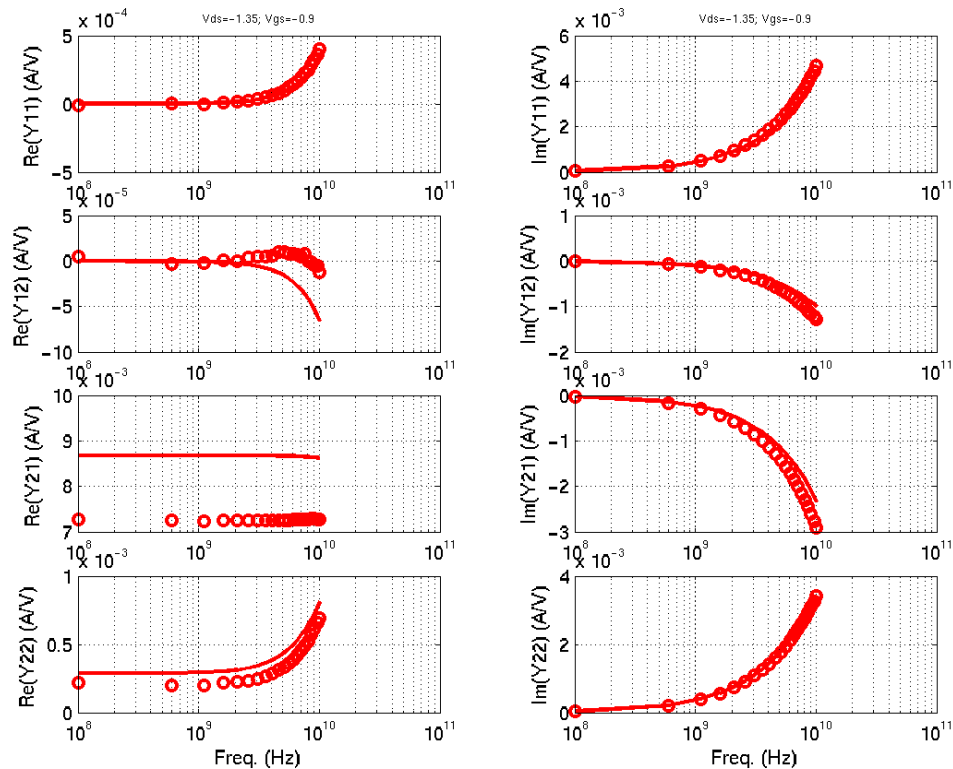
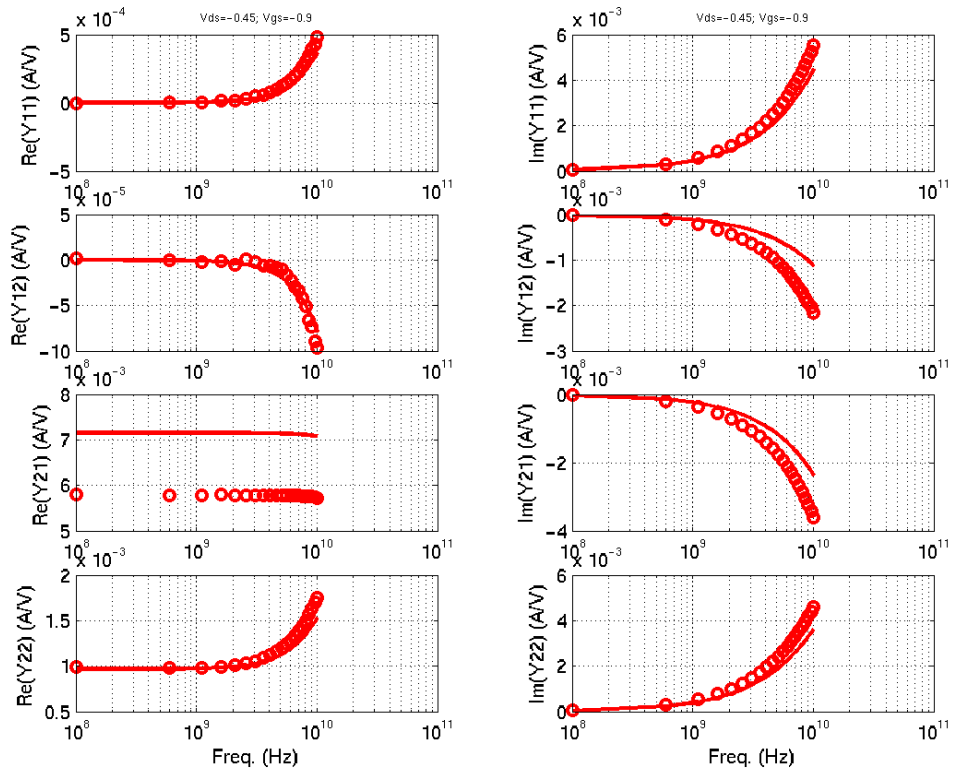
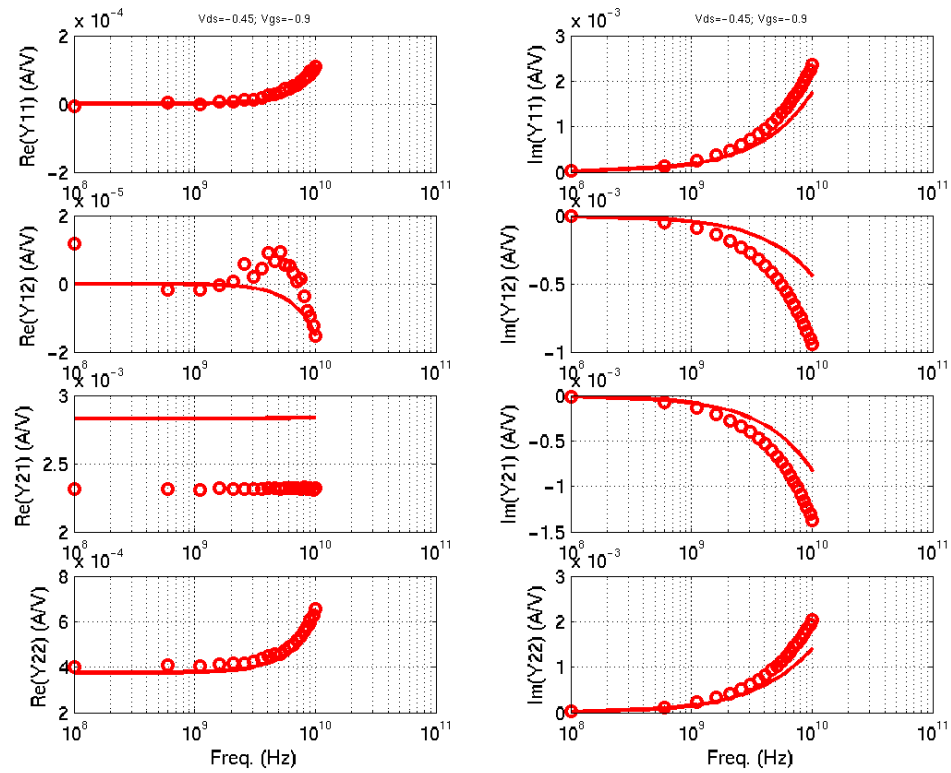


FIGURE 3.16 1p8_PFET_10x2x0p18 (1-sided gate contact, 2-sided substrate contact)



Downloaded by: Camilla Hattala

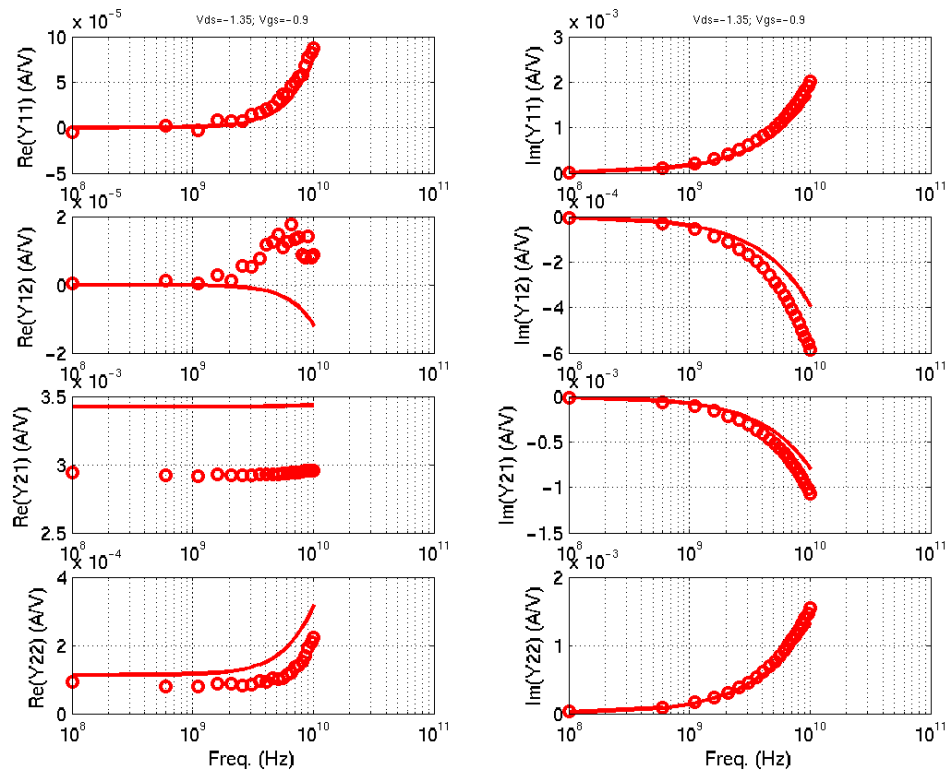


FIGURE 3.17 1p8_PFET_10x10x0p22 (1-sided gate contact, 2-sided substrate contact)

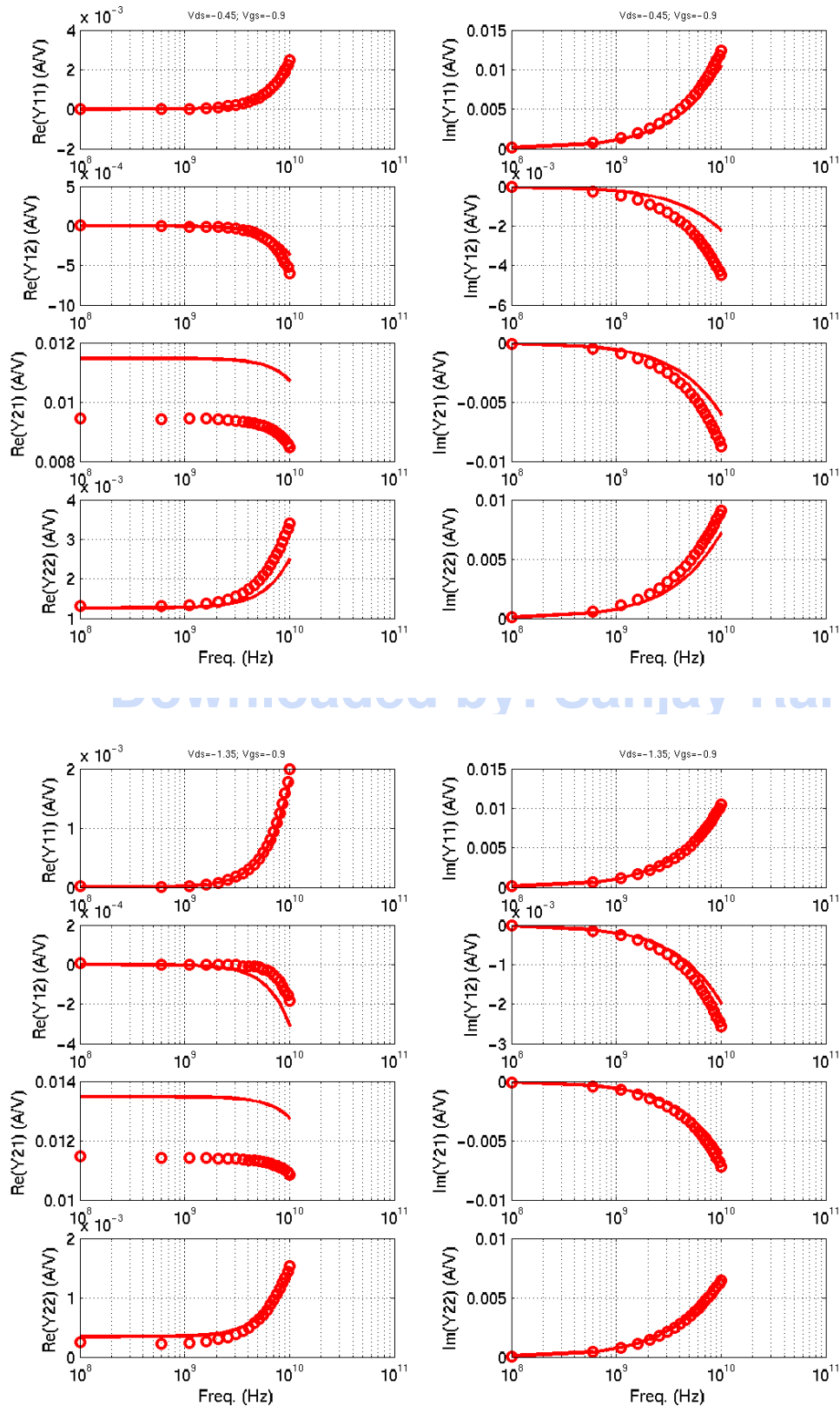


FIGURE 3.18 1p8_PFET_5x10x0p18 (1-sided gate contact, 2-sided substrate contact)

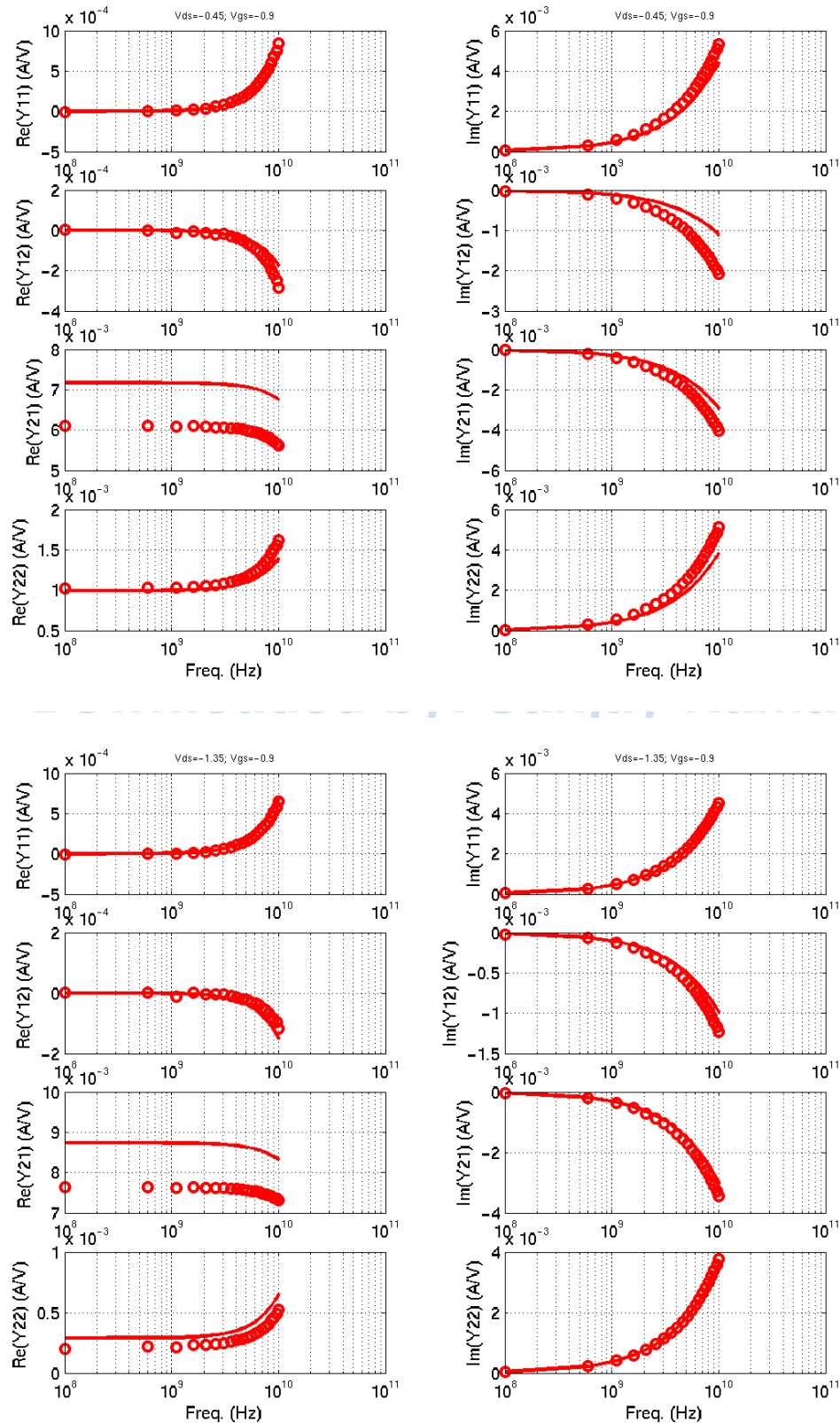


FIGURE 3.19 3p3_NFET_10x5x0p36 (1-sided gate contact, 2-sided substrate contact)

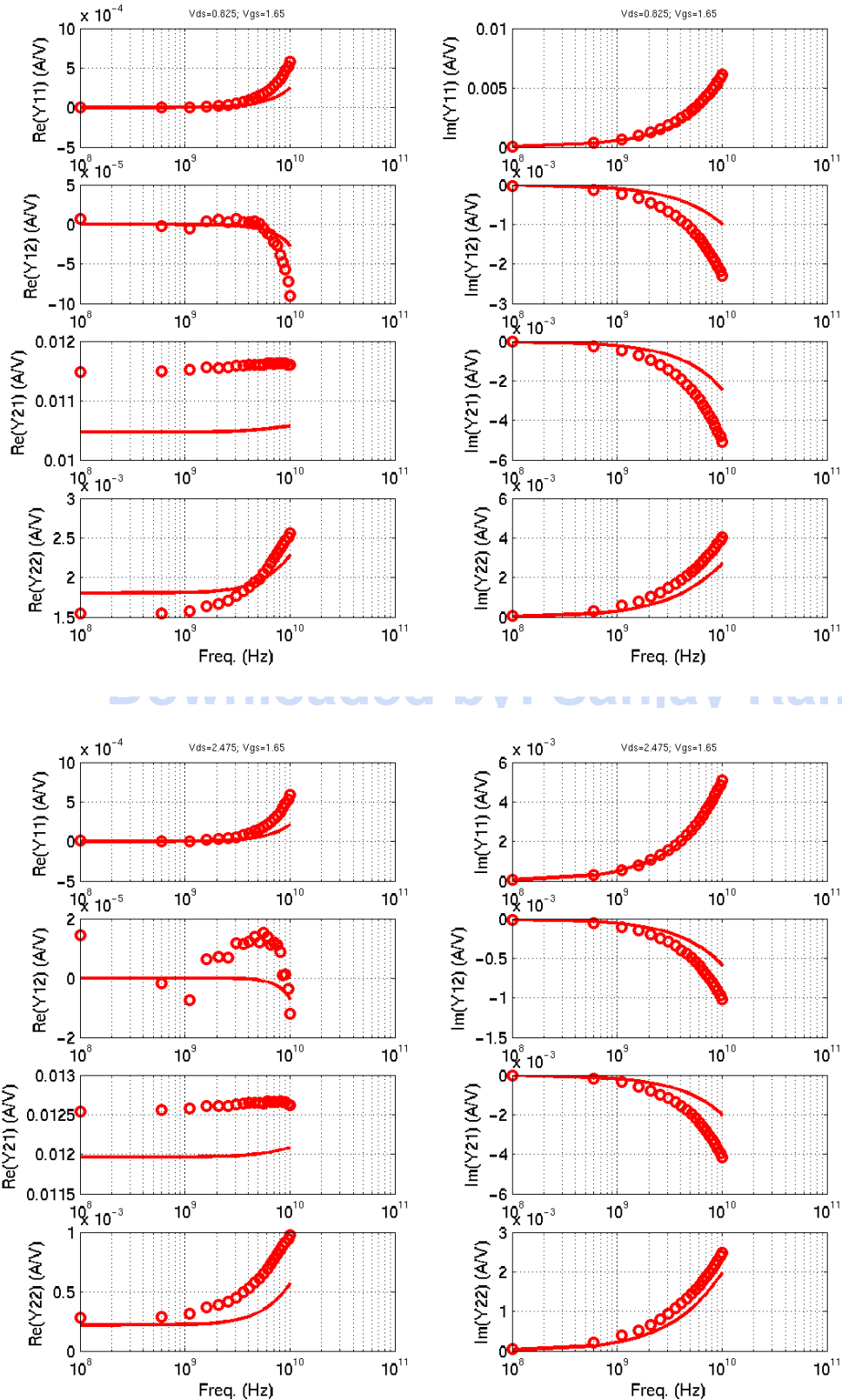


FIGURE 3.20 3p3_NFET_10x2x0p36 (1-sided gate contact, 2-sided substrate contact)

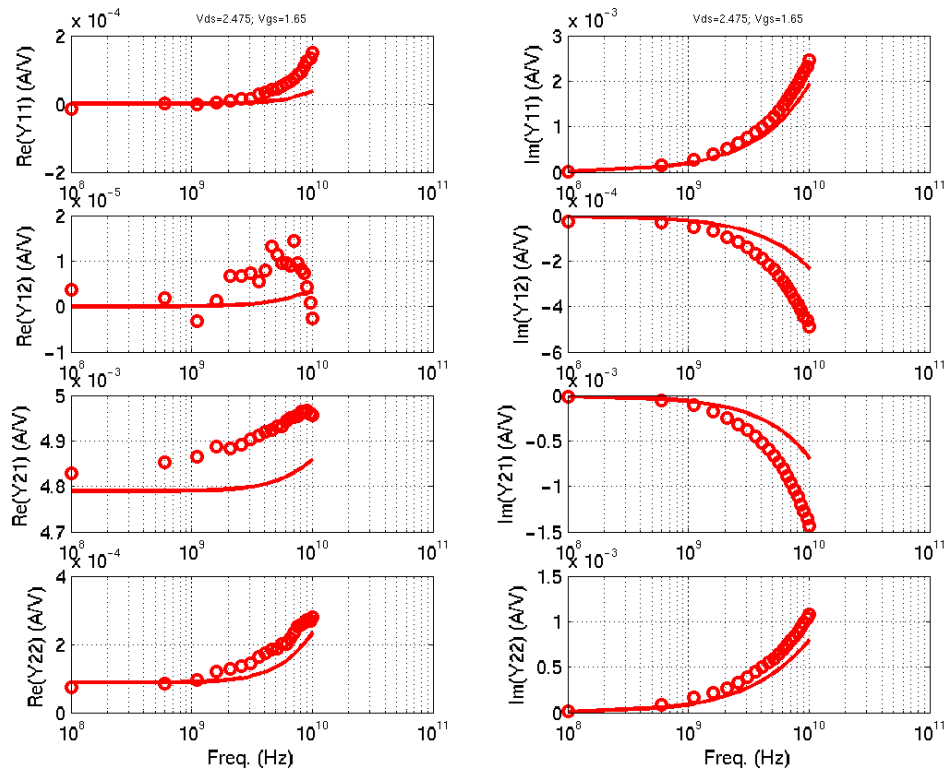
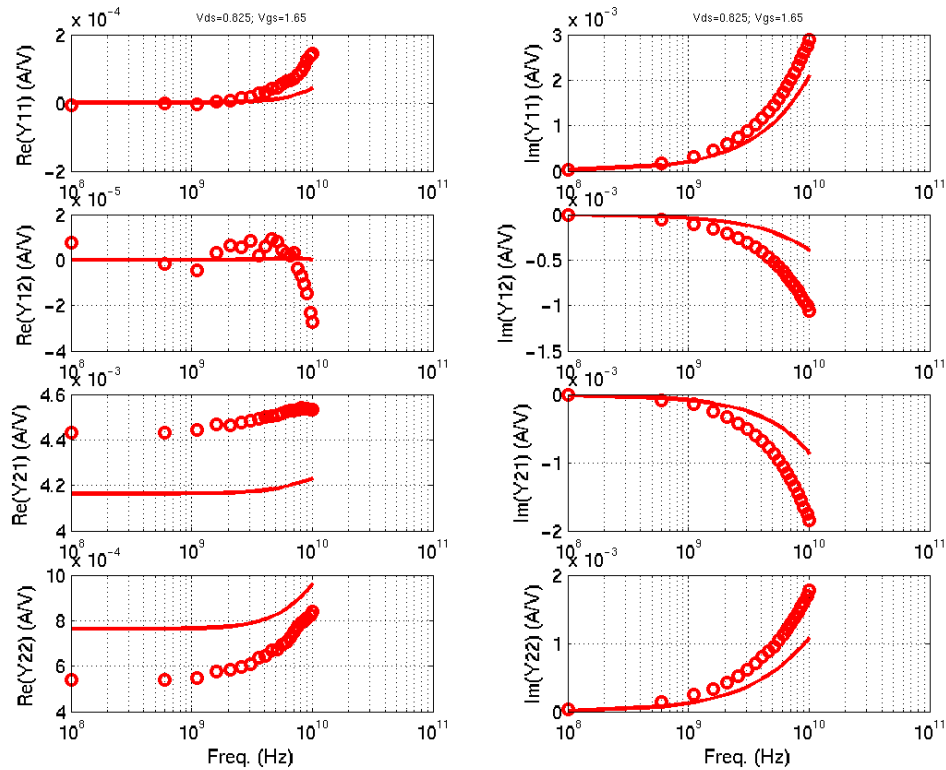


FIGURE 3.21 3p3_NFET_10x10x0p42 (1-sided gate contact, 2-sided substrate contact)

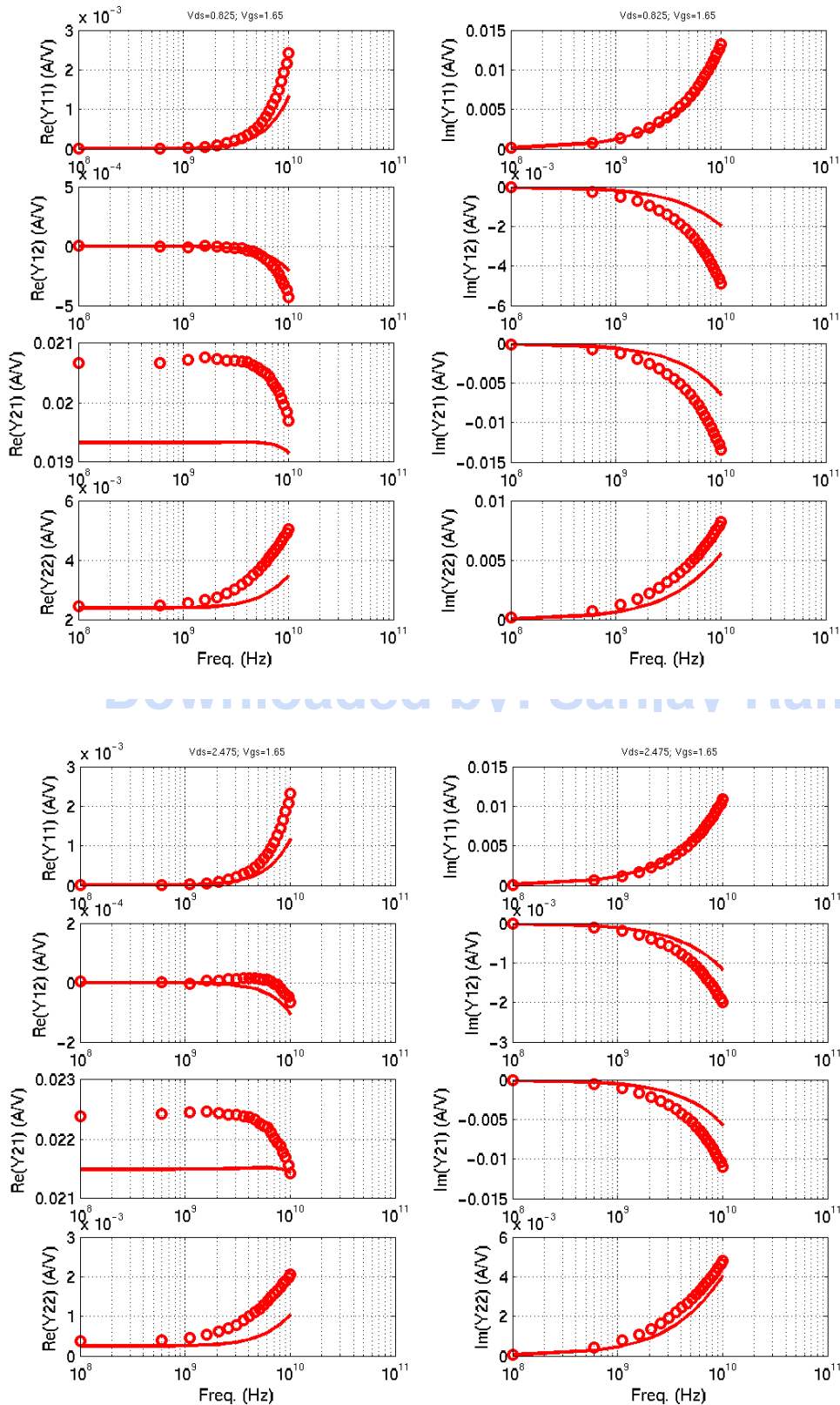


FIGURE 3.22 3p3_NFET_5x10x0p36 (1-sided gate contact, 2-sided substrate contact)

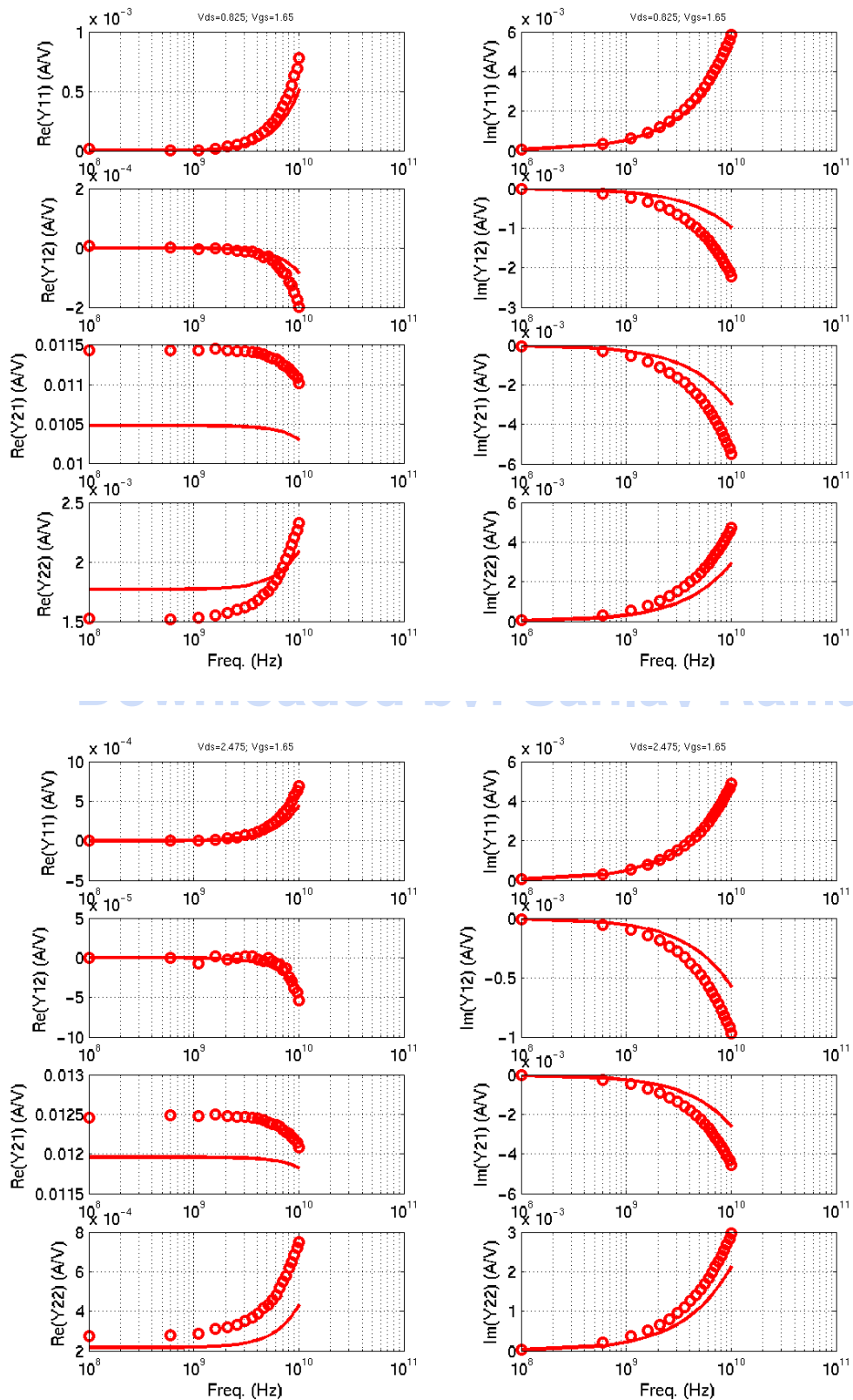


FIGURE 3.23 3p3_NFET_10x5x0p36_ftVsId_Vds_2.475 (1-sided gate contact, 2-sided sub. contact)

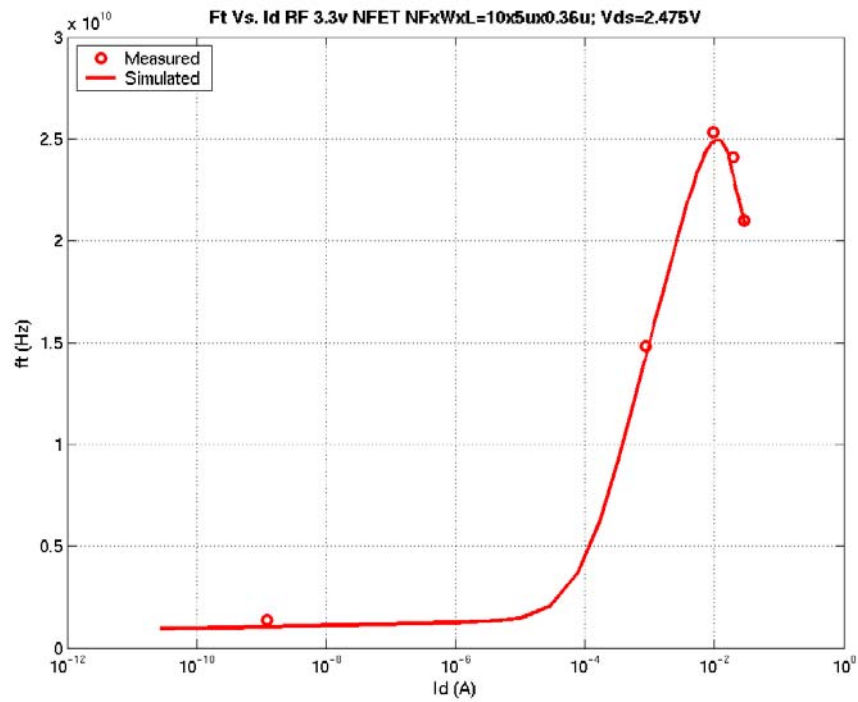


FIGURE 3.24 3p3_PFET_10x4x0p3_ftVsId_Vds_-2.475 (1-sided gate contact, 2-sided sub. contact)

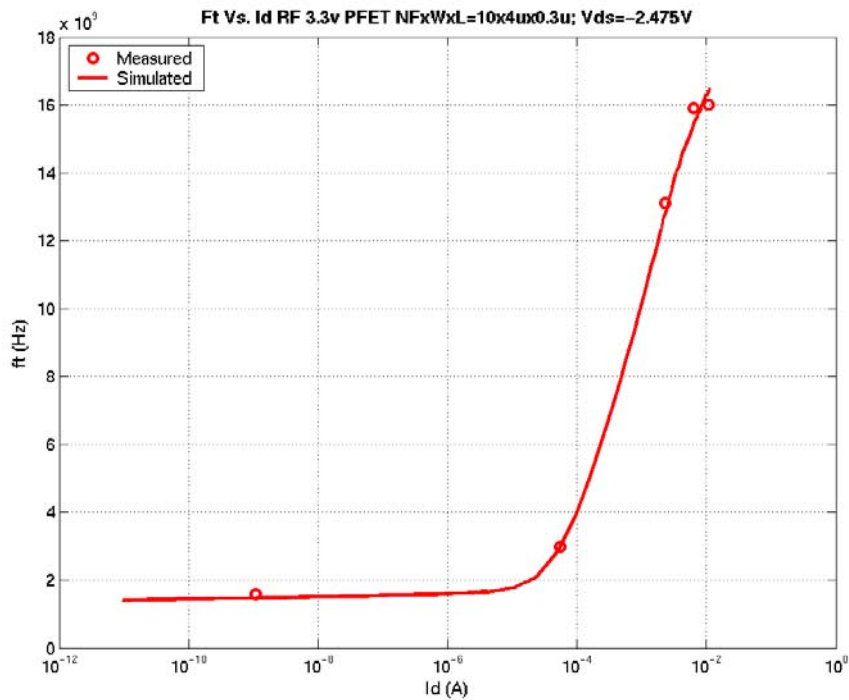


FIGURE 3.25 3p3_PFET_10x5x0p36 (1-sided gate contact, 2-sided substrate contact)

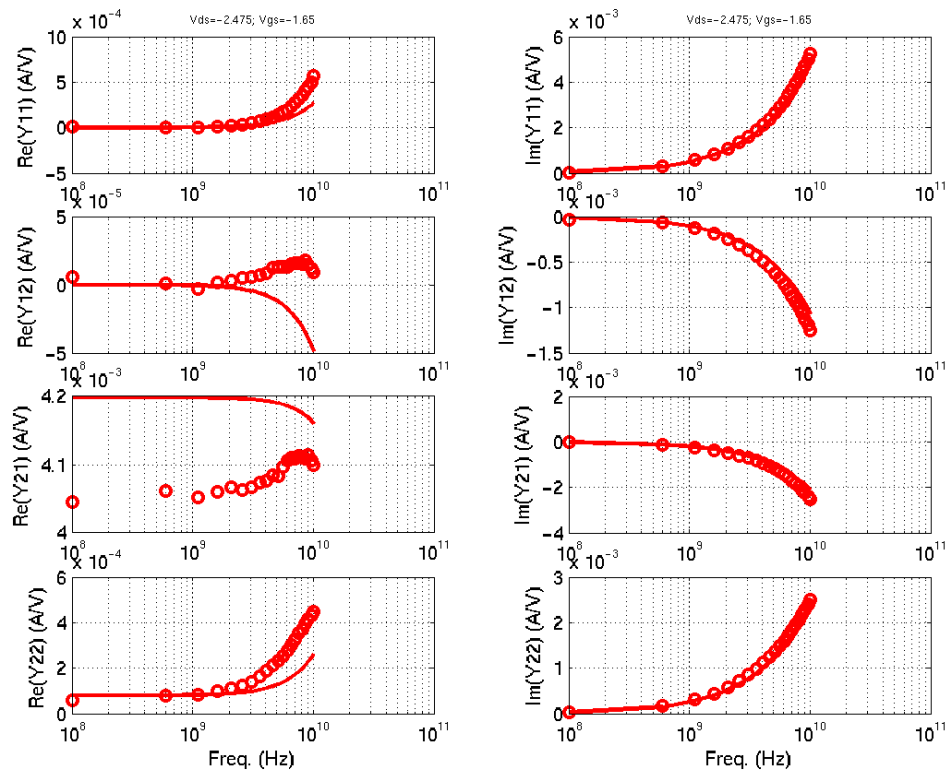
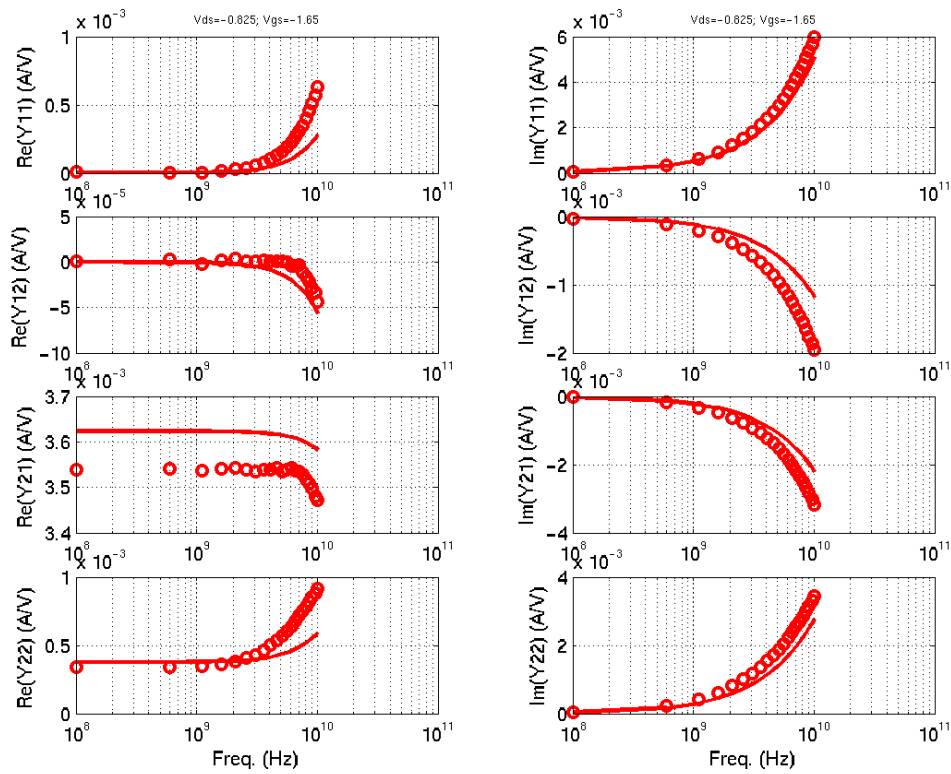


FIGURE 3.26 3p3_PFET_10x2x0p36 (1-sided gate contact, 2-sided substrate contact)

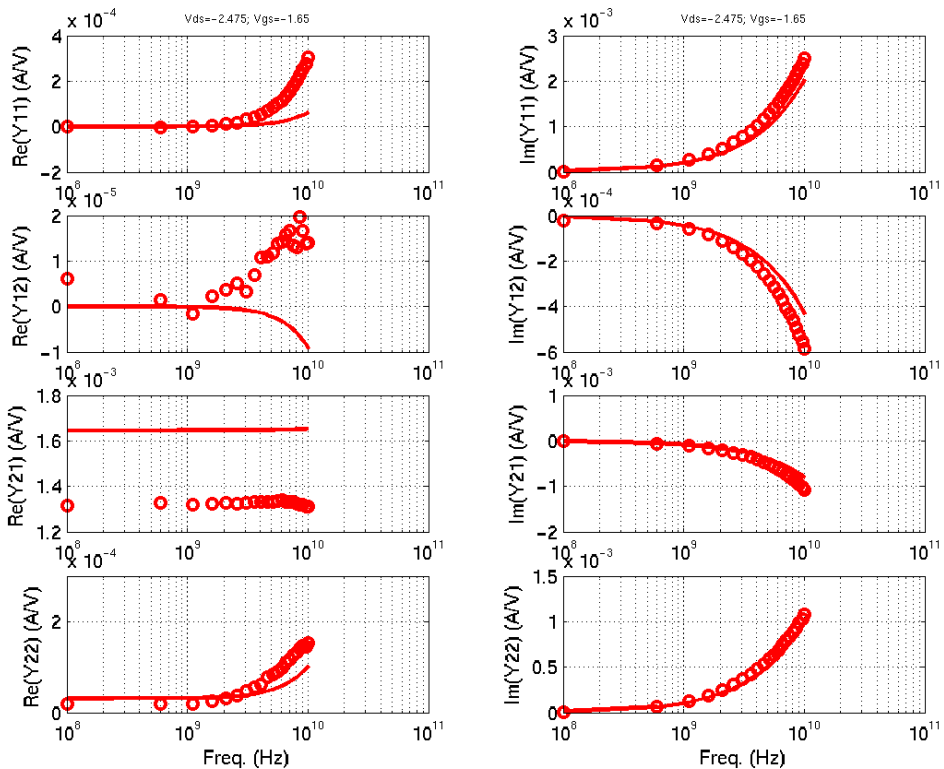
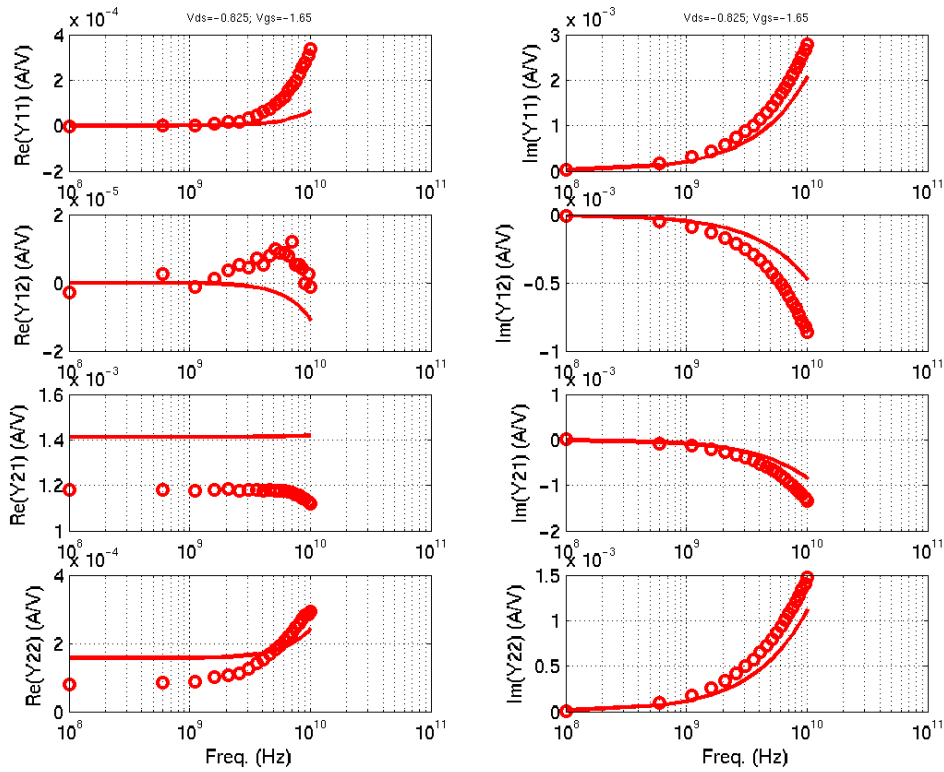


FIGURE 3.27 3p3_PFET_10x4x0p3 (1-sided gate contact, 2-sided substrate contact)

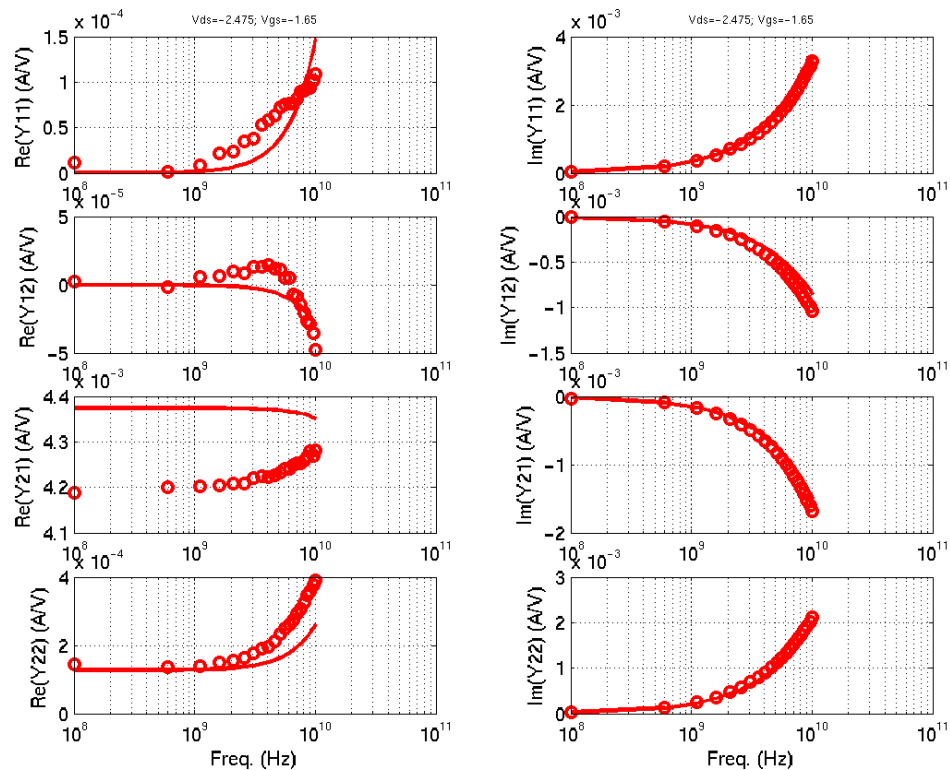
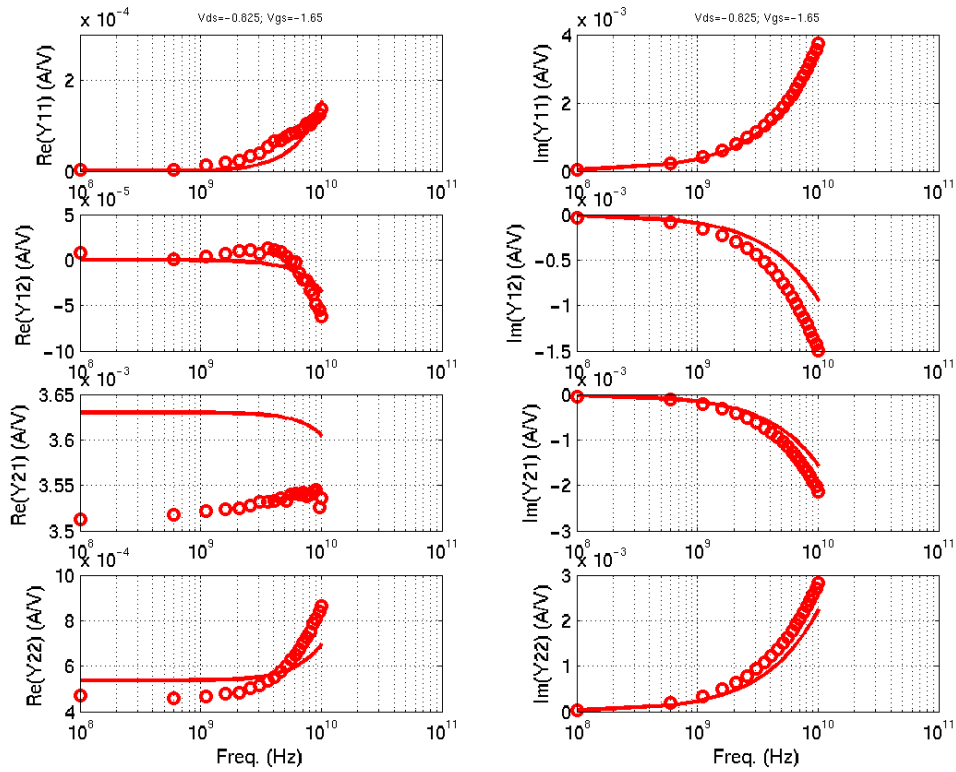
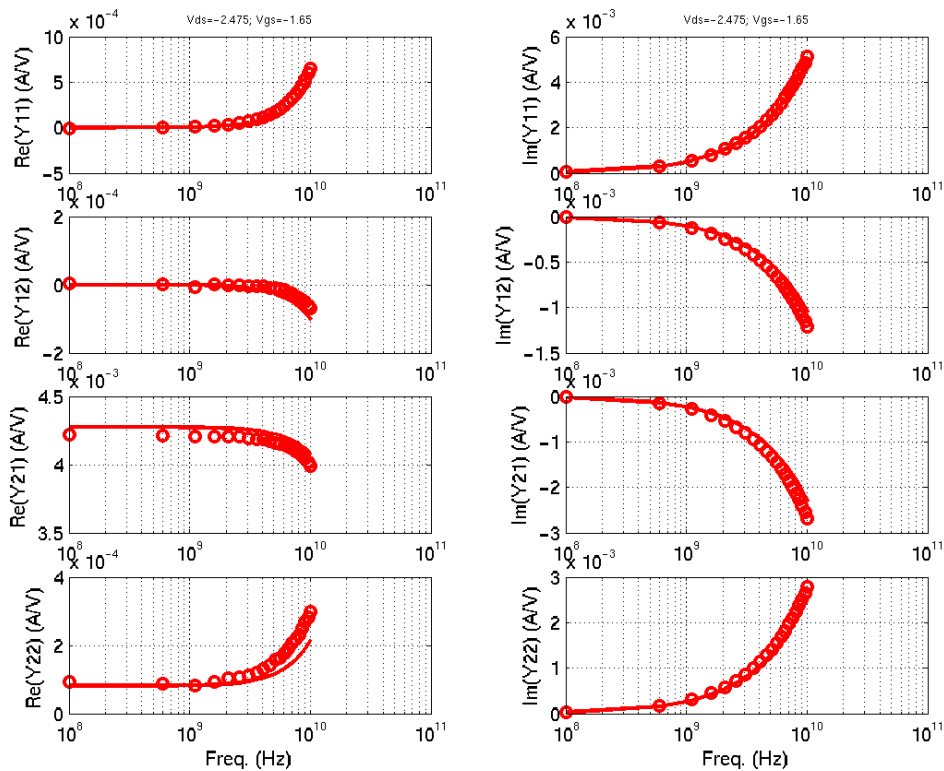
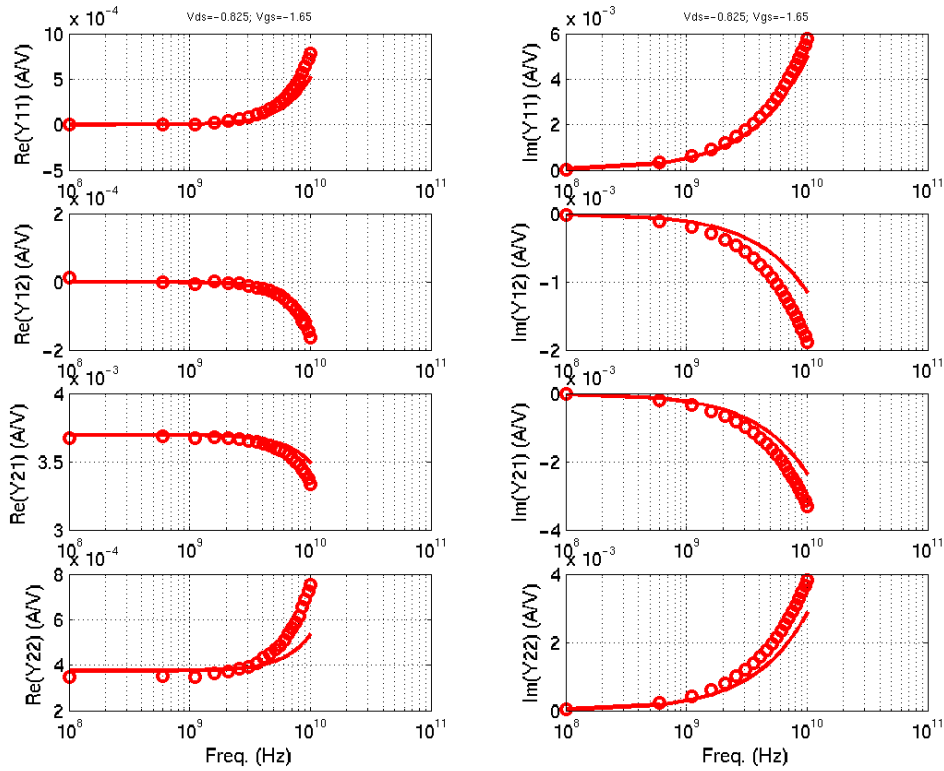


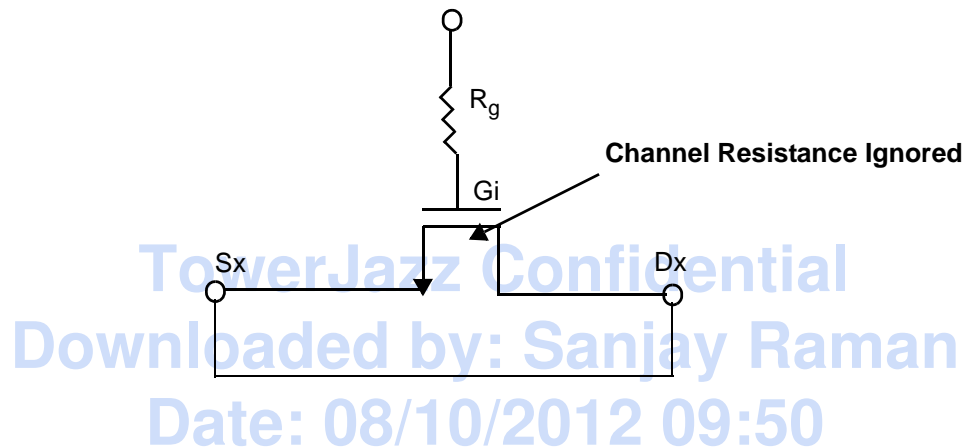
FIGURE 3.28 3p3_PFET_5x10x0p36 (1-sided gate contact, 2-sided substrate contact)



3.7 Series Resistance Modeling inaccuracy: RF FET used as Varactor/Capacitor

RF FETs are sometimes used capacitors or varactors (for example in VCO circuits) with the drain and source tied together to form the one terminal of the capacitor, with the gate functioning as the other terminal. Though this yields a functioning device with the RF model providing a good estimate of the capacitance, the Q of the varactor will not be accurately predicted. This arises from the limitations of the quasi-static compact models (like BSIM3), where the charge elements bypass the series channel resistance, when the drain and source are tied together (Figure 3.29). This is the primary resistive component and will not be simulated. The MOS varactor model accurately accounts for this series resistance, and should be used as the preferred capacitor or varactor element whenever possible.

FIGURE 3.29 MOSFET used as a varactor



3.8 High frequency Noise Modeling

3.8.1 Excess thermal noise in short channel devices

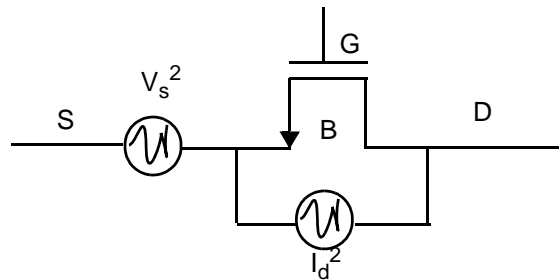
Excess thermal noise, not captured by the BSIM3v3 model, has been observed in short channel devices [2]. There are 2 components to this excess noise: 1. Excess thermal noise in the channel, that manifests itself as noise in the output drain current, and 2. Channel thermal noise induced gate noise that is important at high frequencies (>2 GHz). The default BSIM3v3 model underestimates (1) for velocity saturated short channel devices and does not model (2).

3.8.2 Modeling

To capture the excess noise 2 additional noise sources are added in the 1.8v RF NFET model (Figure 3.30). The voltage noise source on the source side of the FET accounts for gate correlated portion of the drain noise. The same noise source contributes to the induced gate noise through the gate-source overlap capacitor. The drain current noise source accounts for excess thermal noise observed in short channel devices. The magnitude of these noise sources is extracted from high-frequency noise measurements by using a 2-step de-embedding method that subtracts noise contributions from the RF Ground-Signal-Ground pads as well as from the parasitic drain, gate, and substrate resistances. This methodology allows the layout-independent extraction

of the intrinsic noise of the FET. A plot showing the measured and simulated noise data is shown in Figure 3.31. The top row of the plot shows the 4 parameters that characterize the noise in a 2-port linear network; Minimum noise figure (NF_{min}), Noise resistance (R_n), and Γ_{opt} corresponding to the magnitude and phase of the optimum source impedance. The bottom row of plot shows the equivalent gate and drain noise currents and their co-relation.

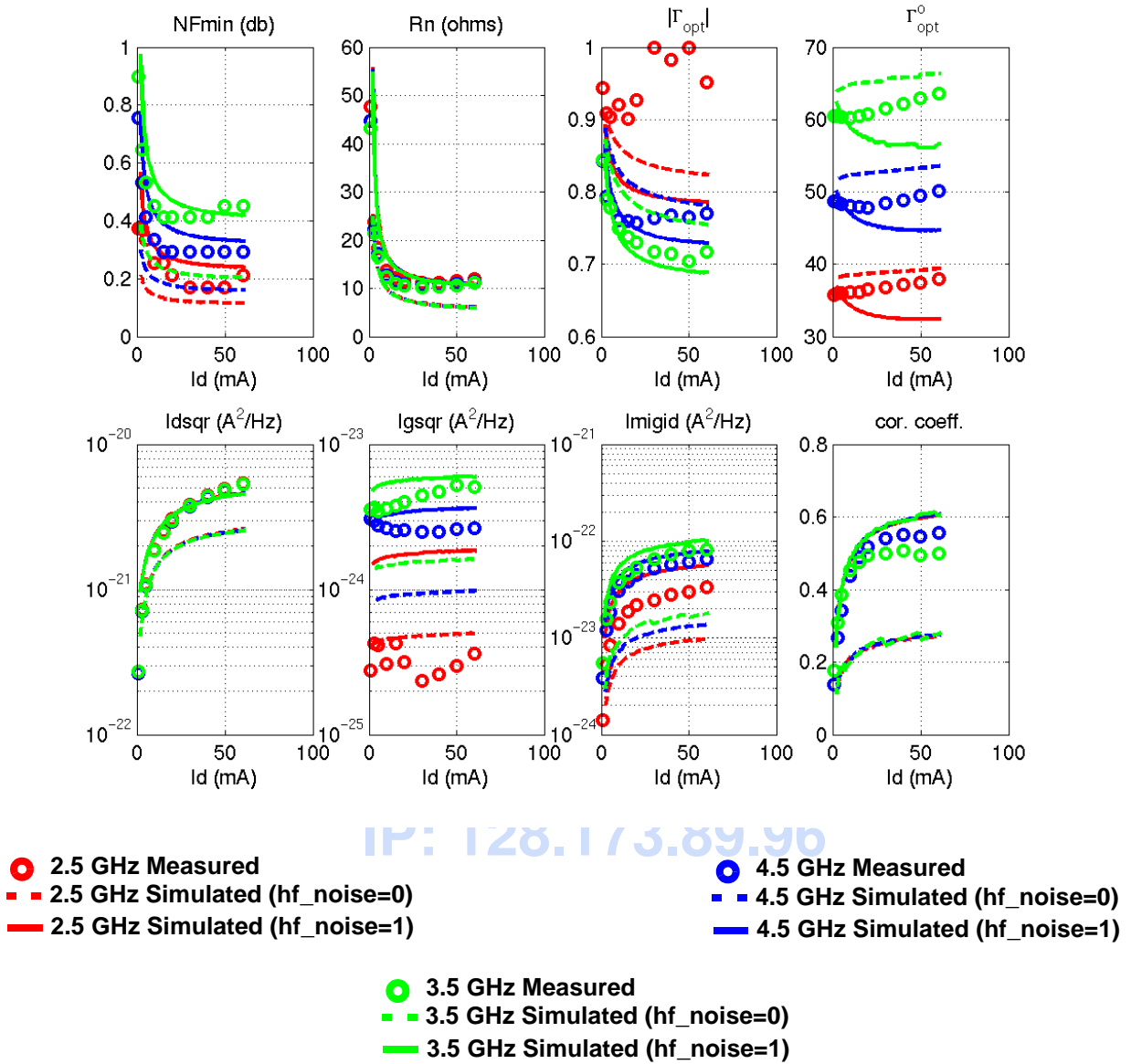
FIGURE 3.30 Excess noise source modeling



3.8.3 Usage guidelines

The high frequency noise model is available for the 1.8v RF NFET. It can be used by setting the “High Frequency Noise = 1” in the CDF window (Figure 3.2). It should be used in noise sensitive applications such as the Low Noise Amplifier. Since the noise sources add a fixed (bias independent) noise magnitude, the noise simulated with this model over-estimates the noise when the device is turned-off ($V_{gs} = 0$). “High Frequency Noise = 0,” if an accurate prediction of noise is needed for off-state device. The model was extracted for $L = 0.18\mu m$, $NF=64$ to 128 , $W=2.5\mu m$. Scaling equations are used to capture the geometry dependence of the model. The model accuracy is expected to decrease as $L > 0.18\mu m$ and as $NF \cdot W < 64 \times 2.5\mu m$.

FIGURE 3.31 Noise measurements compared with the high frequency noise model for a NF=128, W=2.5 μ m, L=0.18 μ m RF NFET.



3.9 Model update History

3.9.1 v3.2

TABLE 3.4 RF FET model specific updates in model release version 3.2

v3.2 update	Devices	Reason	Impact on user
Noimod changed from 2 to 1	All 1.8v and 3.3v FETs	Better off-state prediction of RF thermal noise	Reduced (1/10 - 1/200x) noise for $V_g=0v$. 10-20% change in the on-state ($V_g>V_t$)
RF substrate network changed from II to T	1.8v RF NFET and PFET	Better fit to measured y-parameters (Y22)	Small change in Y22
RF gate resistance	1.8v RF NFET and PFET	Better fit to $Re(Y_{11})$	Reduced R_{gate} - impact on $Re(Y_{11})$ and gate noise

3.9.2 v3.4

TABLE 3.5 RF FET model specific updates in model release version 3.4

v3.4 update	Devices	Reason	Impact on user
Corner/Statistical model oxide thicknesses	All 1.8v and 3.3v RF FETs	Updated to match new E-spec. with tighter variation	No change in NOMINAL model. Reduced corner/statistical model variation in gate oxide capacitance: 1.8v FETs corner model: v3.3a +/- 1Å; v3.4 +/- 1Å 1.8v FETs stat. model: v3.3a +/- 3Å; v3.4 +/- 1.5Å 3.3v FETs corner model: v3.3a +/- 2Å; v3.4 +/- 1.8Å 3.3v FETs stat. model: v3.3a +/- 6Å; v3.4 +/- 3Å
Corner and stat. parameters added to model process variation on drain/source series resistance	All 1.8v and 3.3v RF FETs	More physical corner and statistical models	No change in NOMINAL model. Larger g_m variation in corner and statistical models for short channel FETs
Corner and stat. parameters added to model process variation on gate-source and gate-drain overlap capacitances	All 1.8v and 3.3v RF FETs	Corner and statistical models for overlap capacitance in v3.2 did not capture oxide thickness and ΔL variation	No change in NOMINAL model. Larger gate-source and gate-drain overlap capacitance variation in corner and statistical models
Statistical correlation added to FASTSLOW and SLOW-FAST corners	All 1.8v and 3.3v RF FETs	Improved correlation matching between N and PFETs	Reduced oxide thickness, ΔL , and ΔW variation when simulating with the FASTSLOW and SLOW-FAST corners
RF substrate network changed from II to T	3.3v RF NFET and PFET	Better fit to measured y-parameters (Y22). Both 2-sided and 4-sided ("ringed") substrate contacts are now supported for all 1.8v and 3.3v RF FETs	Small change in Y22
Added salicide-polysilicon contact resistance to the gate resistance	All 1.8v and 3.3v RF FETs	salicide-polysilicon gate resistance is a significant component of gate resistance for narrow width ($<3\mu m$) RF FETs with 2-sided gate contacts	Increased gate resistance seen in $Re(Y_{11})$, especially for narrow FETs ($W<3\mu m$) with 2-sided gate contact layouts

3.9.3 v3.7

TABLE 3.6 RF FET model specific updates in model release version 3.7

v3.7 update	Devices	Reason	Impact on user
Fixed junction capacitance partitioning between area and perimeter	All 1.8 and 3.3v RF FETs	Previous versions used an empirical fit. New partitioning scheme aligns RF and MS model	Minimal change in total junction capacitance
Flicker noise model changed from gm-based to BSIM3	1.8v n and pfet 3.3v n and pfet	Improved modeling of bias dependent flicker noise	Reduced flicker noise at lower gate biases ($\sim V_t$) for most cases
Add "multiplicity" to mismatch model	All FETs	Mismatch should improve with multiple devices	Correct modeling of transistor mismatch for $m > 1$

3.9.4 v4.0

TABLE 3.7 RF FET model specific updates in model release version 4.0

v4.0 update	Devices	Reason	Impact on user
Added x-sigma support	1.8v and 3.3v RF FETs	Add capability to design to process corners other than ± 3 -sigma Isolate device causing failures in FAST/SLOW corner simulations	

3.9.5 v4.1

TABLE 3.8 RF FET model specific updates in model release version 4.1

v4.0 update	Devices	Reason	Impact on user
Flicker noise	3.3V RF PFET	New data on $L=0.3\mu m$ device	Simulated flicker noise is now 2-3x higher for biases close to V_t

3.10 References

1. Steve Hung-Min Jen, Christian C. Enz, David R. Pehlke, Michael Schroter, and Bing J. Sheu, "Accurate Modeling and Parameter Extraction for MOS Transistors Valid up to 10 GHz," IEEE Trans. on Elec. Dev., Vol. 46, No. 11, November 1999.
2. Chih-Hung Chen, M. Jamal Deen, Yuhua Cheng, and Mishel Matloubian, "Extraction of the Induced Gate Noise, Channel Noise, and Their Correlation in Submicron MOSFETs from RF Noise Measurements," IEEE Trans. on Elec. Dev., Vol. 48, No. 12, December 2001.

4.0 HV MOSFET Model

4.1 Device Description

The CA18 process family supports multiple HV FET devices. These are summarized in Table 4.1, with cross-sections illustrated in Figures 4.2 through 4.6. The 12V NFET and 12V PFET share the wells with the 5V CMOS Fets. The extended drains in the 40V NFET and PFET are formed by additional HV-N/Pwell implanted layers. The deep-nwell layer is used to isolate the p-type well regions in the HV NFETs from P-substrate. The 40V devices provide a scalable drift region (L_{drift}), allowing for $R_{\text{DS(on)}}\text{-}BV_{\text{dss}}$ trade-off.

TABLE 4.1 CA18 HV MOS Model summary

HV MOS Name	$ V_{\text{GS}} / V_{\text{DS}} / V_{\text{BS}} $ (V) ¹	CA18 Process Variant	L (μm)	L_{drift} (μm)	W (μm)	NF (Even Only)	Temp. (°C)	Cross- section (Fig. #)	Model
nfet5p0_ld12	0-5/0-10/0	HA, HP	0.5	0.6	2-20	2-5000	-40 - 125	4.1	MM20 + Rdrift(V)
nfet5p0_ld12_iso	0-5/0-10/0	HA, HP	0.8	0.6	2-20	2-5000	-40 - 125	4.2	
pfet5p0_ld12	0-5/0-8/0	HA, HP	0.7	0.6	2-20	2-5000	-40 - 125	4.3	
nfet5p0_ld40	0-5/0-40/0	HA	0.8	0.6-4	2-20	2-5000	-40 - 125	4.4	
nfet5p0_ld40_iso	0-5/0-40/0	HA	0.8	0.6-3.6	2-20	2-5000	-40 - 125	4.5	
pfet5p0_ld40	0-5/0-40/0	HA	0.8	0.6-2.8	2-20	2-5000	-40 - 125	4.6	
nfet3p3_ld	0-3.3/0-10/0	HD,PD,QD	0.5	0.6	2-20	2-500	-40 - 125		BSIM3 + Cgd (V) + Rdrift(V)
pfet3p3_ld	0-3.3/0-8/0	HD,PD,QD	0.7	0.6	2-20	2-500	-40 - 125		
nfet5p0_rfld	0-5/6V/0	HP	0.2		5,10,15,20	2-422	-40 - 125		

1. Maximum value guidelines only. See documents NPB-PS-0711 (Design Application Note for CA18HP, CA18HB, CA18QB, and CA18HA Processes) and NPB-PS-0571 (Design Application Notes for CA18 Processes – Addition of High Voltage LD Fets) for a detailed description of operating voltages for reliable operation and breakdown voltages.

FIGURE 4.1 12V LD-NMOS cross-section

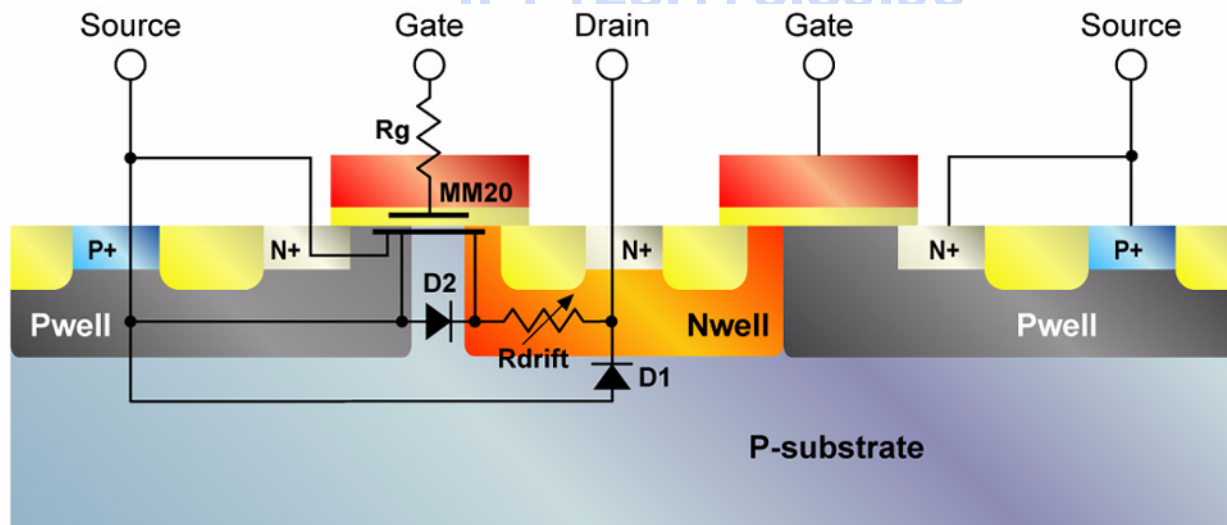


FIGURE 4.2 12V Isolated LD-NMOS cross-section

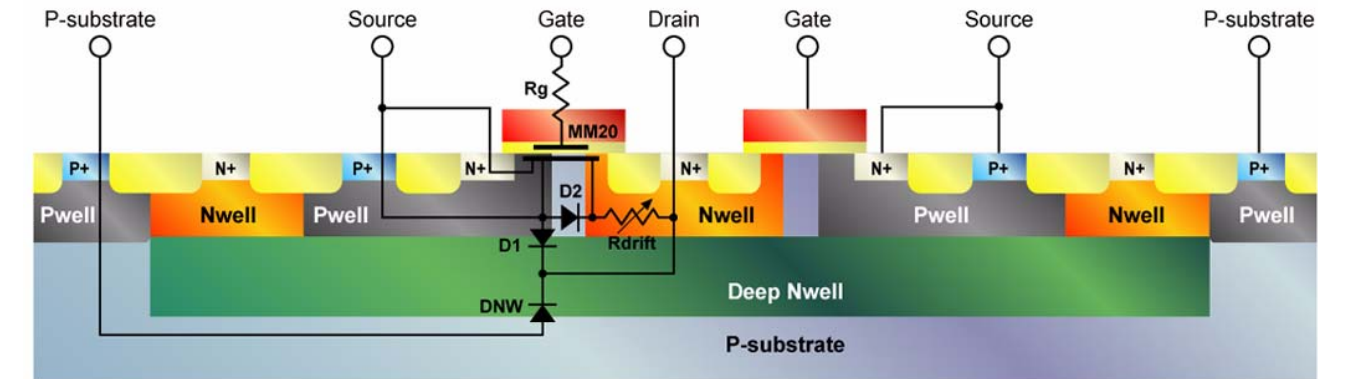


FIGURE 4.3 12V LD-PMOS cross-section

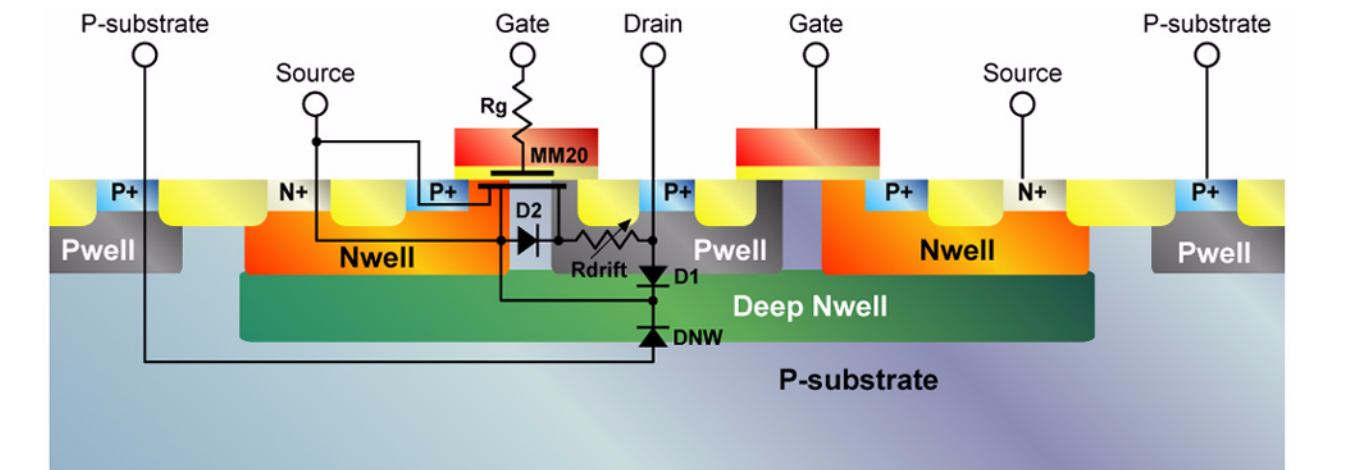


FIGURE 4.4 40V LD-NMOS cross-section

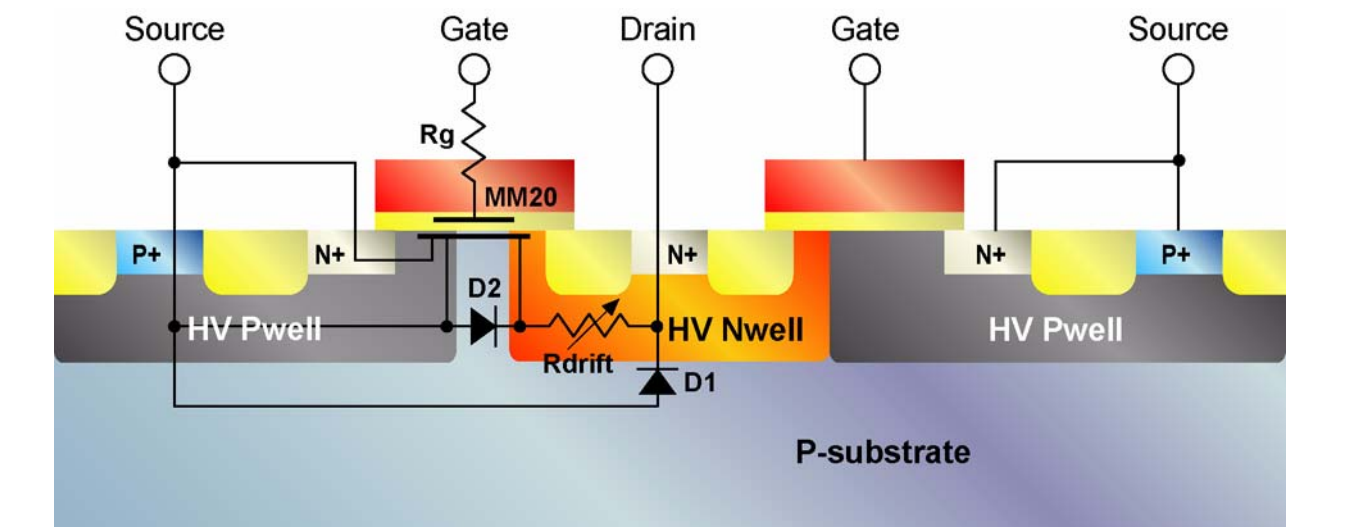


FIGURE 4.5 40V Isolated LD-NMOS cross-section

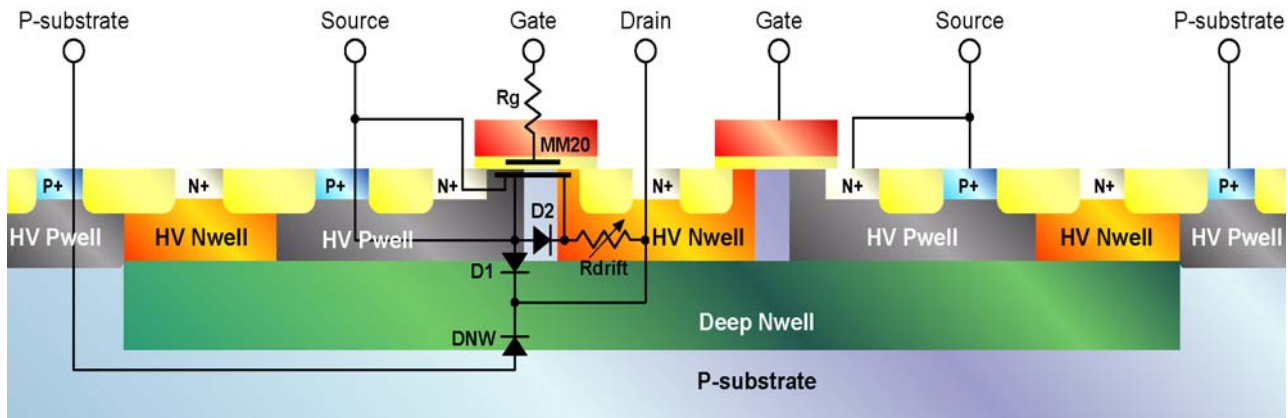
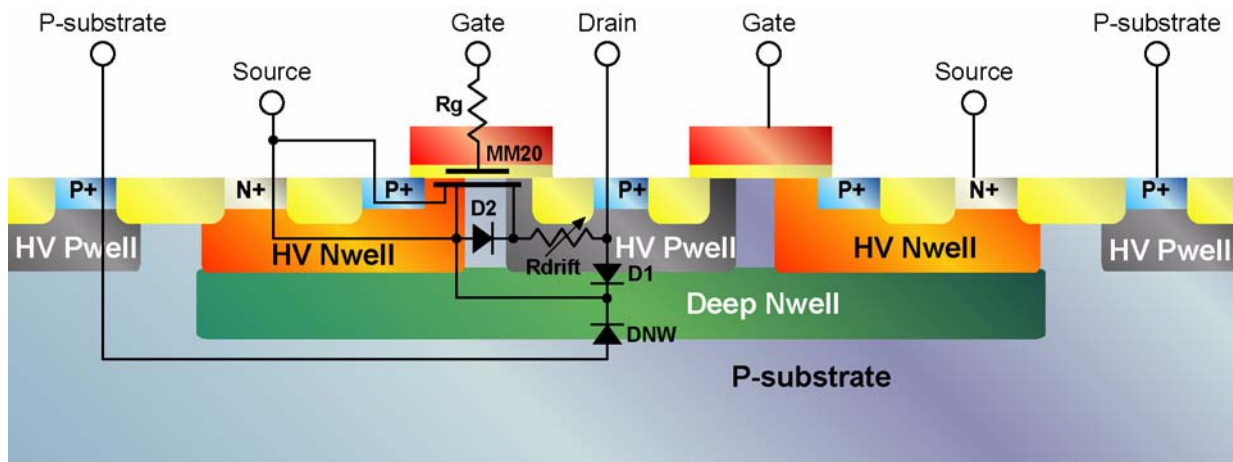


FIGURE 4.6 40V LD-PMOS cross-section



4.2 Model Description

Figure 4.1 shows the 3 terminal sub-circuit used for the HV-NFET devices. The HV-PFETs have an additional terminal to model the deep-nwell to p-substrate diode (Figure 4.3). The core FET is modeled using the MM20 model [1] for the HV FETs in CA18HA. MM20 is an advanced surface potential based LDMOS model which includes an accurate description of the intrinsic channel and drift region under thin oxide. The MM20 model explicitly calculates the “internal” voltage between the channel and the drift regions as a function of the external terminal voltages, providing a physical model for the charge sharing between the regions. The bias dependent extended drift region under STI is, however, not included in MM20 model. This effect is modeled via an external Verilog-A module (R_{drift}). The distributed nature of the drain to bulk coupling is modelled via 2 diodes on either side of R_{drift} . The 3.3V gate oxide HV-FET devices in CA18HD,PD, and QD as well as the 5V RF-LDMOS in CA18HP use a BSIM3 core in conjunction with the R_{drift} module described above. An external gate resistance is added to the core FET to better model the input admittance at high frequencies.

The documentation in the rest of the chapter is for CA18HA FETs listed in the top 6 rows of Table 4.1. No further documentation is presently available for the HV FETs with 3.3V gate oxides in CA18HD,PD,QD or for the 5V RF LDMOS in CA18HP.

4.3 Usage from Design Kit (CDF Options) (CA18HA FETs only)

An illustrated description for various CDF options is provided in Figures 4.7 and 4.8. A key difference between the 12V NFET (12V PFET) and the 40V FETs, is the option to change the drift length in the 40V FETs. Based on the drift length specified, the maximum Vds estimate is provided at the bottom of dialog box. Calculated maximum Vds values are shown in Table 4.2.

TABLE 4.2 40V FET Ldrift vs. Maximum Operation Voltage

L _{drift} (μm)	Maximum Operation Voltage (V)
0.6	20
1.6	32.5
2.0	40
2.4	40

4.3.1 LDMOS Rds-On Calculator (CA18HA FETs only)

The CA18 HV transistor design environment offers a schematic level Rds-On calculator. The calculator outputs an Rds-On prediction that accounts for intrinsic resistance contributions from active device elements (Rdrift, etc) as well as interconnect parasitics from Contact/M1/VIA1/M2. The interconnect parasitic estimation is based on the Jazz LDMOS pcell.

The layout parasitic estimation can be toggled ON and OFF through the Cadence CDF by setting the “Include Metal Parasitics” option as follows:

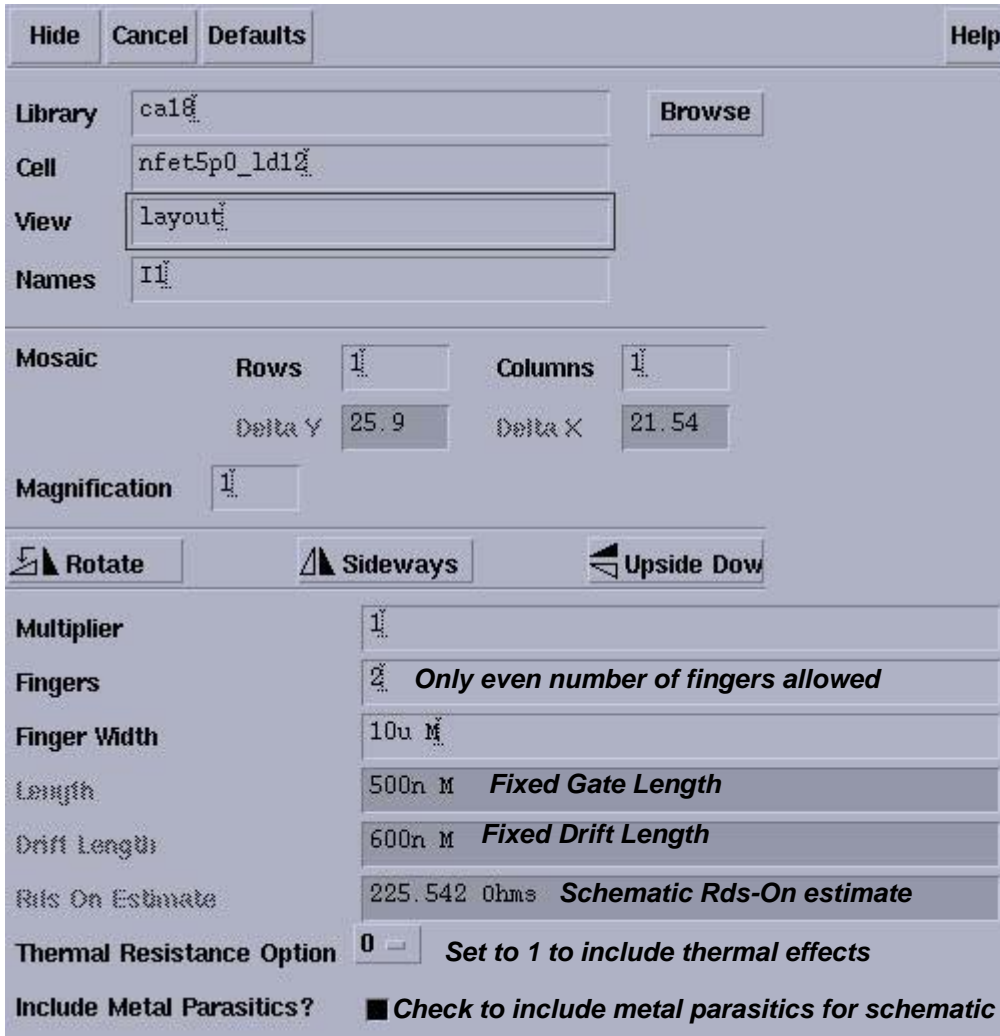
- “Include Metal Parasitics” = Checked: Schematic estimation of Rds-On is reported in the “*Rds-On Estimate*” CDF field. Estimation includes interconnect parasitics
- “Include Metal Parasitics” = Unchecked: Schematic estimation of parasitics is disabled (avoids double counting). All metal interconnect and via parasitics to be accounted for via extraction. With this option, the ideal Rds-On with metal parasitics set to zero is provided.

This CDF tool can be used to design for the optimal Rds-On and to observe how resistance deteriorates due to interconnect parasitics. Please note that the schematic Rds-On prediction tool adds parasitics based on the layers and geometry specific to the Jazz Pcell, which goes up to M2, and also assumes current will travel across the center of the metal lines. This assumption can render higher Rds-On values than physically expected since most layouts will leverage M3 routing due to its large current carrying capability (lower metal resistance) and to distribute current evenly across devices. Hence, as device size increases, larger predicted Rds-On error is expected. For highly precise Rds-On calculation a full post layout extraction is recommended. Eq. 1 describes the Jazz calculator formulation. $R_{ds(in)}$ is the resistance of the intrinsic device. $R_{ds(ext)}$ is the resistance of the metal interconnect including vias.

$$R_{ds(on)} = \frac{R_{ds(in)}}{nf \cdot wf \cdot 10^3} + (IncludeMetalParasitics) \cdot R_{ds(ext)} \quad (EQ 1)$$

For 20-40V LDMOS devices $R_{ds(in)}$ is a function of L_{drift} extracted based on device simulation at $V_d=100mV$ / I_{ds} using different values of L_{drift} . The $R_{ds(ext)}$ is calculated from the Pcell geometry, which includes Contact/ M1/Via1/M2. Since each LDMOS Pcell is different, $R_{ds(ext)}$ values are unique to each device and its input parameters.

FIGURE 4.7 CDF options for 12V NFET in CA18HA



Library	cal8	Browse
Cell	nfet5p0_1d12	
View	layout	
Names	I1	
Mosaic	Rows: 1, Columns: 1, Delta Y: 25.9, Delta X: 21.54	
Magnification	1	
Rotate	Sideways	Upside Down
Multiplier	1	
Fingers	2	Only even number of fingers allowed
Finger Width	10u M	
Length	500n M	Fixed Gate Length
Drift Length	600n M	Fixed Drift Length
Rds On Estimate	225.542 Ohms	Schematic Rds-On estimate
Thermal Resistance Option	0	Set to 1 to include thermal effects
Include Metal Parasitics?	<input checked="" type="checkbox"/>	Check to include metal parasitics for schematic sim.

FIGURE 4.8 CDF options for 40V NFET in CA18HA

Hide Cancel Defaults Help

Library Browse

Cell

View

Names

Mosaic Rows Columns
Delta Y Delta X

Magnification

Multiplier

Fingers *Only even number of fingers allowed*

Finger Width

Length *Fixed Length*

Drift Length *Variable drift length determines max. Vds*

Max Vds Estimate *Max. Vds estimate value*

Rds On Estimate *Schematic Rds-On estimate*

Thermal Resistance Option *Set to 1 to include thermal effects*

Include Metal Parasitics? ☒ *Check to include metal parasitics for schematic sim.*

4.4 Measurements (CA18HA FETs only)

Devices were measured using the Agilent IC-CAP characterization and modeling software. Table 4.3 lists the sizes of FETs that were measured. Three sets of measurements were performed: 1. DC for extraction of MM20 IV and Verilog-A R_{drift} parameters (Tables 4.4 and 4.5), 2. Pulsed DC for extraction of MM20 thermal network parameters (Table 4.6) and 3. RF for extraction of MM20 CV parameters.

TABLE 4.3 List of HV-FET measured devices for model extraction

Fet Dimension	12V NFET	12V PFET	40V NFET	40V PFET
Width (μm)	10	10	50	50
Length (μm)	0.5	0.7	0.8	0.8
No. of Fingers	6	6	2	2
L_{drift} (μm)	0.6	0.8	0.6, 1.2, 1.8, 2.4, 4	0.6, 1.2, 2.4

TABLE 4.4 List of DC measured characteristics 12V NFET and 12V PFET (TYPE=1,-1 for N,P FETs)

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold -Linear	TYPE*0.1	0 to TYPE*5, TYPE*50mV steps	0
Id Vs. Vgs	Threshold - Middle Linear	TYPE*3	0 to TYPE*5, TYPE*50mV steps	0
Id Vs. Vgs	Threshold -Saturation	TYPE*6,9,12	0 to TYPE*5, TYPE*50mV steps	0
Id Vs. Vds	Output	0 to TYPE*12V, TYPE*100mV steps	0 to TYPE*5, TYPE*1V steps	0

TABLE 4.5 List of DC measured characteristics 40V N and PFETs (TYPE=1,-1 for N,P FETs)

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vgs	Threshold -Linear	TYPE*0.1	0 to TYPE*5, TYPE*50mV steps	0
Id Vs. Vgs	Threshold - Middle Linear	TYPE*3	0 to TYPE*5, TYPE*50mV steps	0
Id Vs. Vgs	Threshold -Saturation	TYPE*5,10,20	0 to TYPE*5, TYPE*50mV steps	0
Id Vs. Vds	Output	0 to TYPE*30V, TYPE*100mV steps	0 to TYPE*5, TYPE*1V steps	0

TABLE 4.6 List of pulsed-DC measured characteristics 12V NFET (TYPE=1,-1 for N,P FETs)

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
Id Vs. Vds	Output	0 to TYPE*12V, TYPE*100mV steps	0 to TYPE*5, TYPE*1V steps	0

TABLE 4.7 List of RF measured characteristics 40V N and PFETs (TYPE=1,-1 for N,P FETs)

Characteristic	Type	V_{DS} (V)	V_{GS} (V)	V_{BS} (V)
S-param. vs Vgs and Vds	0.1 to 15.8 GHz	0 to TYPE*20V, TYPE*4V steps	0 to TYPE*5, TYPE*1V steps	0
S-param. vs Vgs and Vds	Spot freq. @ 1GHz	0 to TYPE*20V, TYPE*5V steps	TYPE*5 to TYPE*20, TYPE*5V steps	0

4.5 MM20 Parameter Extraction

4.5.1 DC Parameter Extraction

MM20 (LDMOS) model parameters for low and high-field mobility reduction, velocity saturation, drain-induced barrier lowering, and output conductance are extracted by local optimization of selected parameters the appropriate regions of the measured device characteristics. The low field mobility parameters are extracted from FETs biased in the linear regions at low gate biases. The sheet resistance of the drift region under the isolation is extracted from test structures with varying drift lengths, measured in the linear region at high gate biases. The critical electrical field, which controls the saturation of carriers in the drift region, is extracted from the transition region, with the drain biased between the linear and saturation regimes. Pulsed-dc measurements are used to extract physical output conductance parameters in the absence of thermal self-heating effects for the NFETs. Parametric I_{drain} vs. V_{drain} measurements are used to extract the thermal network to model the conductance in the saturation regime in the presence of self-heating. The temperature dependence of the model parameters was captured through fitting the measured data at -40C and 125C.

4.5.2 Thermal Resistance Effects

Per the previous section, the device thermal resistance is extracted and included as an option in the model through the CDF. The thermal resistance model causes un-physical behavior in the model at typically unused bias regimes of high V_{gs} and high V_{ds} . (see Figure 4.37 for example). If these regions are critical for design, the thermal resistance can be turned off through the CDF as shown in Figure 4.7.

4.5.3 Capacitance Parameter Extraction

4.5.3.1 Gate Capacitance

The gate capacitance is composed of 2 elements: 1. $C_{channel}$: Gate to Intrinsic MOSFET channel/Well region (Pwell in HV NFET, Nwell in HV PFET), and 2. C_{mos} : Gate to Extended Drain over thin oxide (Nwell in HV NFET, Pwell in HV PFET). The MM20 includes both the $C_{channel}$ and C_{mos} including the charge-sharing effects between the two. The gate-to-source/drain/bulk capacitance and gate-to-source/drain overlap capacitances and their bias dependencies were extracted from de-embedded spot frequency (1 GHz) s-parameter measurements on very wide multi-finger FETs.

4.5.3.2 Junction Capacitance

The HV MOSFET devices contain asymmetric source and drain regions. The source/bulk terminal is shorted. The area component of the 12V NFET drain junction is defined by the Nwell to P-SUB., while the HVNwell to P-Substrate defines the same for the 40V NFET. The Pwell to Deep-Nwell and the HV-Pwell to Deep-Nwell layers define the area component of the drain junctions for the 8 and 40V P-FETs, respectively. A peripheral component of the drain capacitance also exists between the Nwell-Pwell for the 12V N-FETs (Nwell-HVPwell for the 40V N-FETs), and the Pwell-Nwell for the 12V P-FETs (HVPwell-Nwell for the 40V P-FETs). The periphery component is currently set to zero, with the entire capacitance lumped into the area component.

4.6 HV MOSFET Verification Plots

The simulated IV and CV characteristics of the HV MOSFETs are compared with the measured data in Figures 4.9 through 4.126. Unless labelled otherwise, the blue-circles are the measured data, and solid red lines are the model prediction.

FIGURE 4.9 40V NFET (nfet5p0_Id40); NFxWxL_Ldrift=2x50x0.8_0.6 μ m; Cg Vs. Vg

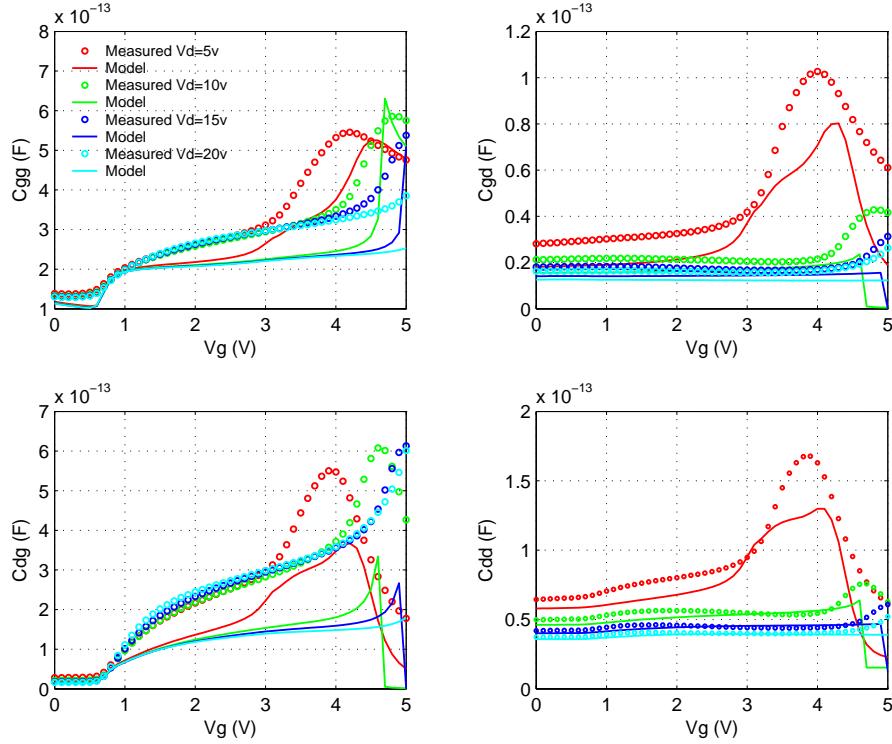


FIGURE 4.10 40V PFET (pfet5p0_Id40); NFxWxL_Ldrift=2x50x0.8_0.6 μ m; Cg Vs. Vg

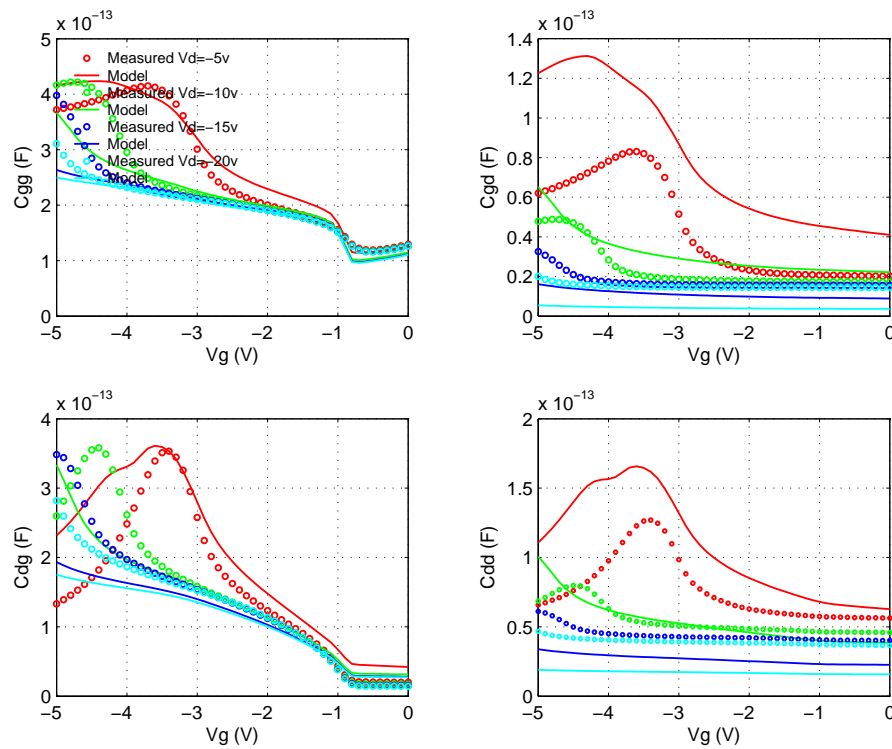


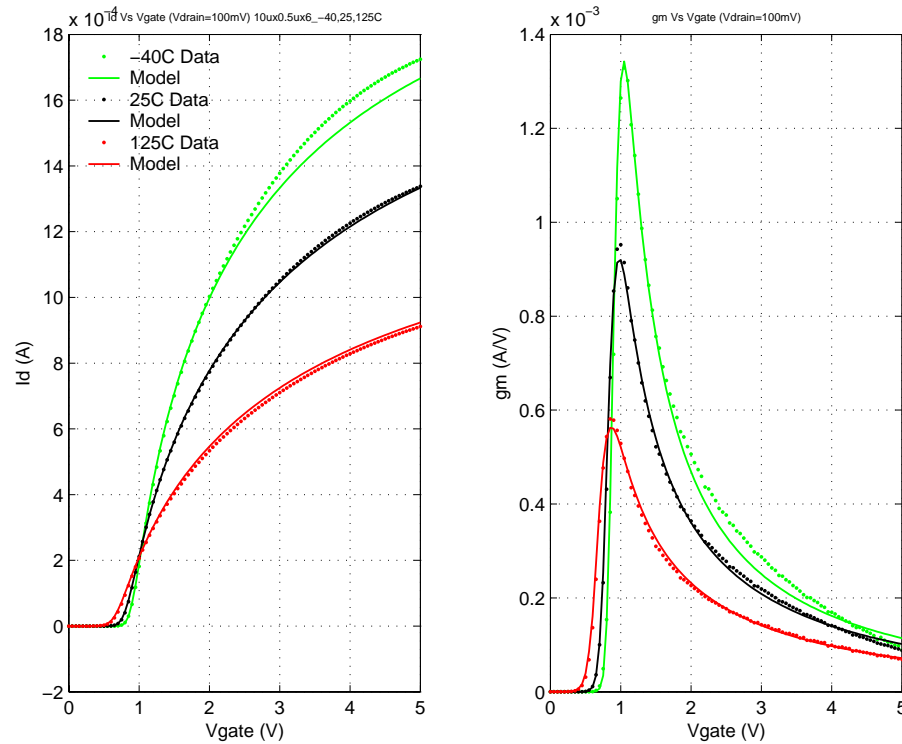
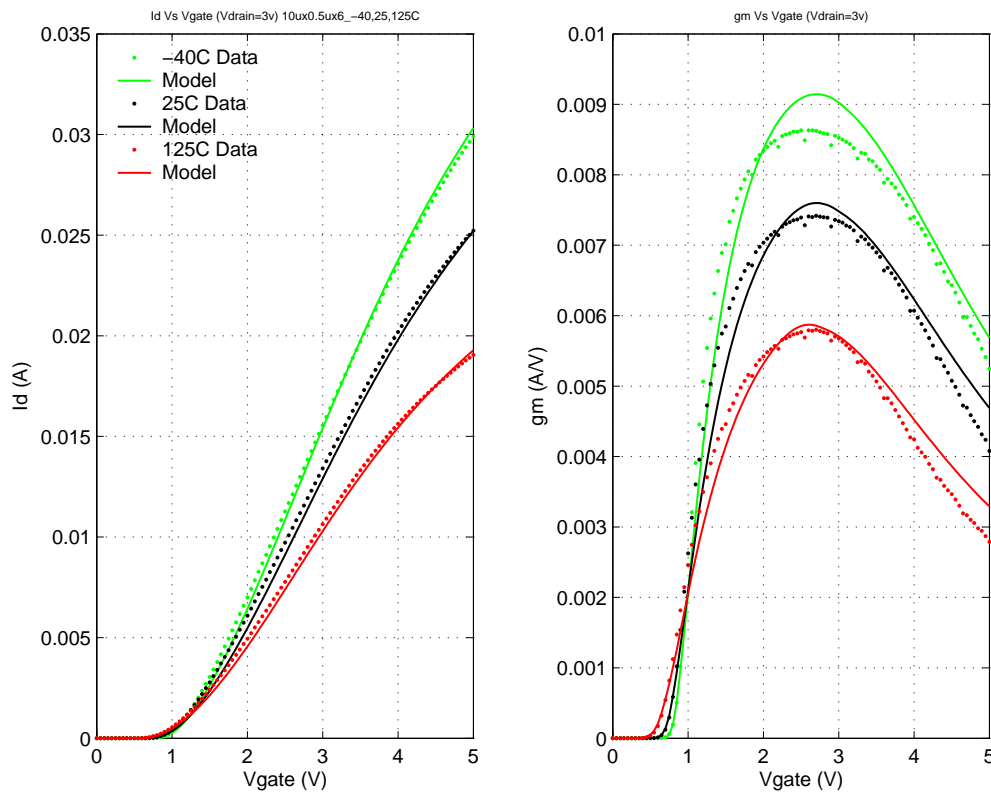
FIGURE 4.11 12V NFET (nfet5p0_Id12); NFxWxL=6x10x0.5 μ m; Id Vs. Vgs; Vds=0.1VFIGURE 4.12 12V NFET (nfet5p0_Id12); NFxWxL=6x10x0.5 μ m; Id Vs. Vgs; Vds=3V

FIGURE 4.13 12V NFET (nfet5p0_Id12); NFxWxL=6x10x0.5 μ m; Id Vs. Vgs; Vds=6V

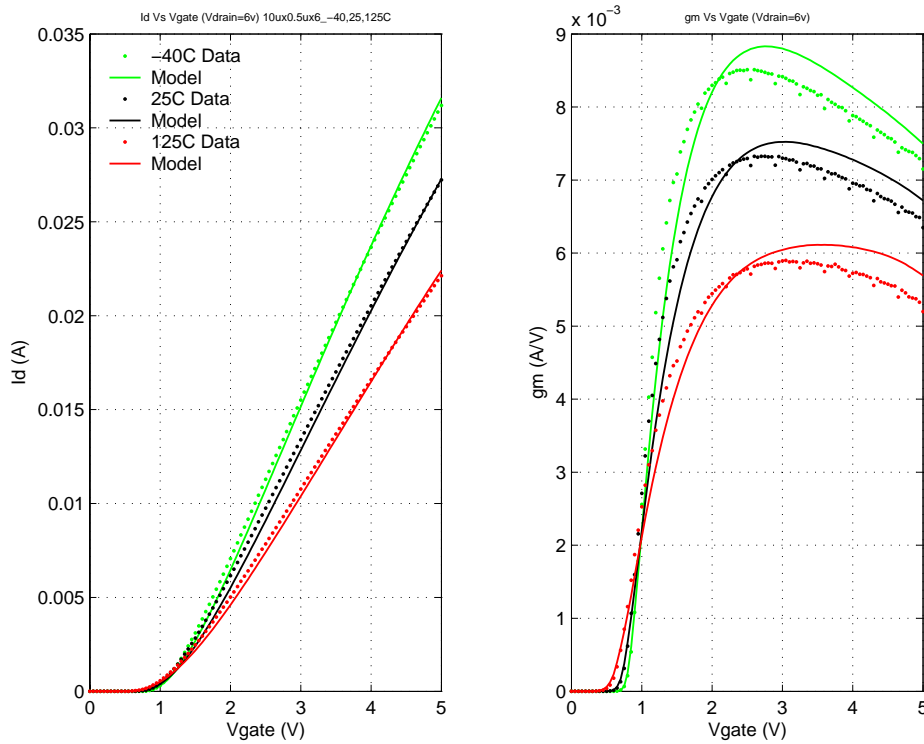


FIGURE 4.14 12V NFET (nfet5p0_Id12); NFxWxL=6x10x0.5 μ m; Id Vs. Vgs; Vds=9V

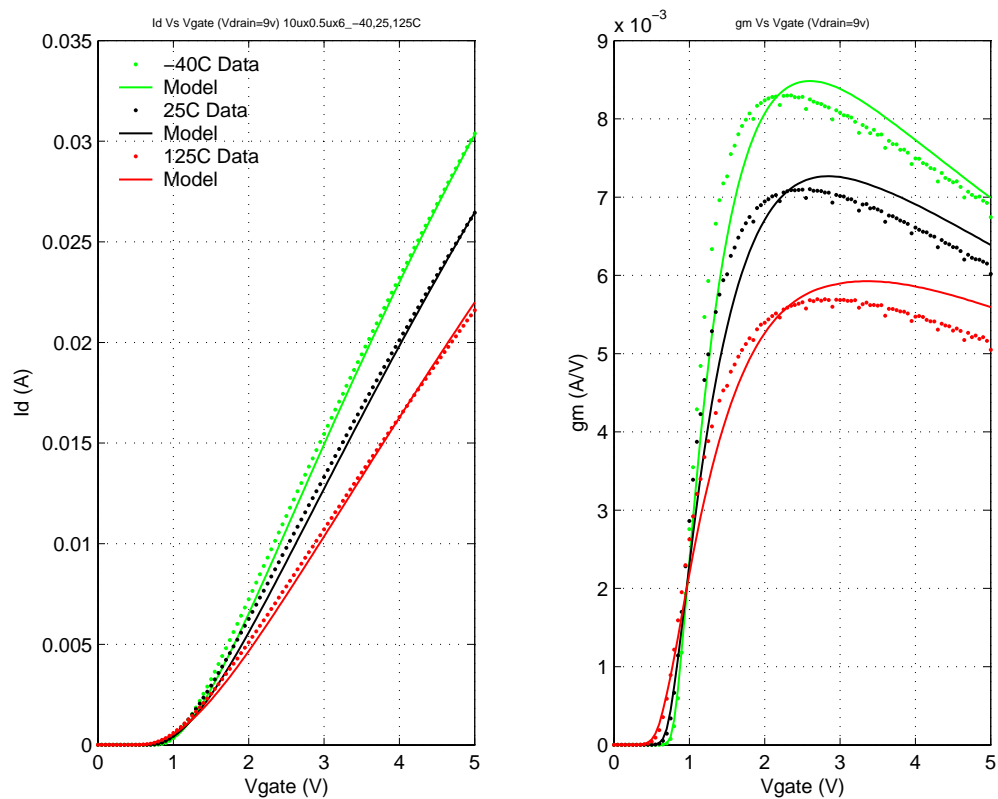


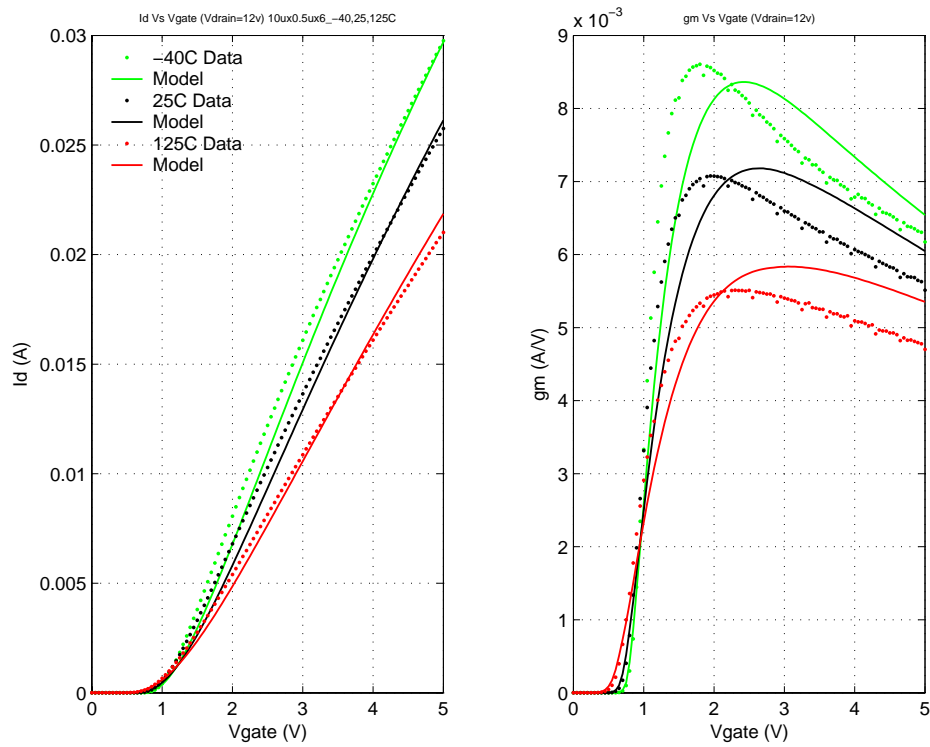
FIGURE 4.15 12V NFET (nfet5p0_Id12); NFxWxL=6x10x0.5 μ m; Id Vs. Vgs; Vds=12V

FIGURE 4.16 12V NFET (nfet5p0_Id12); Id Vs. Vds; Vgs=0,1,...,5V; Temp=-40C

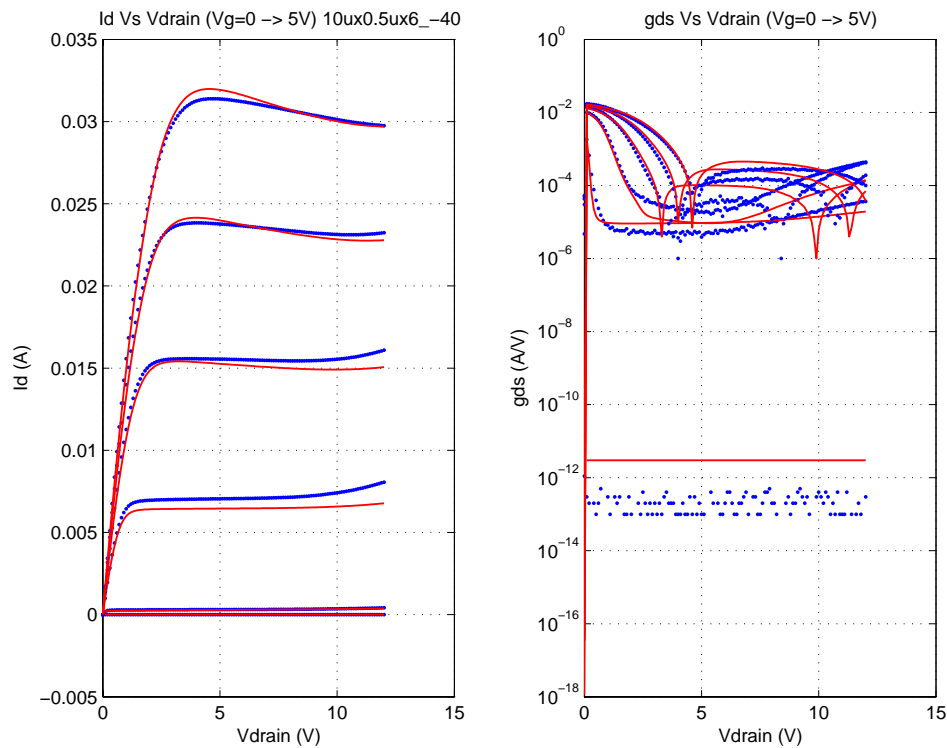


FIGURE 4.17 12V NFET (nfet5p0_Id12); Id Vs. Vds; Vgs=0,1,...,5V; Temp.=25C

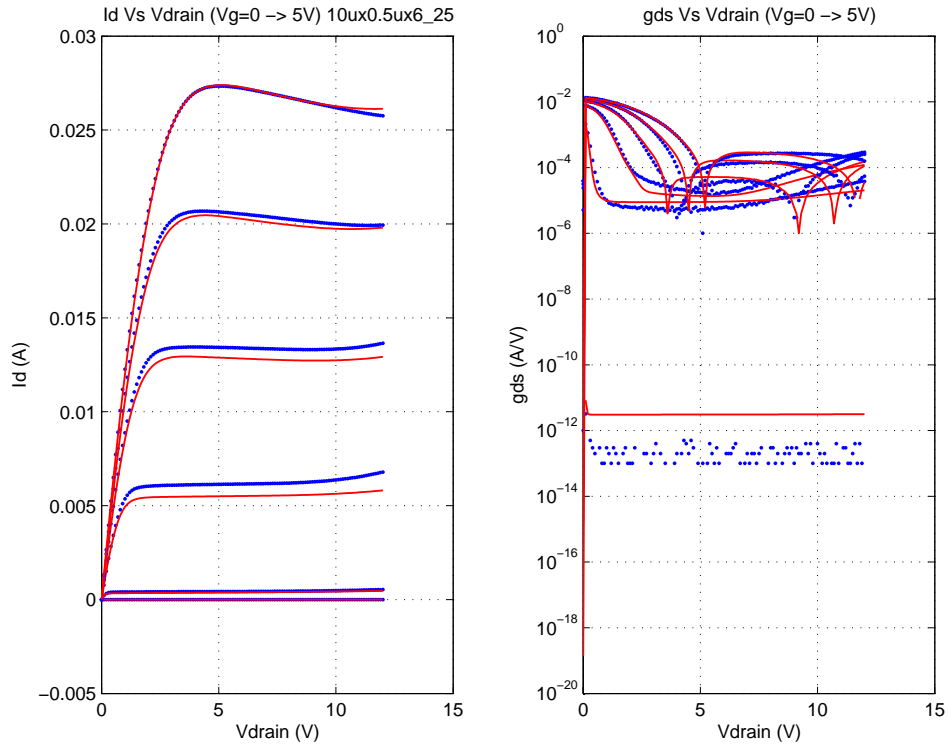


FIGURE 4.18 12V NFET (nfet5p0_Id12); Id Vs. Vds; Vgs=0,1,...,5V; Temp.=125C

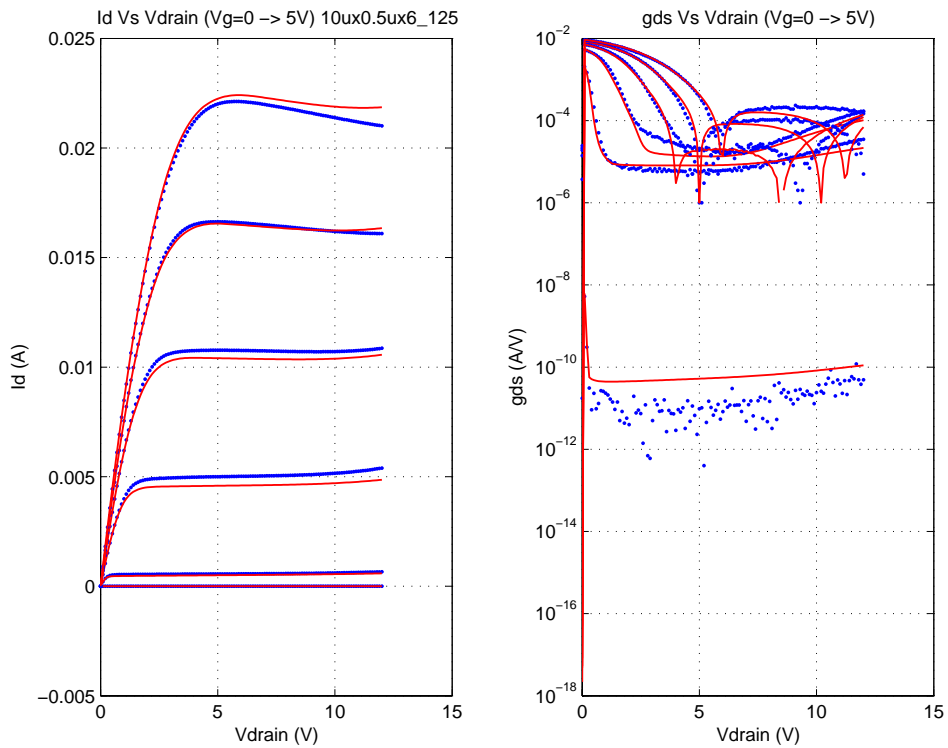


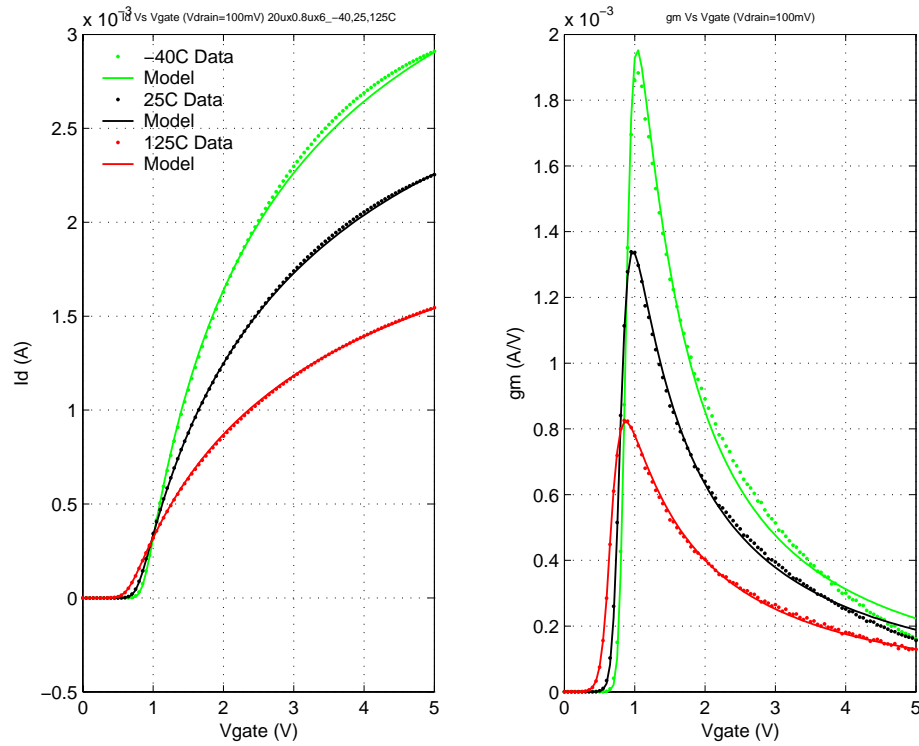
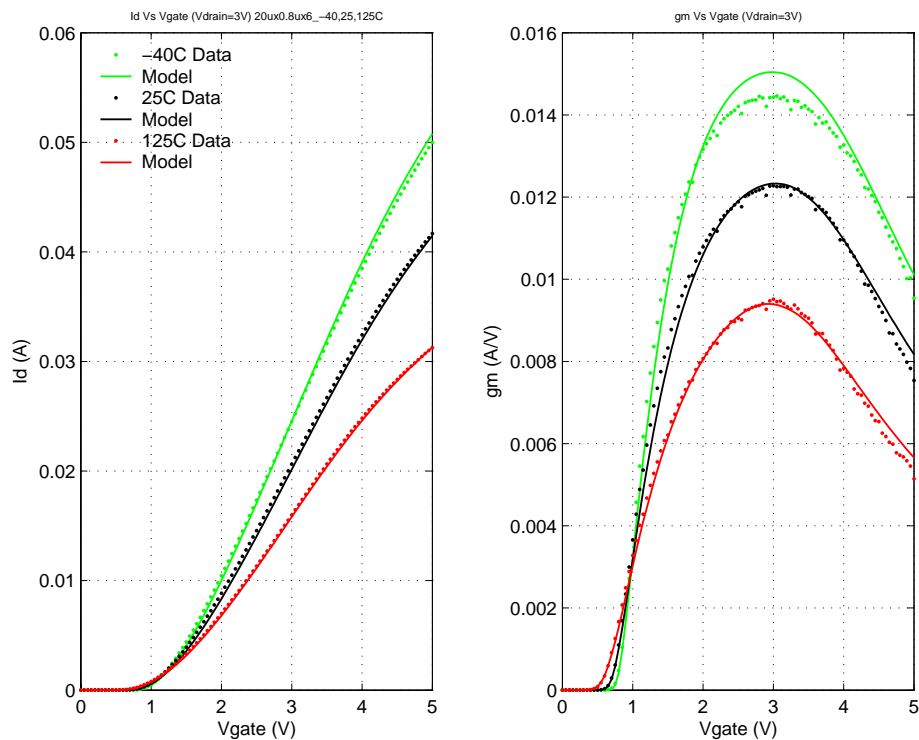
FIGURE 4.19 12V Isolated NFET (nfet5p0_Id12_iso); NFxWxL=6x20x0.8 μ m; Id Vs. Vgs; Vds=0.1VFIGURE 4.20 12V Isolated NFET (nfet5p0_Id12_iso); NFxWxL=6x20x0.8 μ m; Id Vs. Vgs; Vds=3V

FIGURE 4.21 12V Isolated NFET (nfet5p0_Id12_iso); NFxWxL=6x20x0.8 μ m; Id Vs. Vgs; Vds=6V

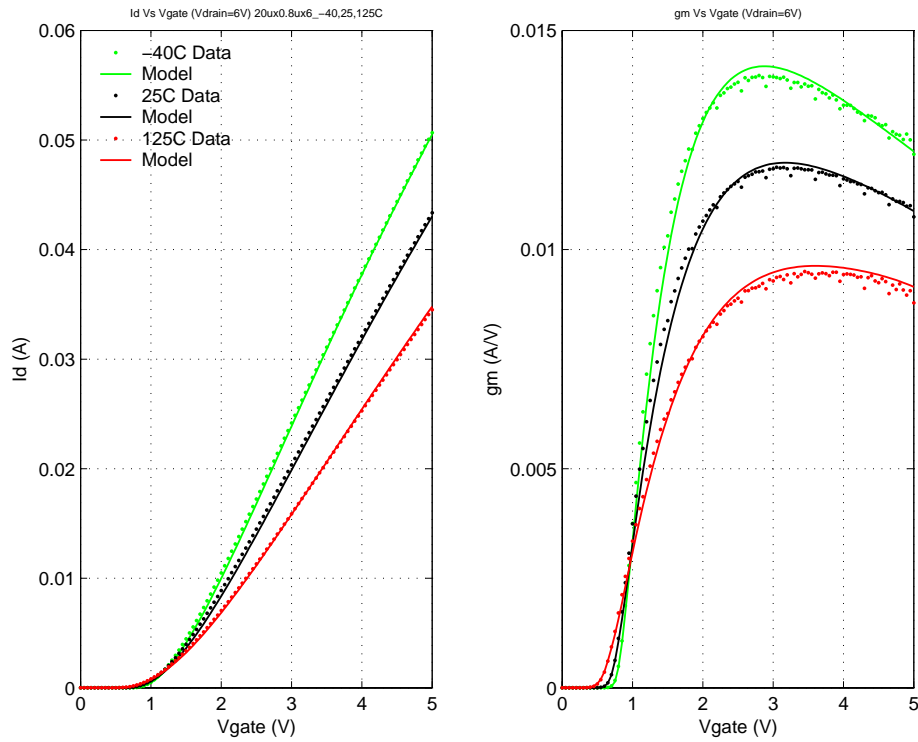


FIGURE 4.22 12V Isolated NFET (nfet5p0_Id12_iso); NFxWxL=6x20x0.8 μ m; Id Vs. Vgs; Vds=9V

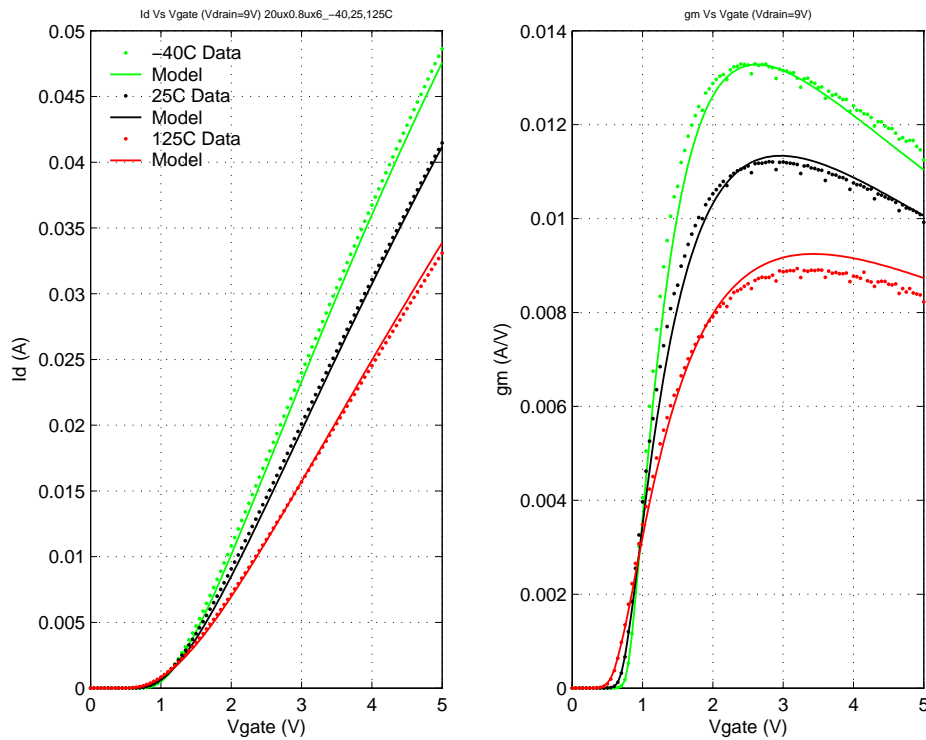


FIGURE 4.23 12V Isolated NFET (nfet5p0_Id12_iso); NFxWxL=6x20x0.8 μ m; Id Vs. Vgs; Vds=12V

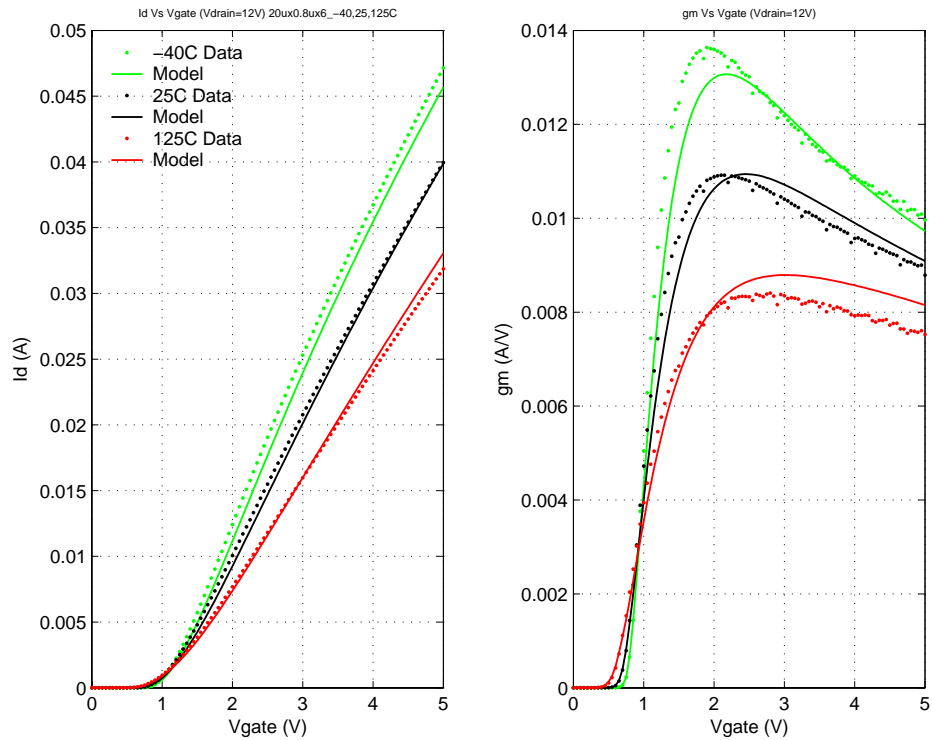


FIGURE 4.24 12V Iso. NFET(nfet5p0_Id12_iso);NFxWxL=6x20x0.8 μ m; Id Vs. Vds; Vgs=0,1,...5V; 25C

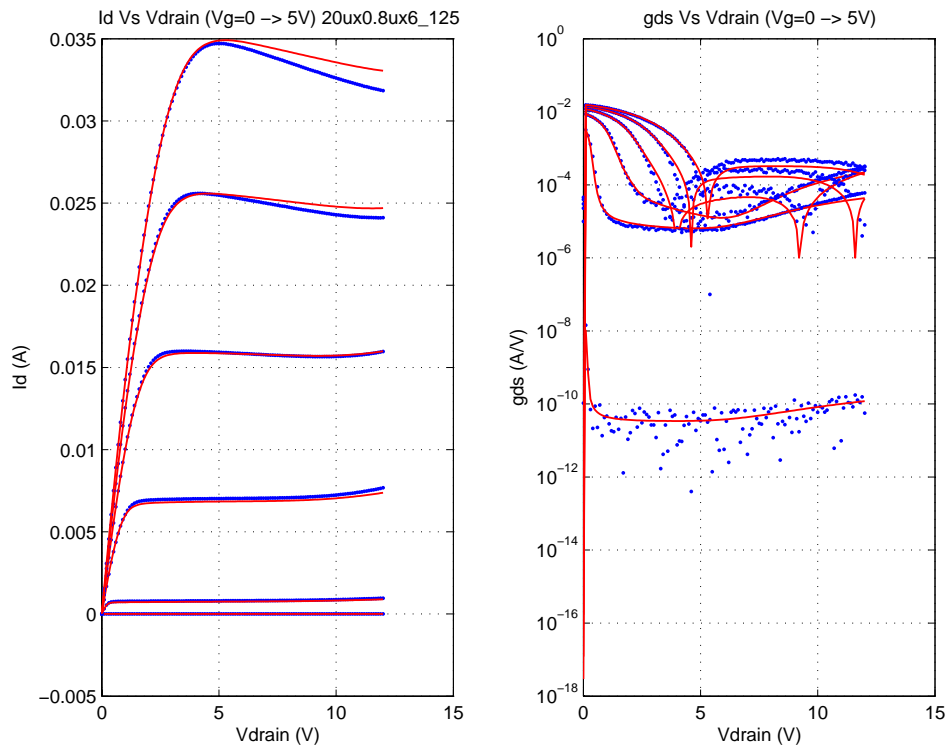


FIGURE 4.25 12V PFET (pfet5p0_Id12); NFxWxL=6x10x0.7 μ m; Id Vs. Vgs; Vds=-0.1V

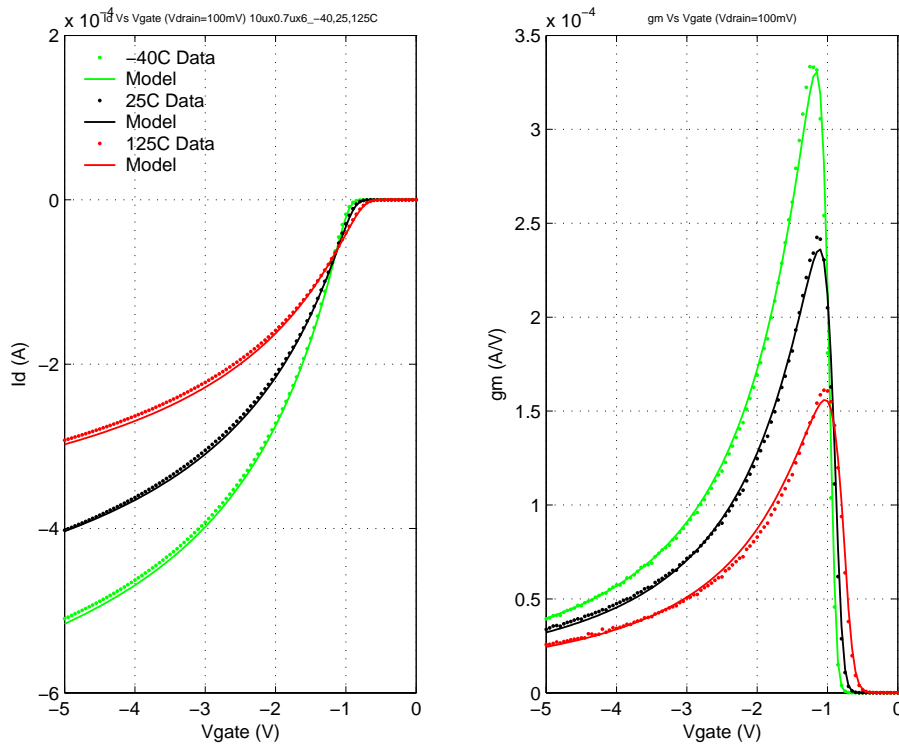


FIGURE 4.26 12V PFET (pfet5p0_Id12); NFxWxL=6x10x0.7 μ m; Id Vs. Vgs; Vds=-3V

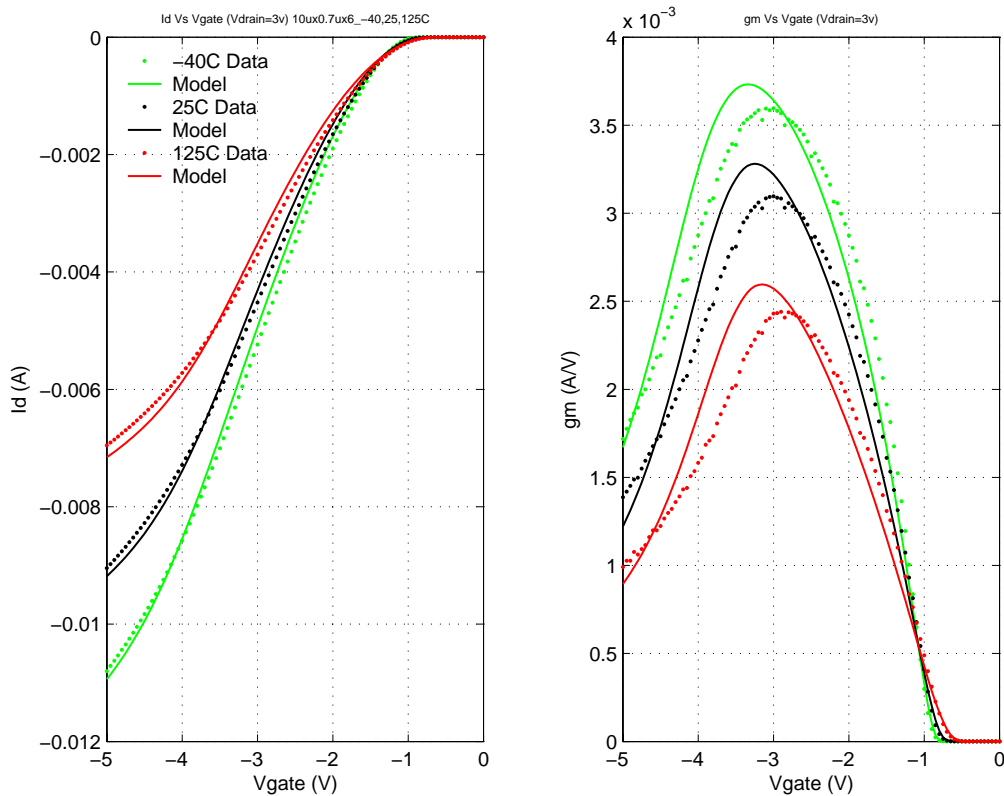


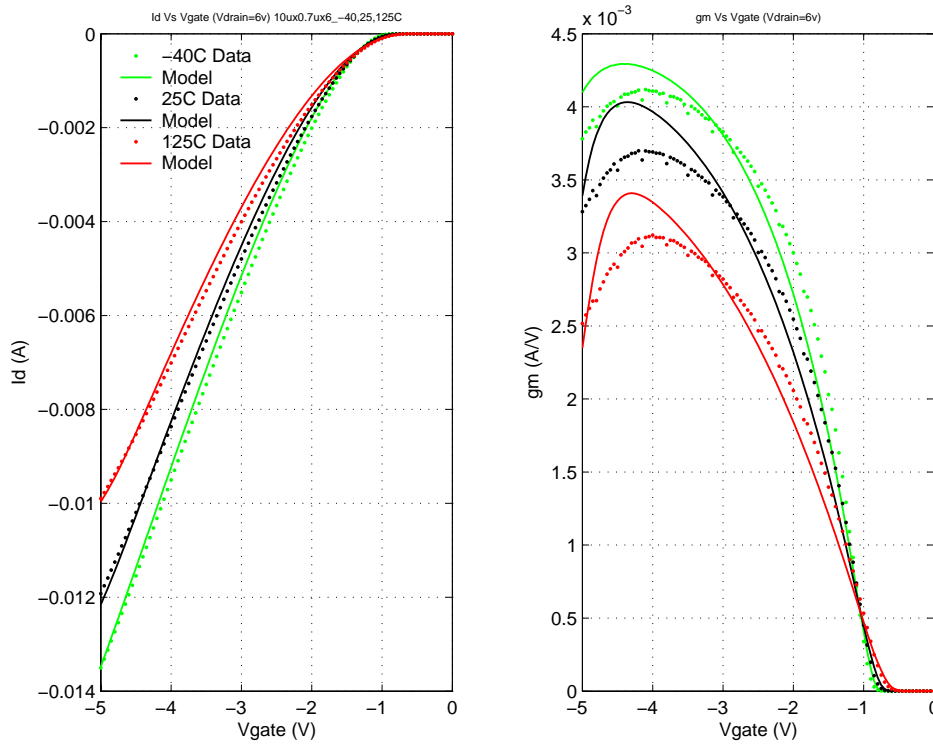
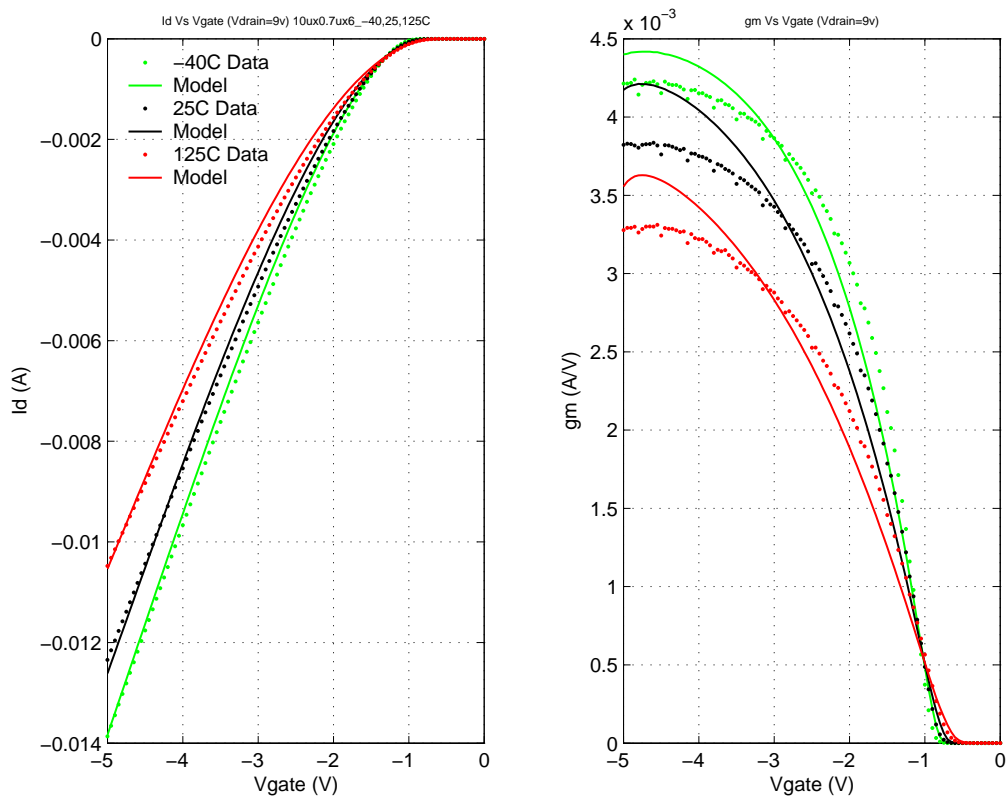
FIGURE 4.27 12V PFET (pfet5p0_Id12); NFxWxL=6x10x0.7 μ m; Id Vs. Vgs; Vds=-6VFIGURE 4.28 12V PFET (pfet5p0_Id12); NFxWxL=6x10x0.7 μ m; Id Vs. Vgs; Vds=-9V

FIGURE 4.29 12V PFET (pfet5p0_id12); NFxWxL=6x10x0.7 μ m; Id Vs. Vgs; Vds=-12V

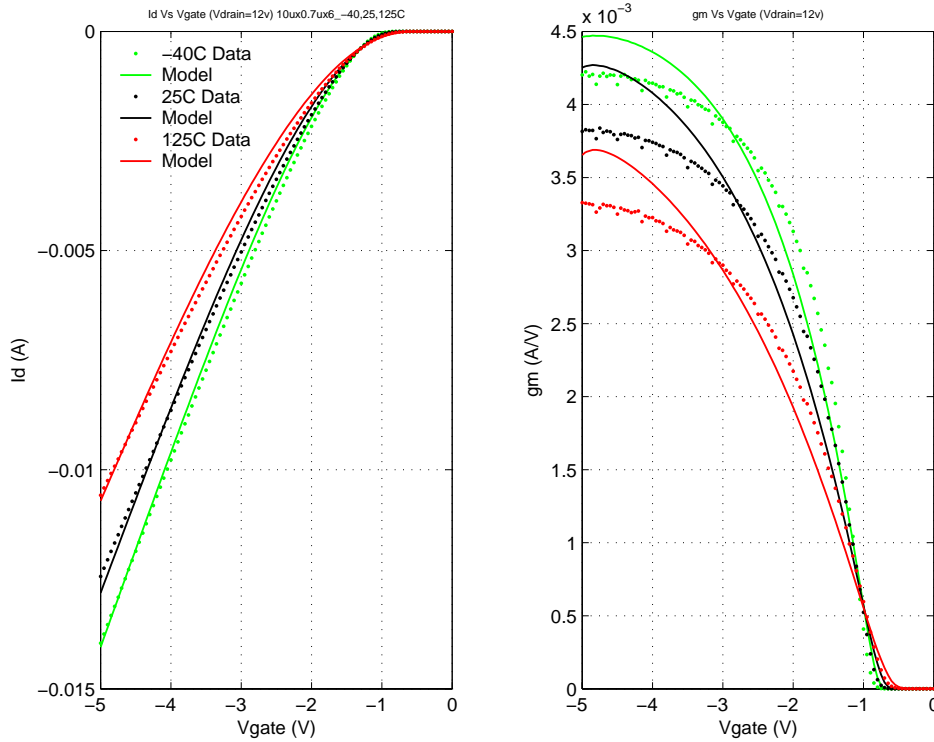


FIGURE 4.30 12V PFET; NFxWxL=6x10x0.7 μ m; Id Vs. Vds; Vgs=0,-1,...,-5V; Temp. = -40C

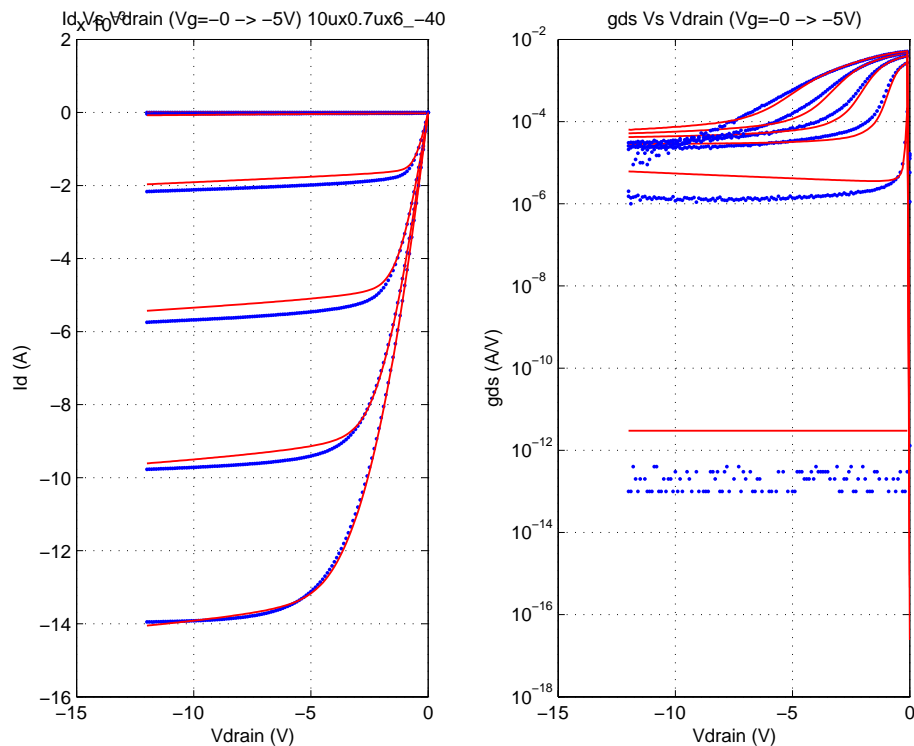


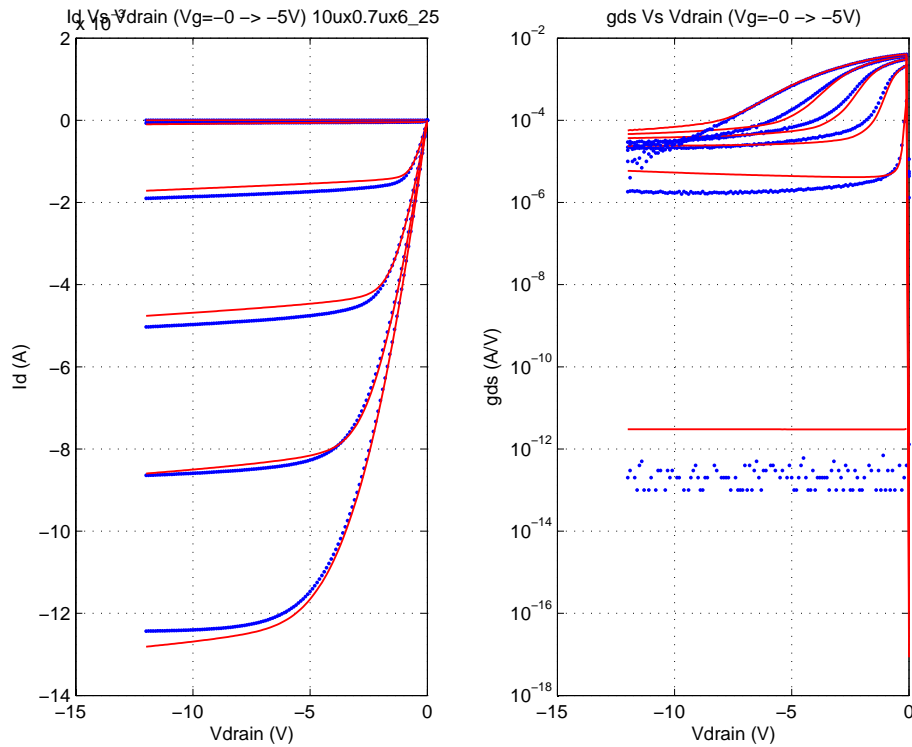
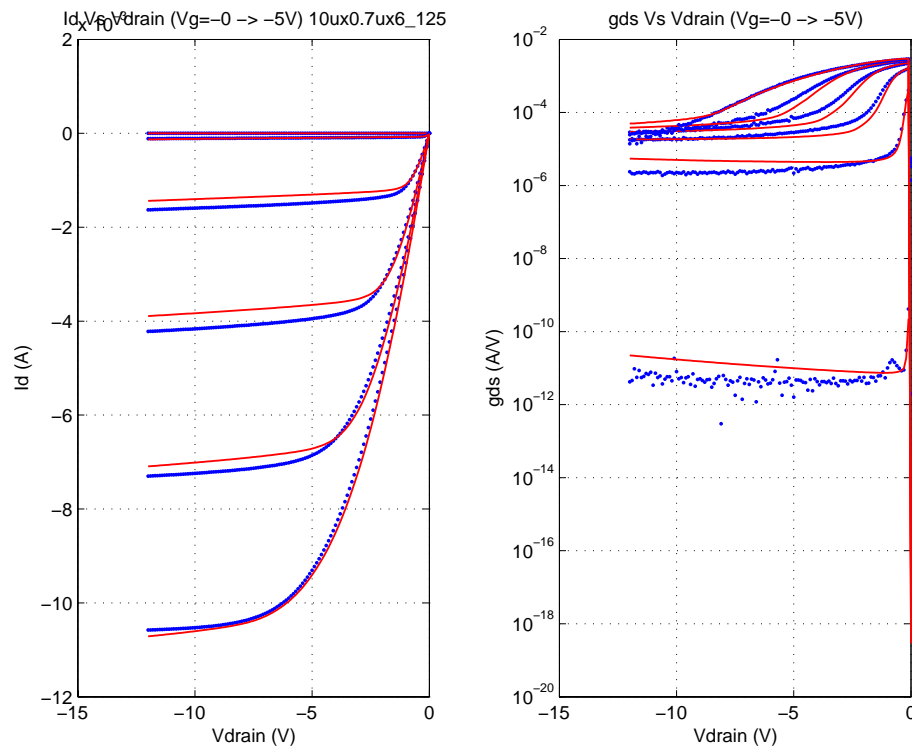
FIGURE 4.31 12V PFET; NFxWxL=6x10x0.7 μ m; Id Vs. Vds; Vgs=0,-1,...,-5V; Temp. = 25C

FIGURE 4.32 12V PFET; NFxWxL=6x10x0.7 μ m; Id Vs. Vds; Vgs=0,-1,...,-5V; Temp. = 125C


FIGURE 4.33 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vgs; Vds=0.1V

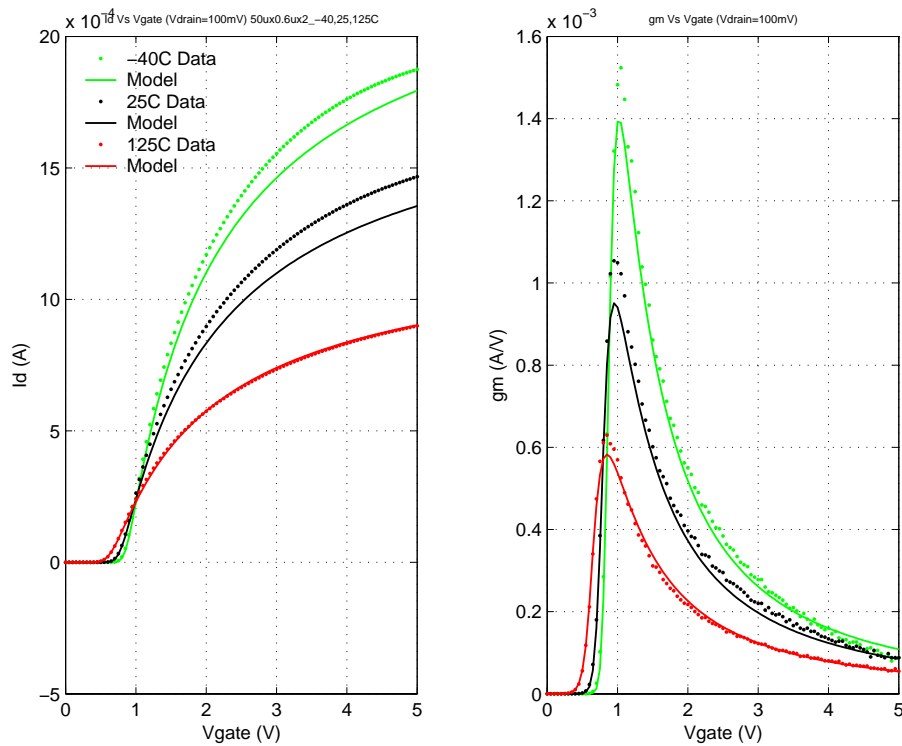


FIGURE 4.34 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vgs; Vds=3V

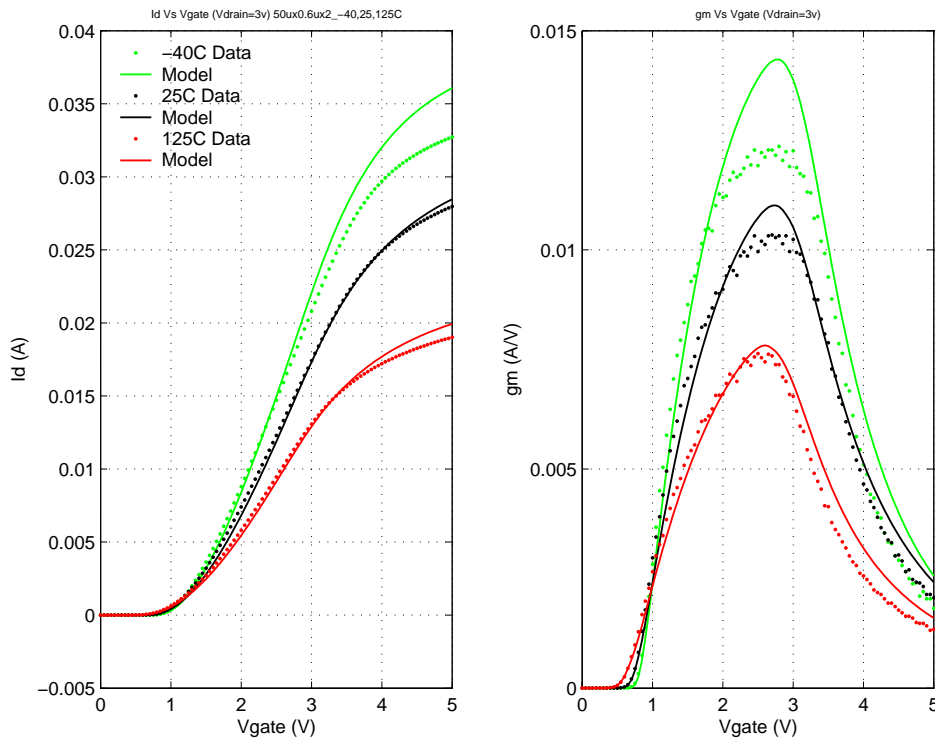


FIGURE 4.35 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vgs; Vds=5V

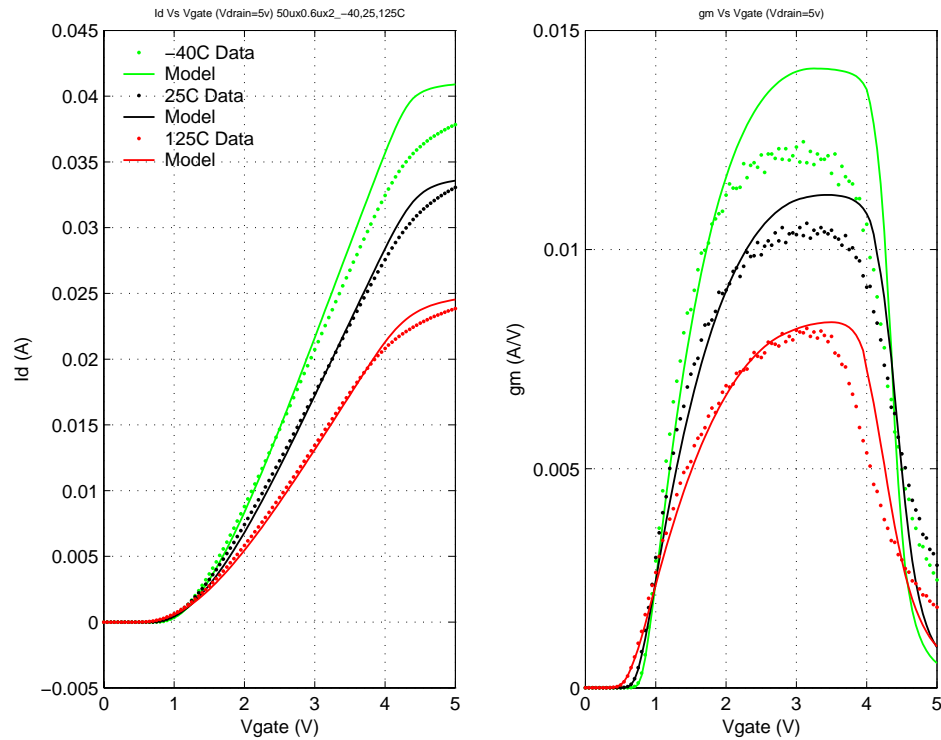


FIGURE 4.36 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vgs; Vds=10V

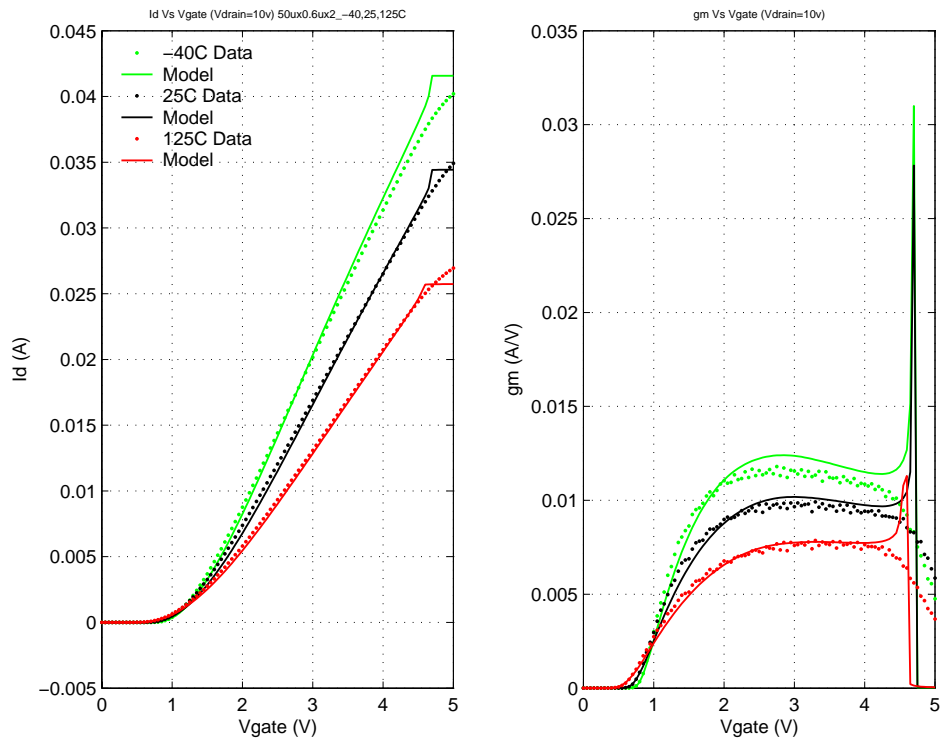


FIGURE 4.37 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vgs; Vds=20V

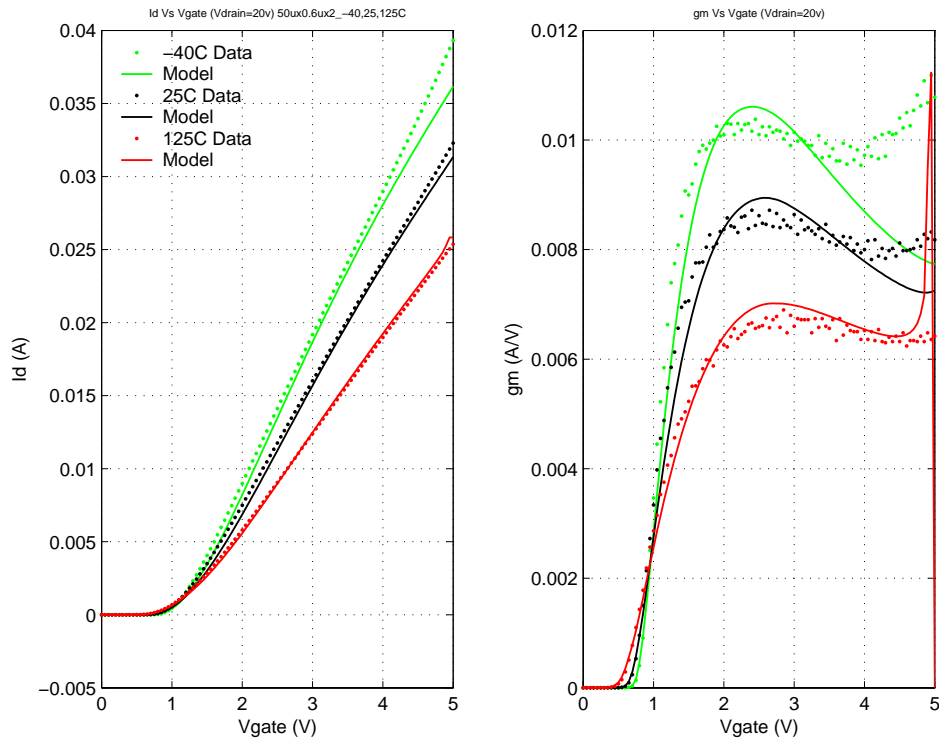


FIGURE 4.38 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vds; Vgs=0,1...5V; -40C

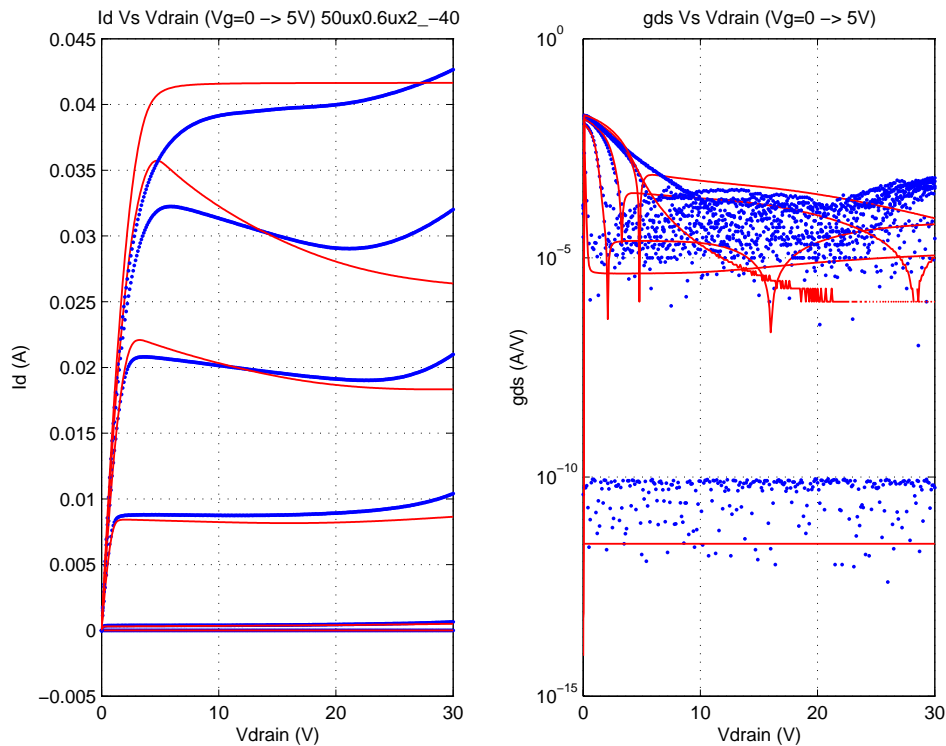


FIGURE 4.39 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vds; Vgs=0,1...5V; 25C

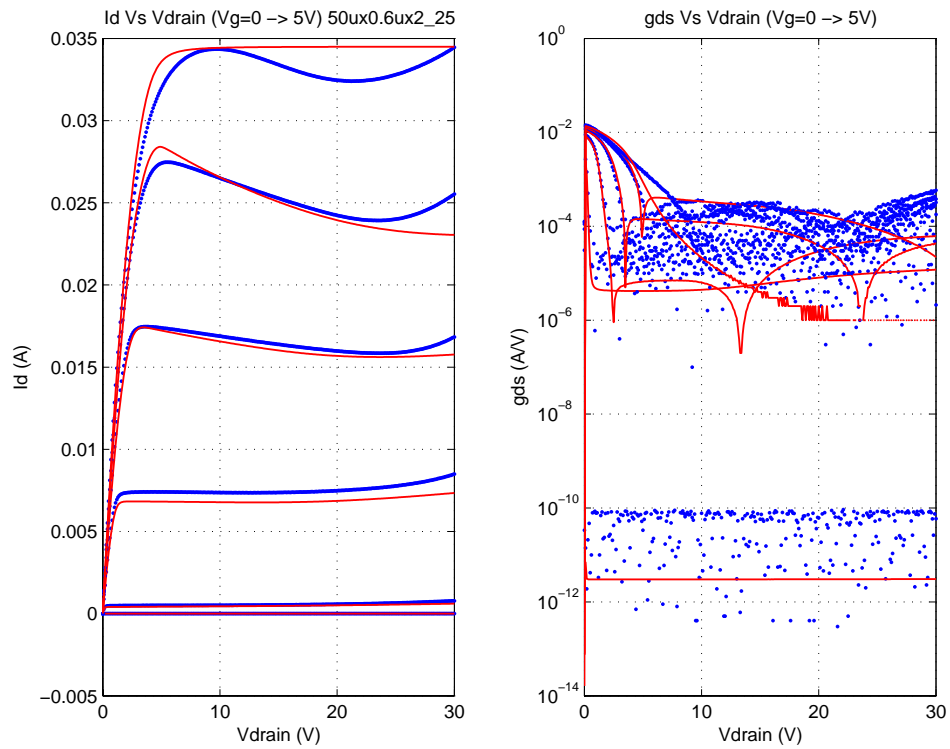


FIGURE 4.40 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_0.6 μ m; Id Vs. Vds; Vgs=0,1...5V; 125C

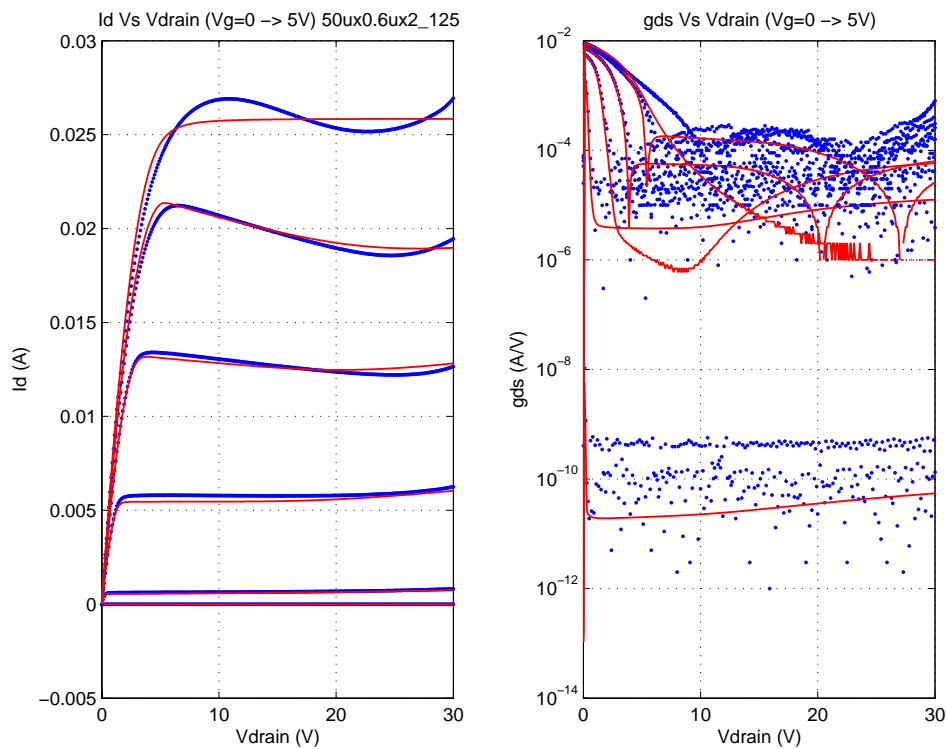


FIGURE 4.41 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vgs; Vds=0.1V

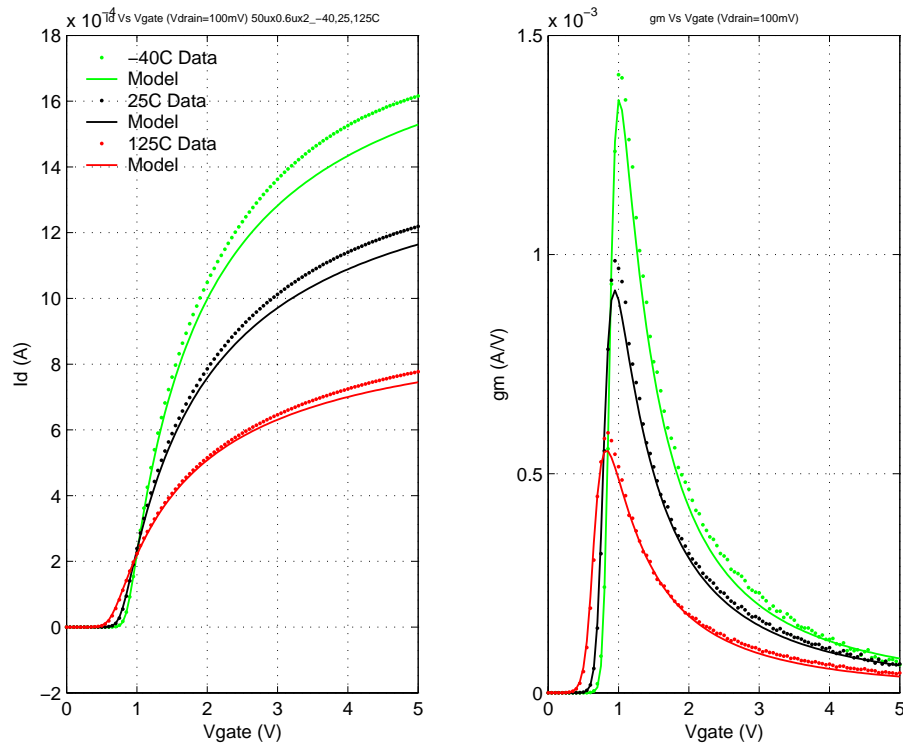


FIGURE 4.42 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vgs; Vds=3V

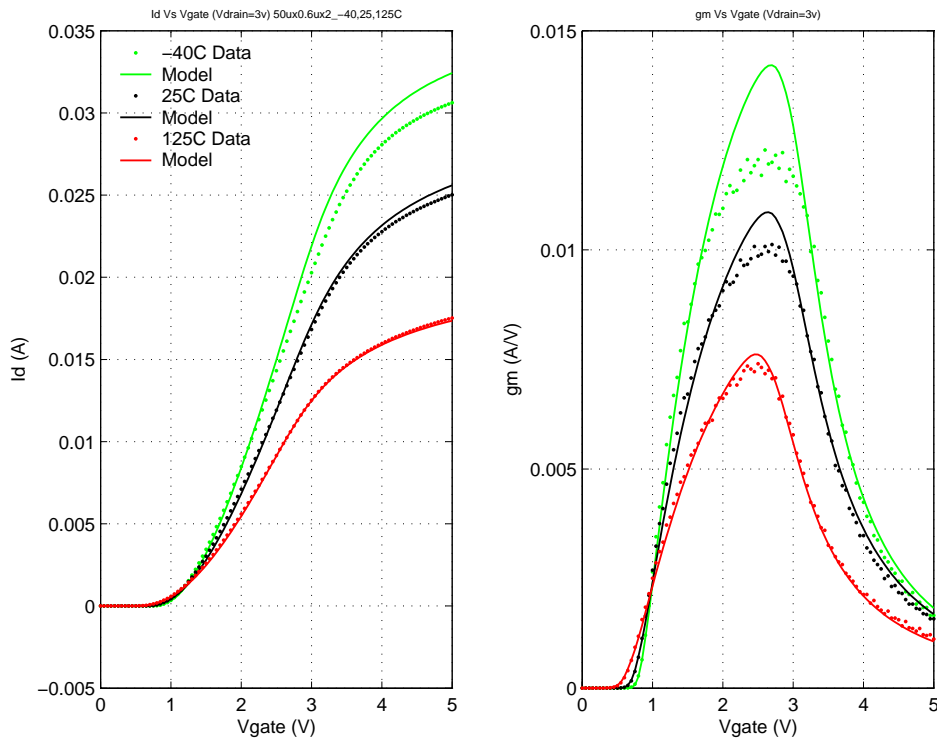


FIGURE 4.43 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vgs; Vds=5V

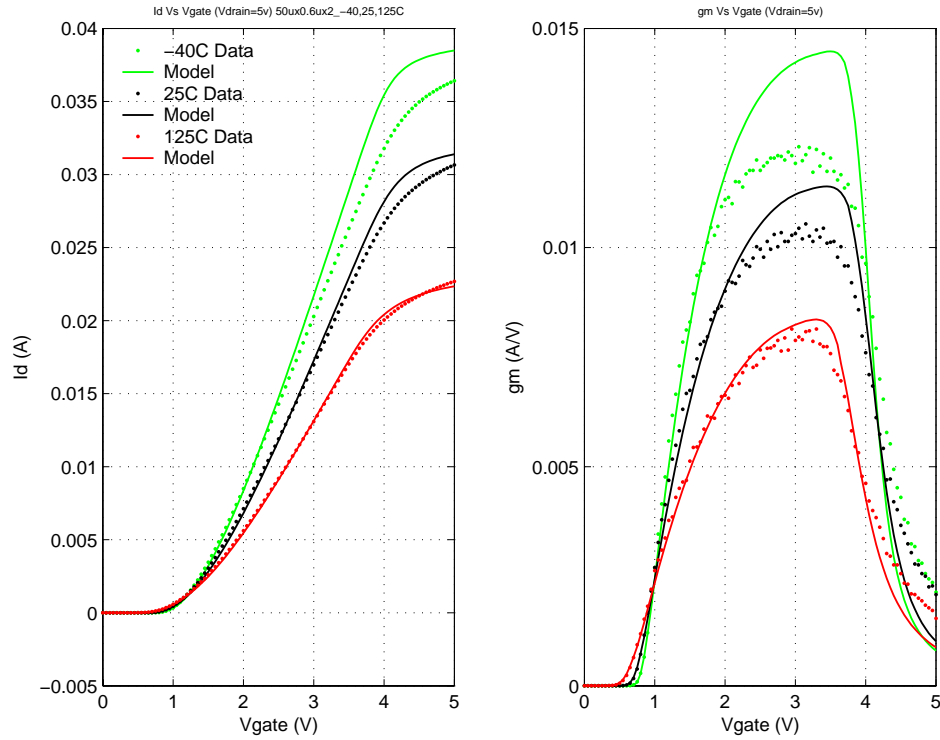


FIGURE 4.44 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vgs; Vds=10V

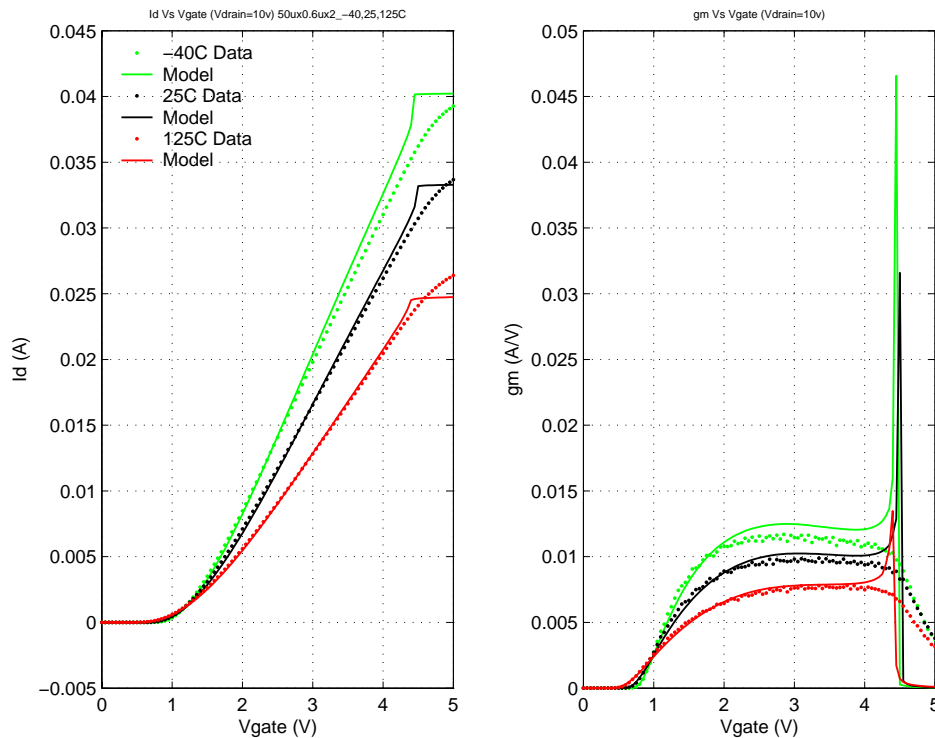


FIGURE 4.45 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vgs; Vds=20V

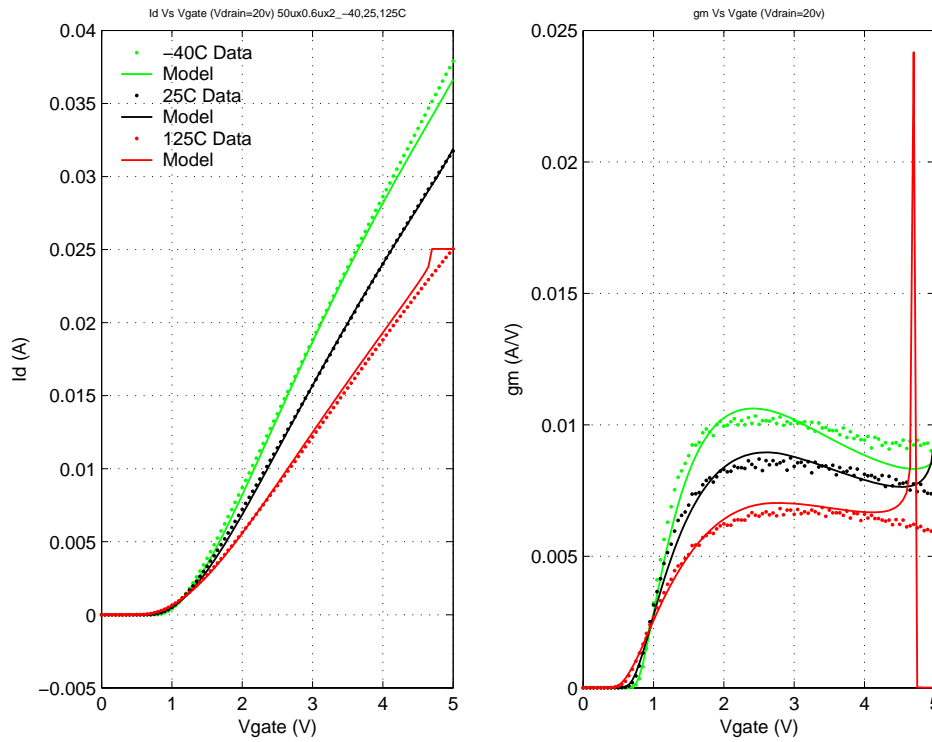


FIGURE 4.46 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vds; Vgs=0,1...5V; -40C

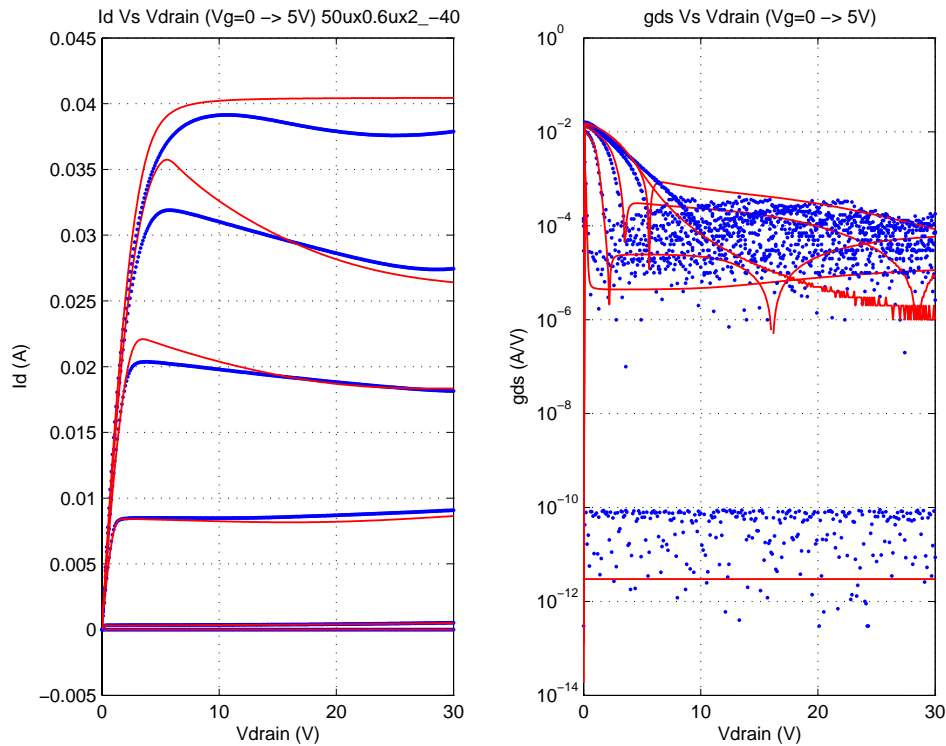


FIGURE 4.47 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vds; Vgs=0,1...5V; 25C

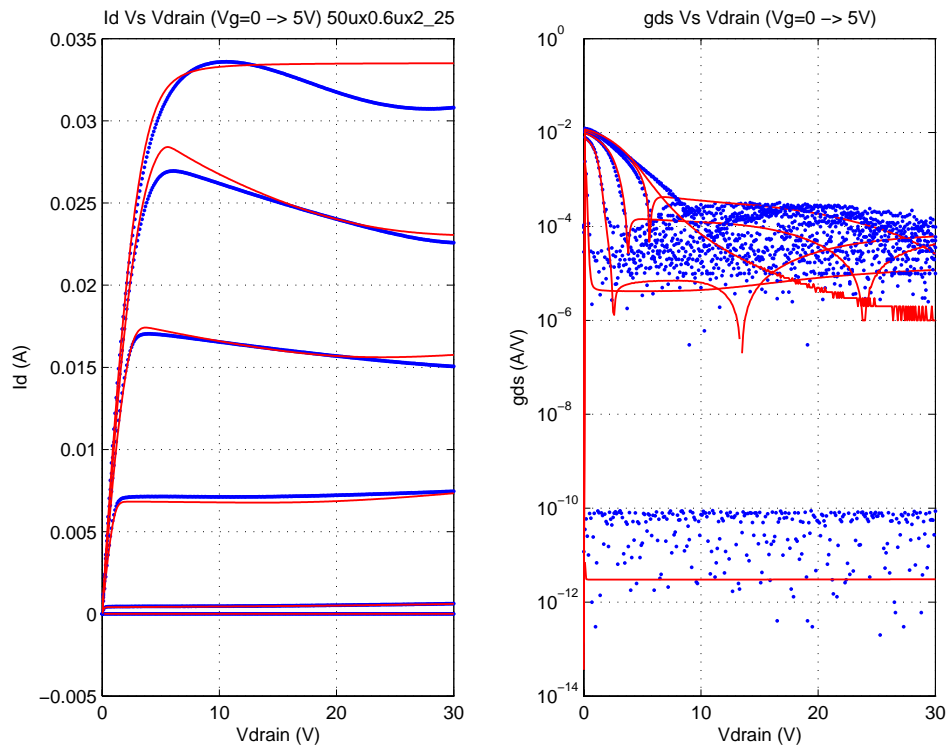


FIGURE 4.48 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.2 μ m; Id Vs. Vds; Vgs=0,1...5V; 125C

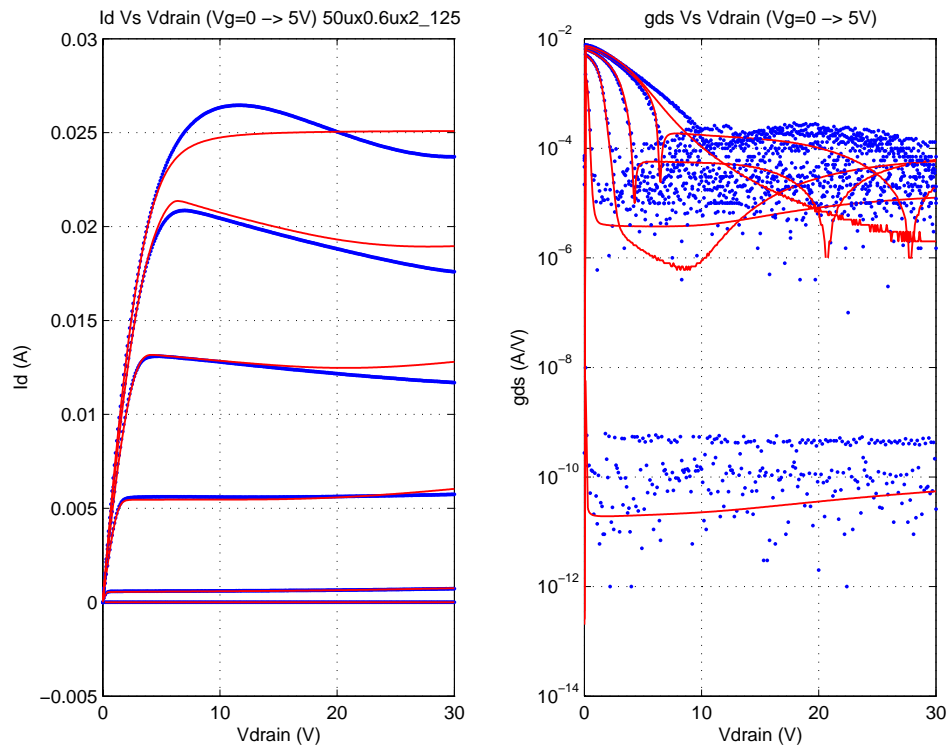


FIGURE 4.49 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.8 μ m; Id Vs. Vgs; Vds=0.1V

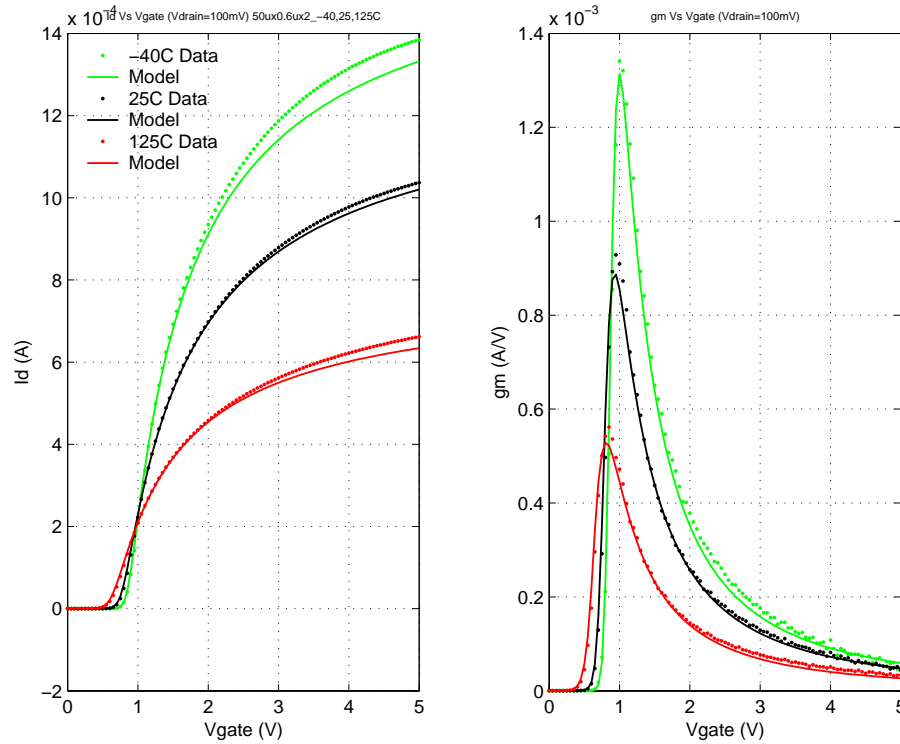


FIGURE 4.50 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.8 μ m; Id Vs. Vgs; Vds=3V

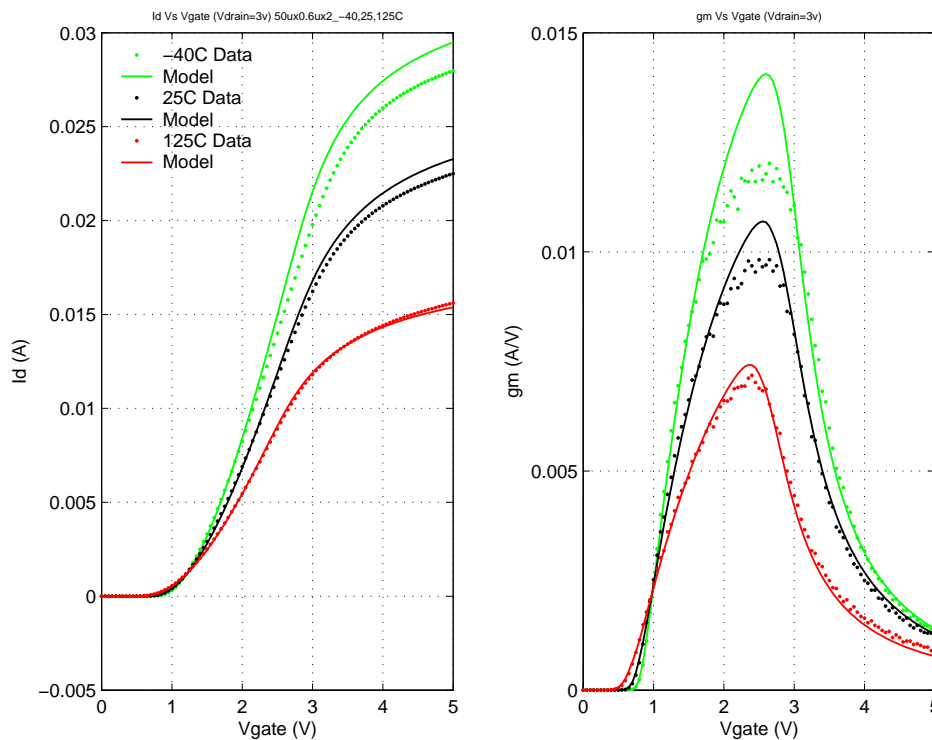


FIGURE 4.51 40V NFET (nfet5p0_id40); NFxWxL_id=2x50x0.8_1.8 μ m; Id Vs. Vgs; Vds=5V

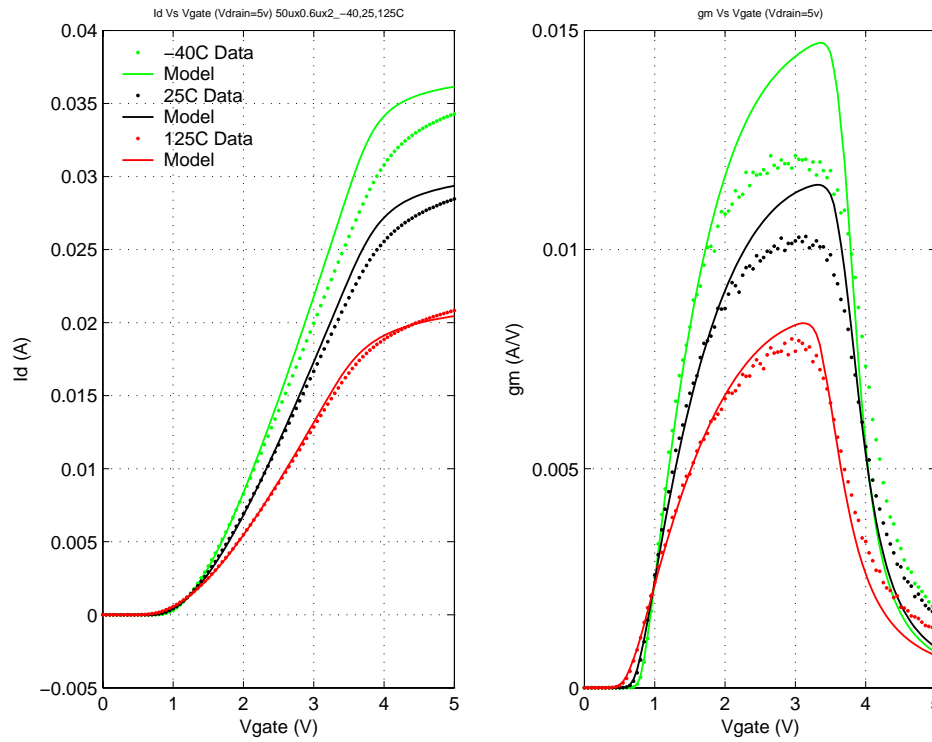


FIGURE 4.52 40V NFET (nfet5p0_id40); NFxWxL_id=2x50x0.8_1.8 μ m; Id Vs. Vgs; Vds=10V

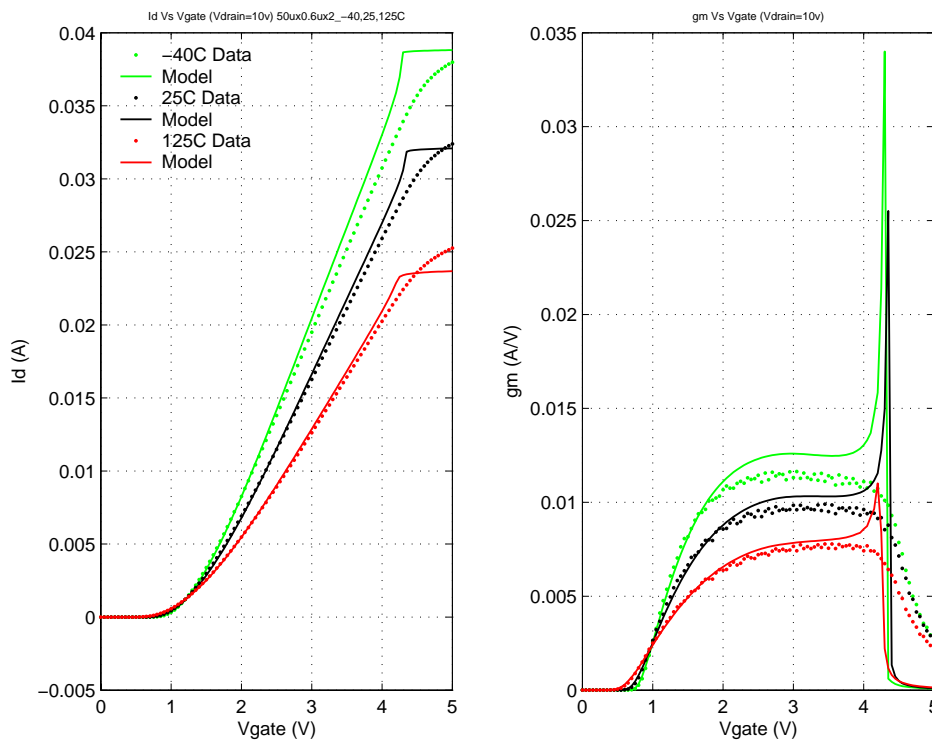


FIGURE 4.53 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.8 μ m; Id Vs. Vgs; Vds=20V

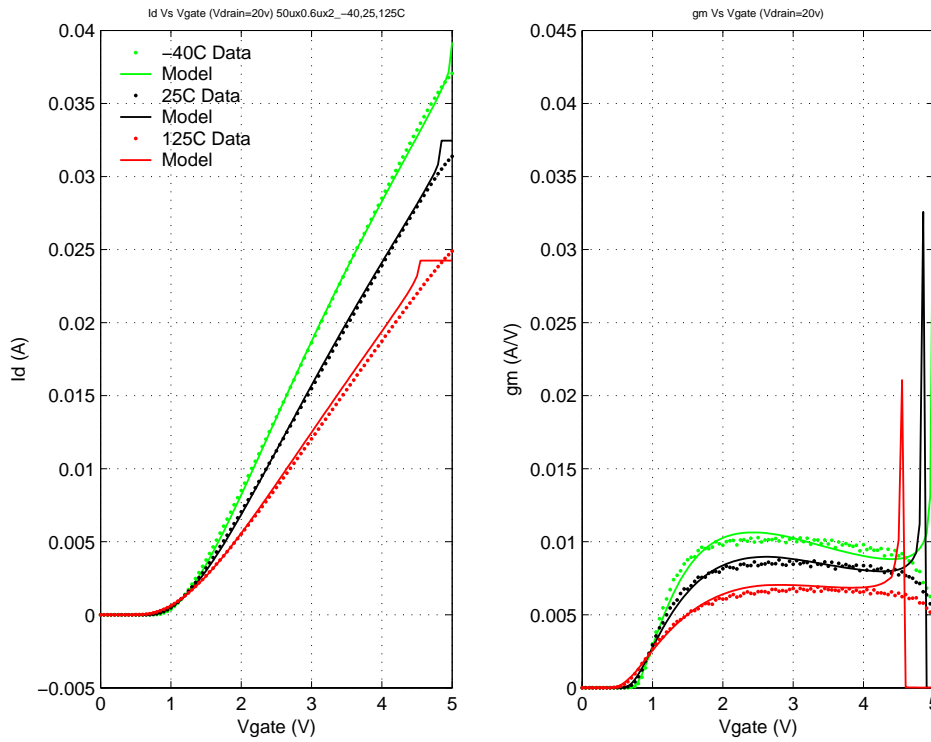


FIGURE 4.54 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.8 μ m; Id Vs. Vds; Vgs=0,1...5V; -40C

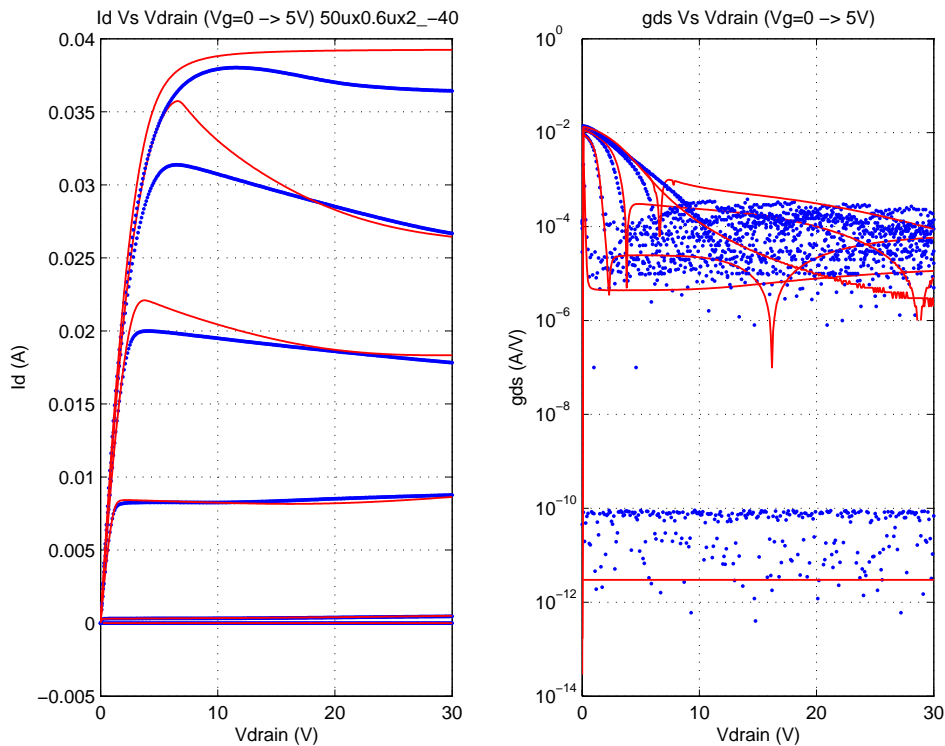


FIGURE 4.55 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.8 μ m; Id Vs. Vds; Vgs=0,1...5V; 25C

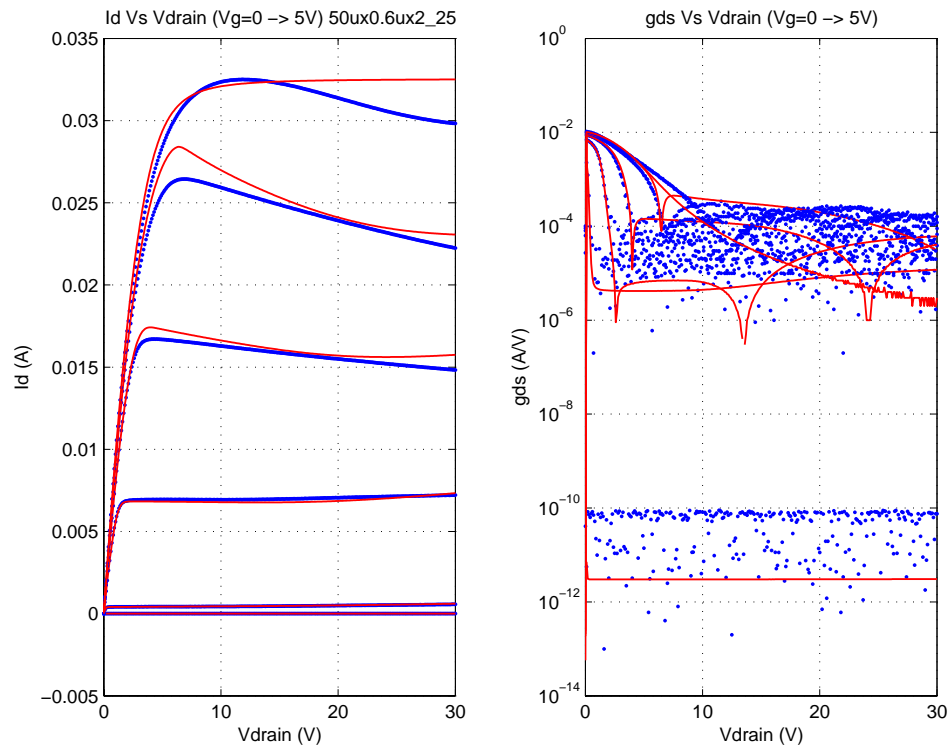


FIGURE 4.56 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_1.8 μ m; Id Vs. Vds; Vgs=0,1...5V; 125C

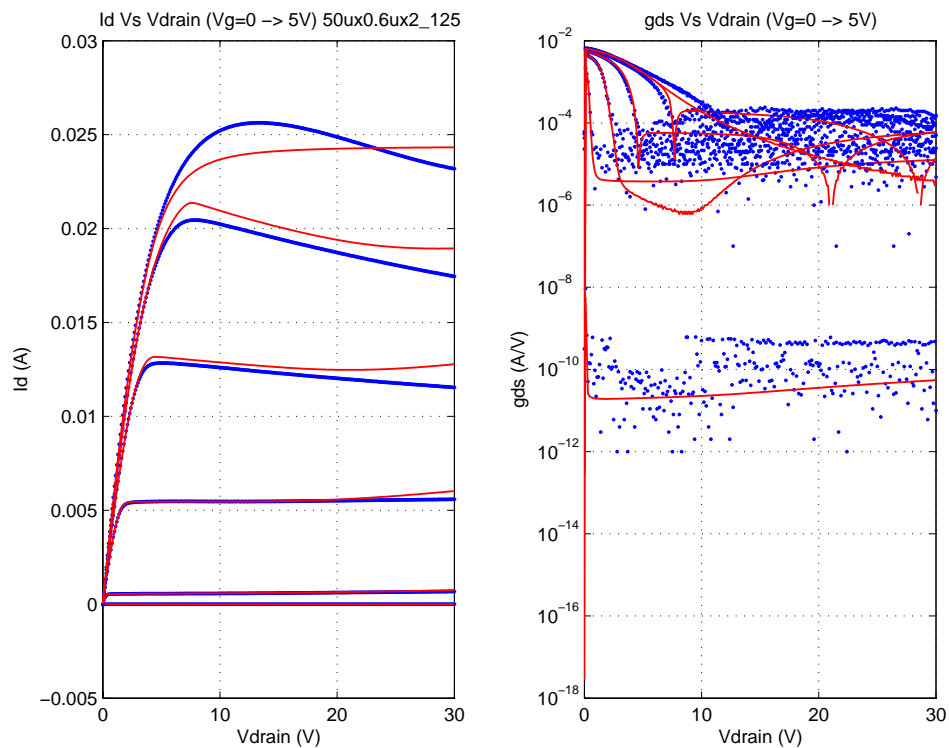


FIGURE 4.57 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vgs; Vds=0.1V

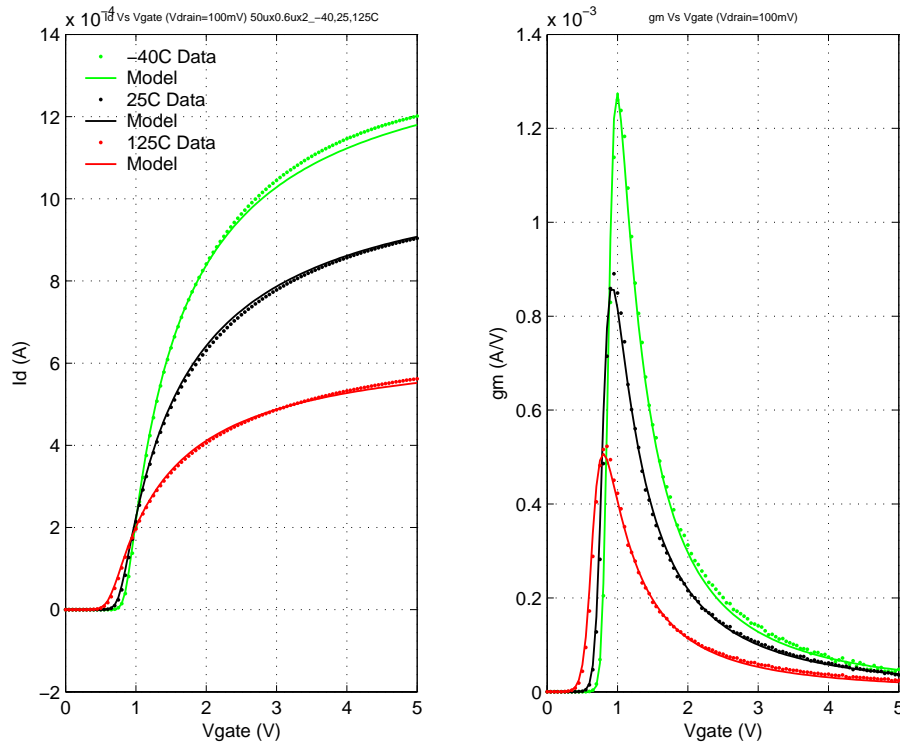


FIGURE 4.58 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vgs; Vds=3V

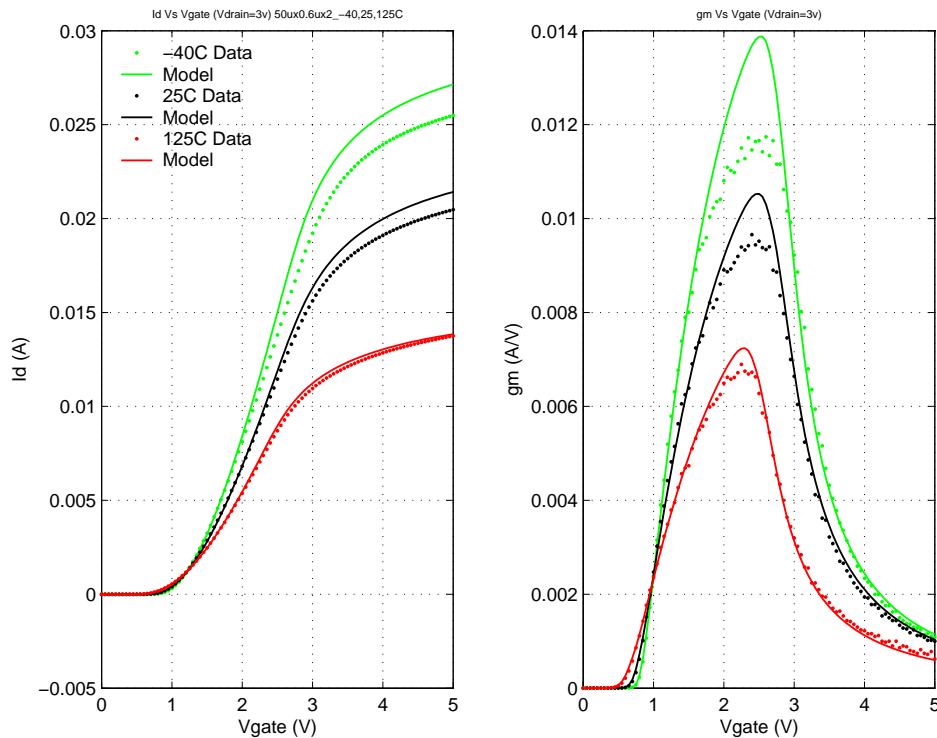


FIGURE 4.59 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vgs; Vds=5V

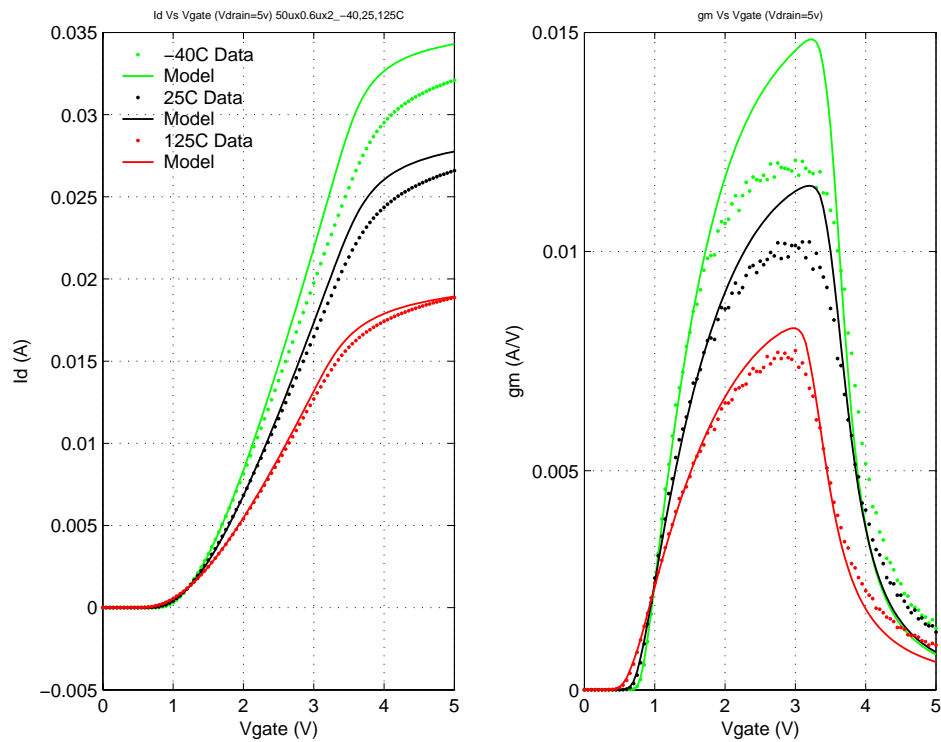


FIGURE 4.60 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vgs; Vds=10V

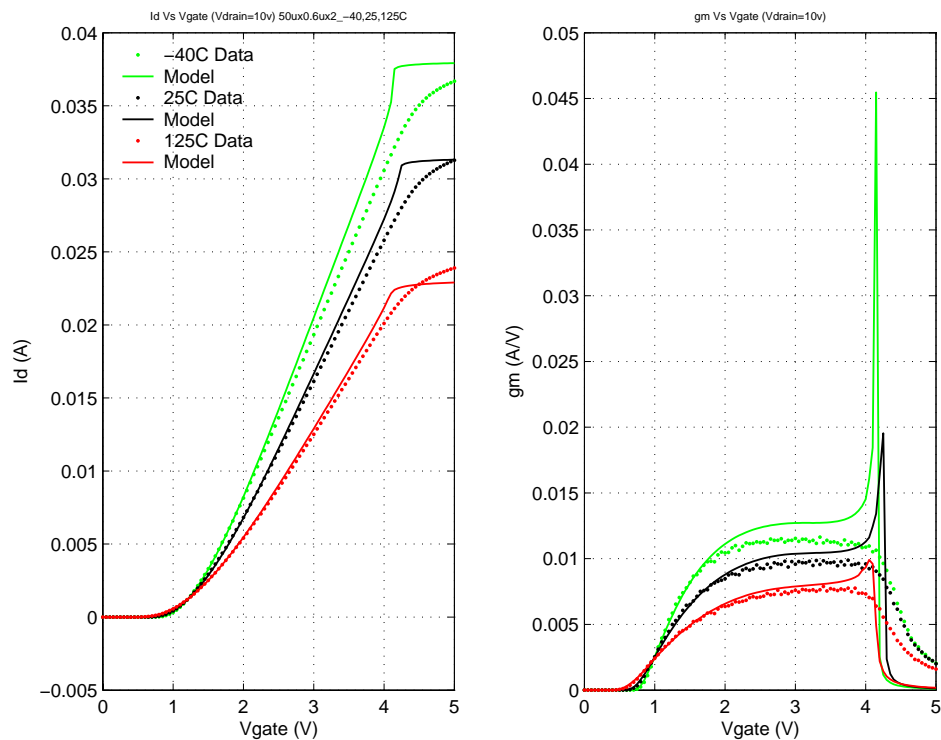


FIGURE 4.61 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vgs; Vds=20V

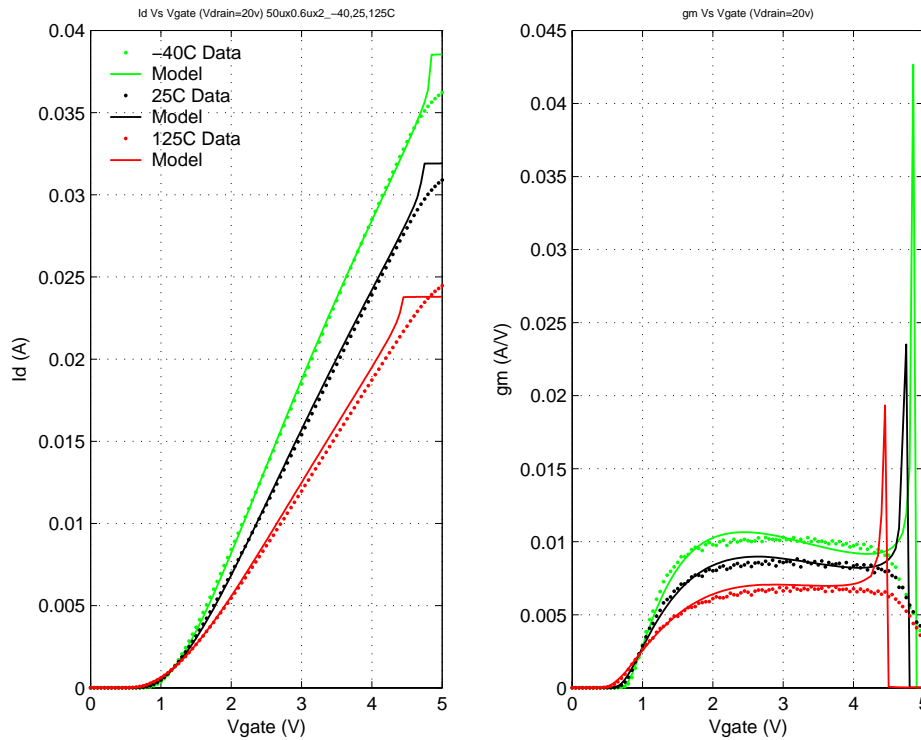


FIGURE 4.62 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vds; Vgs=0,1...5V; -40C

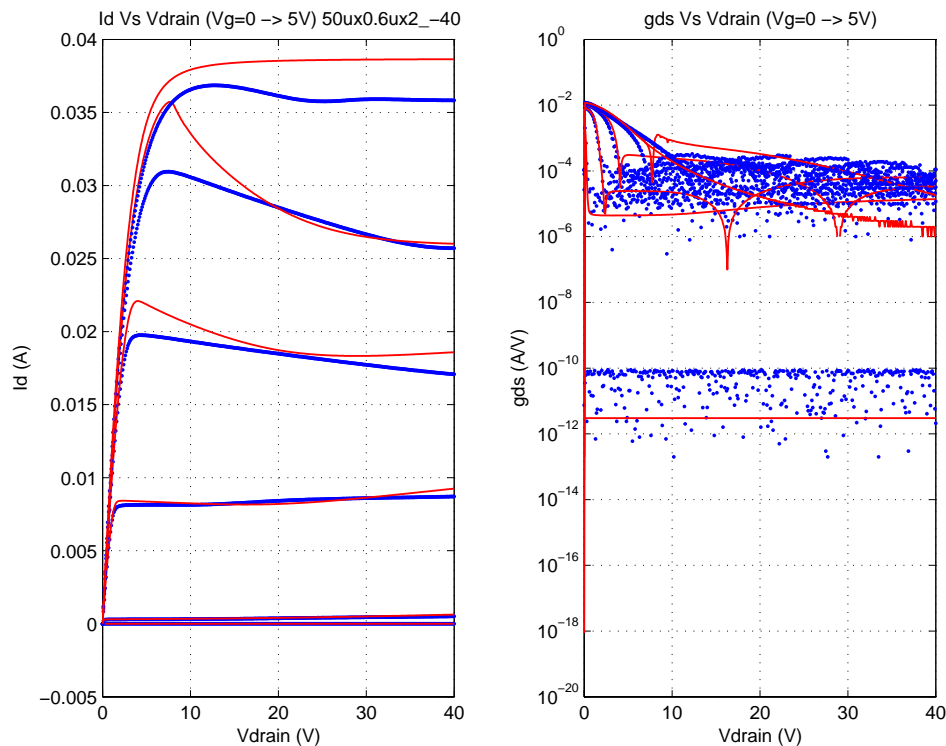
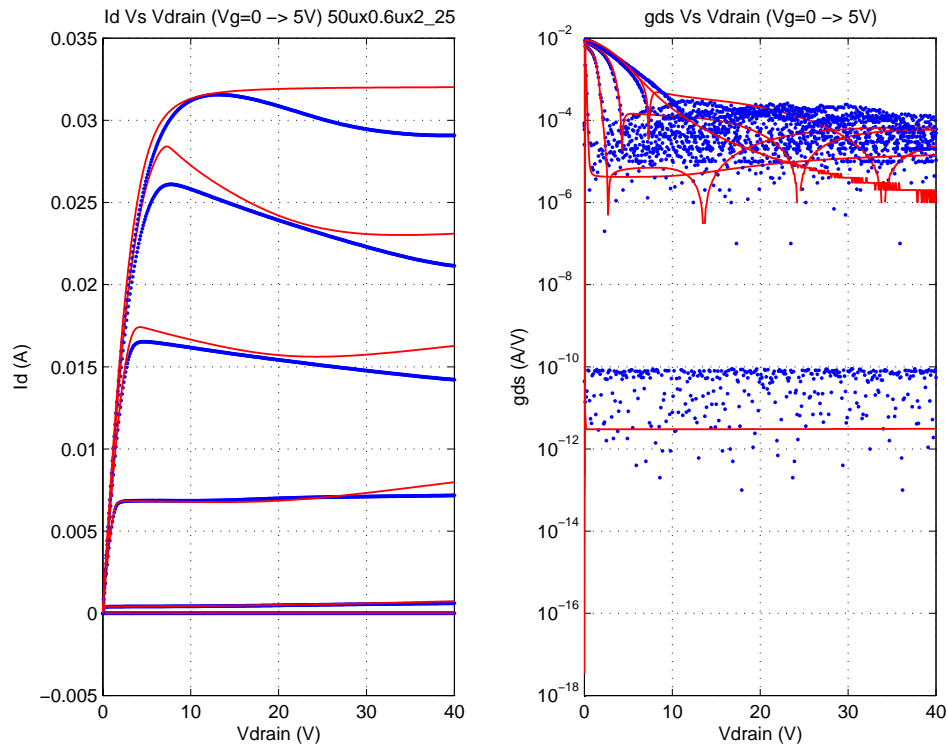


FIGURE 4.63 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vds; Vgs=0,1...5V; 25C



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FIGURE 4.64 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_2.4 μ m; Id Vs. Vds; Vgs=0,1...5V; 125C

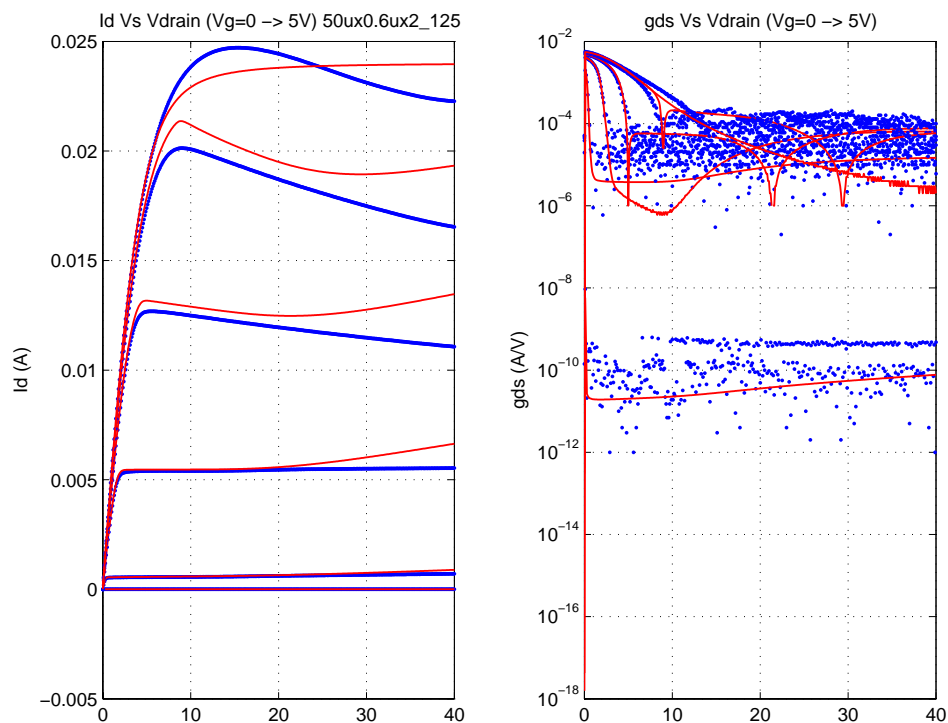


FIGURE 4.65 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vgs; Vds=0.1V

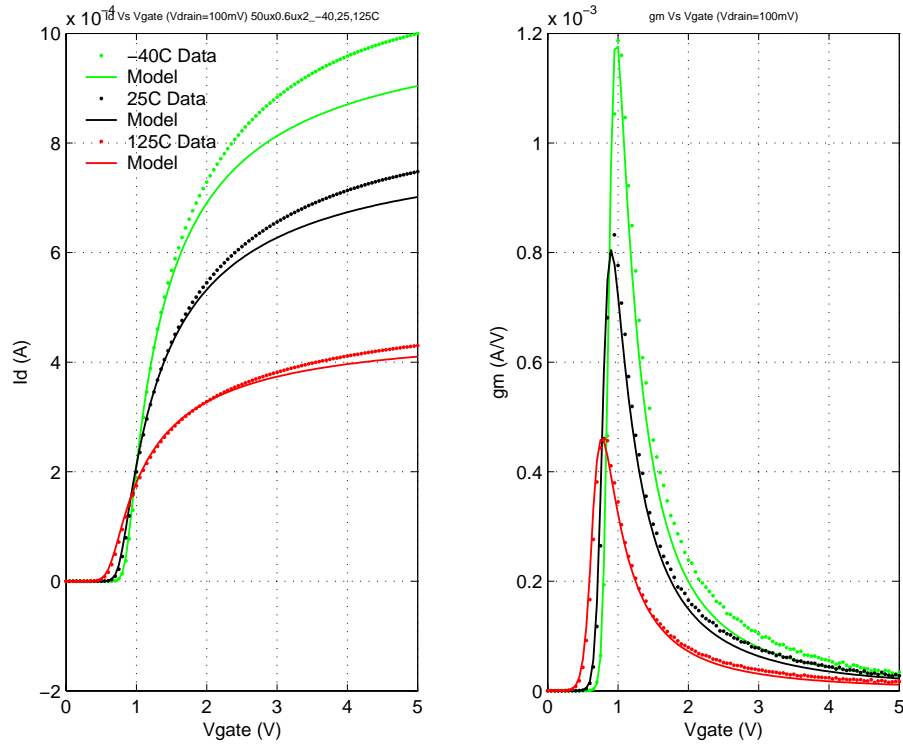


FIGURE 4.66 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vgs; Vds=3V

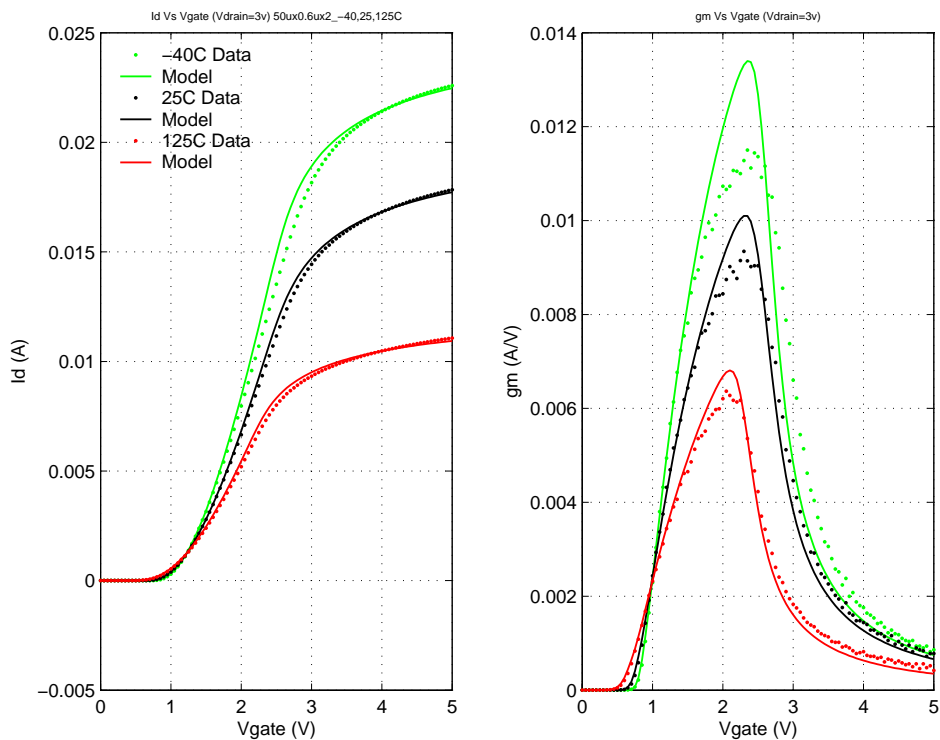


FIGURE 4.67 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vgs; Vds=5V

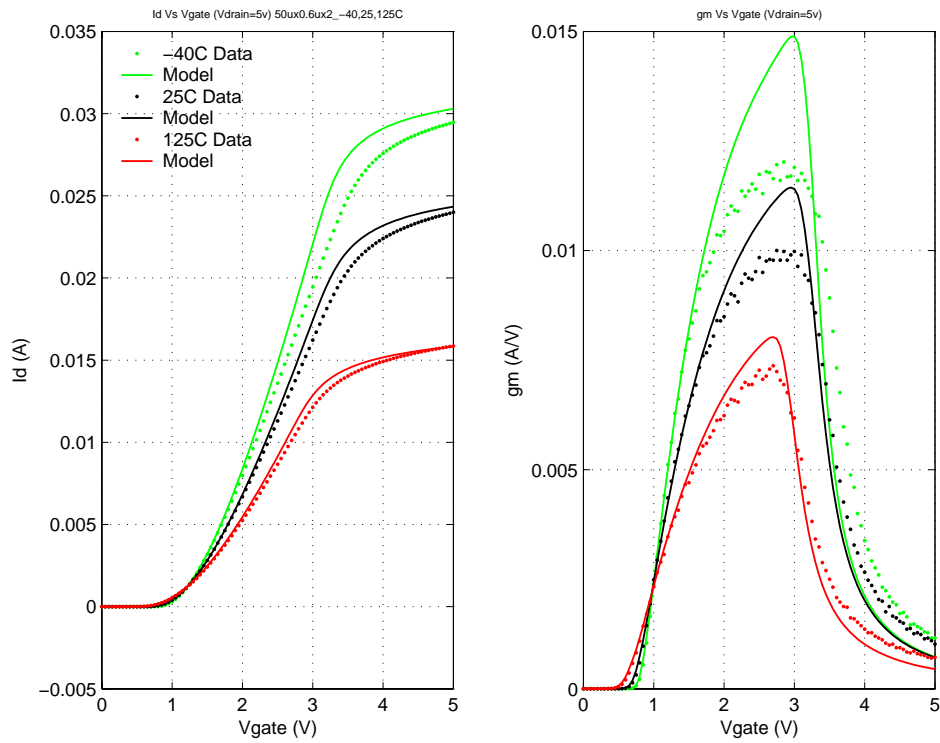


FIGURE 4.68 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vgs; Vds=10V

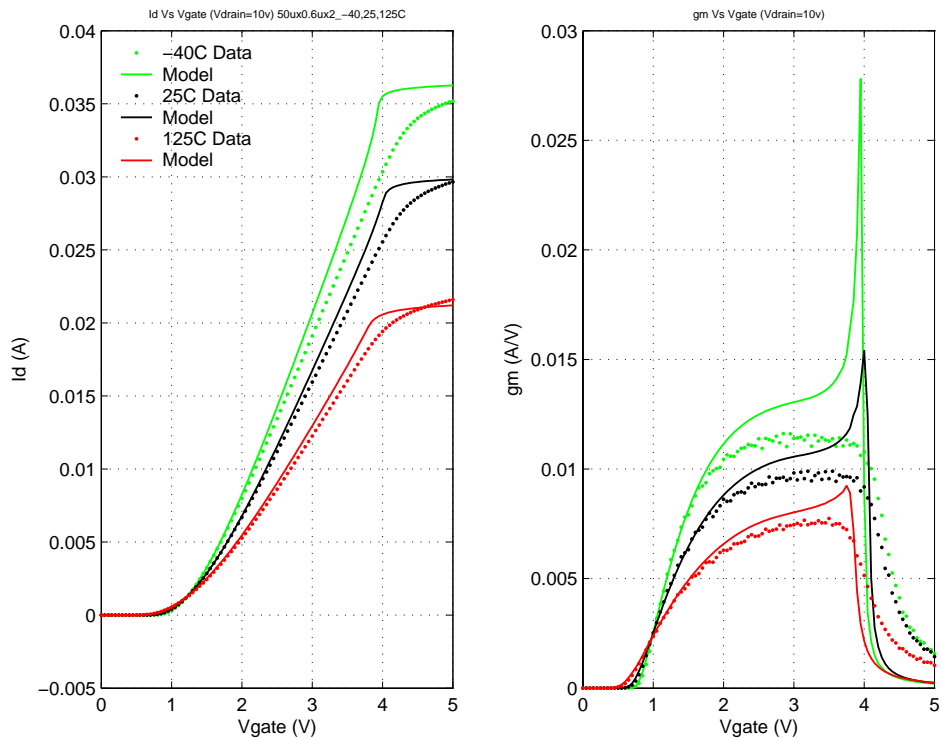


FIGURE 4.69 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vgs; Vds=20V

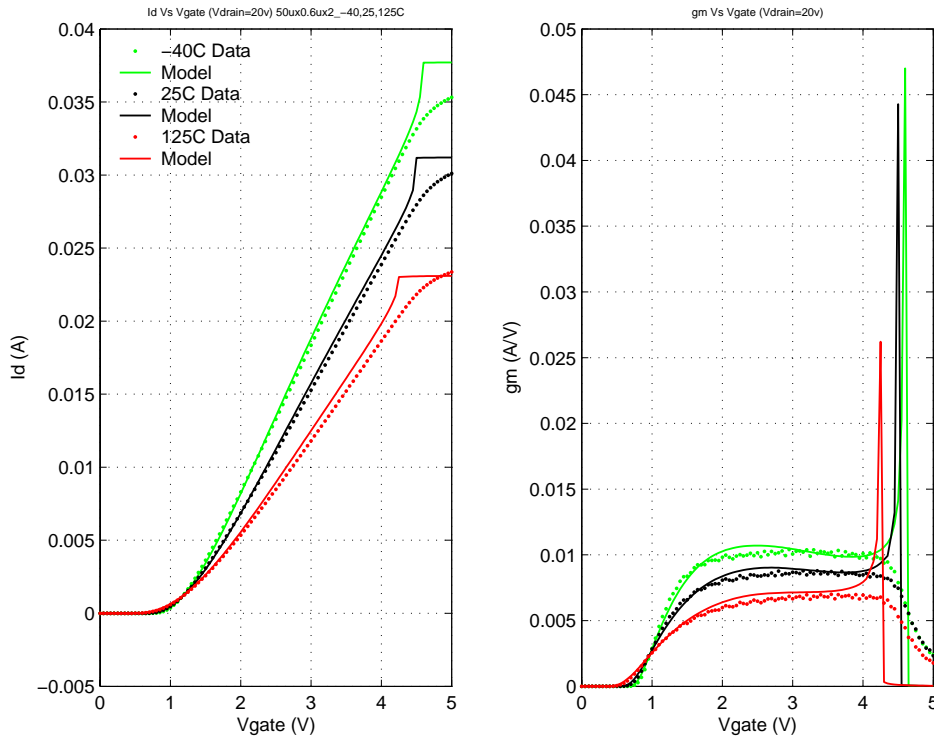


FIGURE 4.70 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vds; Vgs=0,1...5V; -40C

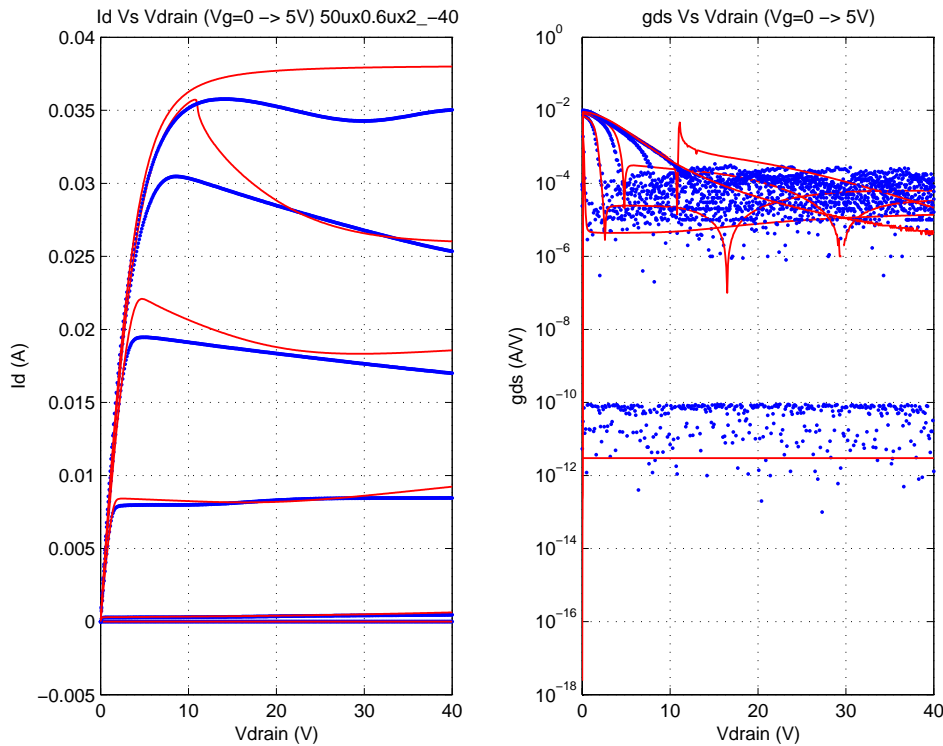
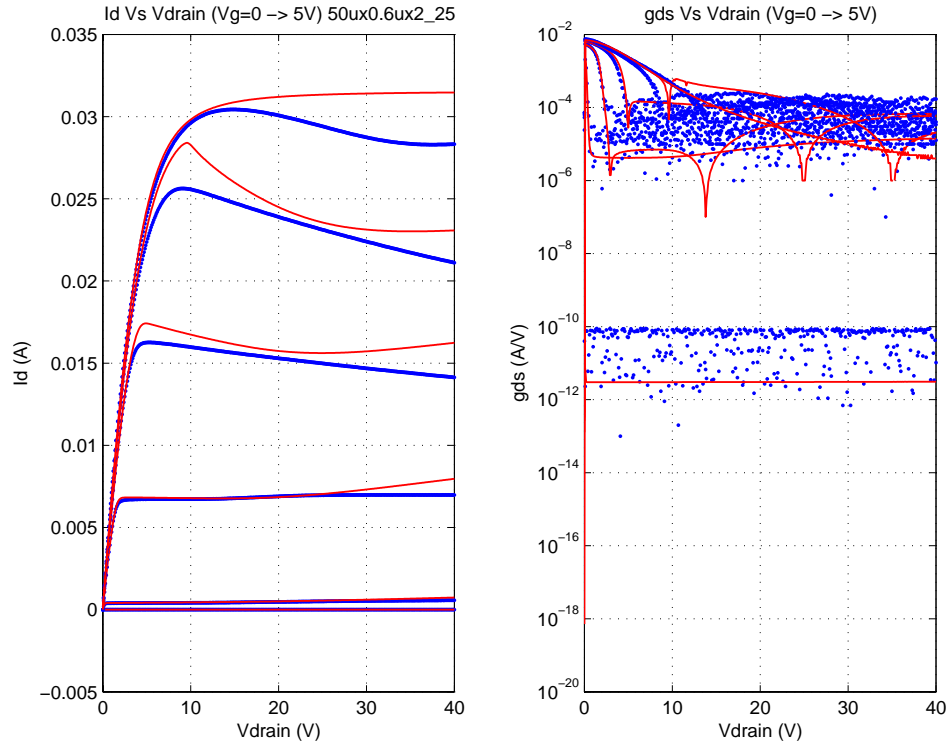


FIGURE 4.71 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vds; Vgs=0,1...5V; 25C



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FIGURE 4.72 40V NFET (nfet5p0_Id40); NFxWxL_Id=2x50x0.8_4 μ m; Id Vs. Vds; Vgs=0,1...5V; 125C

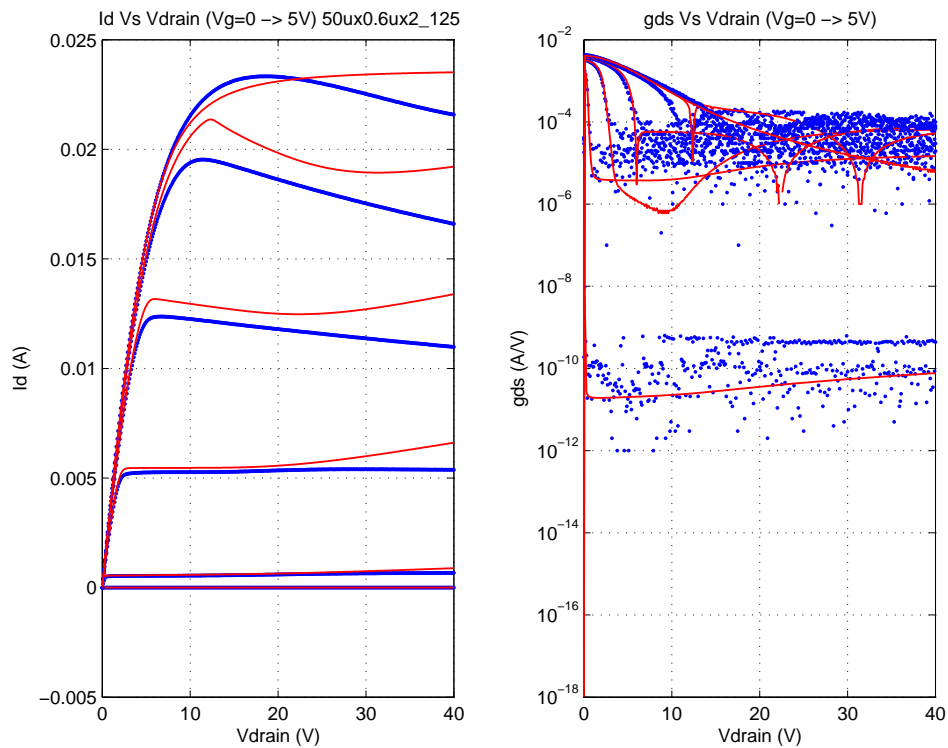


FIGURE 4.73 40V Iso.NFET (nfet5p0_Id40_iso);NFxWxL_Id=6x20x0.6_0.6 μ m;Id Vs. Vgs;Vds=0.1V

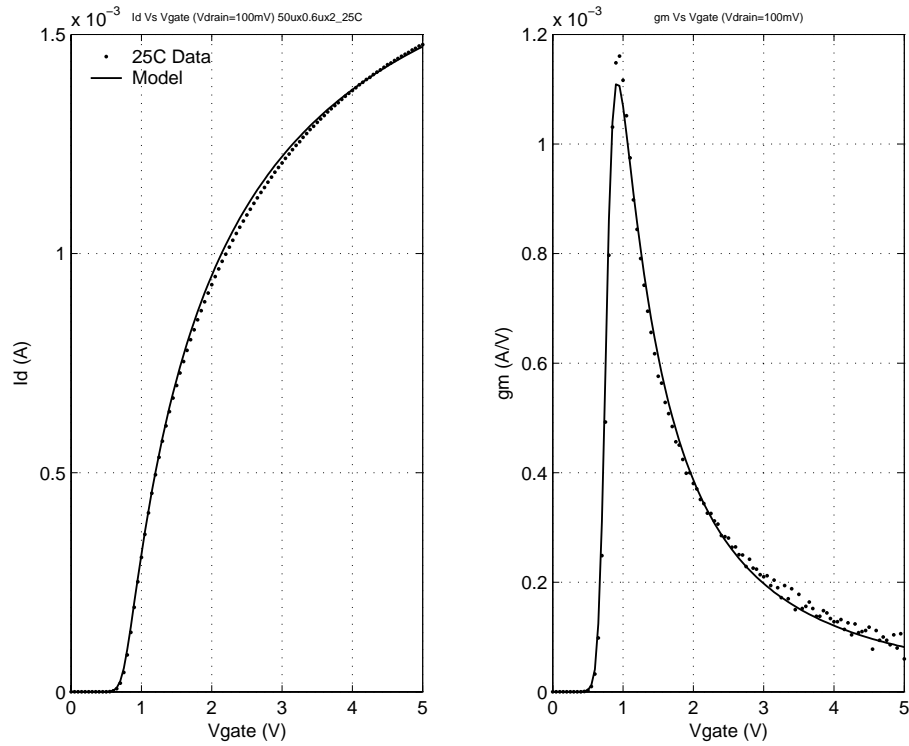


FIGURE 4.74 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_0.6 μ m; Id Vs. Vgs; Vds=3V

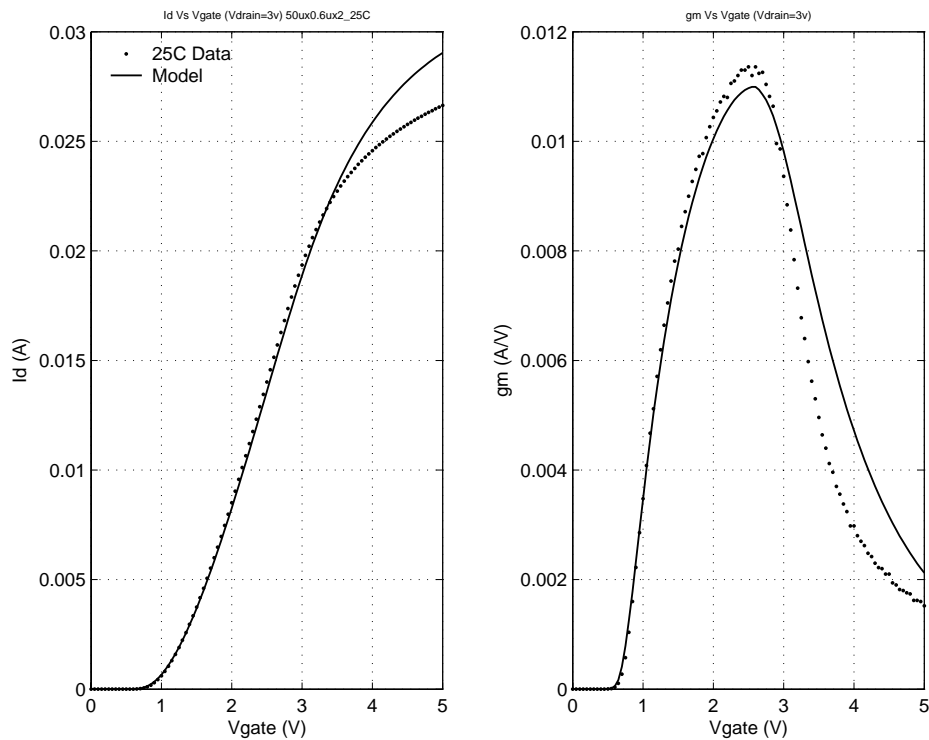


FIGURE 4.75 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_0.6 μ m; Id Vs. Vgs; Vds=5V

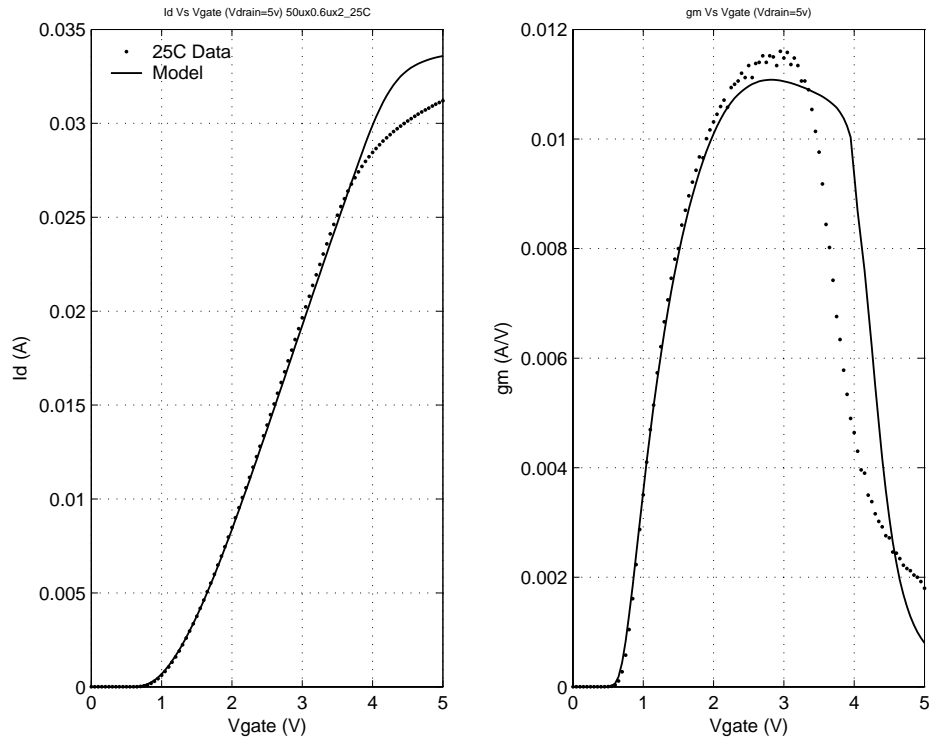


FIGURE 4.76 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_0.6 μ m; Id Vs. Vgs; Vds=10V

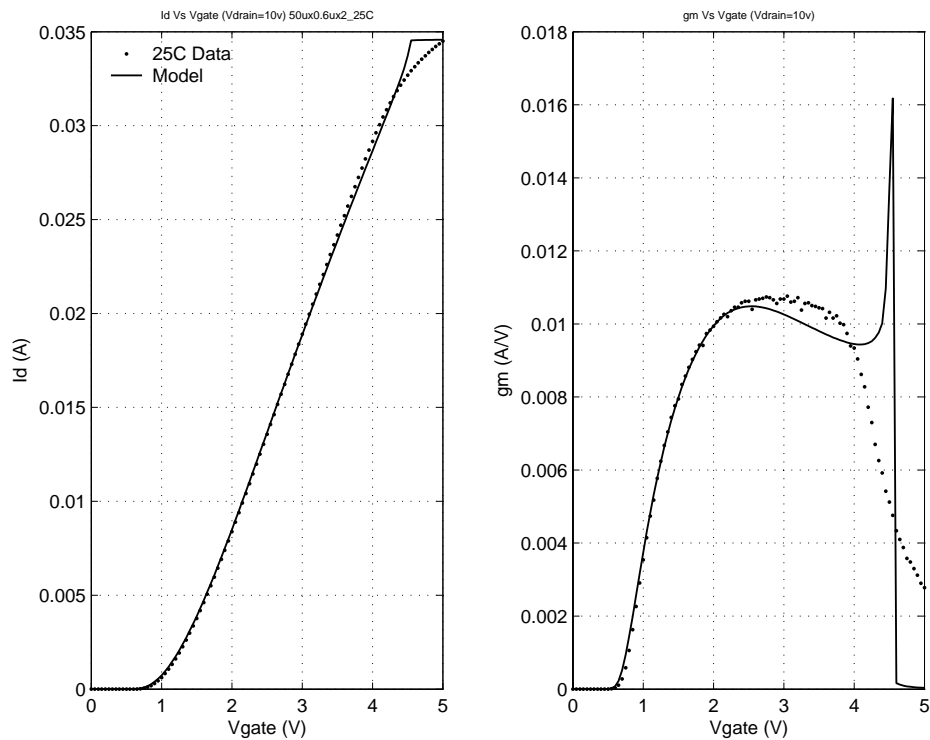


FIGURE 4.77 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_0.6 μ m; Id Vs. Vgs; Vds=20V

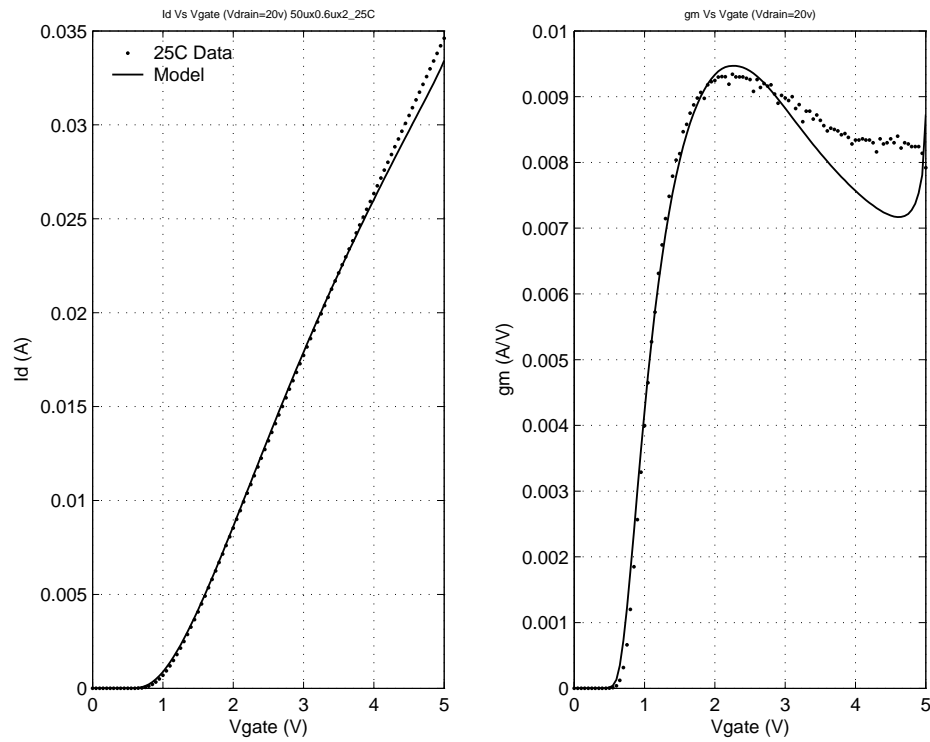


FIGURE 4.78 40V Iso. NFET; NFxWxL_Id=6x20x0.6_0.6 μ m; Id Vs. Vds; Vgs=0,1.5V; 25C

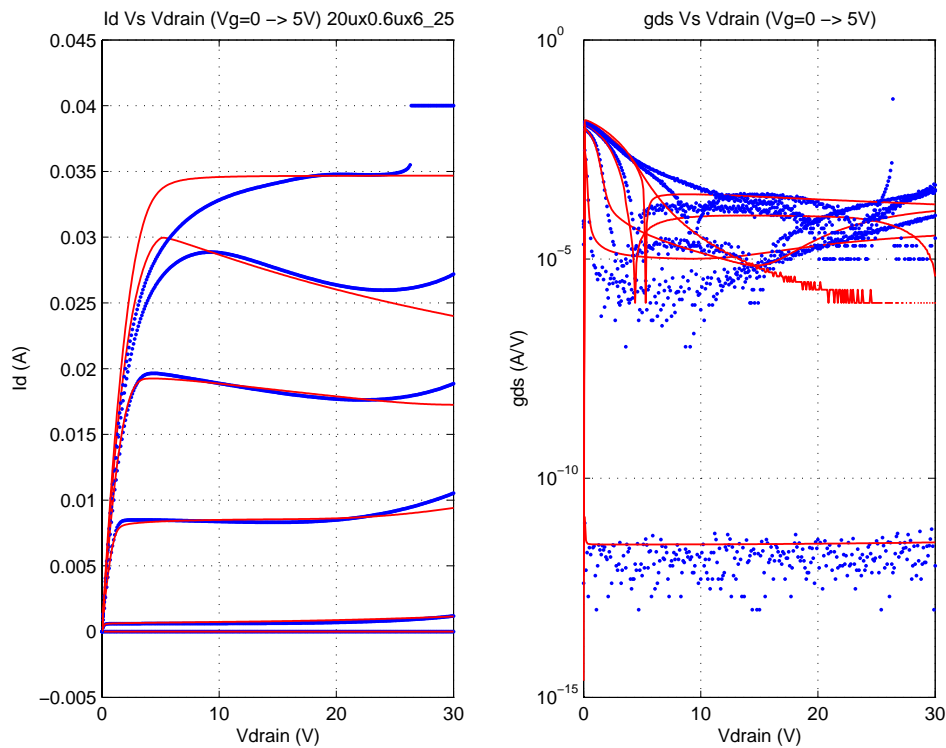


FIGURE 4.79 40V Iso.NFET (nfet5p0_Id40_iso);NFxWxL_Id=6x20x0.6_1.2 μ m;Id Vs. Vgs;Vds=0.1V

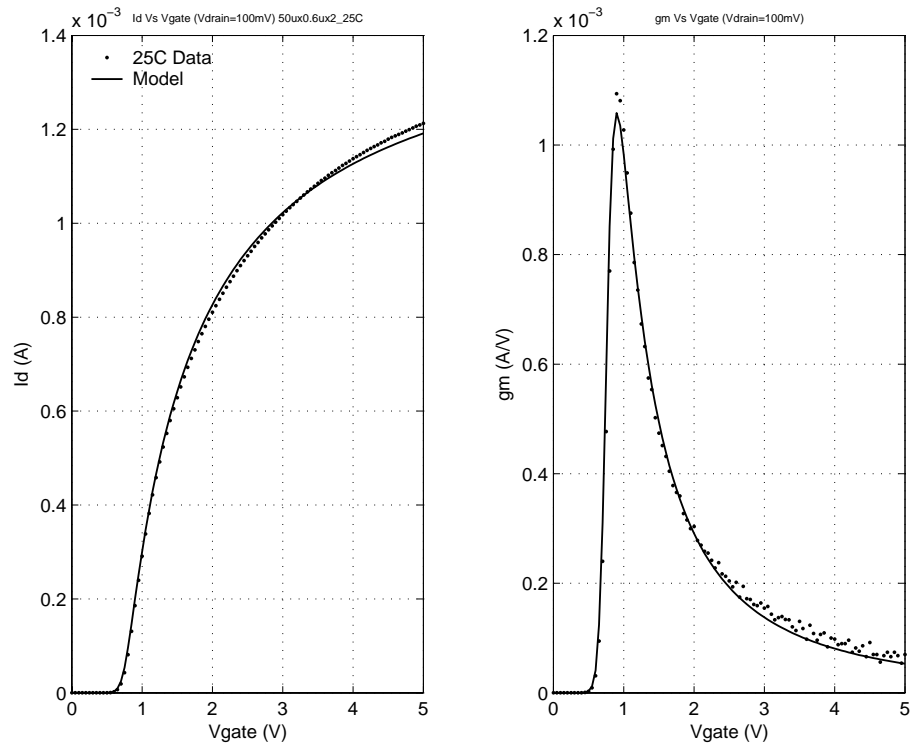


FIGURE 4.80 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.2 μ m; Id Vs. Vgs; Vds=3V

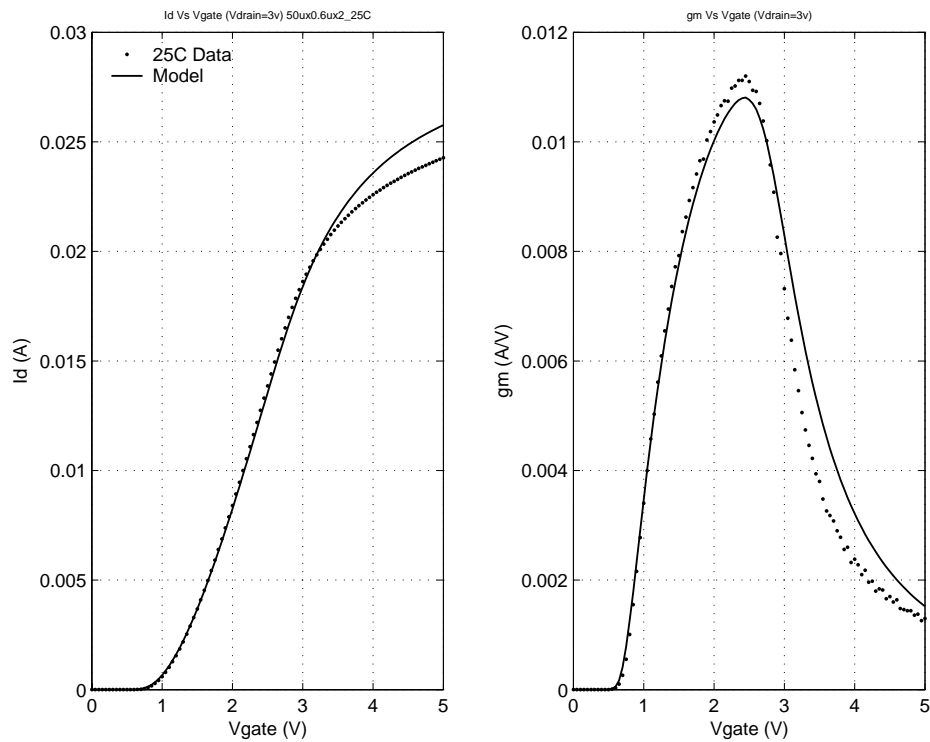


FIGURE 4.81 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.2 μ m; Id Vs. Vgs; Vds=5V

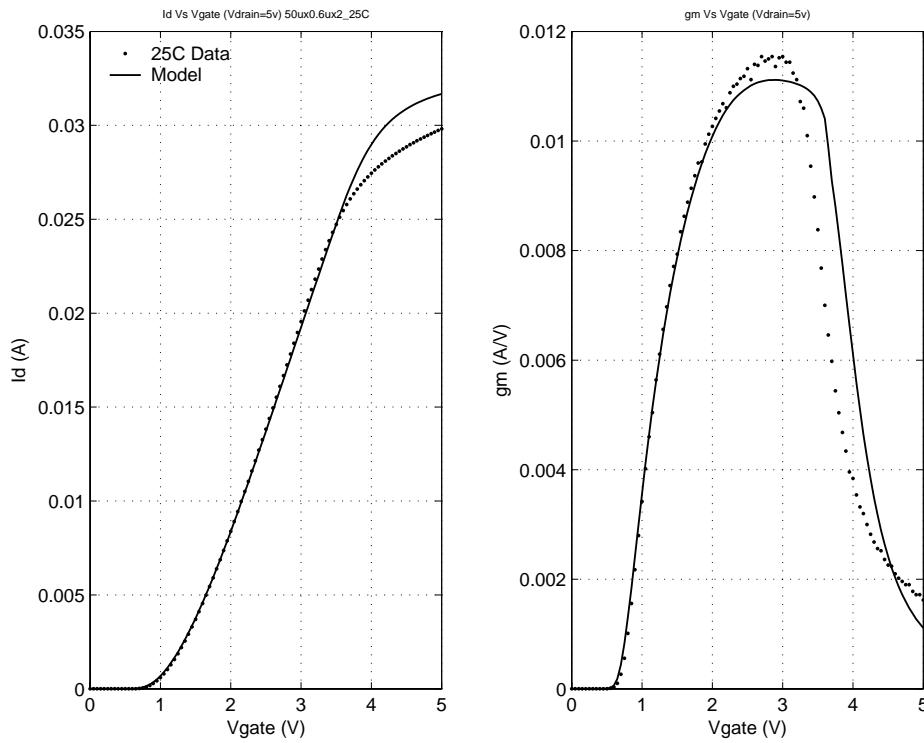


FIGURE 4.82 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.2 μ m; Id Vs. Vgs; Vds=10V

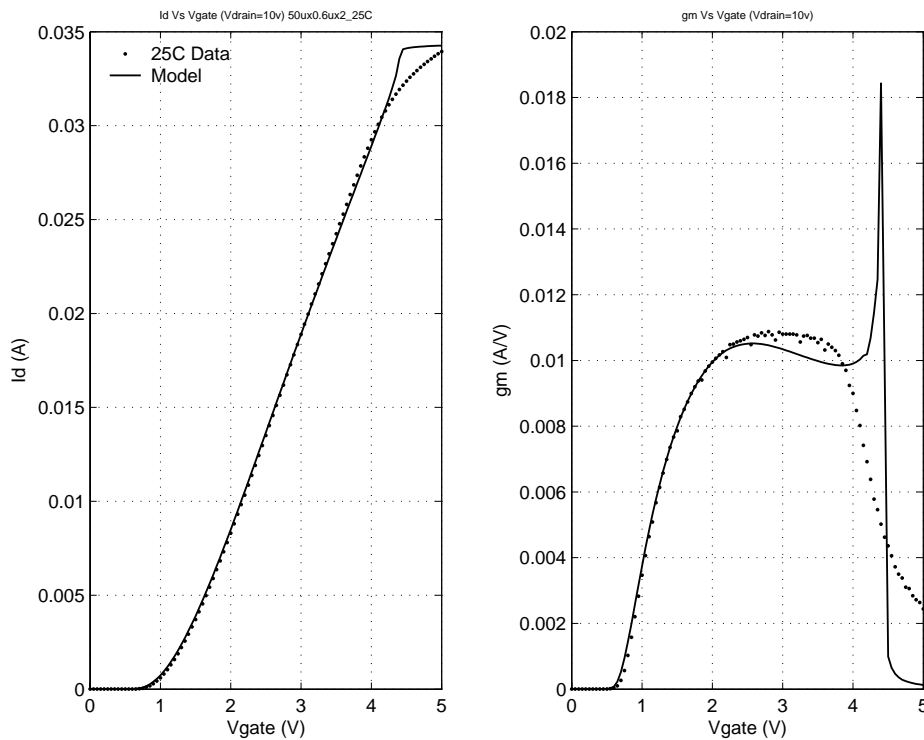


FIGURE 4.83 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.2 μ m; Id Vs. Vgs; Vds=20V

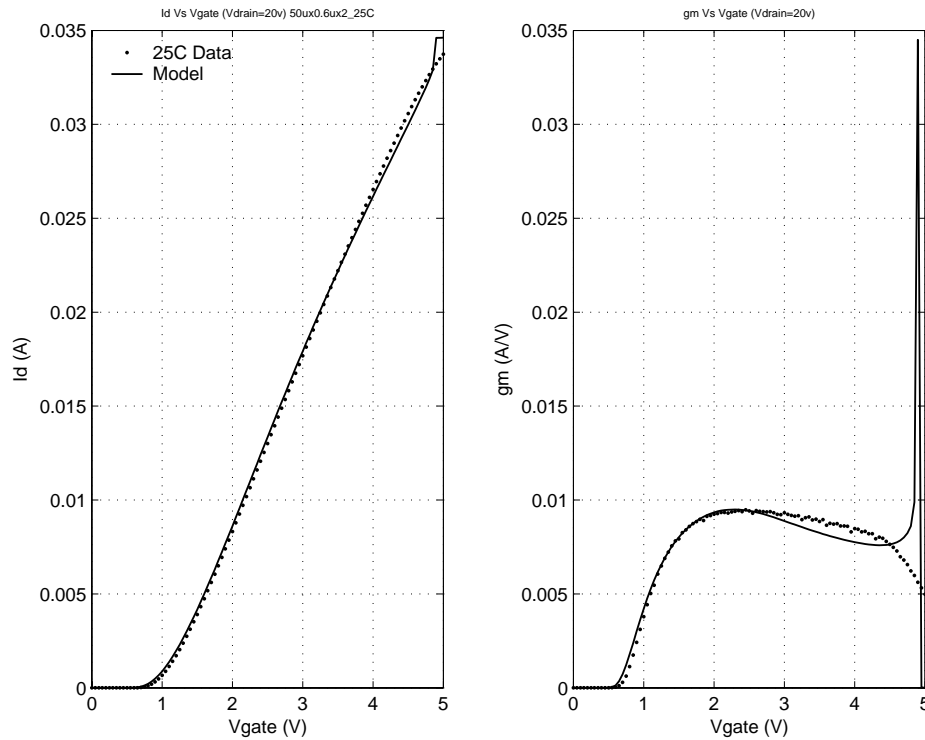


FIGURE 4.84 40V Iso. NFET; NFxWxL_Id=6x20x0.6_1.2 μ m; Id Vs. Vds; Vgs=0,1.5V; 25C

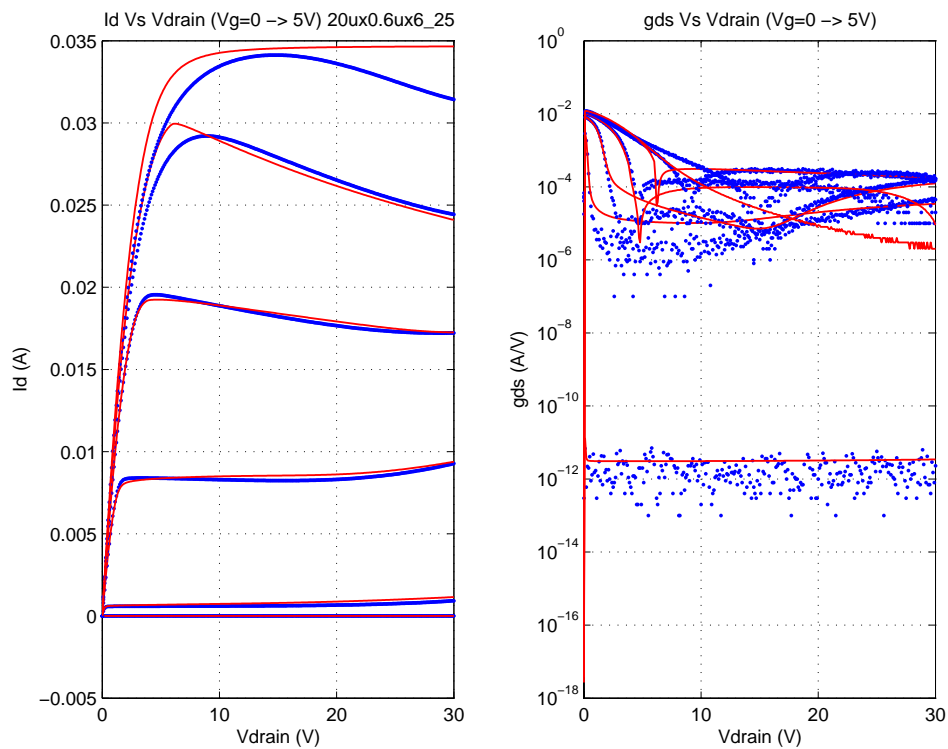


FIGURE 4.85 40V Iso.NFET (nfet5p0_Id40_iso);NFxWxL_Id=6x20x0.6_1.6 μ m;Id Vs.Vgs;Vds=0.1V

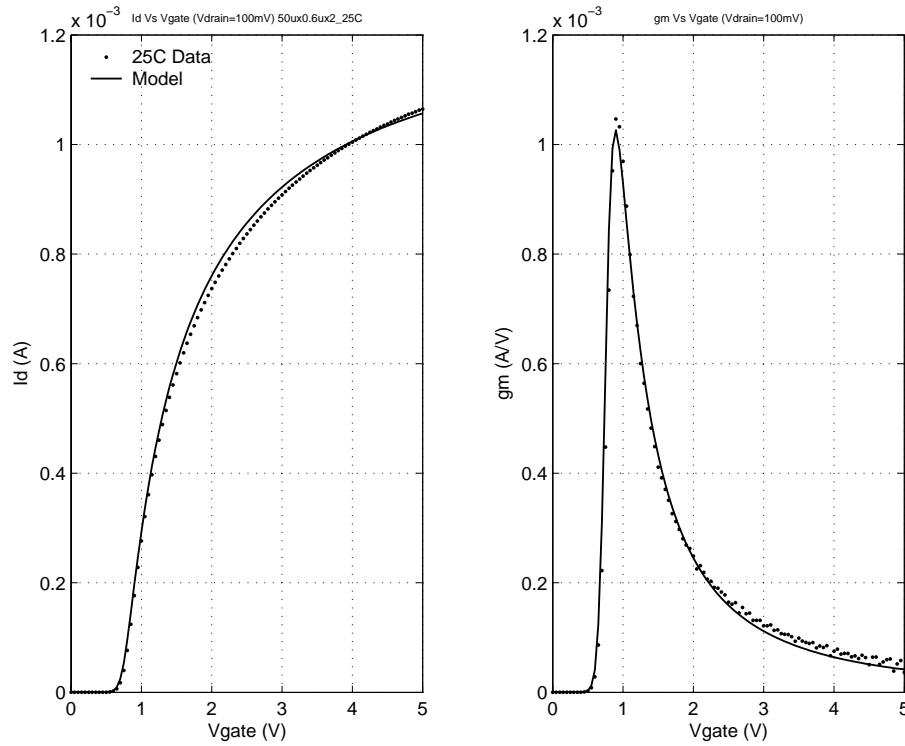


FIGURE 4.86 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.6 μ m; Id Vs. Vgs; Vds=3V

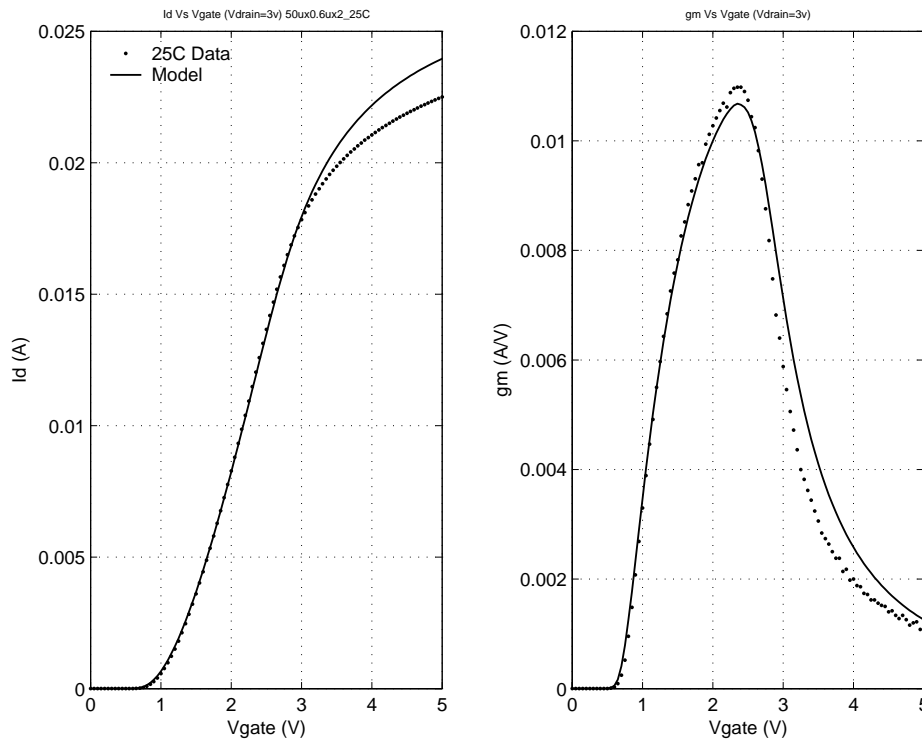


FIGURE 4.87 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.6 μ m; Id Vs. Vgs; Vds=5V

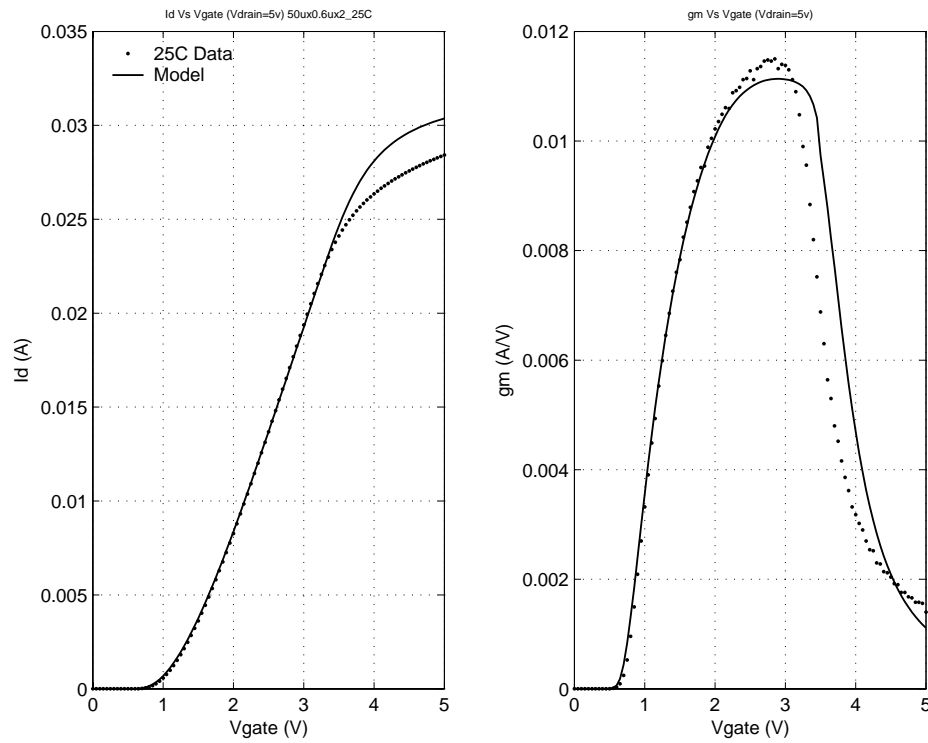


FIGURE 4.88 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.6 μ m; Id Vs. Vgs; Vds=10V

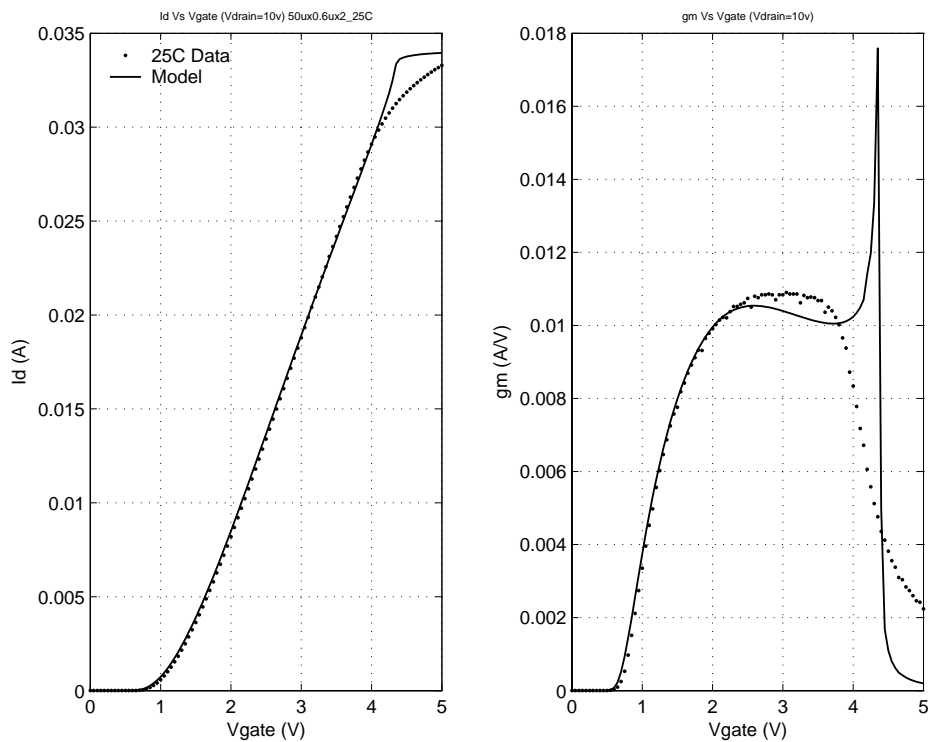


FIGURE 4.89 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_1.6 μ m; Id Vs. Vgs; Vds=20V

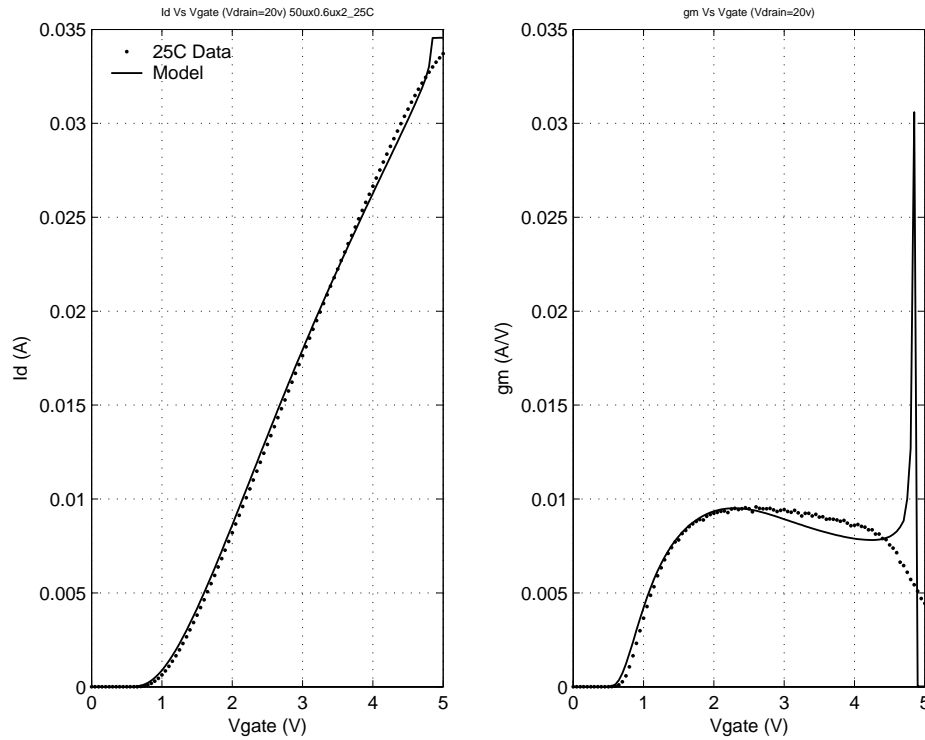


FIGURE 4.90 40V Iso. NFET; NFxWxL_Id=6x20x0.6_1.6 μ m; Id Vs. Vds; Vgs=0,1.5V; 25C

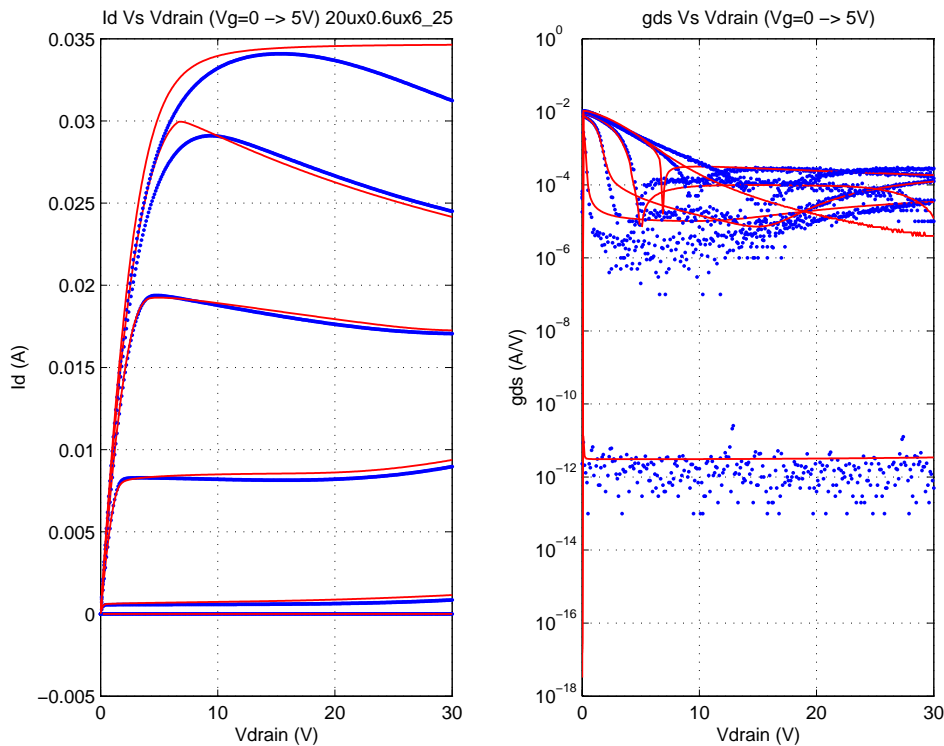


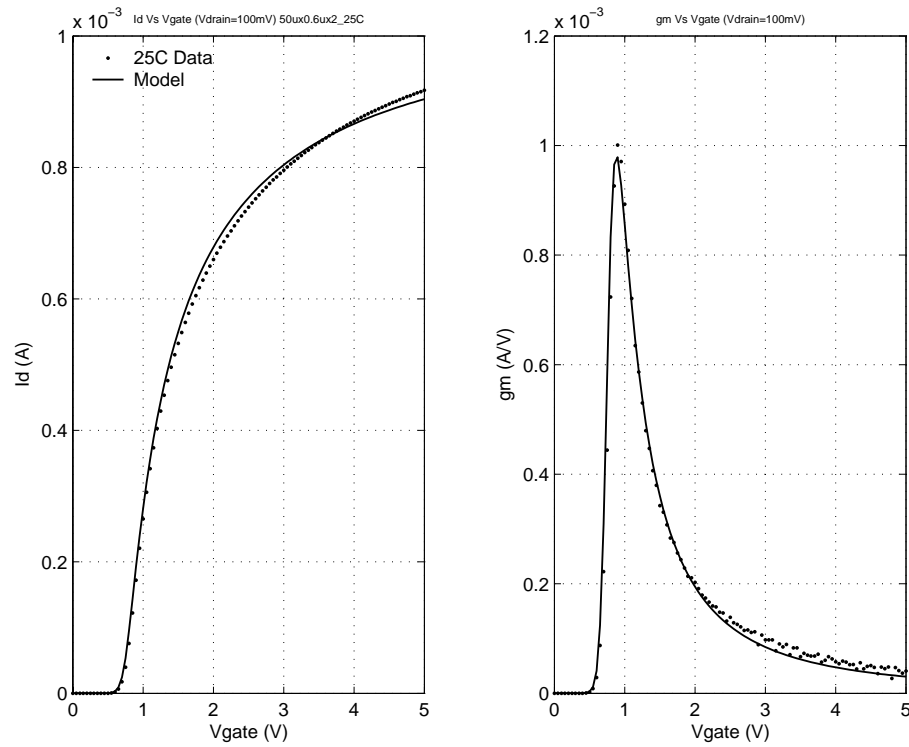
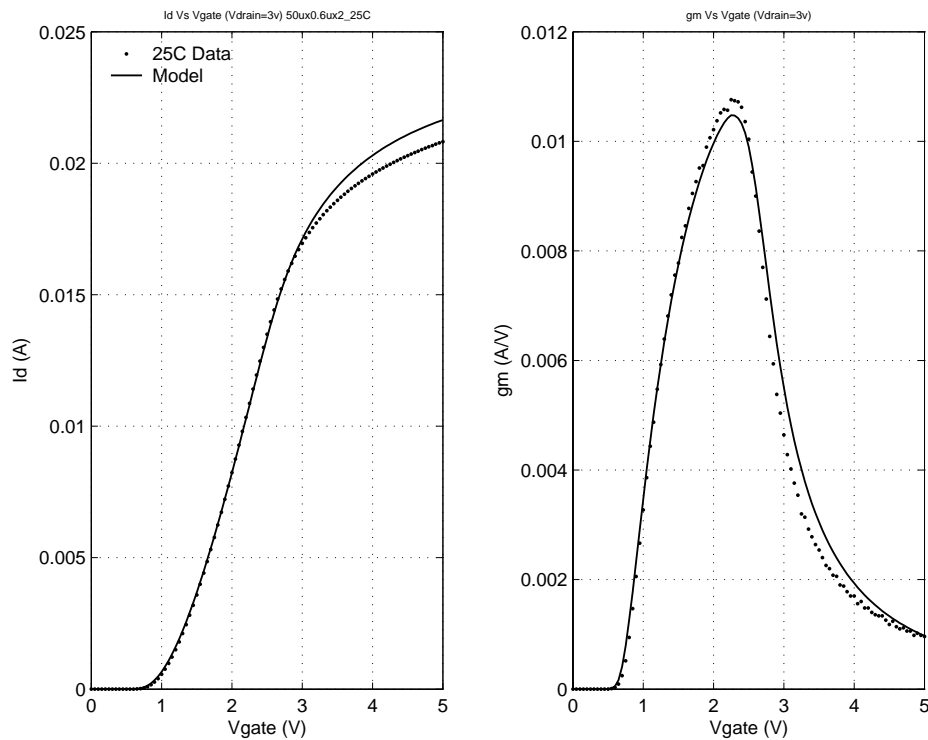
FIGURE 4.91 40V Iso.NFET (nfet5p0_Id40_iso);NFxWxL_Id=6x20x0.6_2.2 μ m;Id Vs. Vgs;Vds=0.1VFIGURE 4.92 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.2 μ m; Id Vs. Vgs; Vds=3V

FIGURE 4.93 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.2 μ m; Id Vs. Vgs; Vds=5V

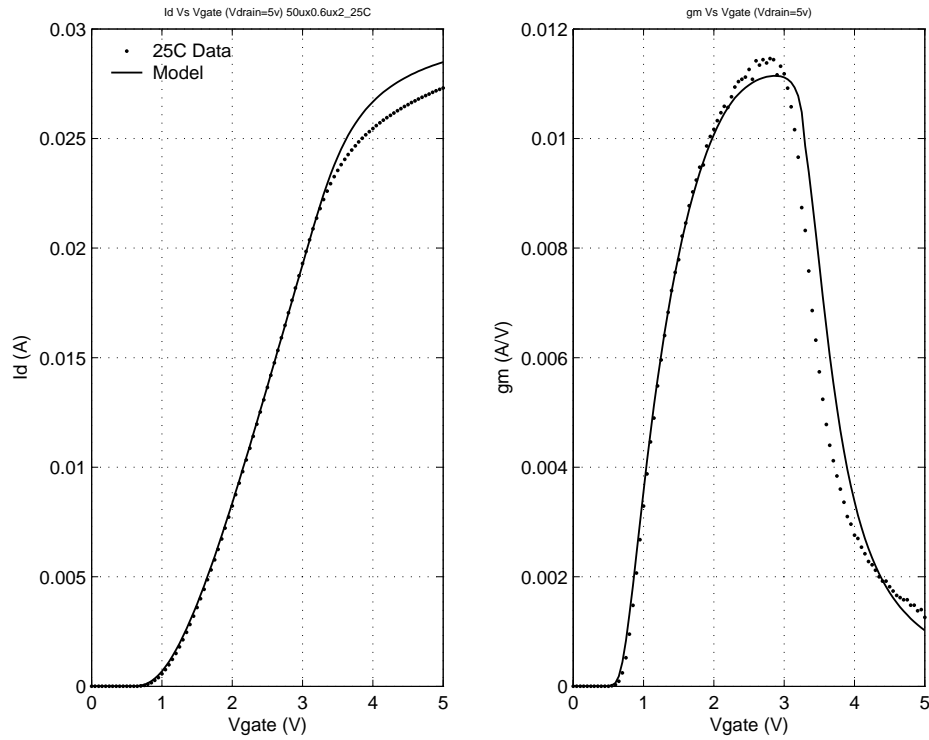


FIGURE 4.94 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.2 μ m; Id Vs. Vgs; Vds=10V

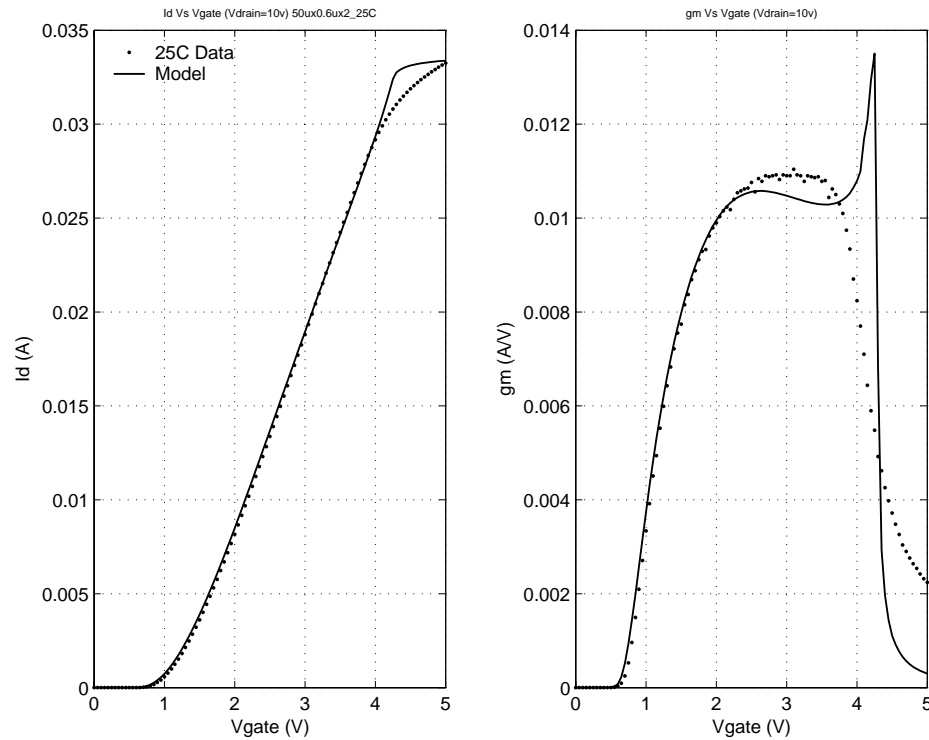


FIGURE 4.95 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.2 μ m; Id Vs. Vgs; Vds=20V

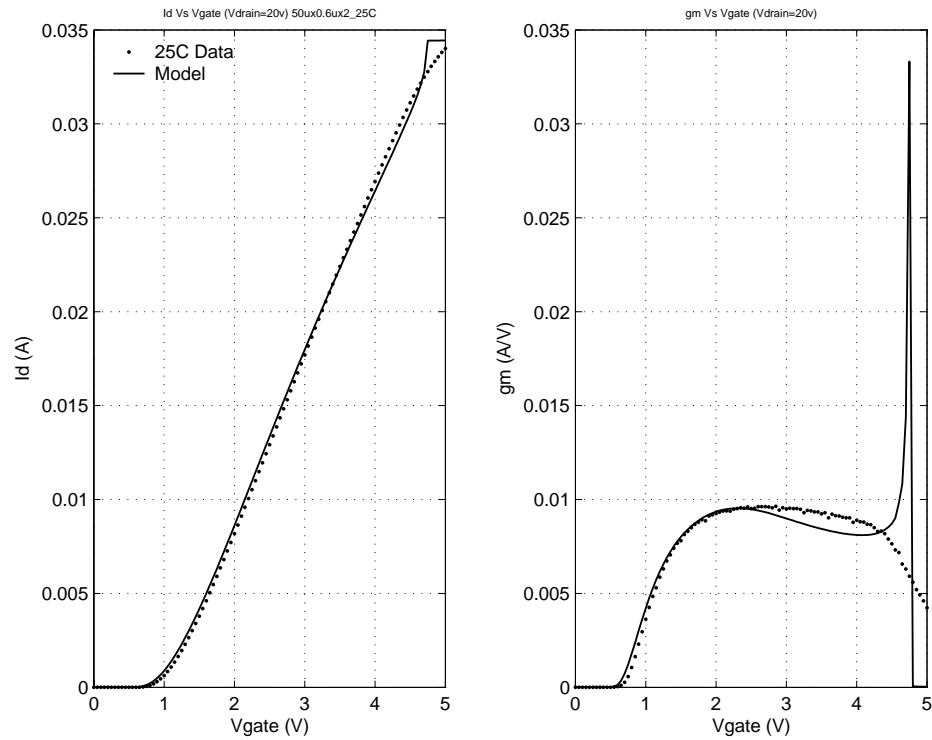


FIGURE 4.96 40V Iso. NFET; NFxWxL_Id=6x20x0.6_2.2 μ m; Id Vs. Vds; Vgs=0,1...5V; 25C

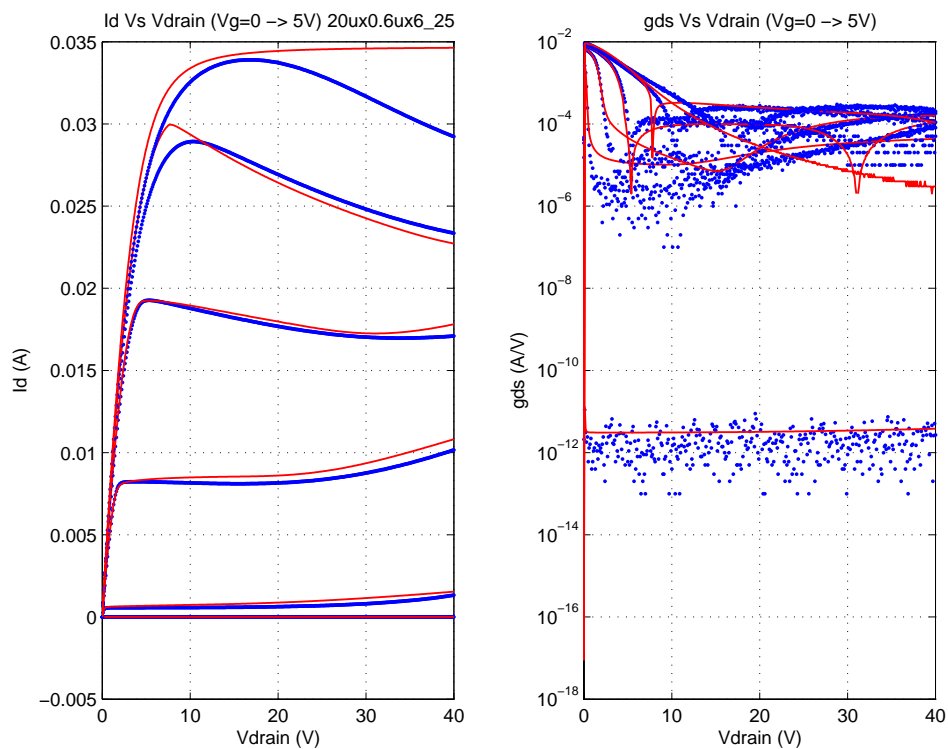


FIGURE 4.97 40V Iso.NFET (nfet5p0_Id40_iso);NFxWxL_Id=6x20x0.6_2.8 μ m;Id Vs.Vgs;Vds=0.1V

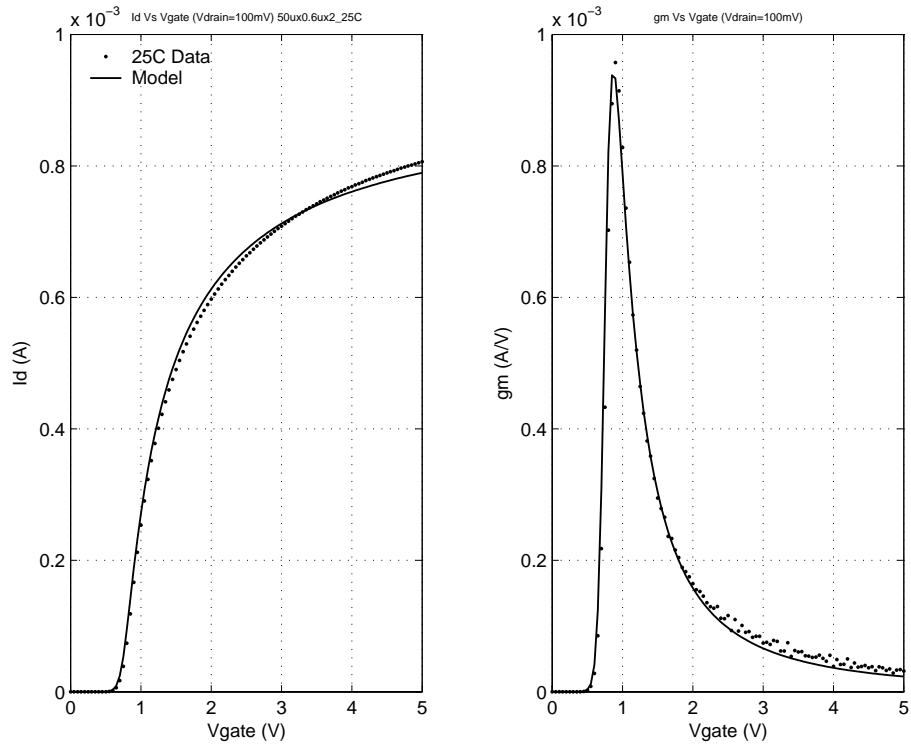


FIGURE 4.98 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.8 μ m; Id Vs. Vgs; Vds=3V

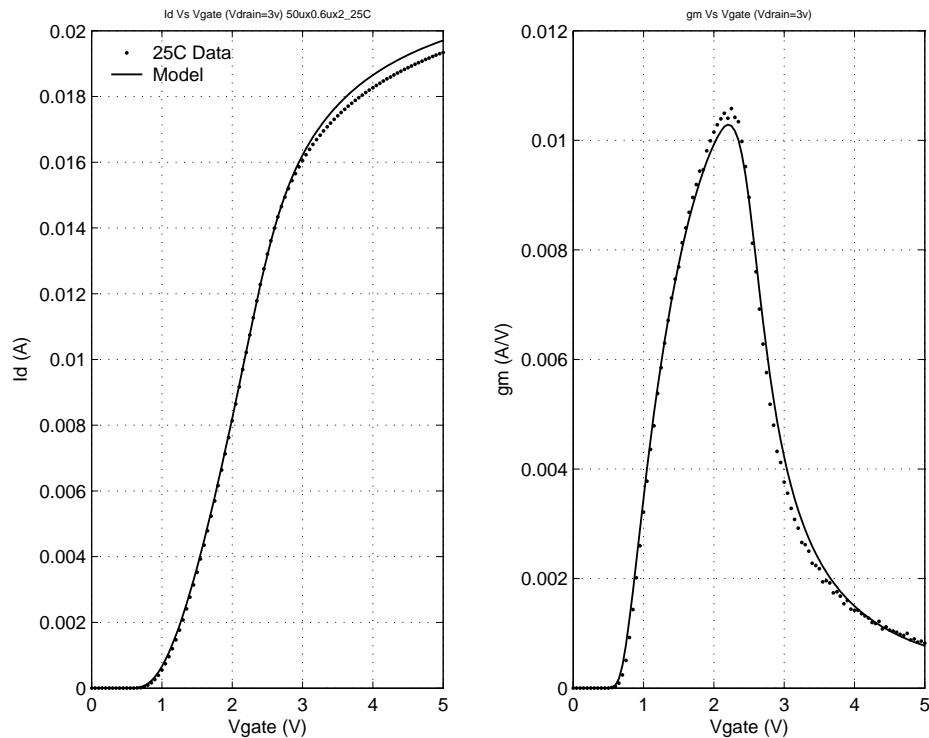


FIGURE 4.99 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.8 μ m; Id Vs. Vgs; Vds=5V

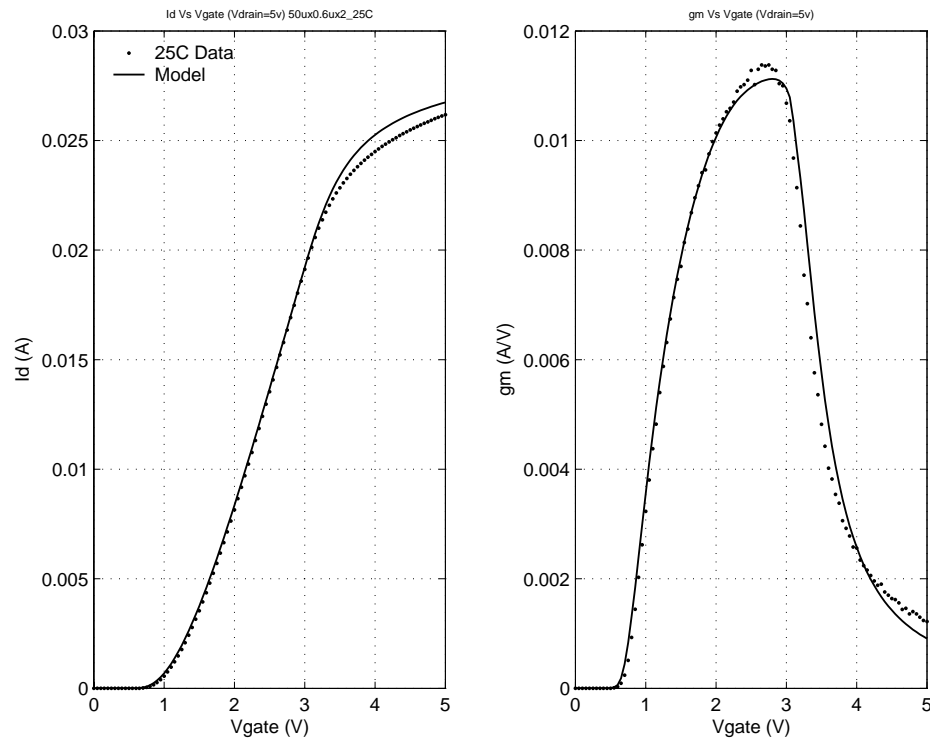


FIGURE 4.100 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.8 μ m; Id Vs. Vgs; Vds=10V

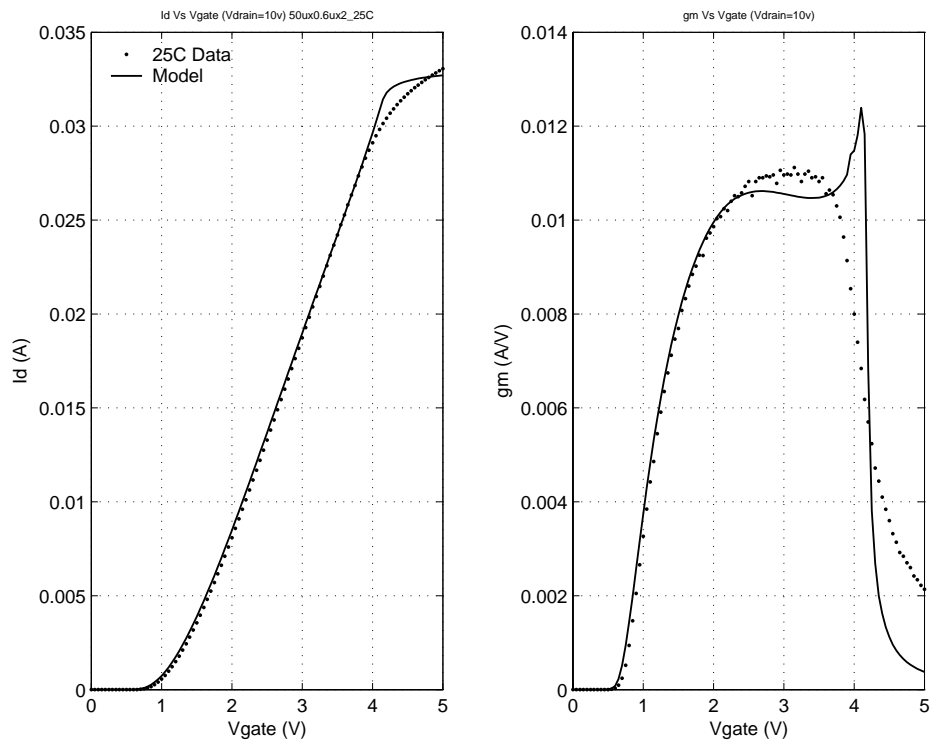


FIGURE 4.101 40V Iso. NFET (nfet5p0_Id40_iso); NFxWxL_Id=6x20x0.6_2.8 μ m; Id Vs. Vgs; Vds=20V

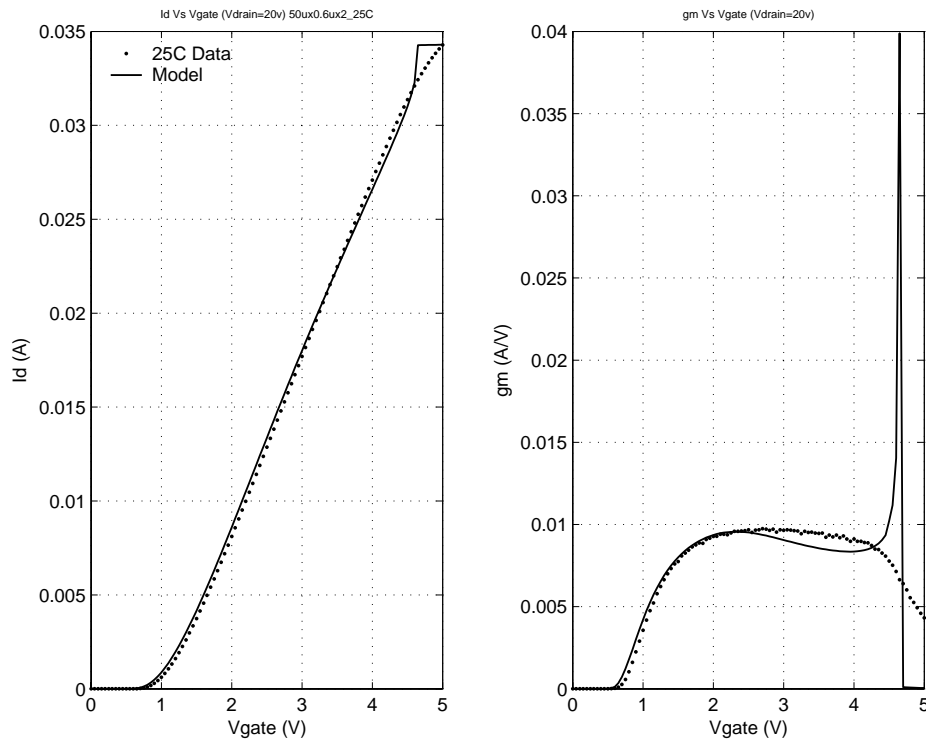


FIGURE 4.102 40V Iso. NFET; NFxWxL_Id=6x20x0.6_2.8 μ m; Id Vs. Vds; Vgs=0,1.5V; 25C

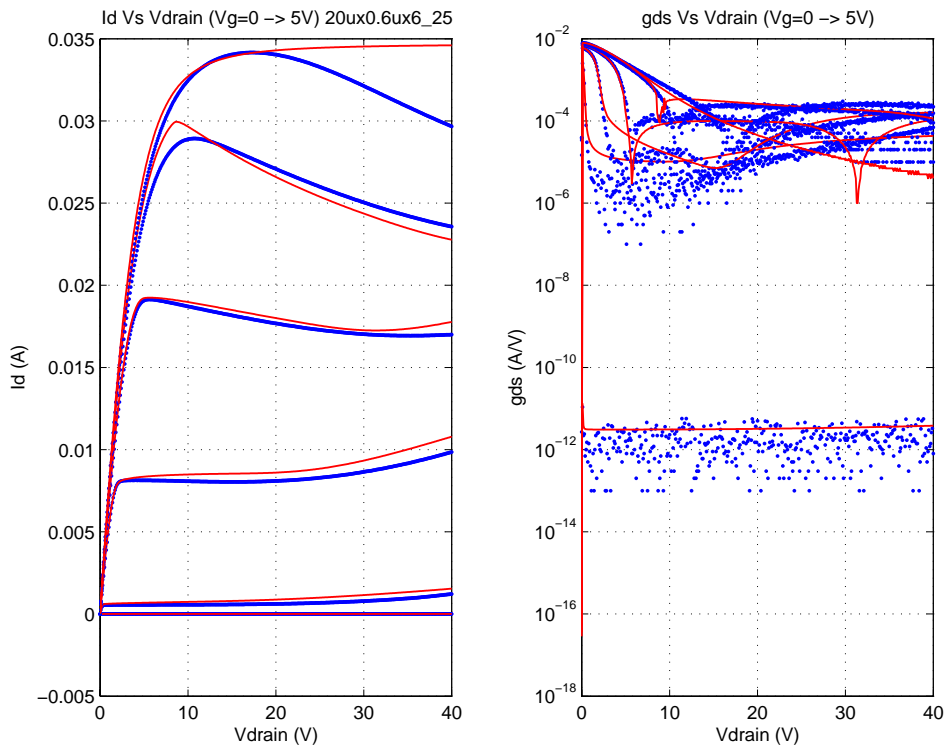


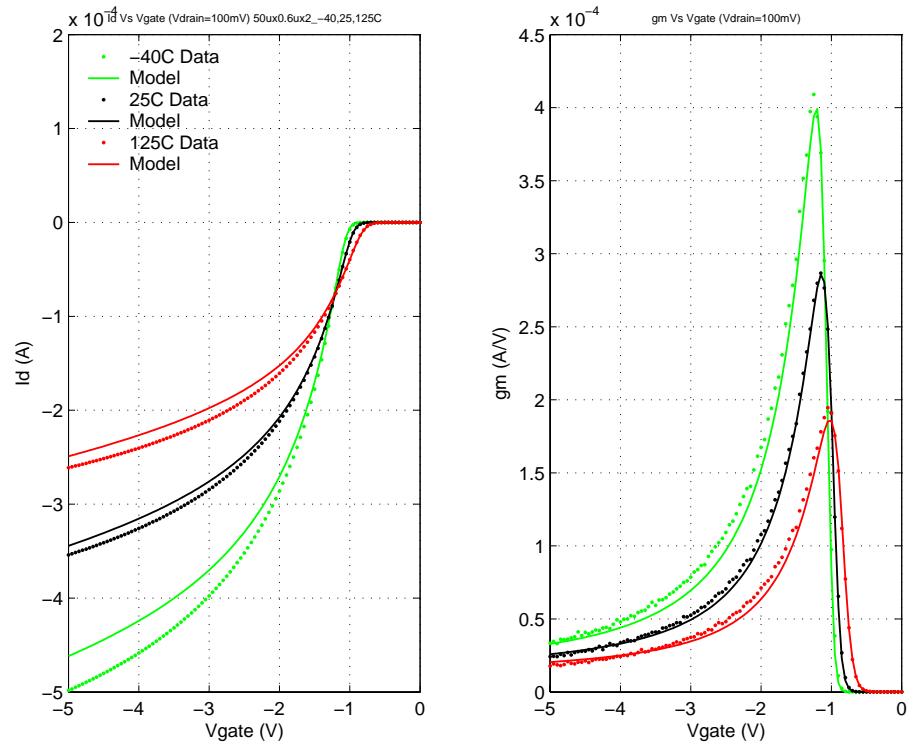
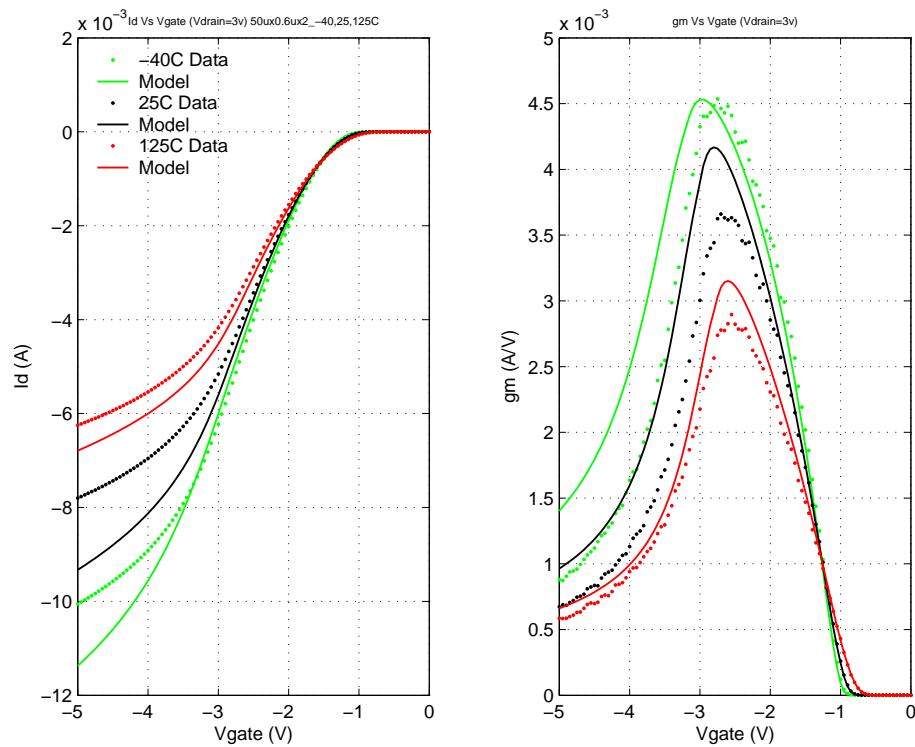
FIGURE 4.103 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_0.6 μ m; Id Vs. Vgs; Vds=-0.1VFIGURE 4.104 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_0.6 μ m; Id Vs. Vgs; Vds=-3V

FIGURE 4.105 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_0.6 μ m; Id Vs. Vgs; Vds=-5V

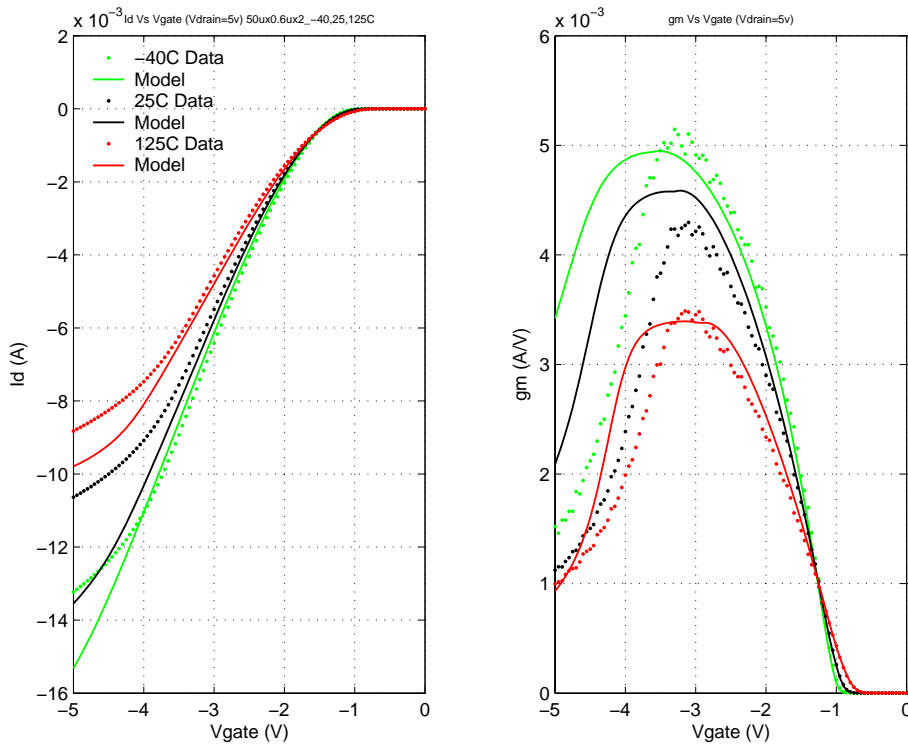


FIGURE 4.106 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_0.6 μ m; Id Vs. Vgs; Vds=-10V

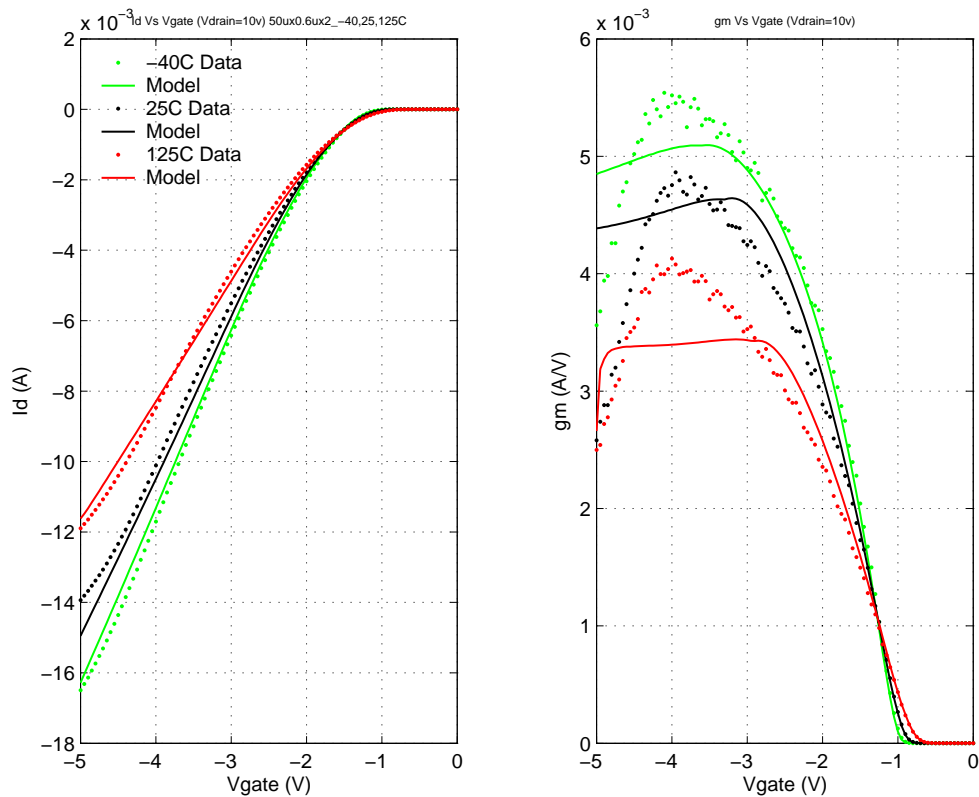


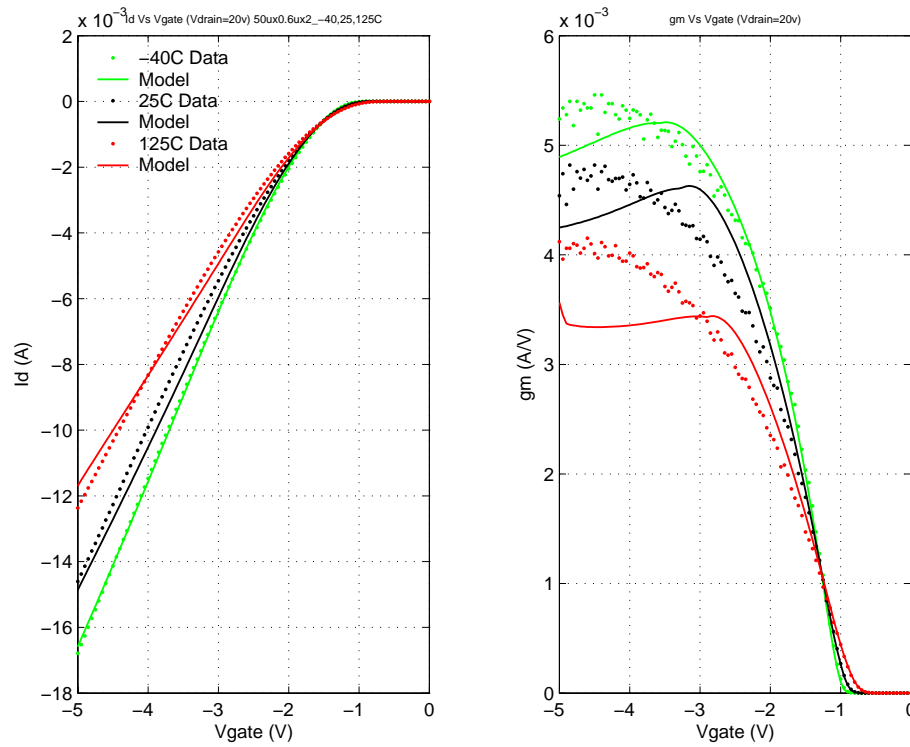
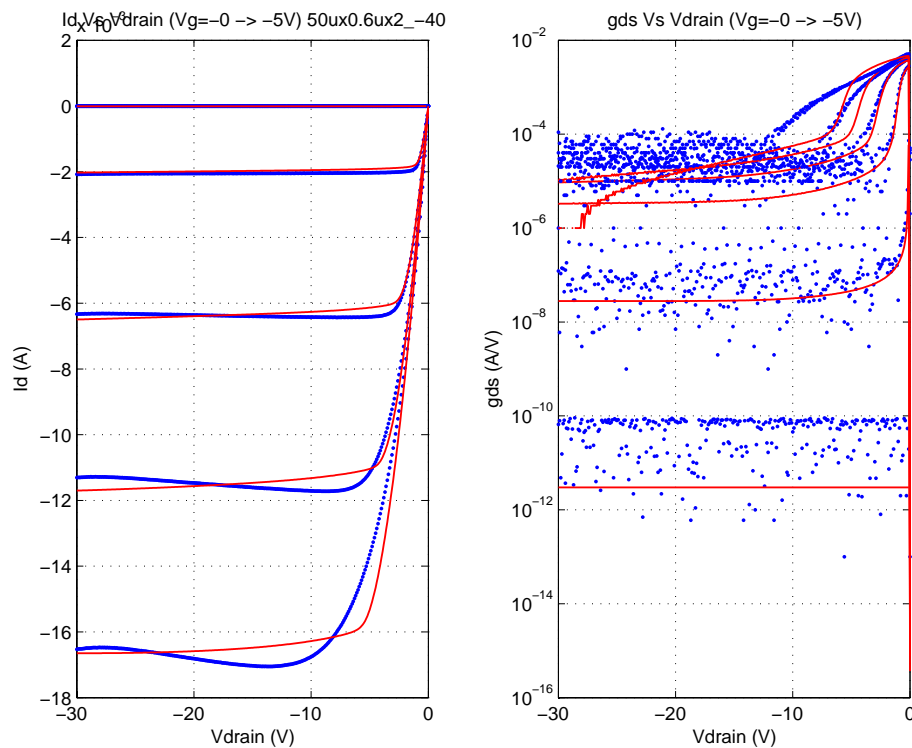
FIGURE 4.107 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_0.6 μ m; Id Vs. Vgs;Vds=-20V

FIGURE 4.108 40V PFET(pfet5p0_Id40);NFxWxL_kd=2x50x0.6_0.6 μ m;Id Vs. Vds;Vgs=0,-1...-5; -40C


FIGURE 4.109 40V PFET(pfet5p0_Id40);NFxWxL_kd=2x50x0.6_0.6 μ m;Id Vs. Vds; Vgs=0,-1...-5; 25C

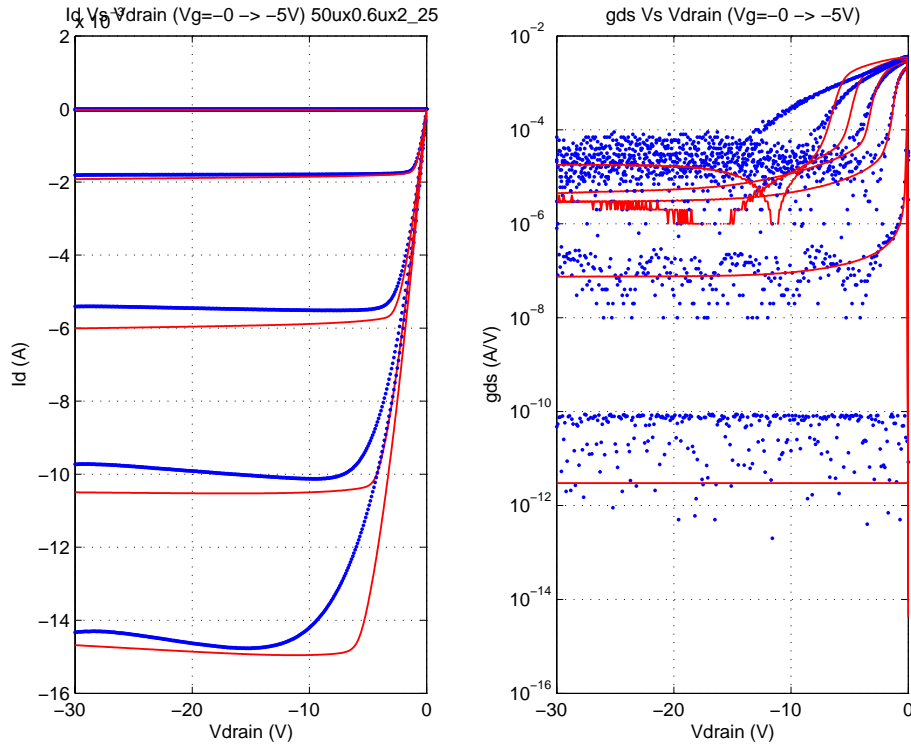


FIGURE 4.110 40V PFET(pfet5p0_Id40);NFxWxL_kd=2x50x0.6_0.6 μ m;Id Vs. Vds; Vgs=0,-1...-5; 125C

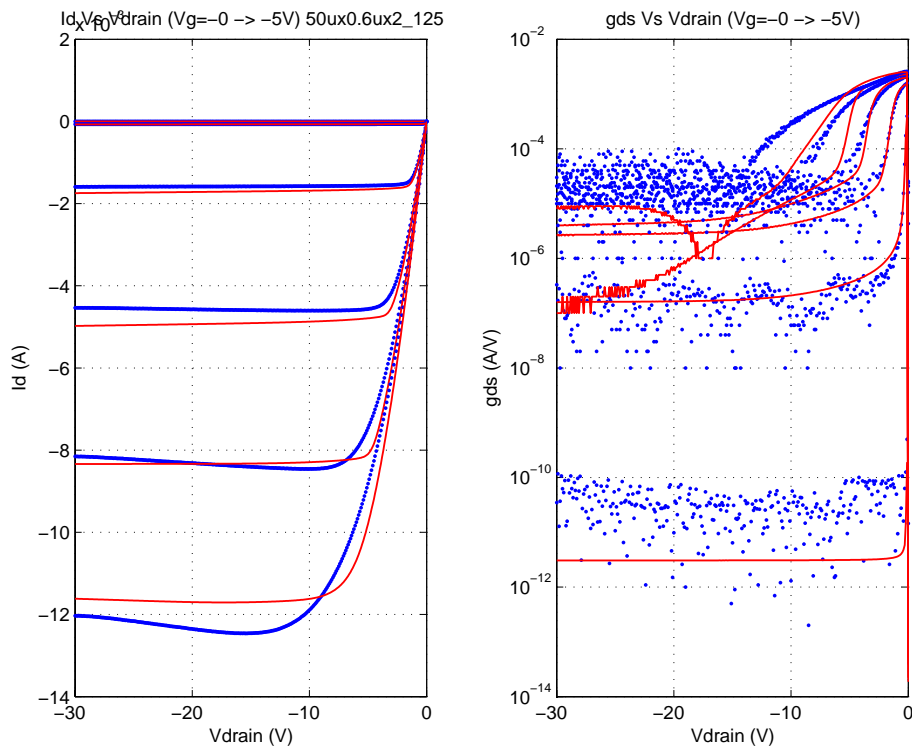


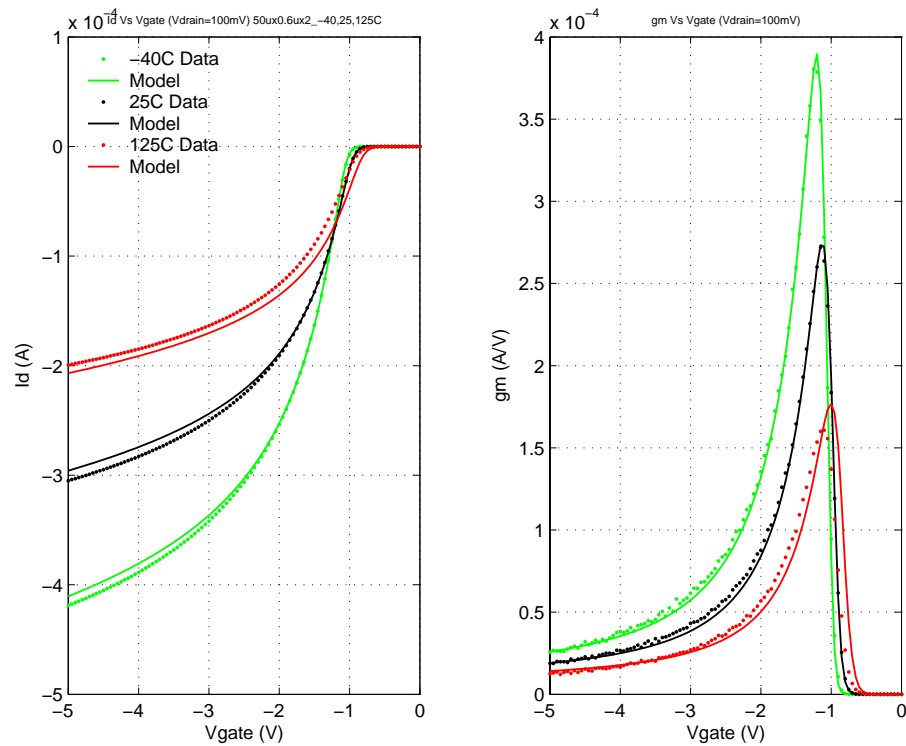
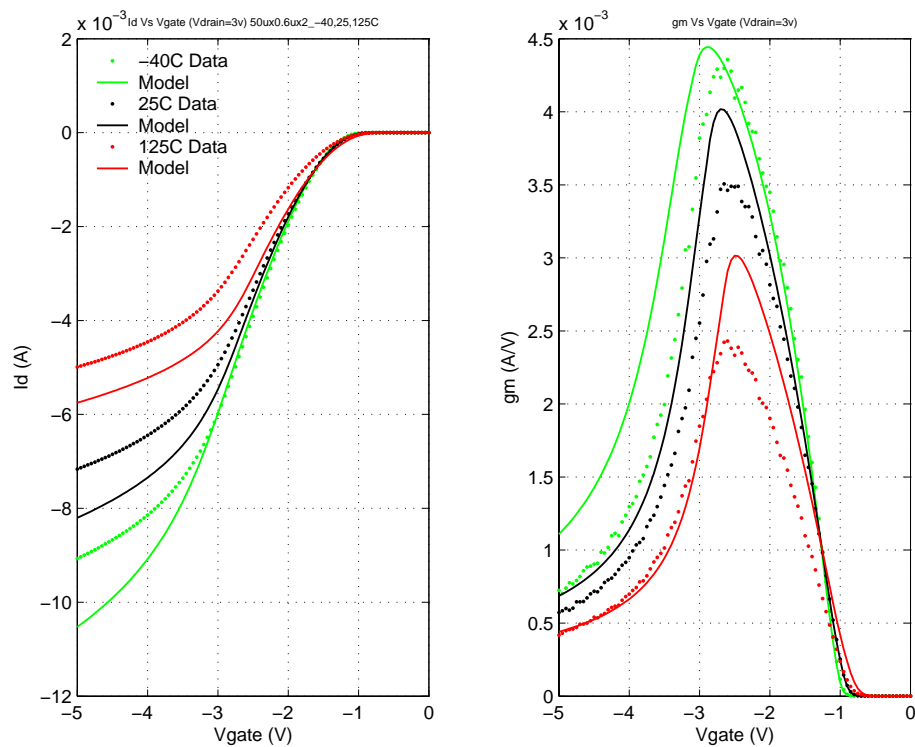
FIGURE 4.111 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_1.4 μ m; Id Vs. Vgs; Vds=-0.1VFIGURE 4.112 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_1.4 μ m; Id Vs. Vgs; Vds=-3V

FIGURE 4.113 40V PFET (pfet5p0_ld40); NFxWxL_Id=2x50x0.6_1.4 μ m; Id Vs. Vgs; Vds=-5V

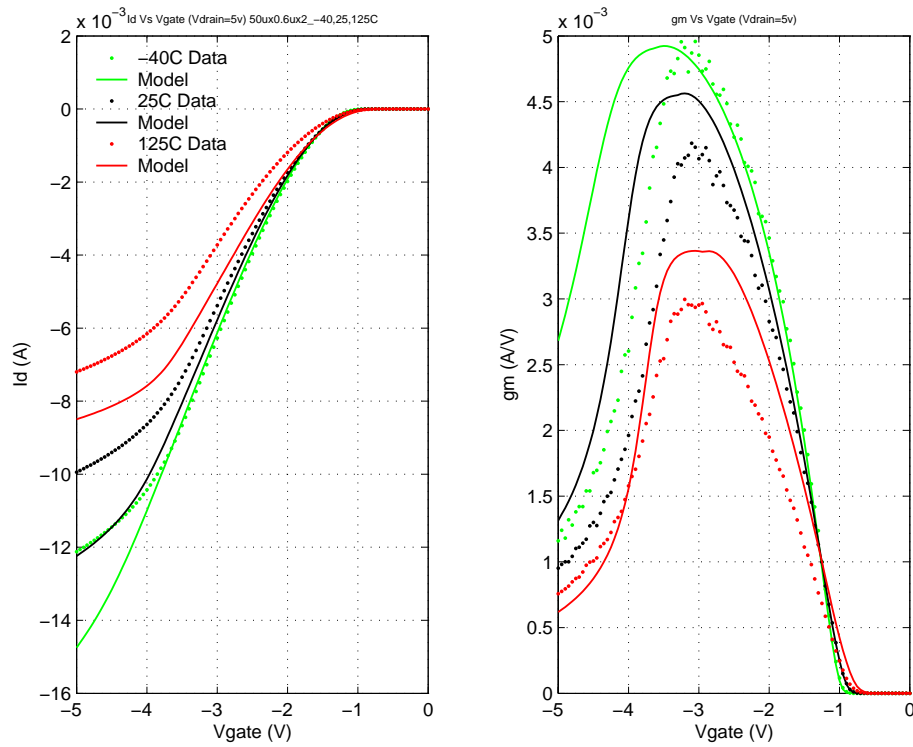


FIGURE 4.114 40V PFET (pfet5p0_ld40); NFxWxL_Id=2x50x0.6_1.4 μ m; Id Vs. Vgs; Vds=-10V

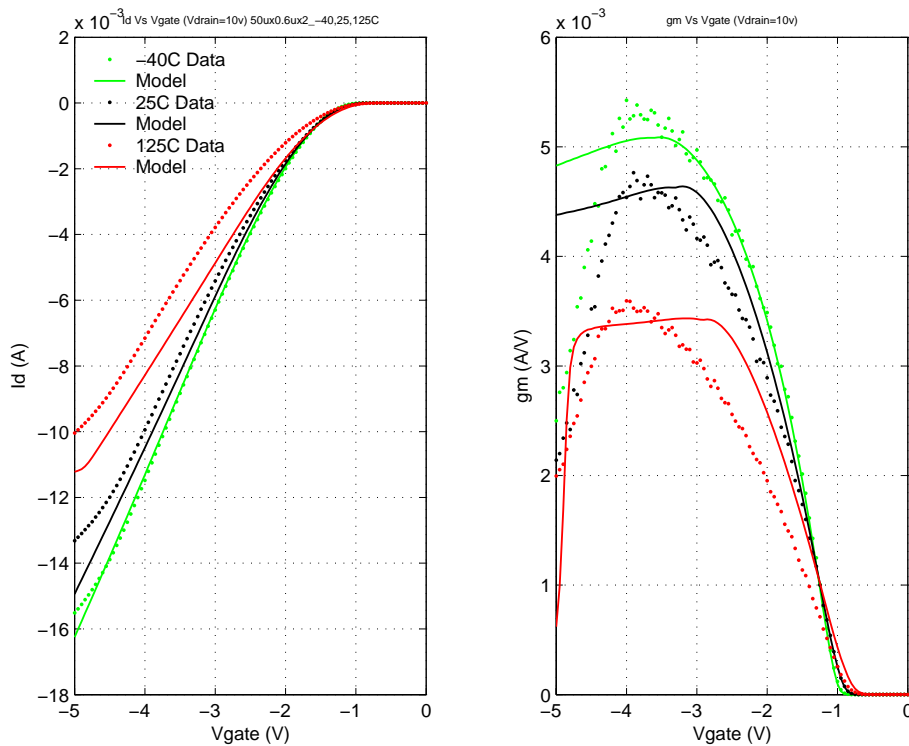


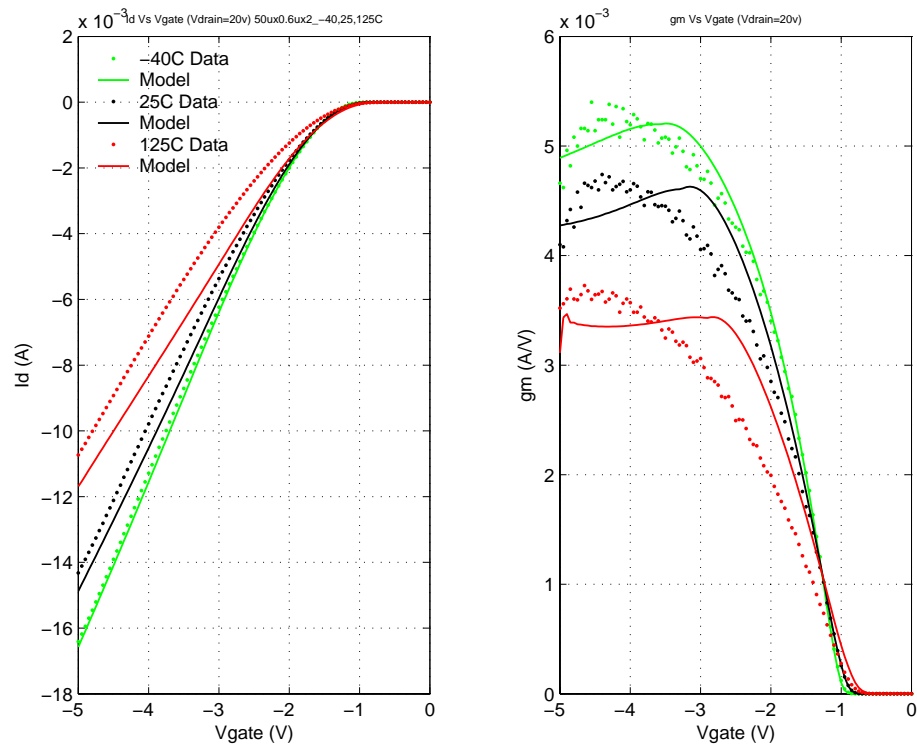
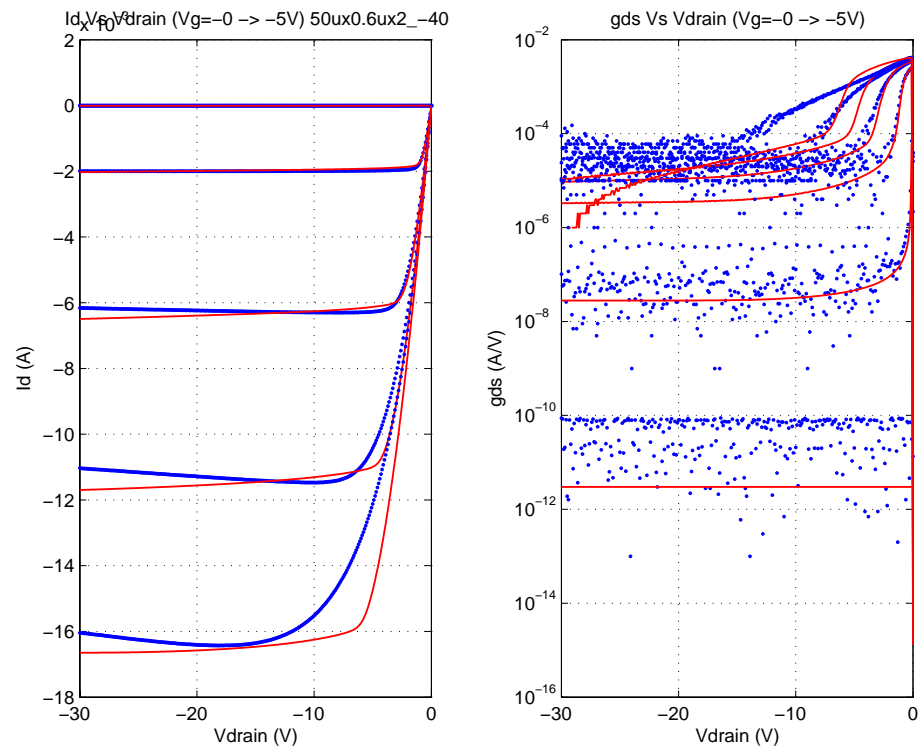
FIGURE 4.115 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_1.4 μ m; Id Vs. Vgs; Vds=-20VFIGURE 4.116 40V PFET (pfet5p0_Id40); NFxWxL_kd=2x50x0.6_1.4 μ m; Id Vs. Vds; Vgs=0,-1...-5; -40C

FIGURE 4.117 40V PFET (pfet5p0_ld40);NFxWxL_kd=2x50x0.6_1.4 μ m;Id Vs. Vds; Vgs=0,-1..-5; 25C

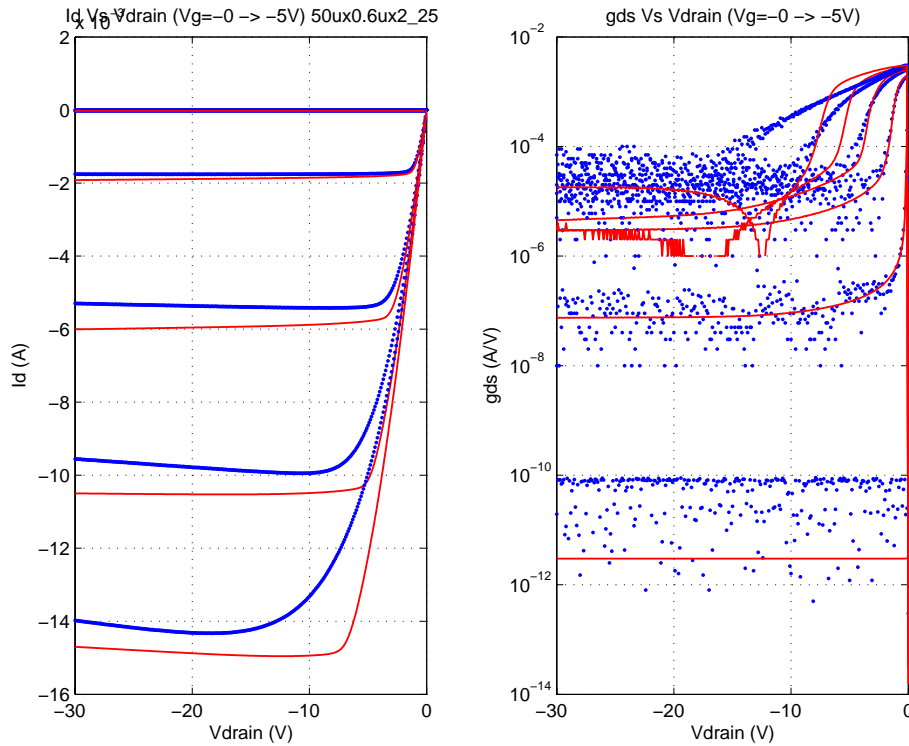


FIGURE 4.118 40V PFET(pfet5p0_ld40);NFxWxL_kd=2x50x0.6_1.4 μ m;Id Vs. Vds; Vgs=0,-1..-5; 125C

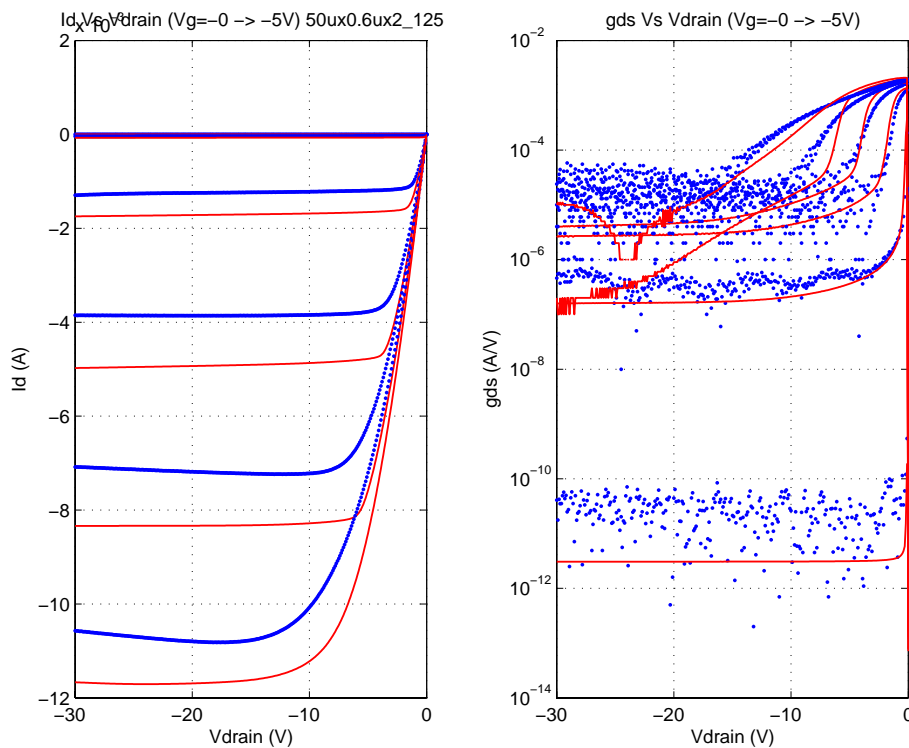


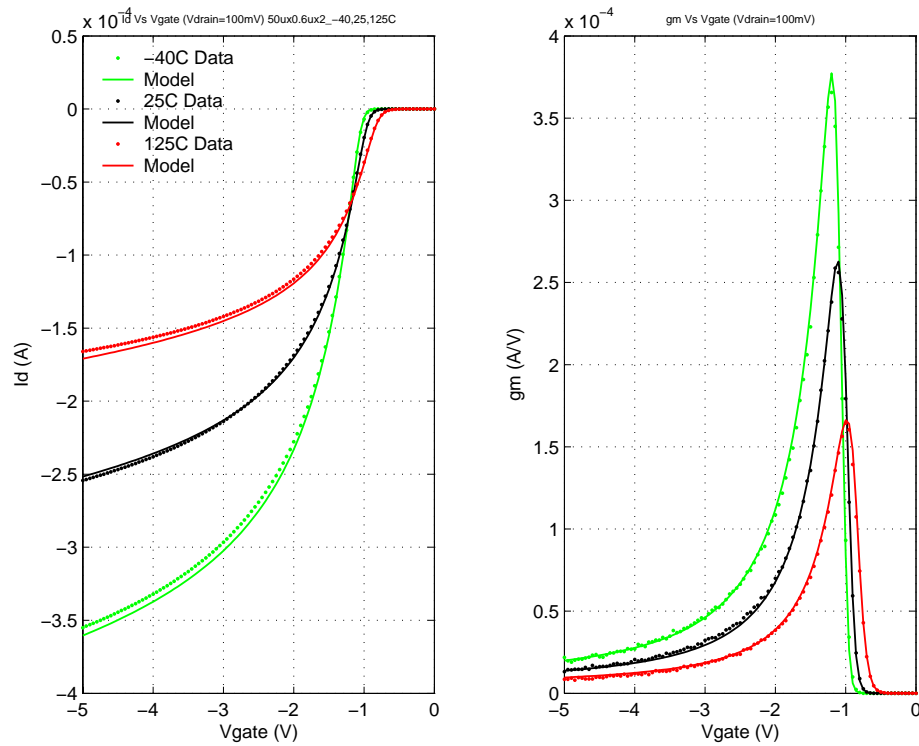
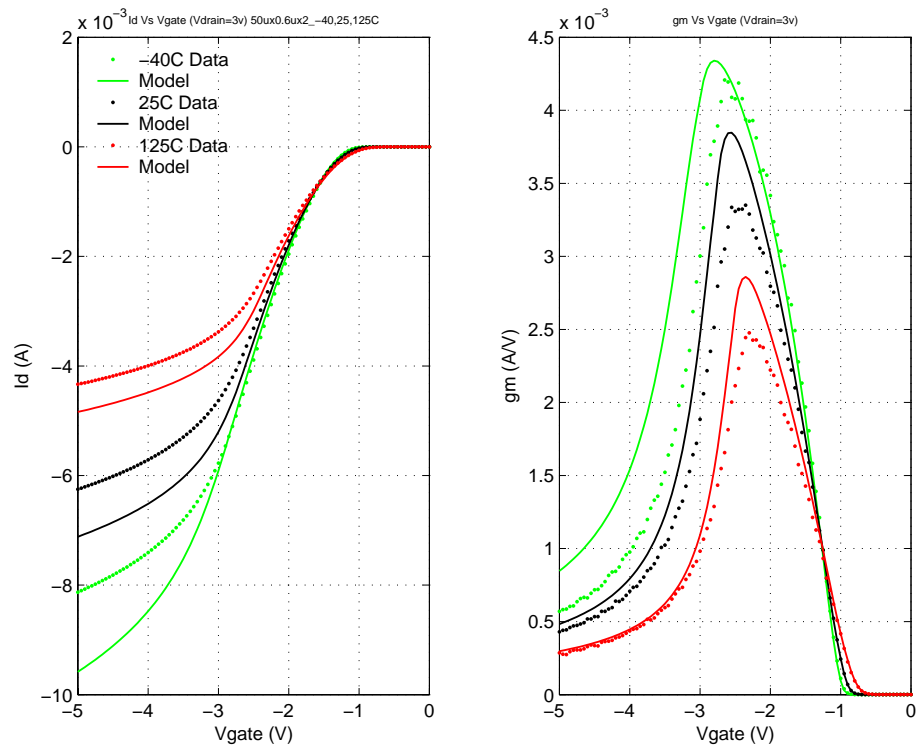
FIGURE 4.119 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_2.4 μ m; Id Vs. Vgs; Vds=-0.1VFIGURE 4.120 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_2.4 μ m; Id Vs. Vgs; Vds=-3V

FIGURE 4.121 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_2.4 μ m; Id Vs. Vgs; Vds=-5V

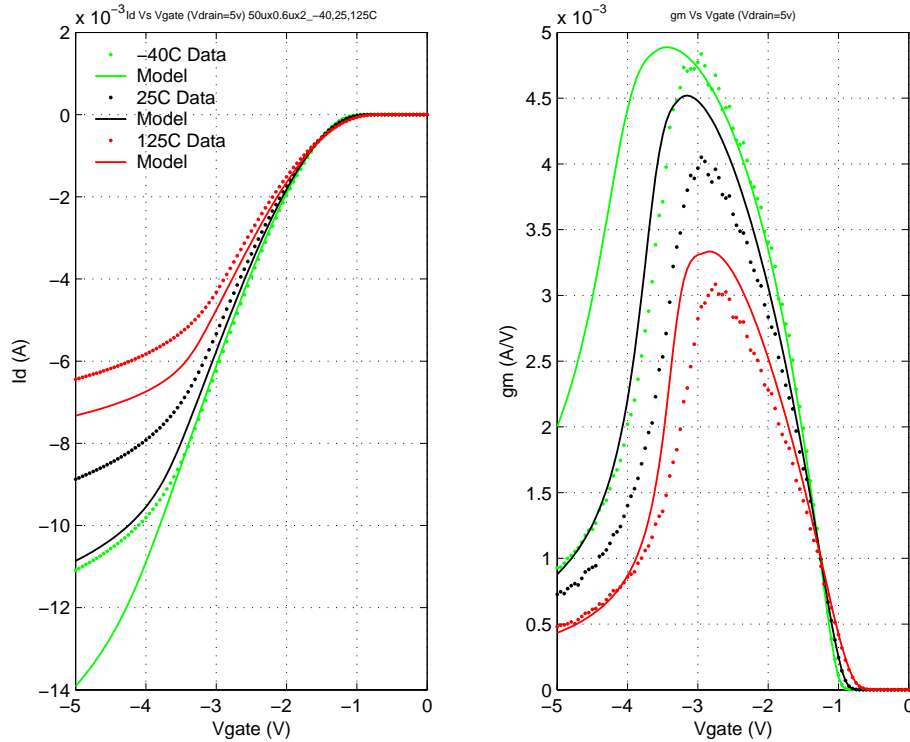


FIGURE 4.122 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_2.4 μ m; Id Vs. Vgs; Vds=-10V

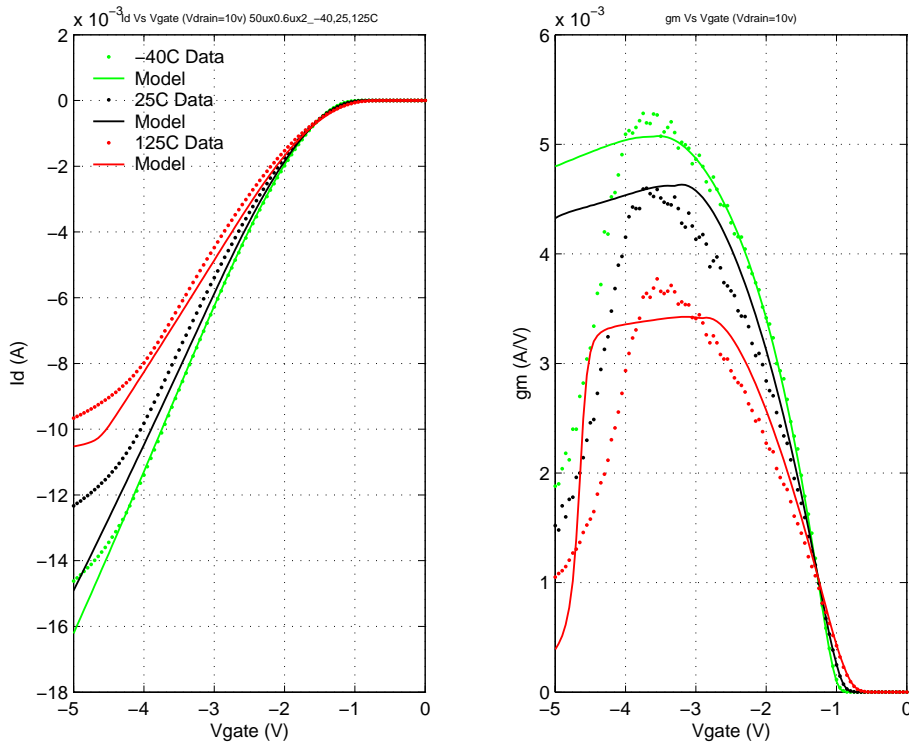


FIGURE 4.123 40V PFET (pfet5p0_Id40); NFxWxL_Id=2x50x0.6_2.4 μ m; Id Vs. Vgs;Vds=-20V

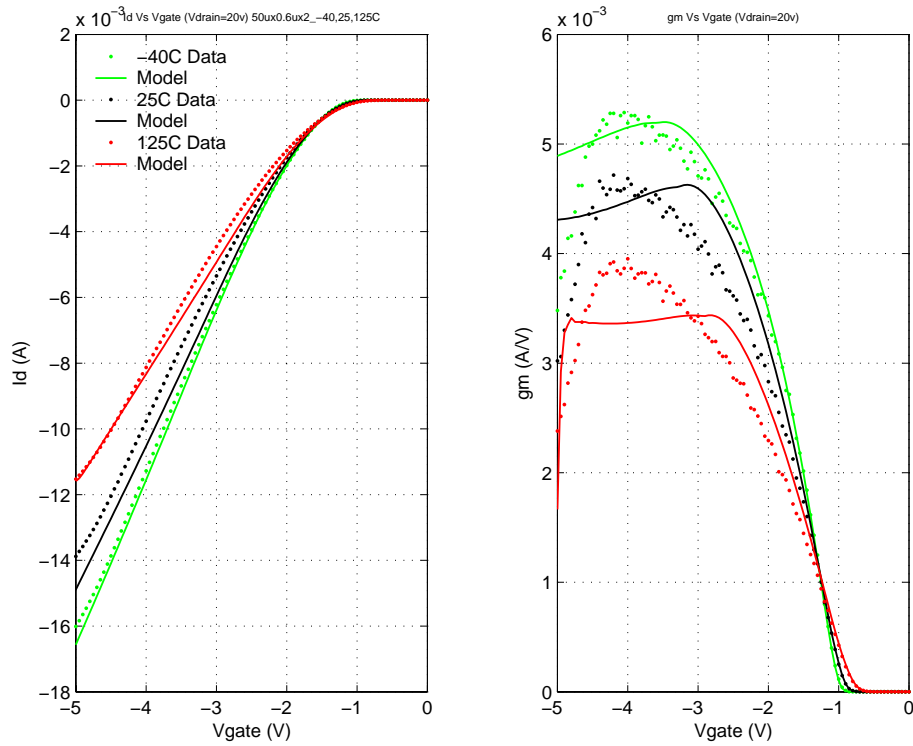


FIGURE 4.124 40V PFET(pfet5p0_Id40);NFxWxL_kd=2x50x0.6_2.4 μ m;Id Vs. Vds;Vgs=0,-1...-5; -40C

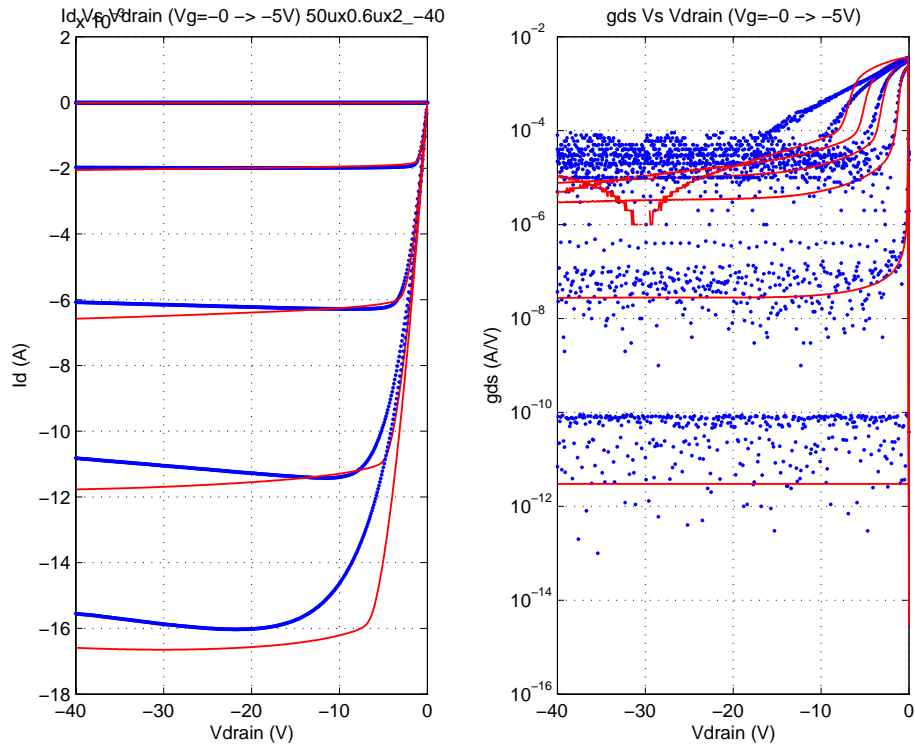


FIGURE 4.125 40V PFET (pfet5p0_ld40);NFxWxL_kd=2x50x0.6_2.4 μ m;Id Vs. Vds;Vgs=0,-1...-5; 25C

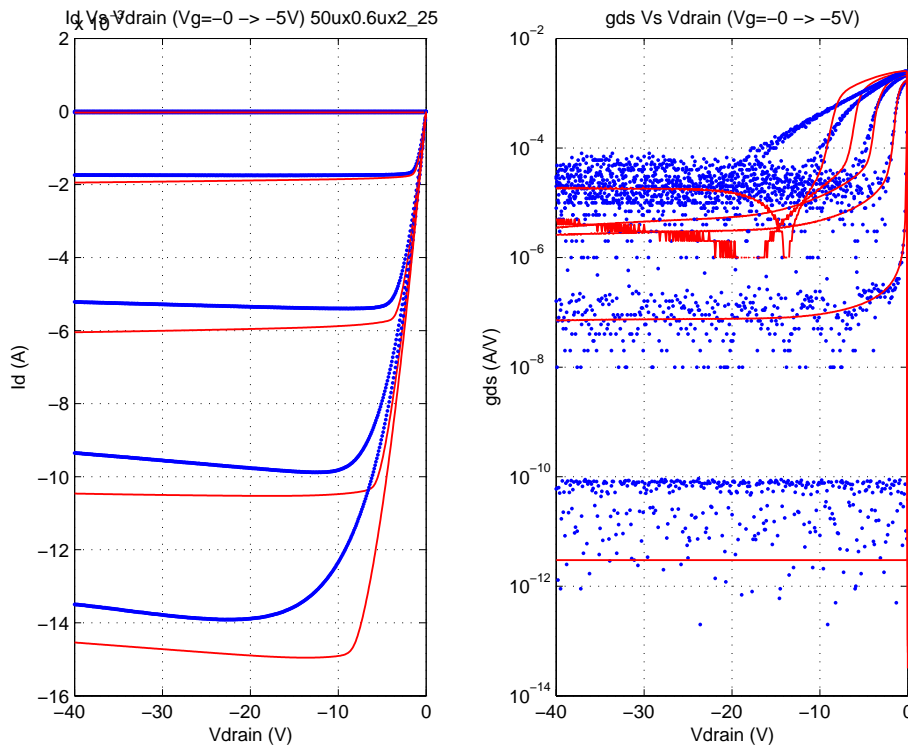
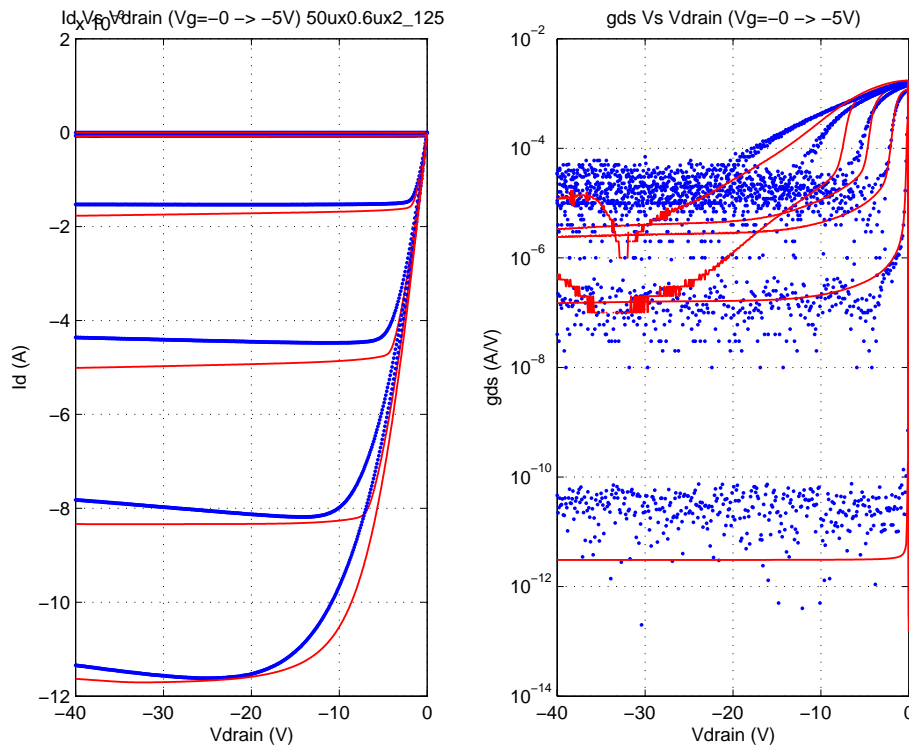


FIGURE 4.126 40V PFET(pfet5p0_ld40);NFxWxL_kd=2x50x0.6_2.4 μ m;Id Vs. Vds;Vgs=0,-1...-5; 125C



4.7 Statistical and Corner Models

Refer to CMOS chapter for statistical/corner model generation and usage. The correlation of the HV FETs with global process variables is accounted for in the statistical models. The extracted process variation from estimated nominal and corner E-specs of the HV process parameters is summarized in Table 4.7. Similarly, the corner model parameters are shown in Tables 4.9 through 4.14. The statistical and corner models will be updated as additional statistical data becomes available.

TABLE 4.8 1- σ variation of HV-FET process parameters in statistical model

Process parameter	12V NFET	12V PFET	40V NFET	40V PFET	Unit
P-substrate doping	10.0	NA	10.0	NA	%
Oxide thickness	3.33	3.33	3.33	3.33	Å
Poly CD	4.2	4.2	4.2	4.2	nm
Channel doping	11	6	14	6	%
N-well doping	17	NA	NA	NA	%
Surface roughness	9	6	5	3	%
Deep N-well doping	NA	10	NA	10	%
P-well doping	NA	10	NA	NA	%
HV N-well doping	NA	NA	14	NA	%
HV P-well doping	NA	NA	NA	6	%

TABLE 4.9 Corner model parameters for 12V NFET (NFxWxL = 6x10x0.5 μ m)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
Drift region	Resistance	Drift region resistance	4.8	3.6	2.3	kOhm
Gate	Resistance	Gate resistance	4.5	3.6	2.7	Ohm
D/B diode	Capacitance	Drain to Bulk Capacitance	41.7	39.7	37.7	fF
MM20 LDMOS	betw	Channel gain factor (W=1 μ m)	214	294	362	μ A/V ²
	cgsow	Gate to source overlap cap. (W=1 μ m)	377	400	425	aF
	kor	Body factor	1084	920	746	mV ^{1/2}
	tox	Oxide thickness	14.3	13.5	12.7	nm
	coxdw	Oxide cap. for int. drift region (W=1 μ m)	0.94	1	1.06	fF
	coxw	Oxide cap. for int. channel region (W=1 μ m)	0.94	1	1.06	fF
	betaccw	Drift region gain factor (W=1 μ m)	190	261	321	μ A/V ²

TABLE 4.10 Corner model parameters for 12V Isolated NFET (NFxWxL = 6x20x0.5 μ m)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
Drift region	Resistance	Drift region resistance	4.5	3.4	2.2	kOhm
Gate	Resistance	Gate resistance	4.9	3.9	2.9	Ohm
D/B diode	Capacitance	Drain to Bulk Capacitance	83.4	79.5	75.5	fF

TABLE 4.10 Corner model parameters for 12V Isolated NFET (NFxWxL = 6x20x0.5μm)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
MM20 LDMOS	betw	Channel gain factor (W=1μm)	139	190	234	uA/V ²
	cgsow	Gate to source overlap cap. (W=1μm)	472	500	531	aF
	kor	Body factor	1.04	0.89	0.72	V ^{1/2}
	tox	Oxide thickness	14.3	13.5	12.7	nm
	coxdw	Oxide cap. for int. drift region (W=1μm)	0.94	1	1.06	fF
	coxw	Oxide cap. for int. channel region (W=1μm)	0.94	1	1.06	fF
	betaccw	Drift region gain factor (W=1μm)	190	261	321	uA/V ²

TABLE 4.11 Corner model parameters for 12V PFET (NFxWxL = 6x10x0.7μm)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
Drift region	Resistance	Drift region resistance	13.9	11.3	8.8	kOhm
Gate	Resistance	Gate resistance	5.8	4.7	3.5	Ohm
D/B diode	Capacitance	Drain to Bulk Capacitance	89	85	80	fF
MM20 LDMOS	betw	Channel gain factor (W=1μm)	53	60	67	uA/V ²
	cgsow	Gate to source overlap cap. (W=1μm)	283	300	318	aF
	kor	Body factor	1003	880	783	V ^{1/2}
	tox	Oxide thickness	14.3	13.5	12.7	nm
	coxdw	Oxide cap. for int. drift region (W=1μm)	0.94	1	1.06	fF
	coxw	Oxide cap. for int. channel region (W=1μm)	0.94	1	1.06	fF
	betaccw	Drift region gain factor (W=1μm)	25.2	28.2	32.0	uA/V ²

TABLE 4.12 Corner model parameters for 40V NFET (NFxWxL = 2x50x0.6μm)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
Drift region	Resistance	Drift region resistance	2.7	2.0	1.2	kOhm
Gate	Resistance	Gate resistance	47	37	28	Ohm
D/B diode	Capacitance	Drain to Bulk Capacitance	48.4	46.1	43.8	fF
MM20 LDMOS	betw	Channel gain factor (W=1μm)	152	167	183	uA/V ²
	cgsow	Gate to source overlap cap. (W=1μm)	283	300	319	aF
	kor	Body factor	0.81	0.66	0.51	V ^{1/2}
	tox	Oxide thickness	14.16	13.36	12.56	nm
	coxdw	Oxide cap. for int. drift region (W=1μm)	1.13	1.2	1.27	fF
	coxw	Oxide cap. for int. channel region (W=1μm)	2.0	2.2	2.34	fF
	betaccw	Drift region gain factor (W=1μm)	114.3	125.7	137.9	uA/V ²

TABLE 4.13 Corner model parameters for 40V Isolated NFET (NFxWxL = 2x50x0.6μm)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
Drift region	Resistance	Drift region resistance	4.3	3.1	1.9	kOhm
Gate	Resistance	Gate resistance	18.1	14.5	10.8	Ohm
D/B diode	Capacitance	Drain to Bulk Capacitance	48.4	46.1	43.8	fF

TABLE 4.13 Corner model parameters for 40V Isolated NFET (NFxWxL = 2x50x0.6 μ m)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
MM20 LDMOS	betw	Channel gain factor (W=1 μ m)	148.4	163.2	179.1	μ A/V ²
	cgsow	Gate to source overlap cap. (W=1 μ m)	283	300	319	aF
	kor	Body factor	0.81	0.66	0.51	V ^{1/2}
	tox	Oxide thickness	14.3	13.5	12.7	nm
	coxdw	Oxide cap. for int. drift region (W=1 μ m)	0.94	1	1.06	fF
	coxw	Oxide cap. for int. channel region (W=1 μ m)	1.88	2	2.12	fF
	betaccw	Drift region gain factor (W=1 μ m)	170.5	187.5	205.8	μ A/V ²

TABLE 4.14 Corner model parameters for 40V PFET (NFxWxL = 2x50x0.6 μ m)

Component	Model Parameter	Description	SLOW	NOM	FAST	Unit
Drift region	Resistance	Drift region resistance	6.5	5.9	4.8	kOhm
Gate	Resistance	Gate resistance	77.6	62.1	46.6	Ohm
D/B diode	Capacitance	Drain to Bulk Capacitance	110.5	105.2	100.0	fF
MM20 LDMOS	betw	Channel gain factor (W=1 μ m)	50.0	54.0	58.2	μ A/V ²
	cgsow	Gate to source overlap cap. (W=1 μ m)	94.3	100	106	aF
	kor	Body factor	0.95	0.85	0.75	V ^{1/2}
	tox	Oxide thickness	14.2	13.4	12.6	nm
	coxdw	Oxide cap. for int. drift region (W=1 μ m)	1.76	1.87	1.98	fF
	coxw	Oxide cap. for int. channel region (W=1 μ m)	1.76	1.87	1.98	fF
	betaccw	Drift region gain factor (W=1 μ m)	3.00	3.24	3.49	μ A/V ²

The comparison of the corner and statistical models to the espec is given in Table 4.15.

TABLE 4.15 Corner and statistical model predictions for HV FETs

Device	E-spec.	SLOW			NOM			FAST		
		Target	Corner	Stat.	Target	Corner	Stat.	Target	Corner	Stat.
12V NFET NFxWxL 6x10x0.5 μ m	rdson ³ (Ω -mm)	6.00	6.08	5.70	4.50	4.50	4.54	3.00	3.28	3.38
	vt (V)	0.85	0.86	0.88	0.70	0.71	0.72	0.55	0.56	0.55
	idsat ¹ (mA)	18.60	19.20	19.90	25.68	27.38	27.50	32.76	35.21	35.10
	beta ² (μ A/V ²)		3383	3520		4606	4630		5836	5740
12V Iso. NFET NFxWxL 6x20x0.5 μ m	rdson ³ (Ω -mm)	7.10	7.20	6.59	5.50	5.32	5.35	3.90	3.96	4.11
	vt (V)	0.85	0.83	0.86	0.70	0.69	0.70	0.55	0.54	0.54
	idsat ¹ (mA)	32.64	30.60	31.60	45.00	43.56	43.80	57.36	55.81	56.00
	beta ² (μ A/V ²)		4877	5060		6657	6700		8404	8340
12V PFET NFxWxL 6x10x0.7 μ m	rdson ³ (Ω -mm)	17.40	17.71	17.40	14.50	14.88	14.80	11.60	12.18	12.20
	vt (V)	-0.91	-0.91	-0.91	-0.81	-0.80	-0.81	-0.71	-0.71	-0.71
	idsat ¹ (mA)	-9.78	-9.73	-9.85	-12.18	-11.65	-11.5	-14.58	-14.06	-13.2
	beta ² (μ A/V ²)		1022	1020		1167	1170		1350	1320

TABLE 4.15 Corner and statistical model predictions for HV FETs

Device	E-spec.	SLOW			NOM			FAST		
		Target	Corner	Stat.	Target	Corner	Stat.	Target	Corner	Stat.
40V NFET NFxWxL_LD 2x50x0.6_2.4μm	rdson ³ (Ω-mm)	13.60	13.75	7.97	10.80	11.02	11.00	8.00	8.11	14.00
	vt (V)	0.82	0.83	0.85	0.68	0.69	0.69	0.54	0.55	0.54
	idsat ¹ (mA)	22.50	23.13	19.30	30.00	31.31	31.80	37.50	42.83	44.30
	beta ² (μA/V ²)		3759	3640		4329	4350		5091	5060
40V Iso. NFET NFxWxL_LD 2x50x0.6_2.2μm	rdson ³ (Ω-mm)	16.40	17.12	9.90	13.10	13.63	14.10	9.80	9.91	18.30
	vt (V)	0.82	0.80	0.81	0.68	0.65	0.66	0.54	0.52	0.51
	idsat ¹ (mA)	22.50	20.57	19.60	30.00	27.56	26.60	37.50	30.04	33.60
	beta ² (μA/V ²)		3543	3390		4088	4060		4820	4730
40V PFET NFxWxL_LD 2x50x0.6_2.4μm	rdson ³ (Ω-mm)	50.00	43.85	45.10	40.00	39.74	39.90	30.00	33.92	34.60
	vt (V)	-0.98	-0.98	-0.98	-0.88	-0.88	-0.89	-0.78	-0.78	-0.79
	idsat ¹ (mA)	-10.50	-13.31	-13.30	-14.00	-14.91	-14.80	-17.50	-17.10	-16.30
	beta ² (μA/V ²)		1207	1200		1321	1320		1476	1440

Notes:

1. Idsat is defined at Vds=5V, Vgs=5V, Vbs=0V for the 12V NFET; Vds=-5V, Vgs=-5V, Vbs=0V for the 12V PFET; Vds=40V, Vgs=5V; Vbs=0V for the 40V NFET, and Vds=-10V, Vgs=-5V; Vbs=0V for the 40V PFET. |Vds|=40V is used during PCM monitoring and E-spec. definition for the 40V FETs. |Vds|=10V is used for corner and statistical model validation in Table 4.15 to minimize the impact of the thermal model equations.
2. There are no E-specs. for beta. The table shows spread in model predictions. Beta is extracted from peak Gm in the linear region (|Vds|=0.1V).
3. Rdson is defined in the linear region as $R_{dson} = (V_{ds}/I_d) \cdot W$, where W is the width of the FET, V_{ds} is 0.1V for the NFETs and -0.1V for the PFETs; I_d is the drain current for a Vgs=5V for the NFETs and -5V for the PFETs

4.8 Mismatch Models

Mismatch models are not supported for HV MOSFETs.

4.9 Flicker Noise

Flicker noise has not been characterized or modeled for the HV FETs.

4.10 Model Update History

4.10.1 v4.0

TABLE 4.16 Mixed-signal model specific updates in model release version 4.0

v4.0 update	Devices	Reason	Impact on user
New MM20 models including corner/statistical	40V N and PFETs	1st release of models	New model available

4.10.2 v4.1

TABLE 4.17 Mixed-signal model specific updates in model release version 4.1

v4.1 update	Devices	Reason	Impact on user
New MM20 models	10 & 40V Isolated NFETs	1st release of models	New model available
Changed BSIM3 based HV FET core model to MM20	12V PFET and 12V NFET	Improve model accuracy	Shifts in DC and AC simulations
New corner and statistical models	12V PFET and 12V NFET	Process variation modeling	Capability available to evaluate impact of process variations on design
Hspice® and ADS® support using MM20 (version MOS2002t) Verilog-A module	All HV FETs in CA18HA	MM20 models were previously available for Spectre® only	Spectre® model uses MM20 (version MOS2001t) primitive Hspice® and ADS® use MM20 (version MOS2002t) Verilog-A component

4.10.3 v4.2

TABLE 4.18 Mixed-signal model specific updates in model release version 4.2

v4.2 update	Devices	Reason	Impact on user
Fixed LDMOS to FET connectivity	All HV FETs in CA18HA	Bug fix	Correct connectivity
Fixed M2 to Active edge distance used in schematic level calculations of parasitic elements	All HV FETs in CA18HA	Bug fix	Improved estimation of parasitics at schematic level
Updated MOS2002t model parameters	All HV FETs in CA18HA	Align to latest updates in MM20 (version MOS2002t)	Change in Hspice® and ADS® simulation results No change in Spectre® simulations

4.11 References

1. A. Aarts, N. Dapos Halleweyn, R. van Langevelde, "A surface-potential-based high-voltage compact LDMOS transistor model," IEEE Trans. on Elec. Devices, Volume 52, Issue 5, May 2005

5.0 Inductor Model

5.1 Device Description

The C18 design kit provides single-ended and differential inductors in a 2.81 μm metal process at M6, M5 or M4 metal top layer. The processes with 6 or 4 metal layers feature square and octagonal spiral geometries, while the process with 5 metal layers currently only has square inductor geometries. The minimum line and space for the octagonal geometries is by 0.01 μm larger than for the square inductors to account for the grid snapping at the 45 degree sides and to not violate DRC rules. The inductor layout cells use a “pwe” layout layer to block the pwell field implant leaving the substrate below the inductors as psub. An overview of inductor specific information for each technology is given in Table 5.1.

TABLE 5.1 Inductor Technologies in C18

Technology / Inductor Feature	HR / HD	PW54 / PD	QA / QD
Geometries	square / octagon	square	square / octagon
Substrate below Inductors	psub	psub	psub
Top Metal Layer	6	5	4
Top Metal Thickness	2.81 μm	2.81 μm	2.81 μm
Minimum Linewidth / space (Square Inductor)	2.5 / 2.0 μm	2.5 / 2.0 μm	2.5 / 2.0 μm
Minimum Linewidth / space (Octagonal Inductor)	2.51 / 2.01 μm	---	2.51 / 2.01 μm
Single-Ended Inductor Shield	square / octagon	square	square / octagon
Differential Inductor Shield	no	no	no
Silicon Validation of Models	yes	no ^a	no [a]

- a. Not all technologies have been validated with silicon data. The models are fully scalable over geometry and across technologies due to the physical basis of the model equations. Extensive silicon data augmented with electromagnetic simulations in various technologies ensure accurate models.

For single-ended inductors an optional ground shield drawn in salicided active is available. The capacitive effect of the packaging compound can be taken into account by selecting the dielectric constant of the compound through the inductor Component Description Format (CDF). An inductor instance is defined by its dimensions and can be modified through the CDF. A schematic cross section of an inductor over substrate is shown in Figure 5.1. The substrate ties in the cross section view are drawn for completeness of the example. Further information on substrate contacts is given in Section 5.2.6.1. Layout snap shots of single-ended and differential inductors in square and octagonal geometries are shown in Figure 5.2 through Figure 5.5.

FIGURE 5.1 Cross section view of inductor

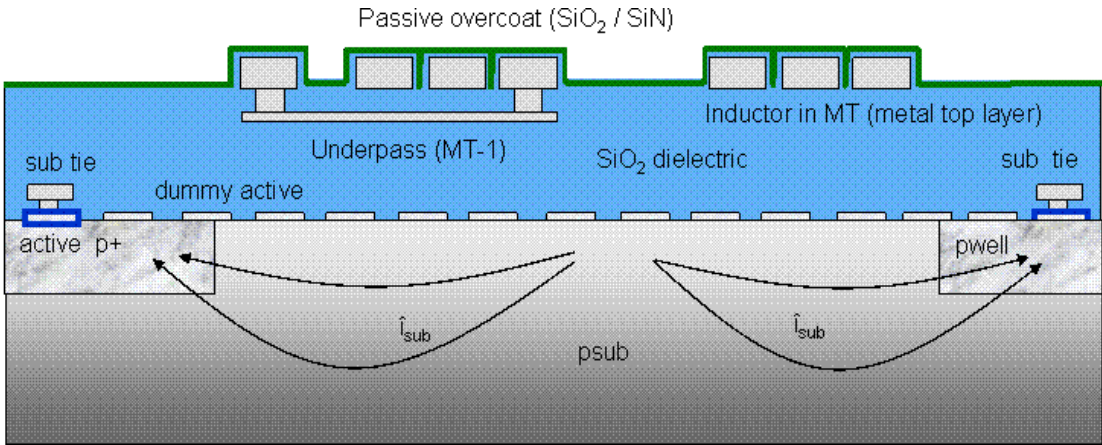


FIGURE 5.2 Square Single-Ended Inductor

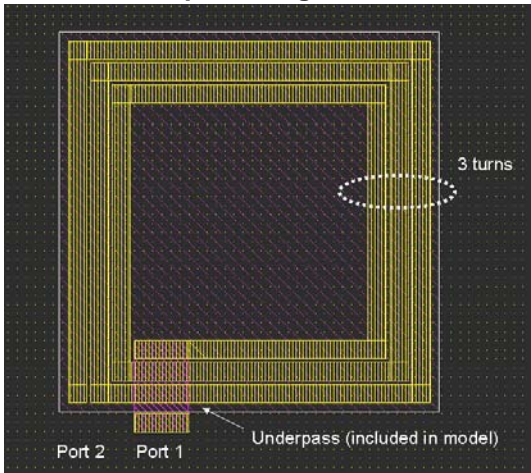


FIGURE 5.3 Square Differential Inductor

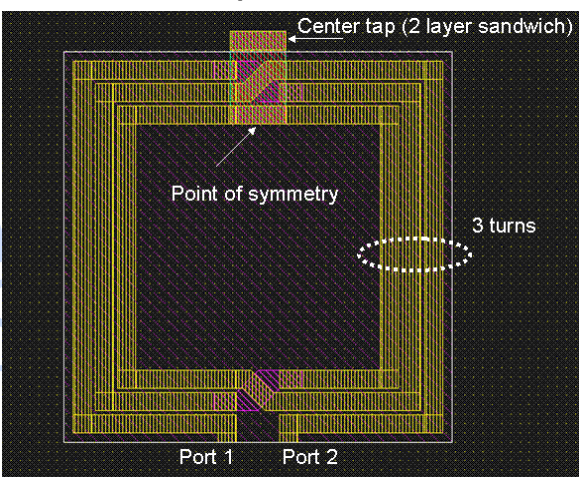


FIGURE 5.4 Octagon Single-Ended Inductor

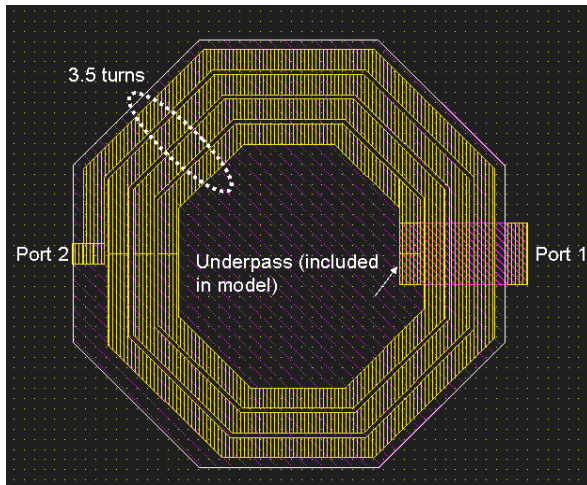
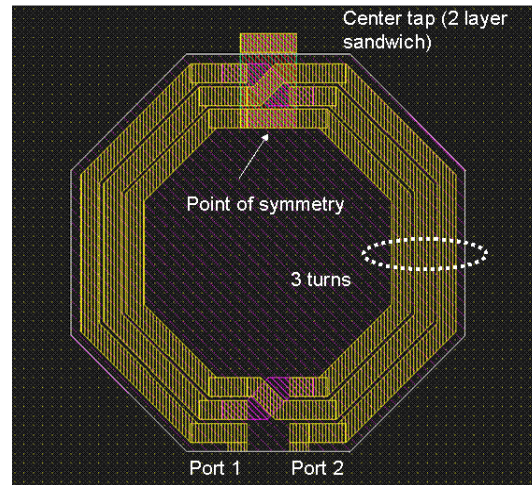


FIGURE 5.5 Octagon Differential Inductor



5.1.1 Inductor Layout Generator (PCELL)

The inductor layout generator creates the layout using the information entered through the CDF properties window. For singled-ended inductors, the inner end is connected to port 1 by an underpass, that is included in the model. The underpass exit can be chosen between “straight” and “perpendicular” which refers to the angle of the underpass to the last spiral segment. While both exit orientations are available on the square inductor for all full and fractional turn numbers, on the octagonal inductor the exit is forced to perpendicular for the fractional quarter turns and can only be chosen between “straight” and “perpendicular” for the full turn layout. The width of the underpass is scaled by a factor 3 with respect to the inductor line width. The maximum scaled width is $30\mu\text{m}$, beyond which the underpass width is set equal to the inductor line width.

Differential inductors offer the choice of a center tab through the CDF property. To minimize the dc resistance, the tab width is scaled by 3 to a maximum width of $30\mu\text{m}$. For line width greater $30\mu\text{m}$ the tab width is set equal to the inductor line width. To reduce the parasitic of the tab connection, the tab exit from the symmetric point in the core of the inductor is routed vertically down and then sandwiched in the 2 metal layers beneath the crossover layer. In case that greater flexibility is needed in designing the tab, the layout pcell can be flattened and the tab can be customized. However it should be avoided to run the tab through the core of the inductor to avoid increasing the ac resistance and degrading quality factor Q of the inductor.

The designer must verify that the number of vias drawn at the cross-overs or underpass connections are sufficient to carry the current in the inductor. For allowable current densities please refer to the electrical specifications document. If additional vias are required, the layout pcell can be flattened and vias be added manually.

5.2 Model Description

The inductor modeling within the design kit is enabled through the JAZZ Inductor ToolBox (JIT). The JIT is a matlab program which takes as inputs inductor layout parameters and produces netlist component values for the inductor sub circuit model. The layout parameters entered through the inductor CDF in the design kit are outer dimension, line width, line space and number of turns.

5.2.1 Sub-circuit representation

The equivalent circuit representations of single-ended and differential inductors are shown in Figure 5.6 and Figure 5.7, respectively. The individual model components which are listed in Table 5.2, are based on physical models and are computed using geometrical and electrical process specification (espec) information.

FIGURE 5.6 Sub-Circuit Model for Single-Ended Inductor

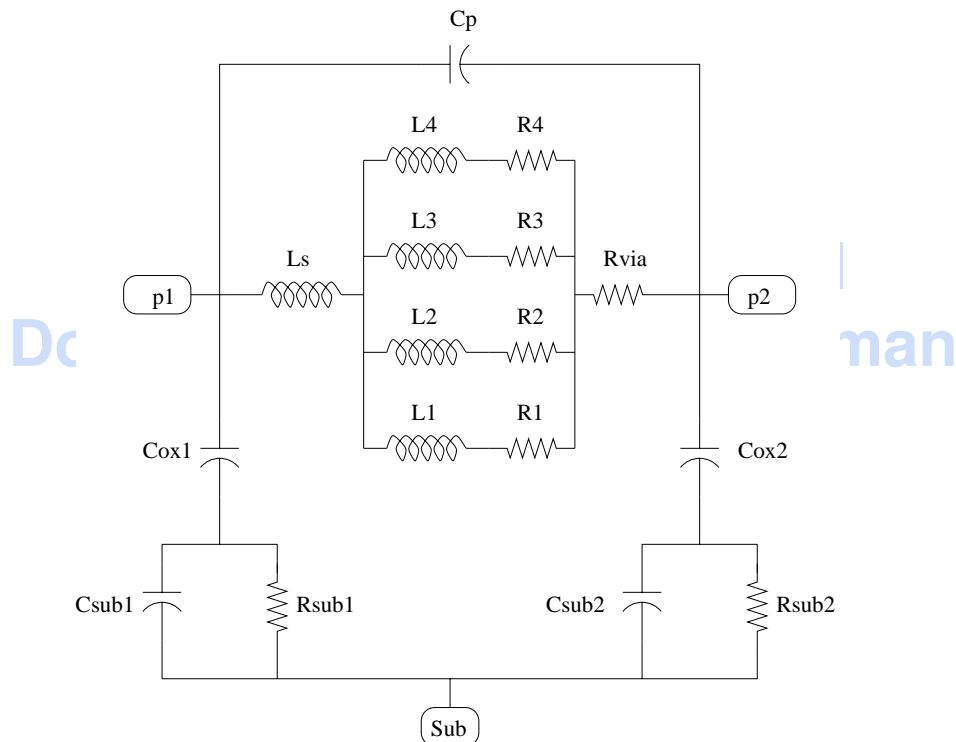
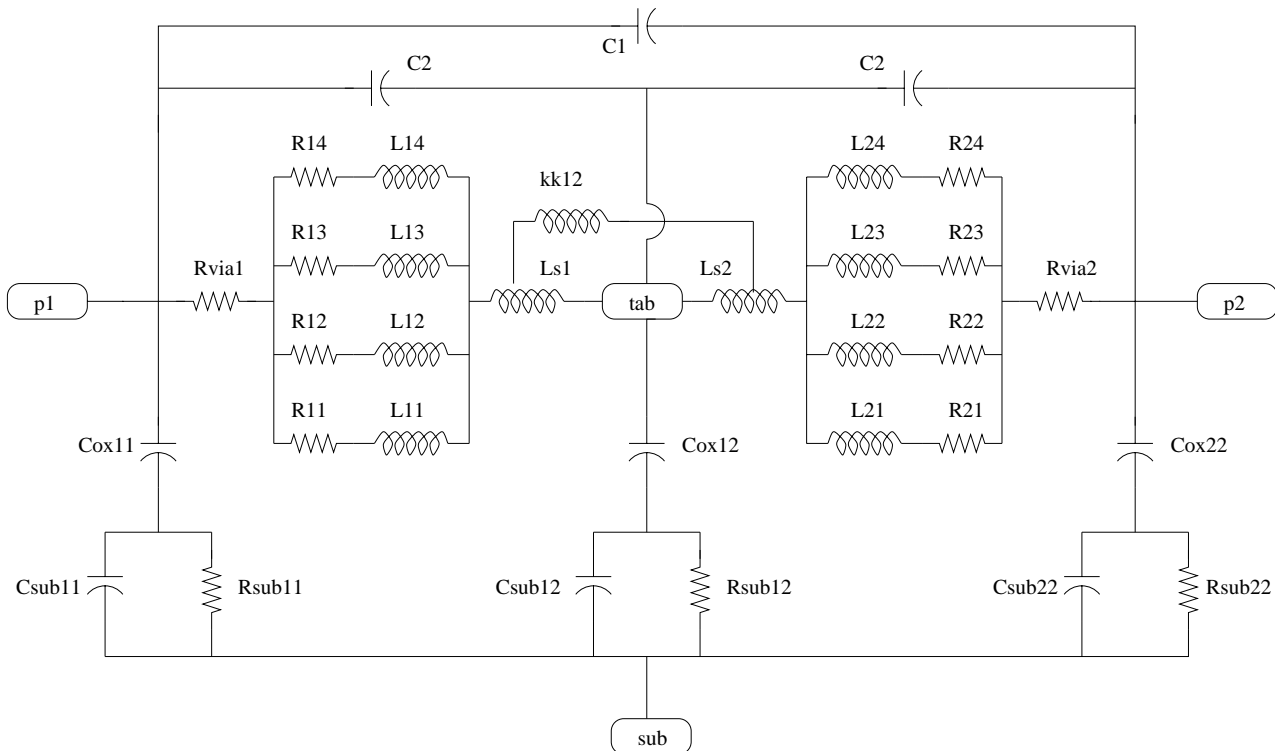


FIGURE 5.7 Sub-Circuit Model for Differential Inductor

TABLE 5.2 Inductor Model Components

Component	Description
Csub	Substrate capacitance
Rsub	Substrate resistance
Cox	Oxide capacitance
Cp / C1, C2	Interwinding and cross-over capacitance
Rvia	Underpass / cross-over via resistance
Ls	Inductor series inductance
R1 - R4	Ladder resistance components (equal to R of spiral and underpass / cross-over)
L1 - L4	Ladder inductance components (circuit phase equal to phase at low frequency)
kk	Mutual inductance

The radio frequency (RF) skin effect pushes the current at higher frequencies to the surface of the metal line, effectively increasing the resistance of the inductor (AC resistance). This effect is modeled using a ladder circuit comprised of resistors and inductors that approximate the conductor as 4 concentric shells. The parallel combination of resistors in the ladder circuit resistance corresponds to the DC resistance of the inductor, while the inductance of the ladder corresponds to the internal inductance of the metal trace. This internal inductance is due to the flux linkage of the current to itself and is gradually turned off as the current conducting cross-section is restricted with increasing frequency. For this reason, a droop of the inductance from the DC value is observed on inductors that are affected by the skin effect.

Series inductance and mutual coupling are calculated using the Grover - Greenhouse formulations [1]. The ac resistance model and the series inductance describe the rising section of the Q curve and determine the peak Q value that is achievable with a particular inductor design.

The interwinding capacitance or feed forward capacitance, electrically couples the ports of the inductors. The oxide capacitance couples the inductor to the substrate. Both capacitances are significant in determining the self-resonant frequency of the inductor. Their values are calculated using a 2 dimensional interconnect solver. The packaging compound material affects primarily the interwinding capacitance whose value will increase with the dielectric constant of the material.

The substrate parasitic resistance is empirically fit to inductor RF measurements. The substrate capacitance is calculated using a simple fringing capacitance formulation. These parasitic affect the roll-off section and the shape of the Q curve.

Single-ended inductors can be drawn over active ground shield to improve the Q value. The sub circuit topology is identical to the case of unshielded inductor in Figure 5.6. Using a ground shield lowers the substrate resistance by moving the ground return path from bulk silicon to the shield structure. The reduced ground return resistance is absorbed into the substrate resistance component, leaving the circuit topology unchanged.

5.2.2 Model selection

The inductor CDF allows for selection of geometric information of "Xsize", "Ysize", "Width", "Spacing", "Number of Turns" and information on operating frequency and frequency range. After modification of these properties, the inductor performance results and sub circuit component values for the nominal case at the nominal temperature of the circuit simulator are calculated and displayed. For proper simulation results it is necessary to include a substrate pin connected to ac ground into the schematic. The substrate pin name must be identical to the CDF parameter name defined under "Substrate Node".

For differential inductors, the center tab connection point is included in the model. Simulated results returned from the RF simulation engine and inductor performance CDF results listed in Table 5.3 must match closely.

TABLE 5.3 Inductor CDF Performance Results

Performance	Description
PeakQ / PeakqDiff	maximum Q value
FPeakQ / FPeakqDiff	frequency at Peak Q
SRF / SRFDiff	self resonance frequency
Qinterest / QinterestDiff	Q value at operating frequency
Linterest / LinterestDiff	effective inductance at operating frequency
Rinterest / RinterestDiff	effective resistance at operating frequency
Lfgoes0 / Lfgoes0Diff	effective inductance as frequency approaches zero (Ldc)
Rfgoes0 / Rfgoes0Diff	effective resistance as frequency approaches zero (Rdc)

The performance data for single ended and differential inductors are calculated differently. In single-ended configuration, the port 1 terminal at the inner end of the spiral inductor is connected to ac ground. The resulting impedance seen at the outer terminal port 2 is:

$$R + j \cdot X = \frac{1}{Y_{22}} \quad (\text{EQ 1})$$

In differential configuration, the ground connection of the equivalent circuit is assumed a virtual, floating ground and the resulting impedance from port 1 to port 2 is:

$$R + j \cdot X = Z_{11} + Z_{22} - 2 \cdot Z_{12} \quad (\text{EQ 2})$$

The reported metrics in the differential inductor CDF use the impedance from port to center tab, which is half the value from port 1 to port 2 or:

$$R + j \cdot X = \frac{1}{2} \cdot (Z_{11} + Z_{22} - 2 \cdot Z_{12}) \quad (\text{EQ 3})$$

The inductor Q, L and R as reported in the inductor CDF are calculated from the single-ended or differential impedance ZL:

$$Q = \frac{\text{imag}(Z_L)}{\text{real}(Z_L)} \quad (\text{EQ 4})$$

$$L = \frac{\text{imag}(Z_L)}{2 \cdot \pi \cdot \text{freq}} \quad (\text{EQ 5})$$

$$R = \text{real}(Z_L) \quad (\text{EQ 6})$$

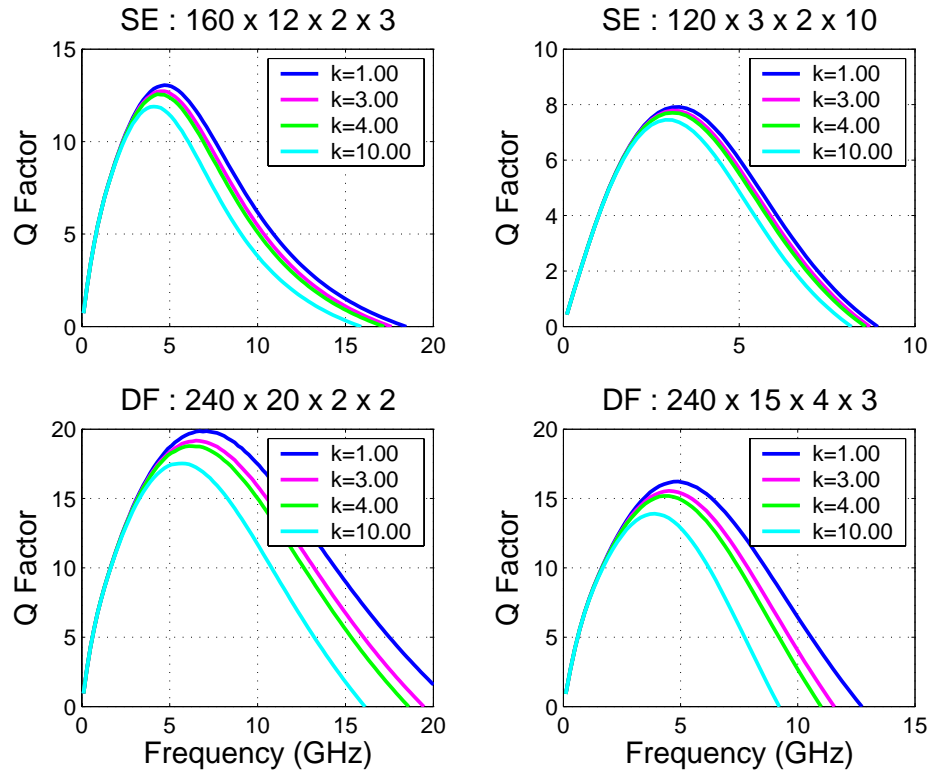
Since the parasitic capacitance of the underpass exit of the single-ended inductor is associated with the inner terminal port 1, the Q at port 2 is higher than the Q at port 1. In single-ended analysis, the admittance Y22 in the impedance equation is replaced by admittance Y21 to extract series inductance and series resistance.

5.2.3 Packaging Compound Material

The packaging compound material affects the interwinding capacitance and its value will increase with the dielectric constant of the material. Through the CDF a relative permittivity ϵ_r in the range from 1 to 10 can be entered to account for the effect of the packaging dielectric on the inductor performance. The default value is 1 which represents air. Increasing ϵ_r will reduce the Q and self-resonant frequency of the inductor. Due to its stronger sensitivity to the interwinding capacitance, the differential inductor performance is more affected by the packaging material than the single-ended inductor. An example of the Spectre simulated Q curve on 4

inductors in the 2.81 μm M6 process as a function of various packaging dielectric permittivities is provided with Figure 5.8.

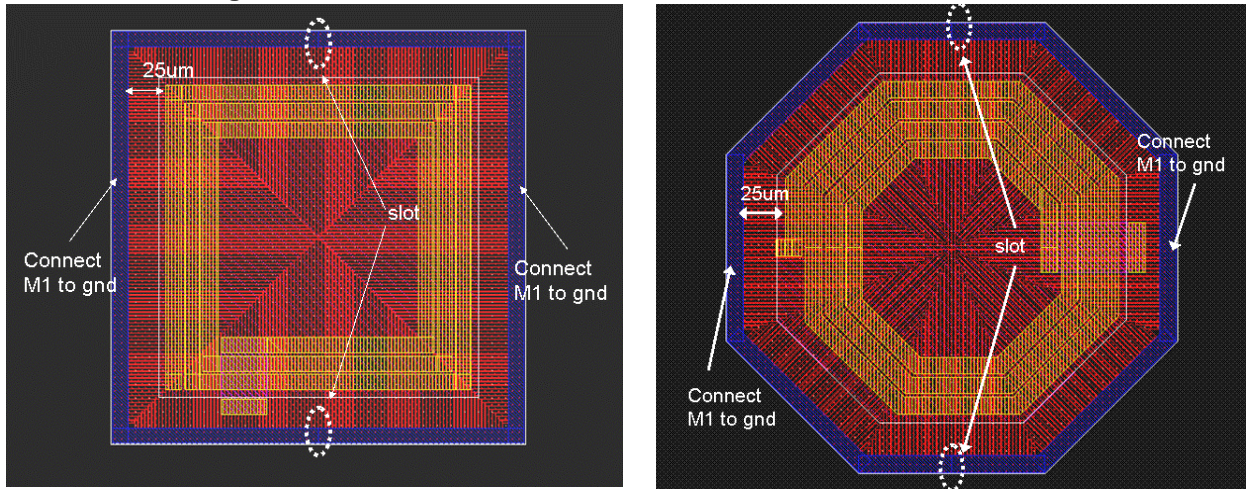
FIGURE 5.8 Effect of Packaging Compound on Inductor Q



5.2.4 Ground Shield in salicided Active

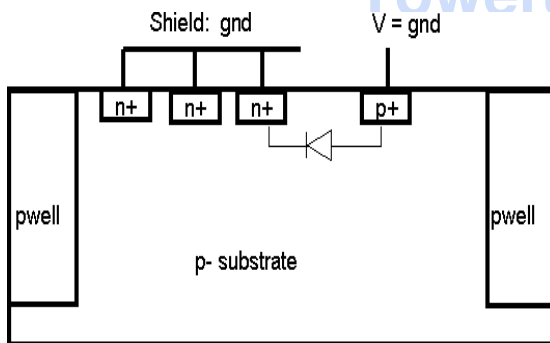
For single-ended inductors the Q performance can be boosted by inserting a ground shield below the inductor. A layout snapshot of square and octagonal inductors with shield is shown in Figure 5.9. The shield is by default 25 μm per side larger than the inductor (outside edge of inductor to inside edge of shield metal 1). A metal 1 frame at the perimeter of the shield connects the shield fingers which are drawn in active, keeping the resistive loss over the shield small. This frame is slotted at the top and bottom to prevent a closed current loop and should be connected to ac gnd at the 2 sides of the frame segment. The connection however must not short out the slots.

FIGURE 5.9 Single-Ended Inductors with Gnd Shield

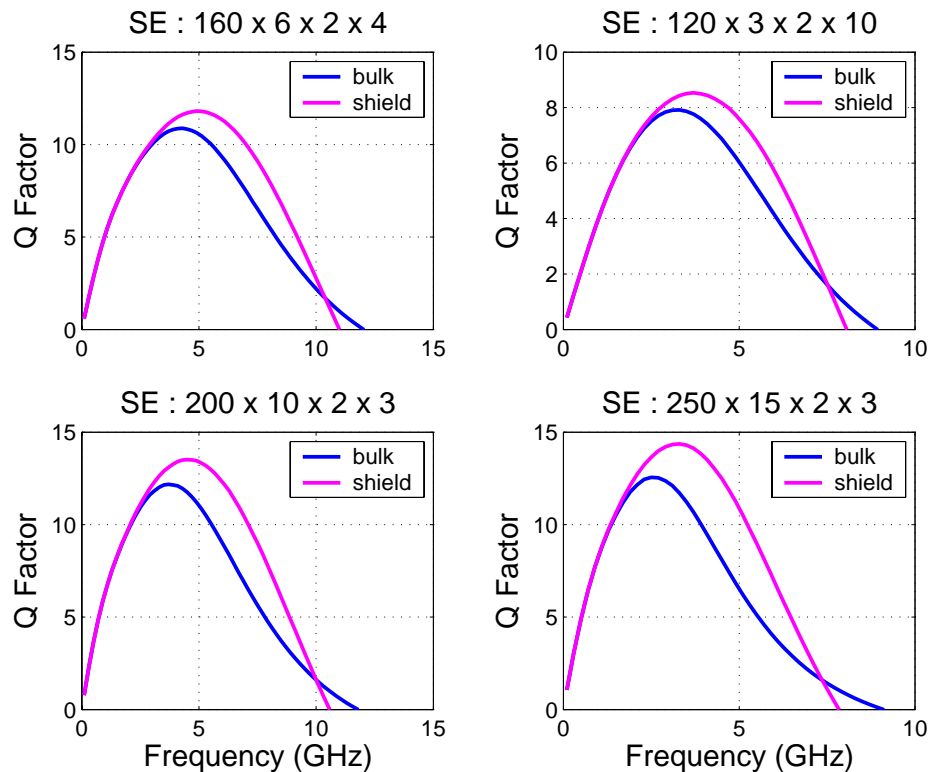


The shield fingers are drawn in salicided n+ active and are located in the p-substrate. With the substrate and shield connected to gnd, the shield forms a zero biased “pn”-junction with the substrate. A schematic drawing of the shield and associated junctions is shown in Figure 5.10. This configuration was used for silicon model validation.

FIGURE 5.10 Shield Connection



The ground shield structure defines an alternative current return path at a lower resistance than the return path through silicon to substrate contacts for the unshielded case. Since the resulting substrate resistance is much lower, a very different dome-like shape Q curve is obtained, rendering the Q more broadband. The effective capacitance to the substrate is increased, approaching C_{ox} as the return path resistance decreases, reducing the self-resonant frequency. An example of the Spectre simulated Q curve on 4 inductors in the $2.81\mu\text{m}$ M6 process with and without shield is shown in Figure 5.11.

FIGURE 5.11 Effect of Shield on Inductor Q

5.2.5 Octagonal Geometry

The performance of the inductor Q can be improved by using an octagonal geometry over the square geometry. When comparing a differential inductor with the same dimensions in square and octagon shape, the trace of the octagon is 17.2% shorter than the square leading to a higher Q and SRF with lower L and R (Figure 5.12). If the octagonal design is adjusted by reducing the line width or by increasing the outer dimension to match the same low frequency inductance and resistance as the square design, it can be seen that the octagon has an inherently better Q than the square inductor.

The differential inductor layout pcell allows a minimum of 1 turn for the octagon while the square differential requires a minimum of 2 turns. The single-ended device starts with 1.25 turns for both octagon and square layouts. A layout snapshot of minimum turn octagonal inductors is shown Figure 5.13 and Figure 5.14. The single-ended octagon is asymmetric in its layout with the lower left quadrant sides forming the “step-in” turn. A symmetric layout 1 turn single-ended device can be realized by using the 1 turn differential inductor without the center tab.

FIGURE 5.12 Q-Performance for Octagon versus Square

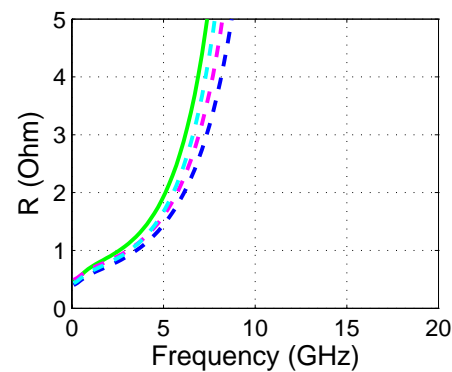
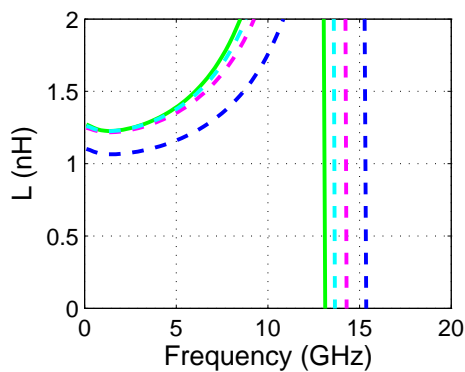
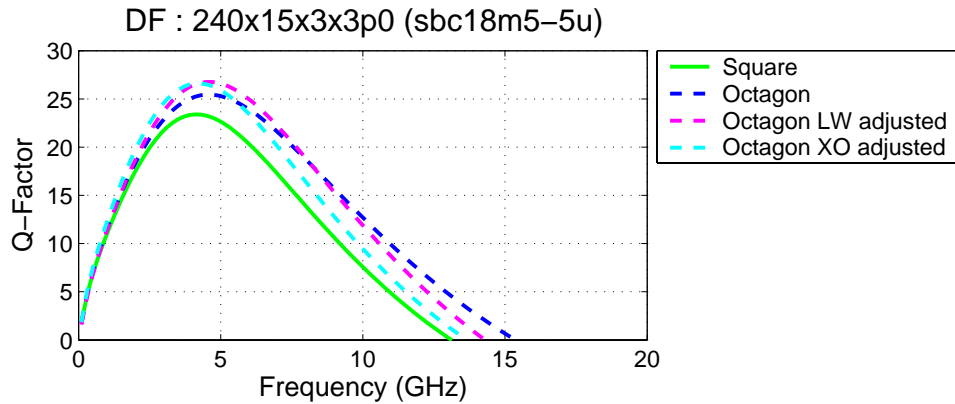
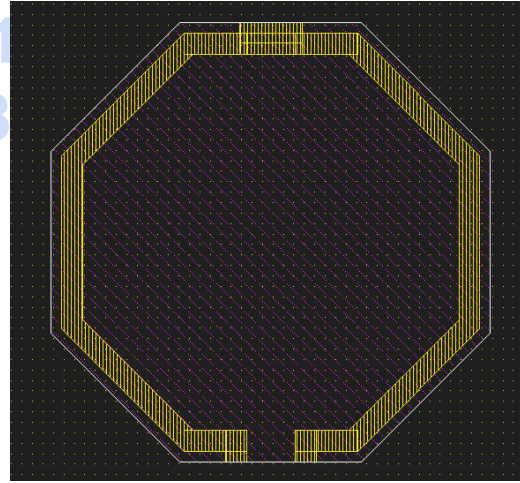
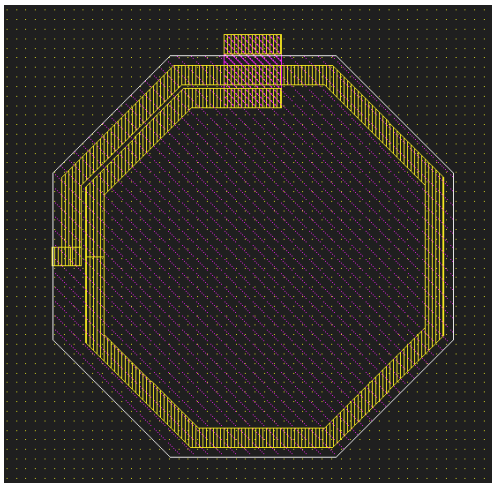


FIGURE 5.13 Single-Ended Octagon N=1.25

FIGURE 5.14 Differential Octagon N=1



5.2.6 Model Accuracy

5.2.6.1 Substrate Contacts

The ground-signal-ground 2-port test structure used for RF measurement on the intrinsic inductor structure, ties the silicon substrate to the equipment ground of the RF probe station and network analyzer. These

substrate ties are at a distance of 75 μm - 100 μm from the inductor. To provide balanced ground return [3], the ground pads are connected between both S-parameter ports by a 100 μm wide bar in top metal which is surrounding the inductor, rendering the structure essentially into a coplanar waveguide. This configuration provides an ideal return path for the signal current to flow back through this bar to the ground probes of the port from which the signal originated. In an actual chip design this bar may not be present, but the measurement obtained on the structure with ideal return path will correspond to the intrinsic inductor as used in the design.

Substrate contacts are not included in the layout PCELL and need to be carefully considered when manually added in the vicinity to the inductor [4]. For a single-ended inductor, substrate ties within approximately 75 μm will affect the Q of the inductor. Generally an increase in Q is observed by reducing the substrate resistance. Concurrently, the effective capacitance to the substrate is increased, approaching C_{ox} in the limit of $R_{sub}=0$ (see Figure 5.6). Thus, the self resonance decreases due to the added capacitance. For differential inductors, substrate ties within 75 μm can cause asymmetry, degrading the Q [4]. In both cases the tie ring should not be a closed loop to avoid an induced current loop from lowering the inductor L through negative mutual coupling.

5.2.6.2 Inductor Q and Current Crowding

The models are verified for inductors using a line space of 2 μm and inductance values greater than 0.3 nH. Inductors with a high layout density suffer from excessive ac resistance due to the proximity or current crowding effect [5]. This effect is not included in the models and such inductors will not be modeled accurately in terms of ac resistance and Q factor. The JIT warns the user of poor inductor designs with a message prompting to reduce the layout density to below 75%. The inductor search tool that can be accessed through the inductor CDF offers a database of approximately 5000 single-ended inductors and 1800 differential inductors that are modeled well and do not exhibit the proximity effect issue.

5.2.6.3 Inductor Q Extraction

The traditional approach to Q extraction which is used for the design manual plots and for the JIT reporting in the unix background window from which the design kit was invoked, defines Q as the ratio of imaginary part of impedance to the real part of impedance

$$Q = \frac{\text{imag}(Z_L)}{\text{real}(Z_L)} \quad (\text{EQ } 7)$$

This arbitrary definition has the awkward property that the Q is zero at self-resonance when the reactive terms of capacitance and inductance cancel and the impedance is purely real. In some applications when the inductor is used as a resonant tank, a more appropriate method of defining Q would be to use the 3 dB bandwidth of impedance or the rate of change of phase of admittance when the inductor is shunted with a capacitor to resonate it at the frequency of interest [6]. The resulting admittance of inductor and shunt capacitor is

$$Y = \frac{1}{Z_L} + j \cdot \omega \cdot C_{Shunt} \quad (\text{EQ } 8)$$

The shunt capacitance will resonate the device at the frequency of interest ω_0 canceling the admittance of the inductor.

$$C_{Shunt} = -\frac{\text{imag}\left(\frac{1}{Z_L}\right)}{\omega_0} \quad (\text{EQ 9})$$

For each frequency, the device is shunted to resonate. The Q at this frequency is calculated by dividing the frequency point f_0 by the 3dB frequency bandwidth of the magnitude of impedance of the shunted device.

$$Q = \frac{f_0}{\Delta f_{3dB}} \quad (\text{EQ 10})$$

Alternatively, the incremental change in phase of admittance at the frequency point f_0 can be used to calculate Q.

$$Q = \frac{f_0}{2} \cdot \left(\frac{\angle Y(f_0 + \Delta f) - \angle Y(f_0 - \Delta f)}{2 \cdot \Delta f} \right) \quad (\text{EQ 11})$$

Both methods return the same result but are fundamentally different to the result using equation [7]. These alternative methods are more computational intensive and require a finer frequency step size for the impedance vector to lead to a stable converged Q result. A resolution on the order of 10 MHz was found suitable and can be generated from the measurement or simulation data using cubic spline fitting. An example of shunt capacitance over frequency, tuned inductor and the Q results obtained with the different methods on measurement data of 2.81 μm M6 single-ended and differential inductors is shown in Figure 5.15 and Figure 5.16, respectively.

FIGURE 5.15 Q Methods on Single-Ended Inductor

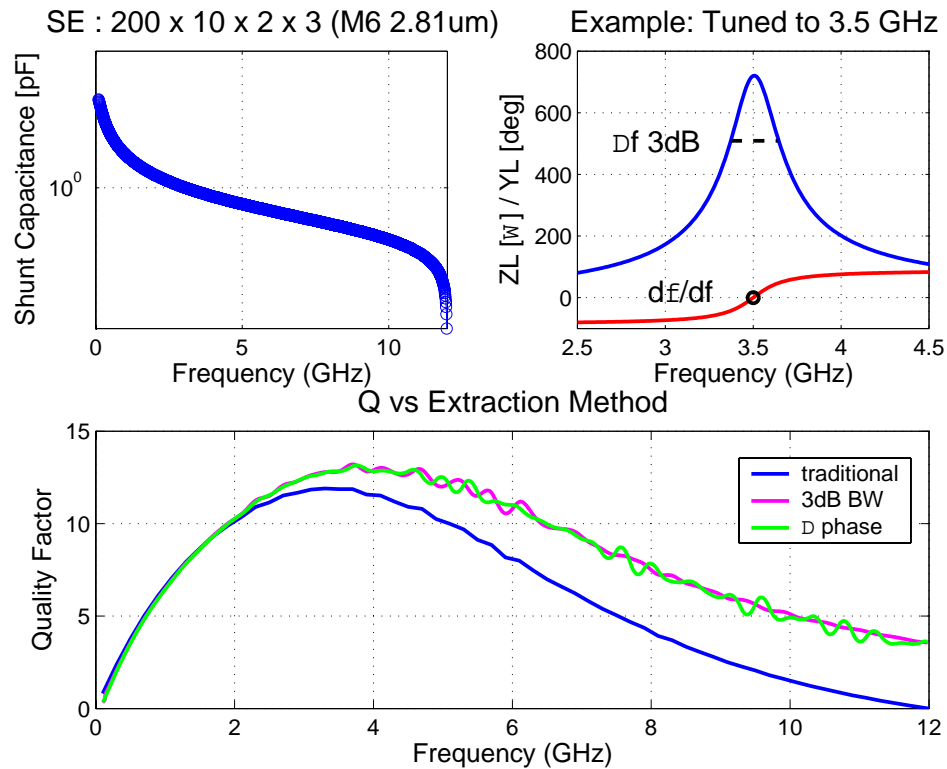
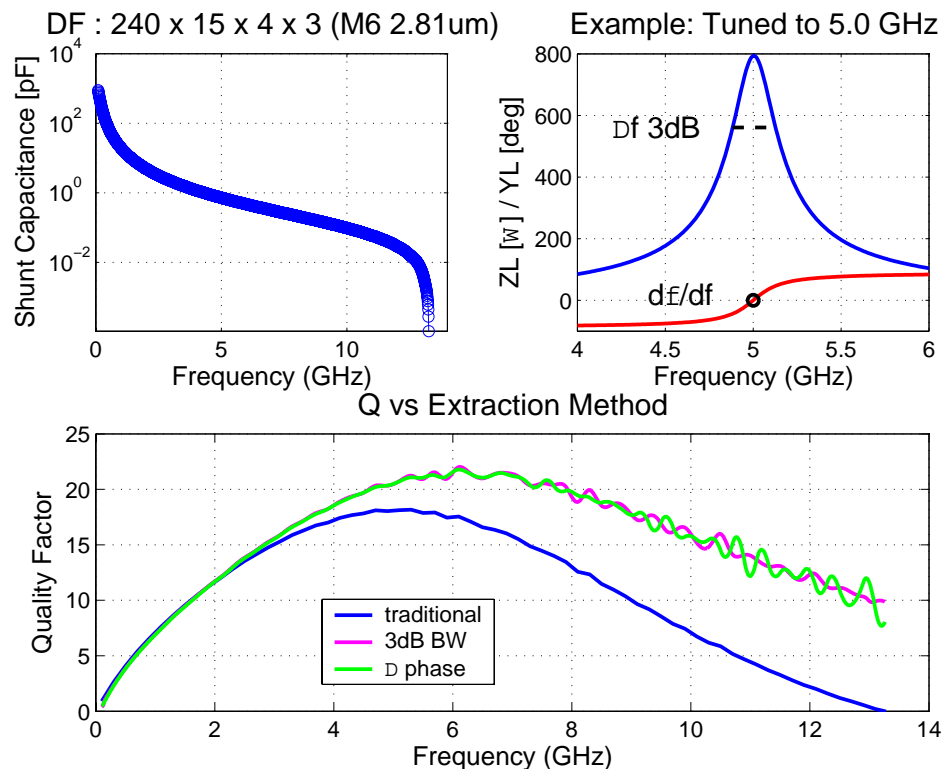


FIGURE 5.16 Q Methods on Differential Inductor

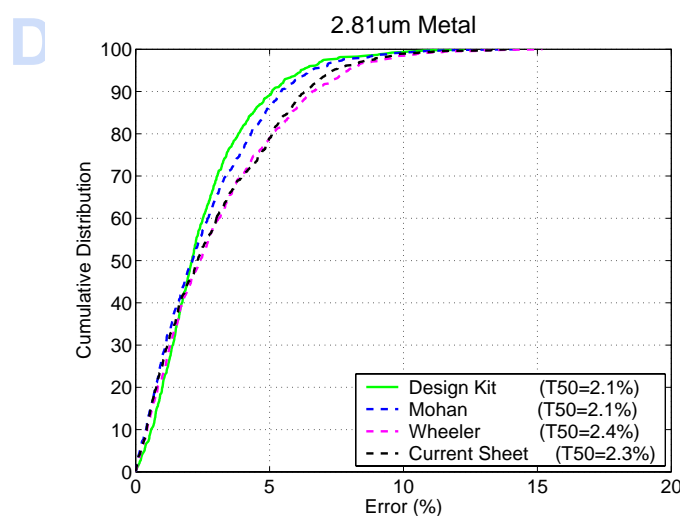


5.2.6.4 Inductance Accuracy

5.2.6.4.1 Square Geometry Inductors

Since it is difficult to obtain an accurate inductance result for the intrinsic device due to inherently small inductance on most inductor designs and contributing effects from the signal feeds, the accuracy of dc inductance was determined through comparison to electromagnetic simulations. The design kit model results on a set of 750 inductors with inductances ranging from 0.3 nH to 12 nH were bench marked against ASITIC [7] numerical simulations, similar to the study described by Mohan et.al [8]. The model inductance is calculated with the JIT using the Grover - Greenhouse equations on the inductor layout as generated by the design kit layout PCELL. ASITIC constructs and solves inductance and capacitance matrices if a low frequency, for example 1 kHz is chosen, which is the electrical analog to solving Maxwell's equation. For comparison, the inductance was also computed using Mohan's empirical equation, modified Wheeler and modified current sheet equations, all described by Mohan et.al. Figure 5.17 shows the cumulative inductance error distributions with respect to the ASITIC result for 2.81 μm metal inductors. From the cumulative error plots, a typical inductance error of 2.1% (median or T50) is obtained for 2.81 μm metal inductors demonstrating the accuracy of the design kit equations. The JIT results are slightly better than the alternatives provided by Mohan. The connecting feed lines to the inductor are not included in the design kit model and need to be accounted for separately by inductance extraction on the actual layout.

FIGURE 5.17 Cumulative error of dc inductance



5.2.6.4.2 Octagonal Geometry Inductors

The accuracy of the inductance models for octagonal single-ended and differential inductors were benchmarked against MIT's FastHenry [9]. FastHenry is a three-dimensional inductance extraction program that computes the frequency dependent self and mutual inductances and resistances between conductors of complex shape.

The difference of the inductance result between design kit model and FastHenry is shown on a large set of 4455 octagonal single-ended inductors and 1485 octagonal differential inductors in the 2.81 μm metal process

with Figure 5.18 and Figure 5.19. The geometry space covered by the histograms ranges from 3 to 35 μm line width, 2 to 10 μm line space and 1 to 9 turns. The JIT results are well within 2% of the FastHenry result. The connecting feed lines to the inductor are not included in the design kit model and need to be accounted for separately by inductance extraction on the actual layout.

FIGURE 5.18 Inductance Calculation Accuracy (Octagonal Single-Ended Inductor)

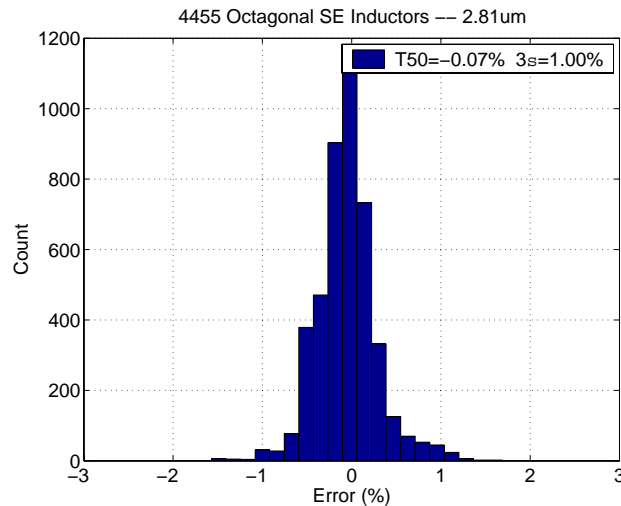
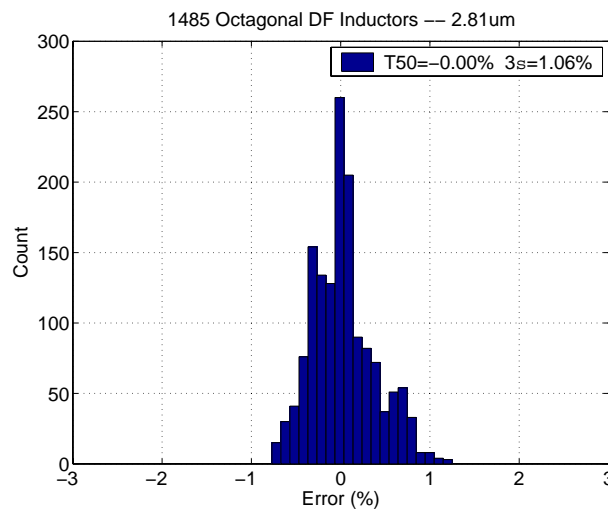


FIGURE 5.19 Inductance Calculation Accuracy (Octagonal Differential Inductor)



5.3 Model Verification

5.3.1 Silicon Validation

The inductor models have been verified by comparing measured high frequency characteristics at 25 $^{\circ}\text{C}$ temperature with the Spectre simulation on the corresponding intrinsic device. Since the inductor verification in silicon requires the use of ground-signal-ground pads and feed lines to connect the device, the measurement results are afflicted with considerable parasitic capacitances, inductances and resistances. These parasitic

effects were removed from the measured data to yield the intrinsic device by subtracting the pad admittance followed by an ABCD matrix multiplication to remove the feed lines. Any deembedding approach is imperfect and the result will only be the approximate true device. Substrate contacts are located in the ground-signal-ground test fixture which is generally at a distance of 75 μ m to 100 μ m to the inductor. Examples of Spectre simulated and measured Q, L, R results for various square single-ended inductors and for differential inductors in square and octagonal geometries in 2.81 μ m metal 6 are shown in subsequent Figure 5.20 through Figure 5.52. The title of each plot describes the inductor type with “SE” for single-ended or “DF” for differential inductor and indicates in parentheses the layout style of square or octagonal geometry. The dimensional information is following the inductor type information in sequence of outer dimension, line width, line space and turns. The specific process and JIT information is marked in the legend.

FIGURE 5.20 Inductor Model Verification

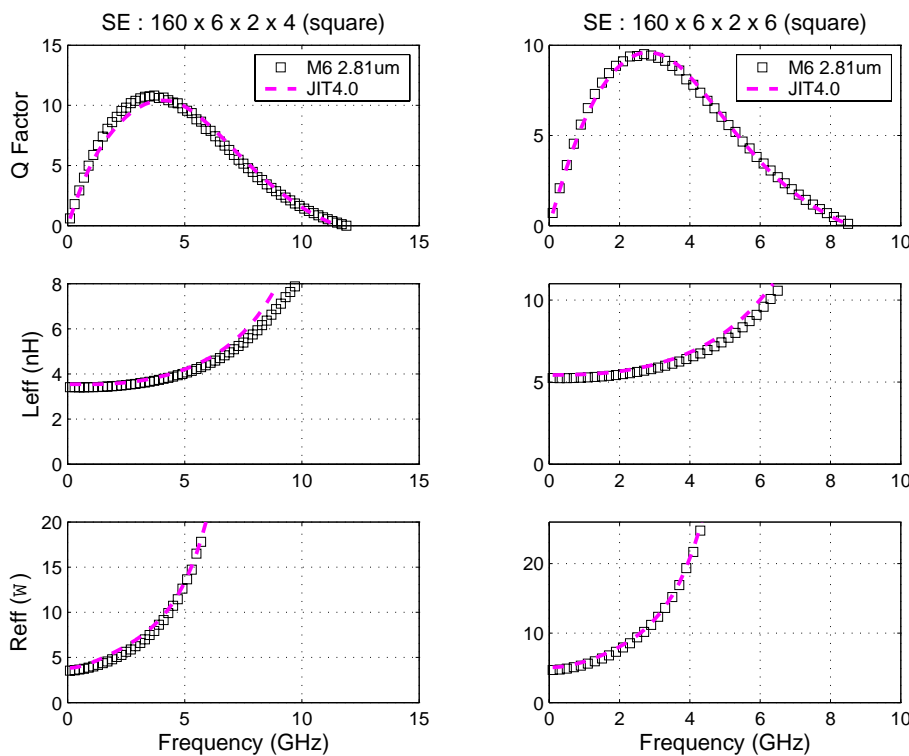


FIGURE 5.21 Inductor Model Verification

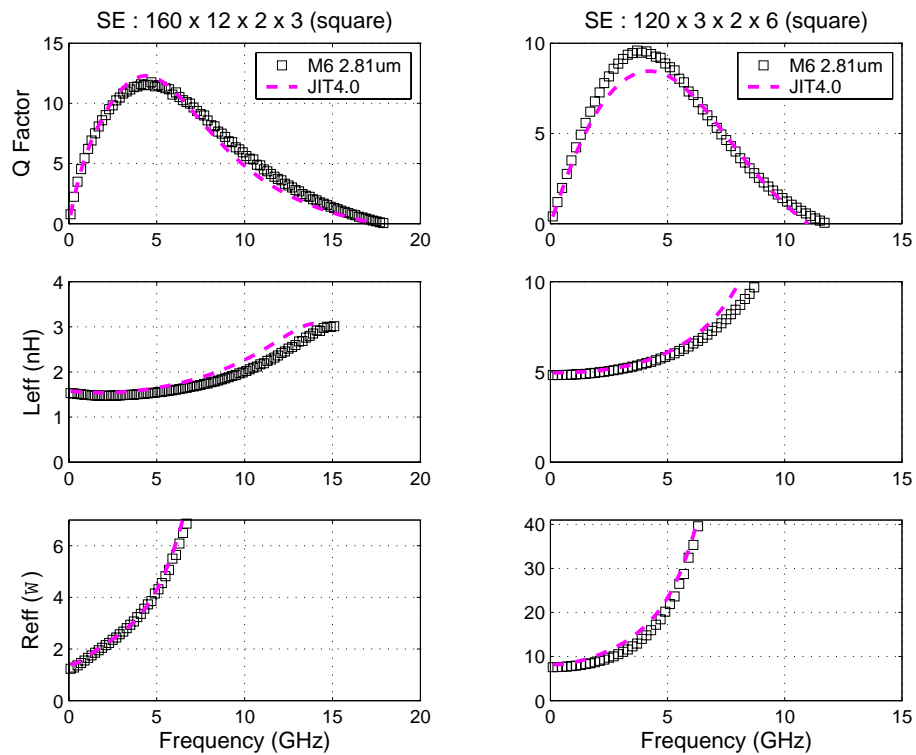


FIGURE 5.22 Inductor Model Verification

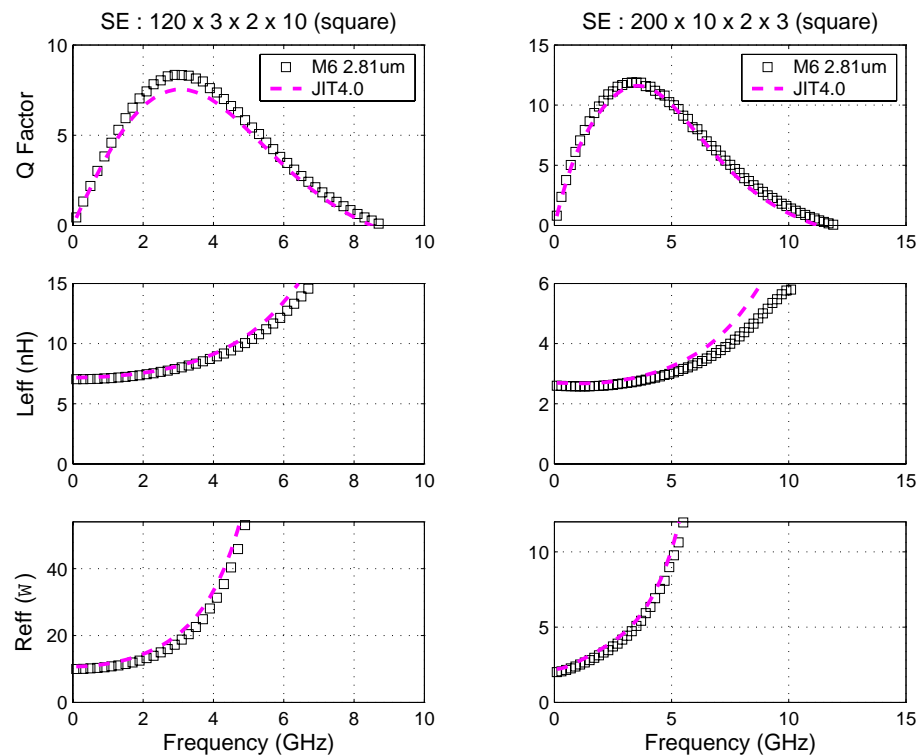


FIGURE 5.23 Inductor Model Verification

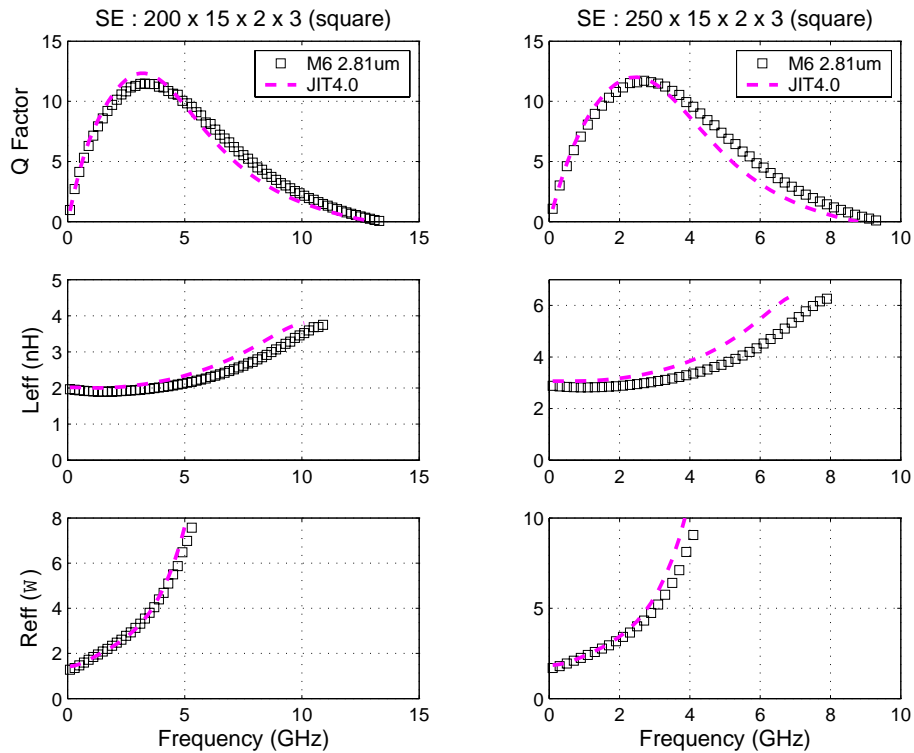


FIGURE 5.24 Inductor Model Verification

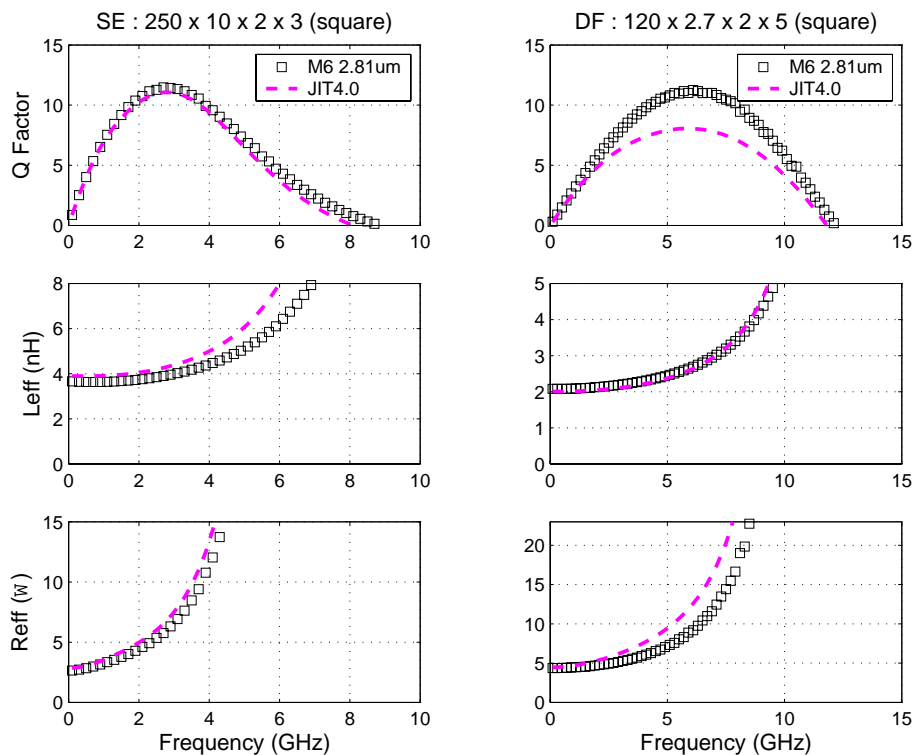


FIGURE 5.25 Inductor Model Verification

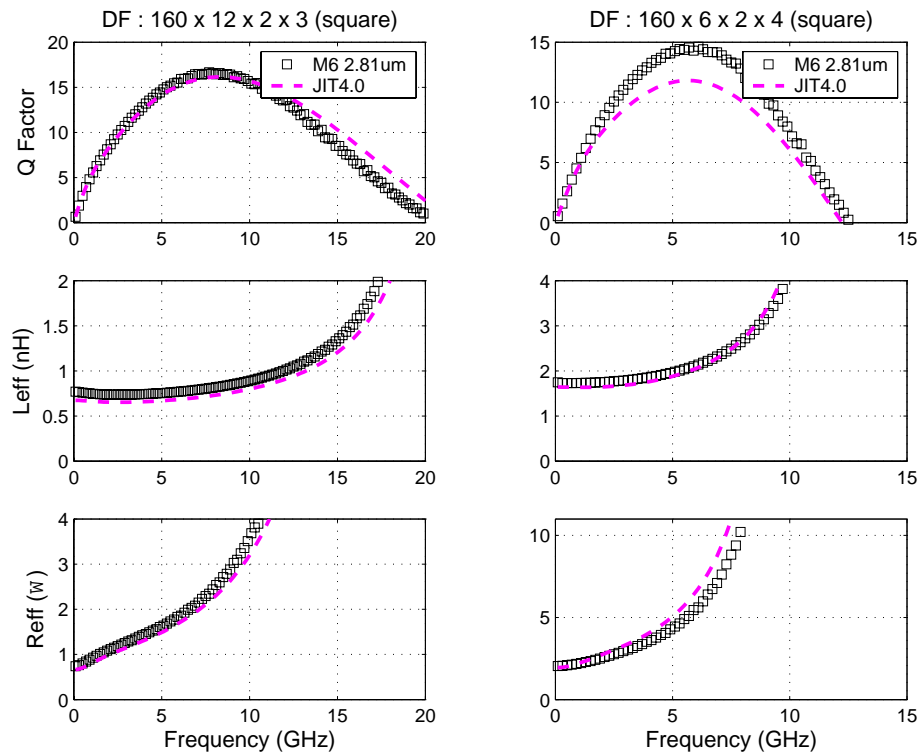


FIGURE 5.26 Inductor Model Verification

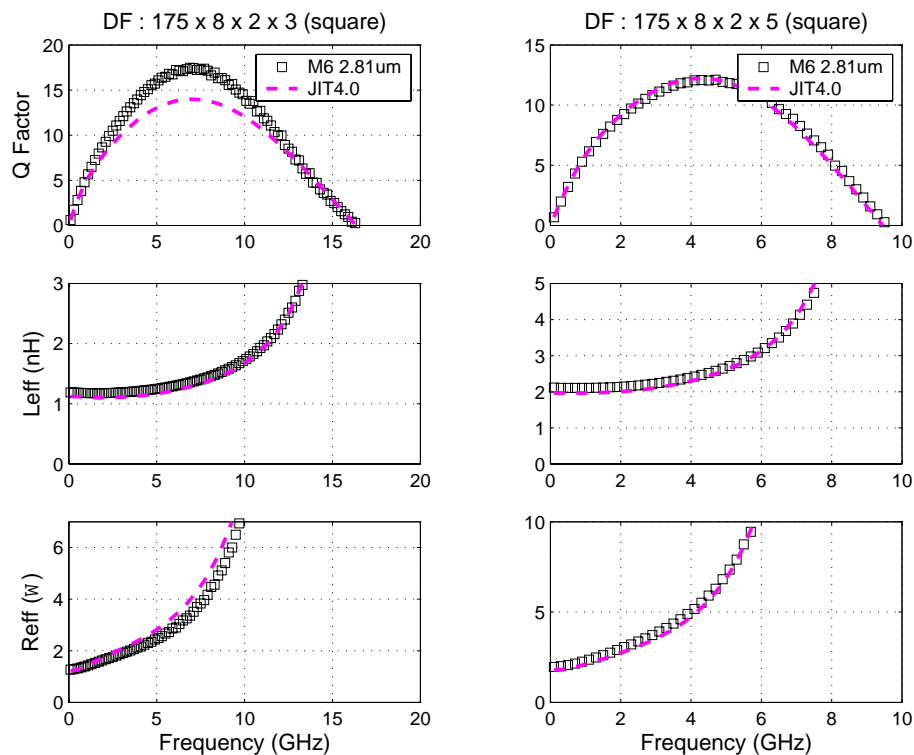


FIGURE 5.27 Inductor Model Verification

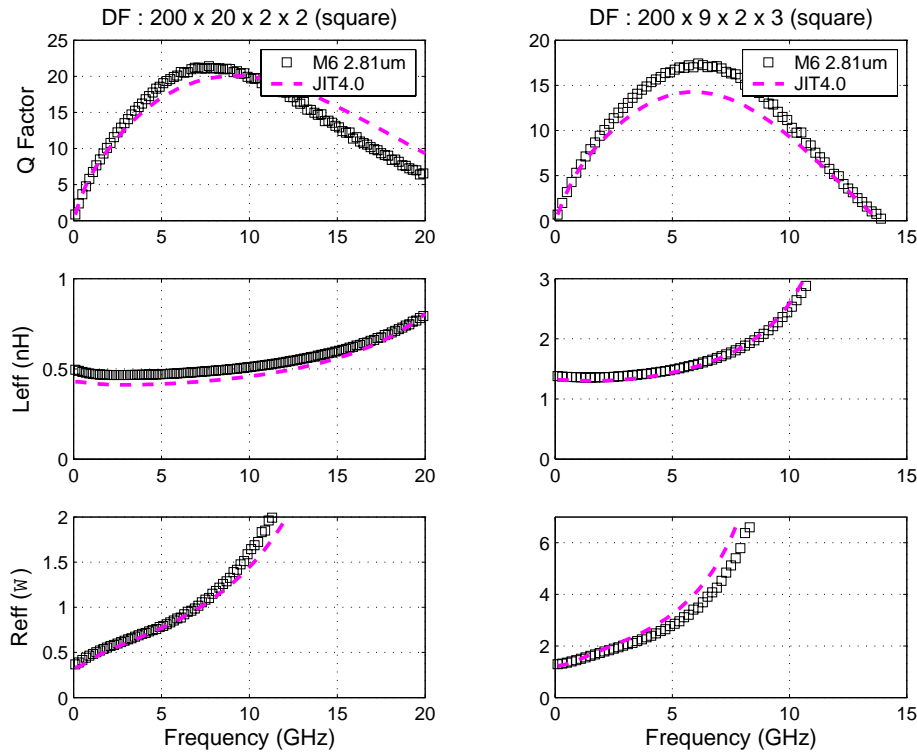


FIGURE 5.28 Inductor Model Verification

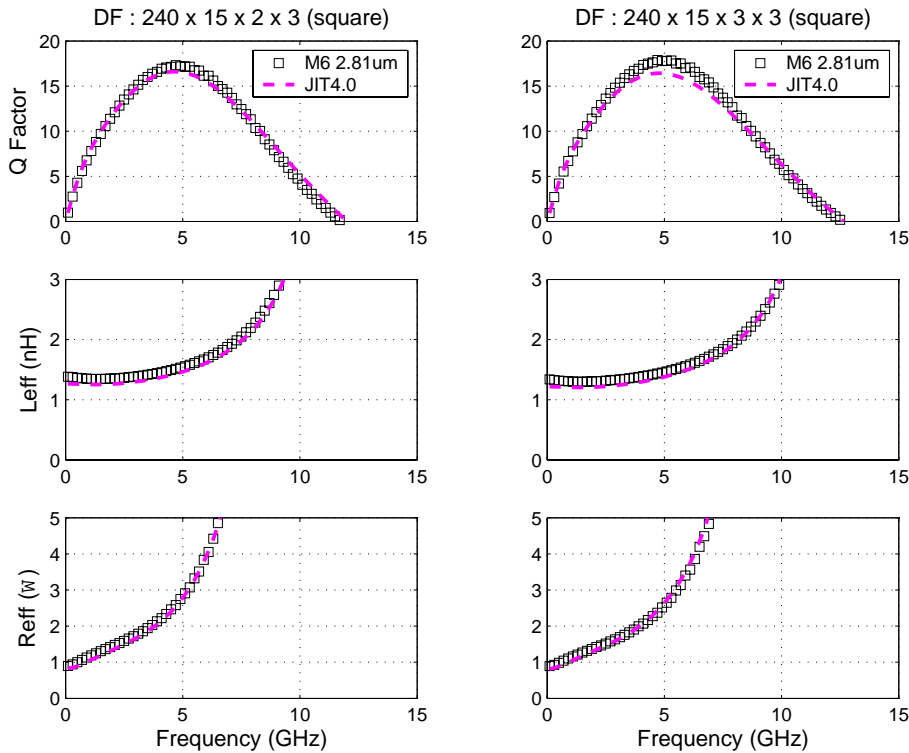


FIGURE 5.29 Inductor Model Verification

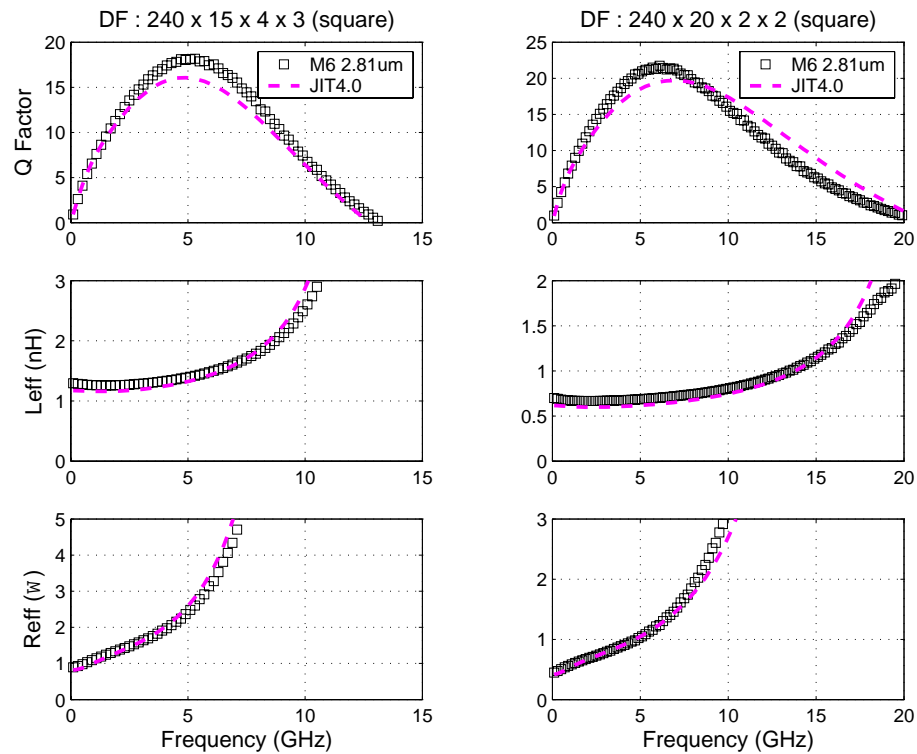


FIGURE 5.30 Inductor Model Verification

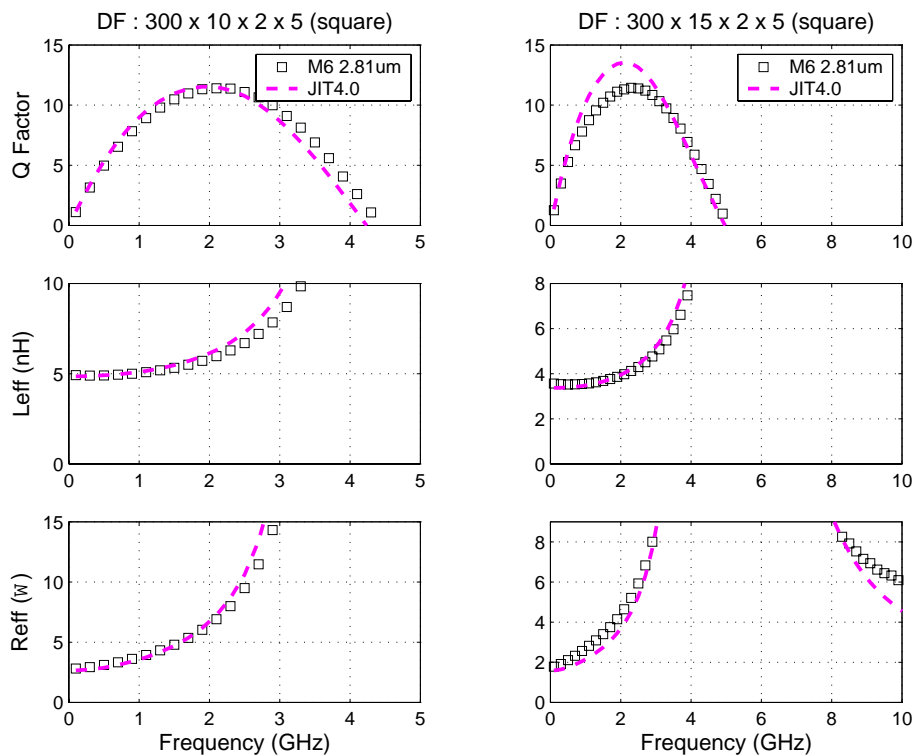


FIGURE 5.31 Inductor Model Verification

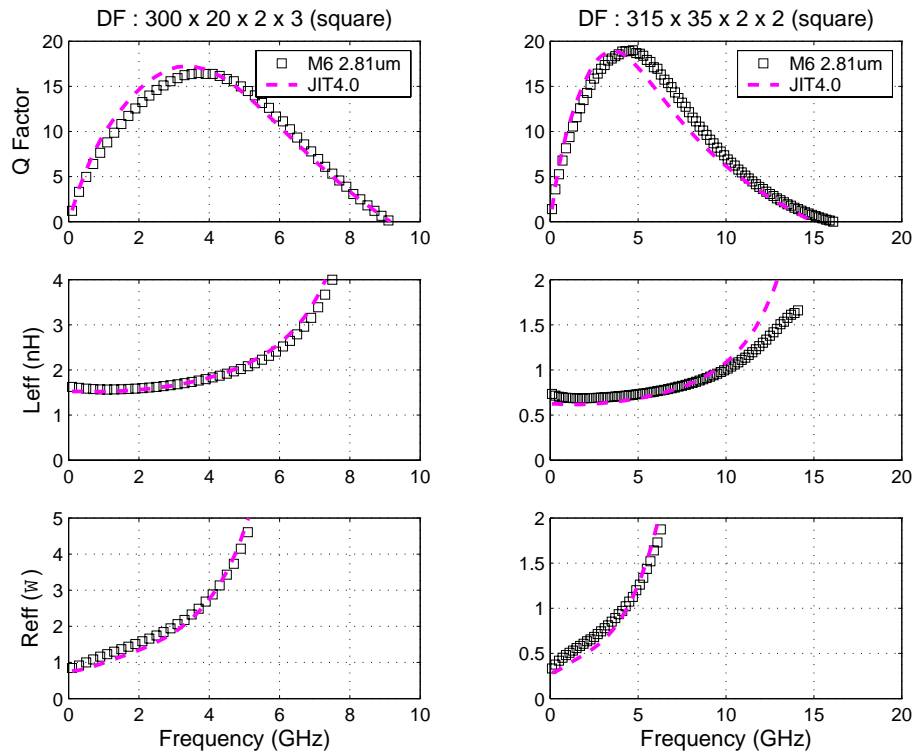


FIGURE 5.32 Inductor Model Verification

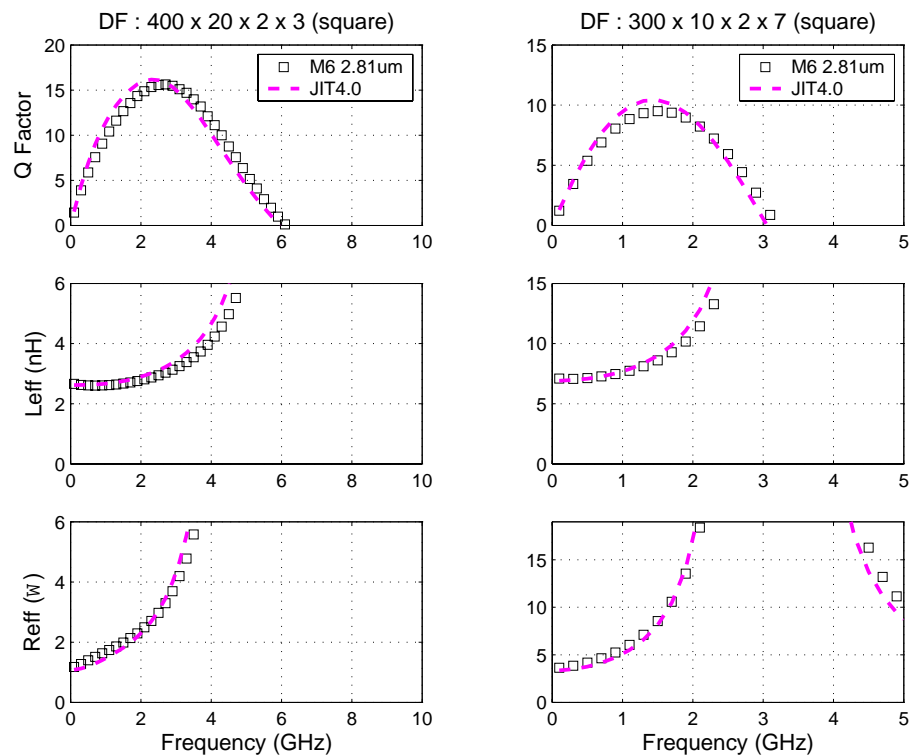


FIGURE 5.33 Inductor Model Verification

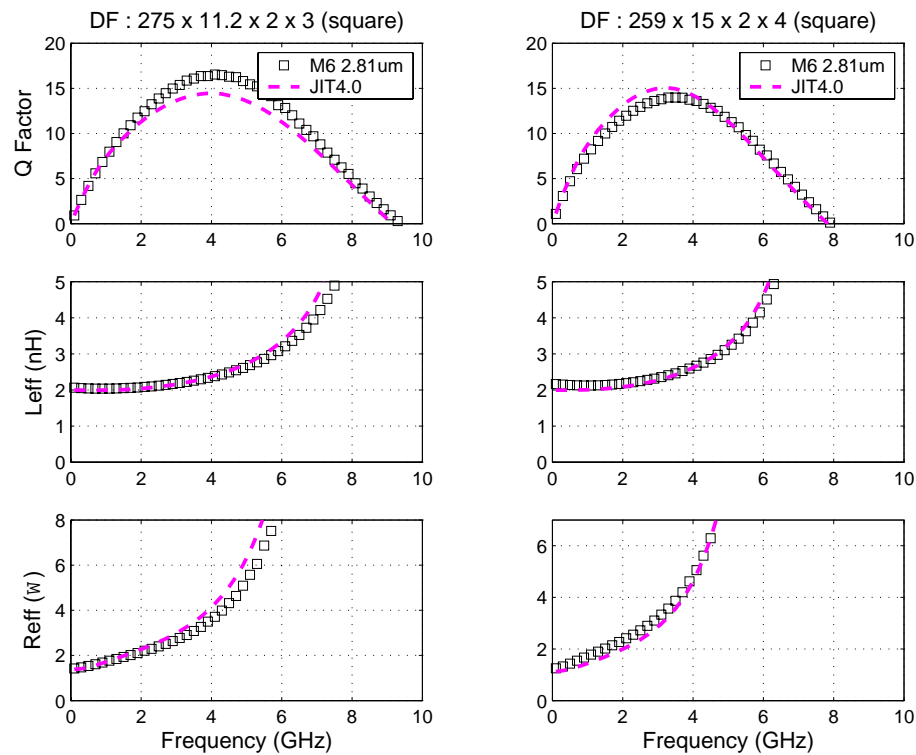


FIGURE 5.34 Inductor Model Verification

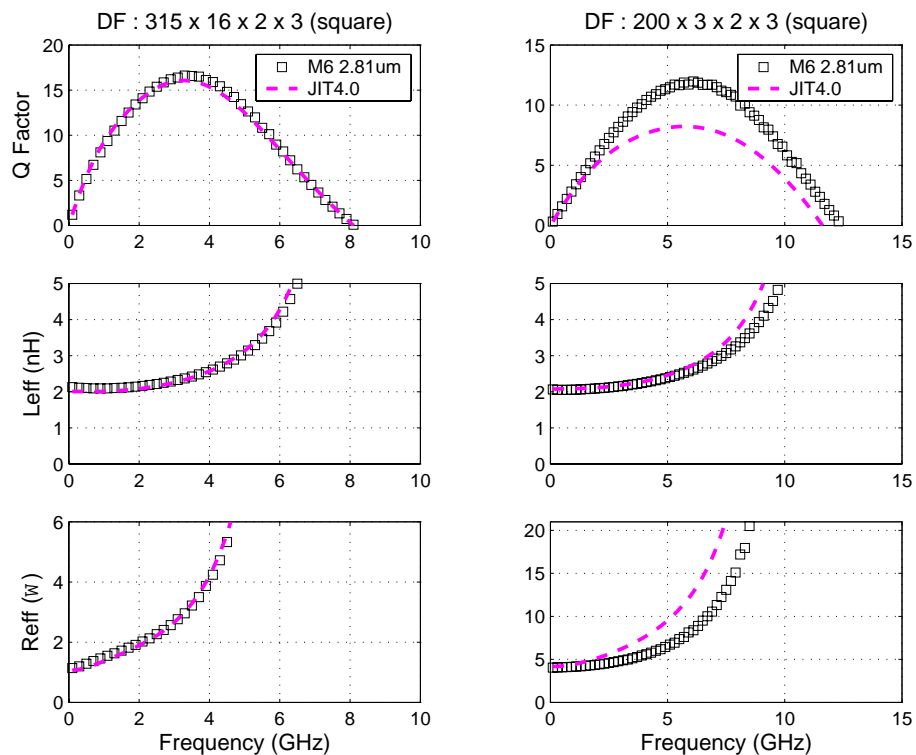


FIGURE 5.35 Inductor Model Verification

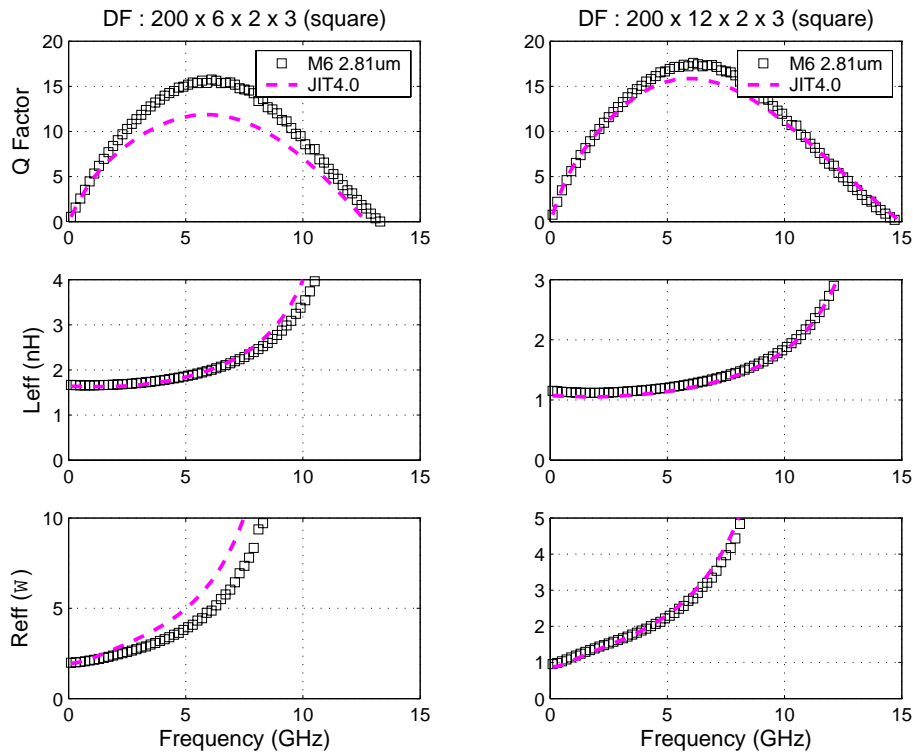


FIGURE 5.36 Inductor Model Verification

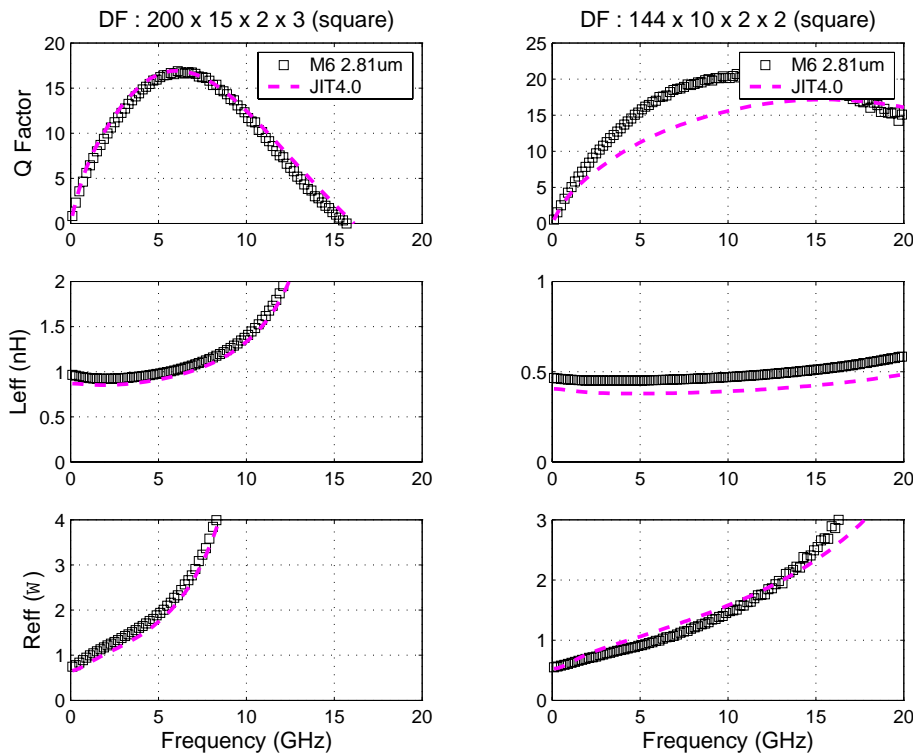


FIGURE 5.37 Inductor Model Verification

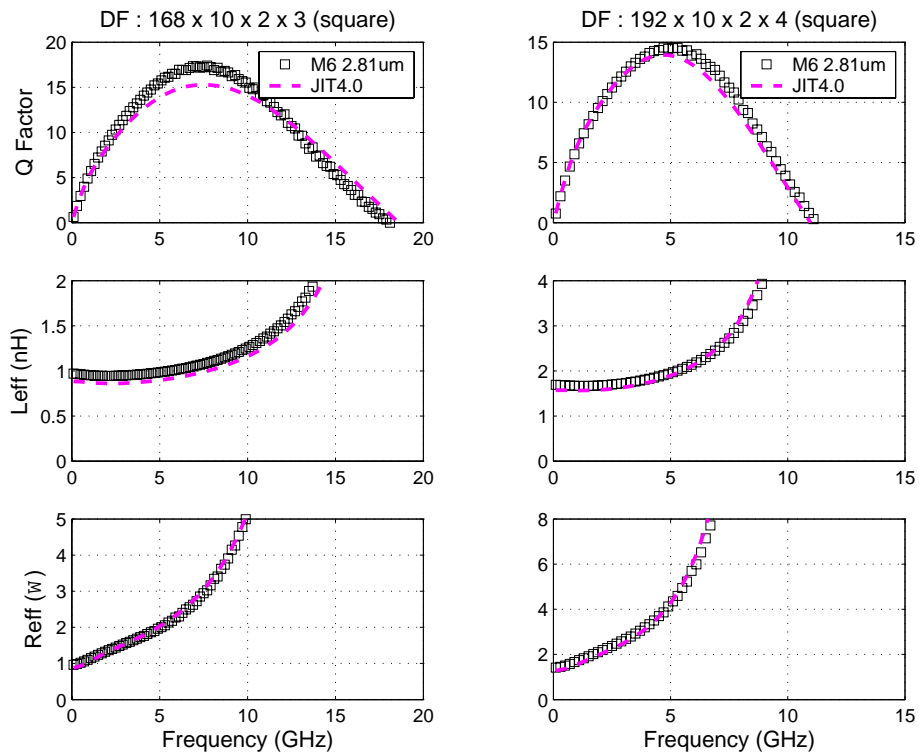


FIGURE 5.38 Inductor Model Verification

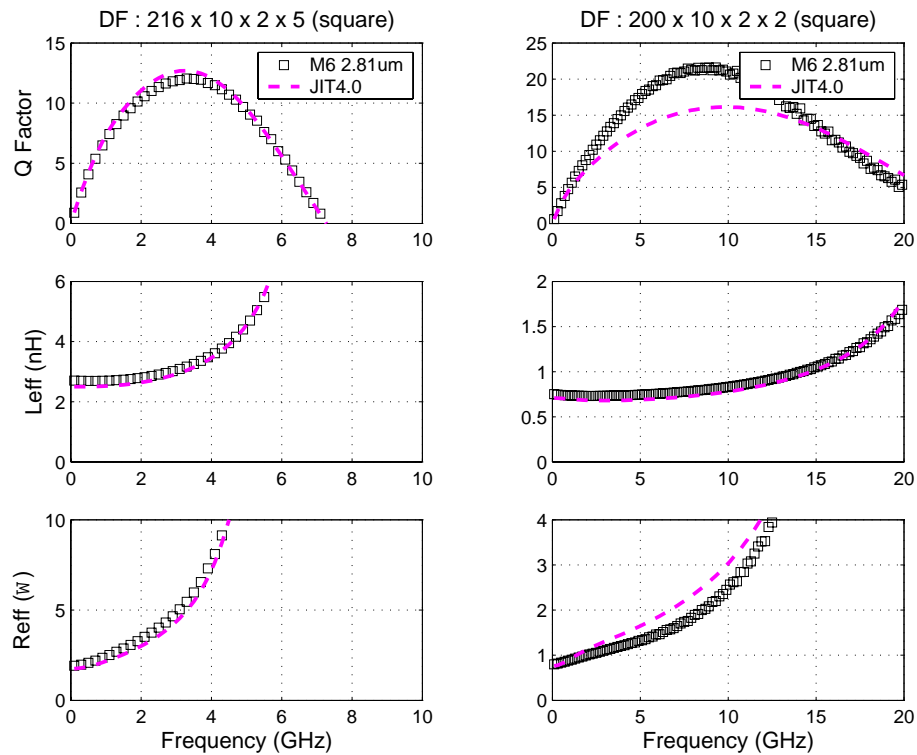


FIGURE 5.39 Inductor Model Verification

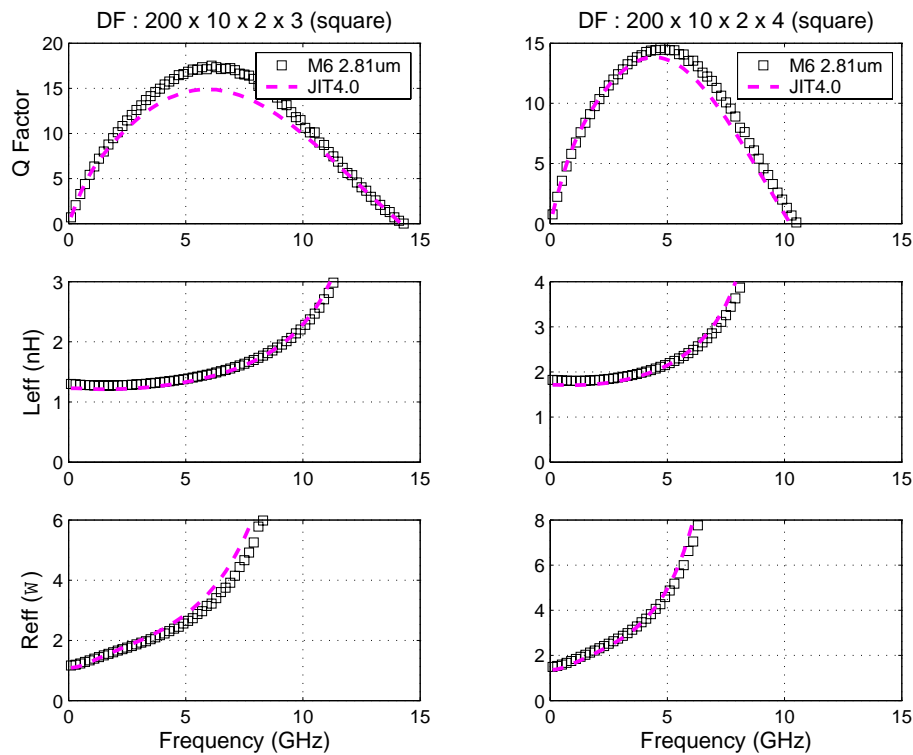


FIGURE 5.40 Inductor Model Verification

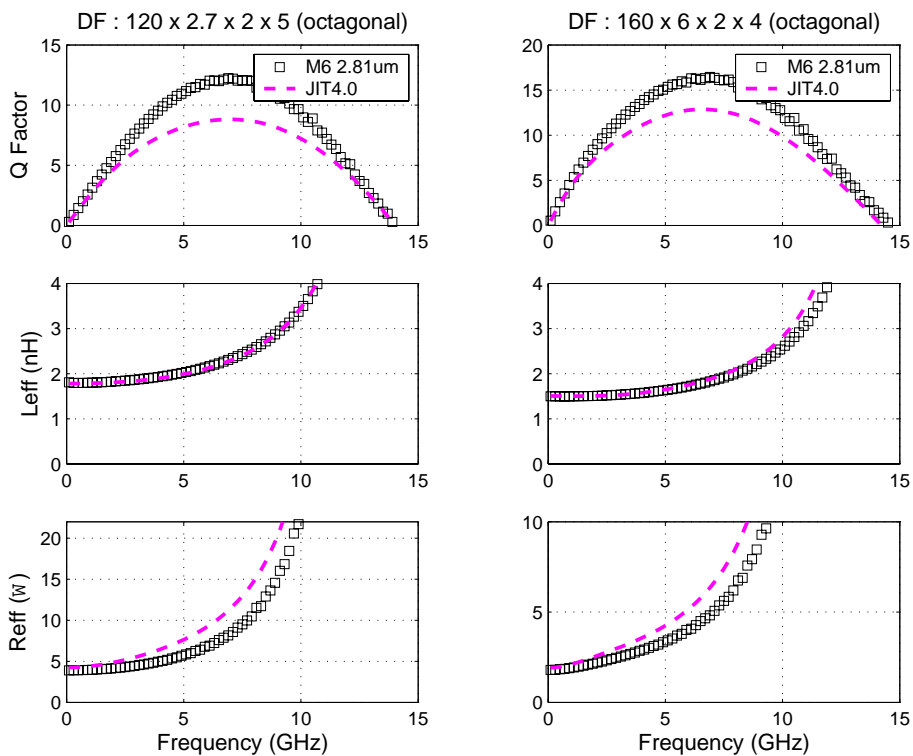


FIGURE 5.41 Inductor Model Verification

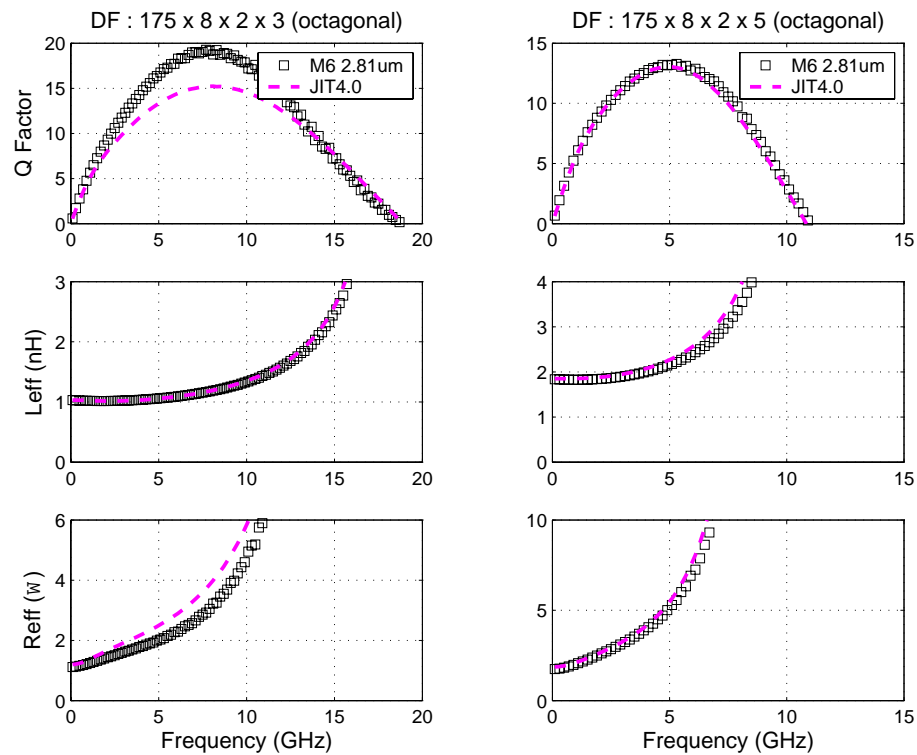


FIGURE 5.42 Inductor Model Verification

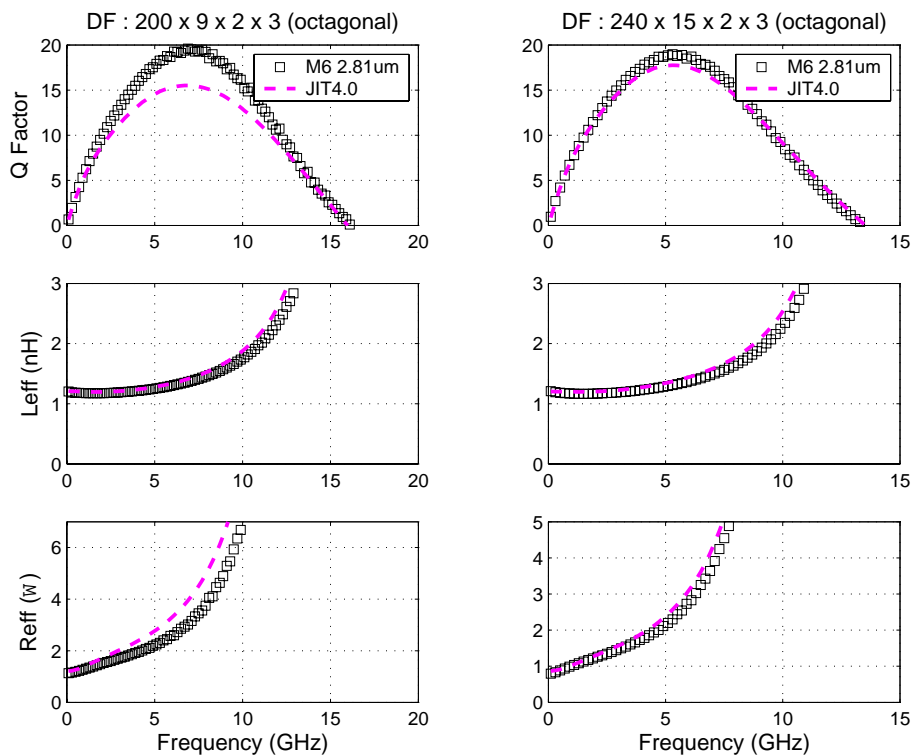


FIGURE 5.43 Inductor Model Verification

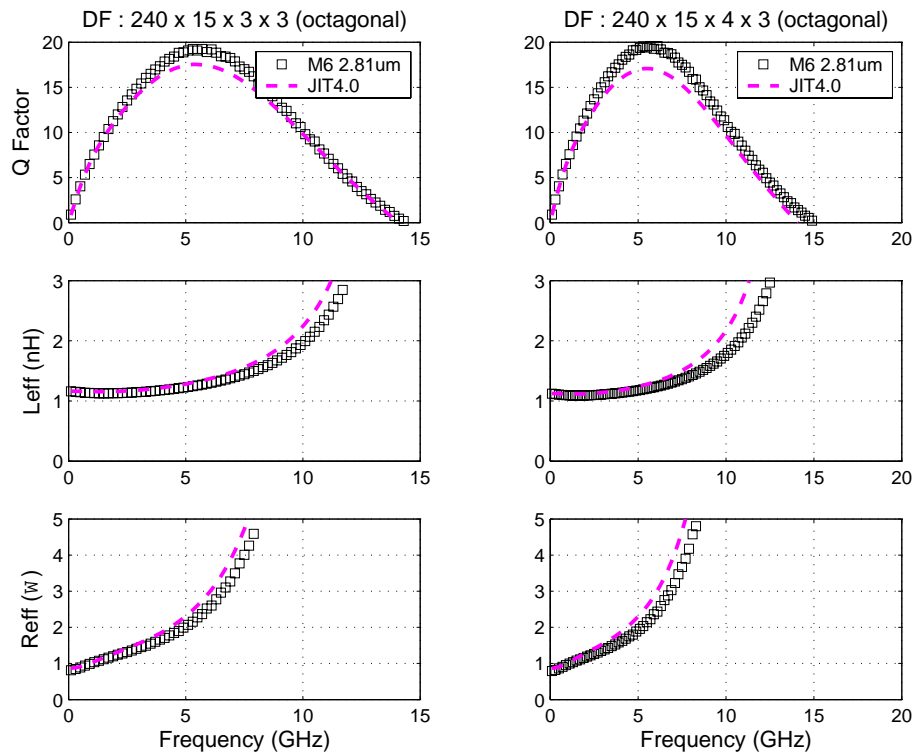


FIGURE 5.44 Inductor Model Verification

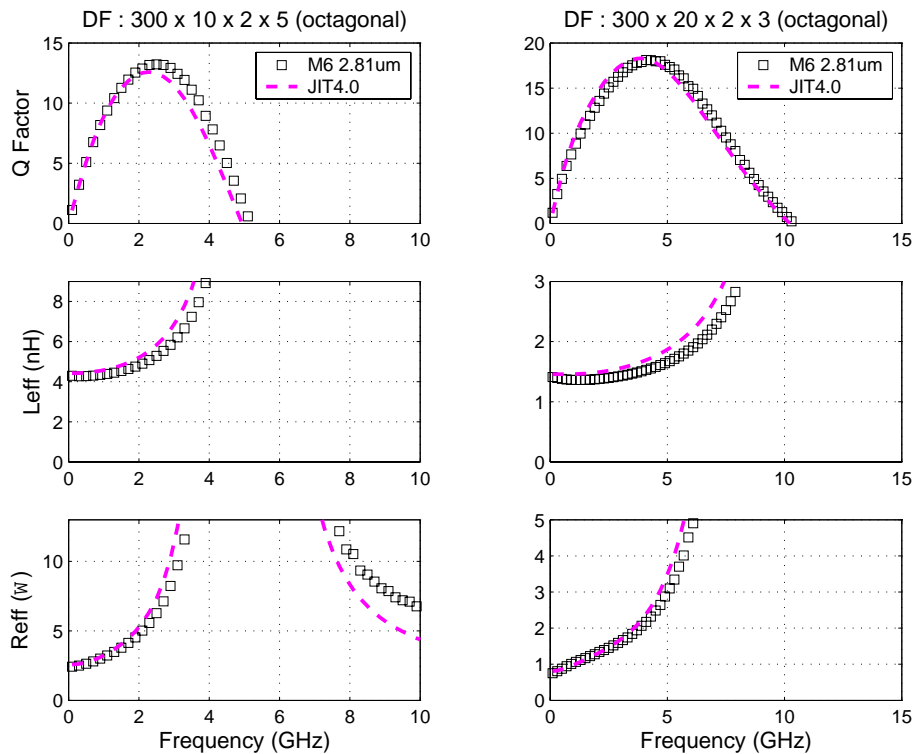


FIGURE 5.45 Inductor Model Verification

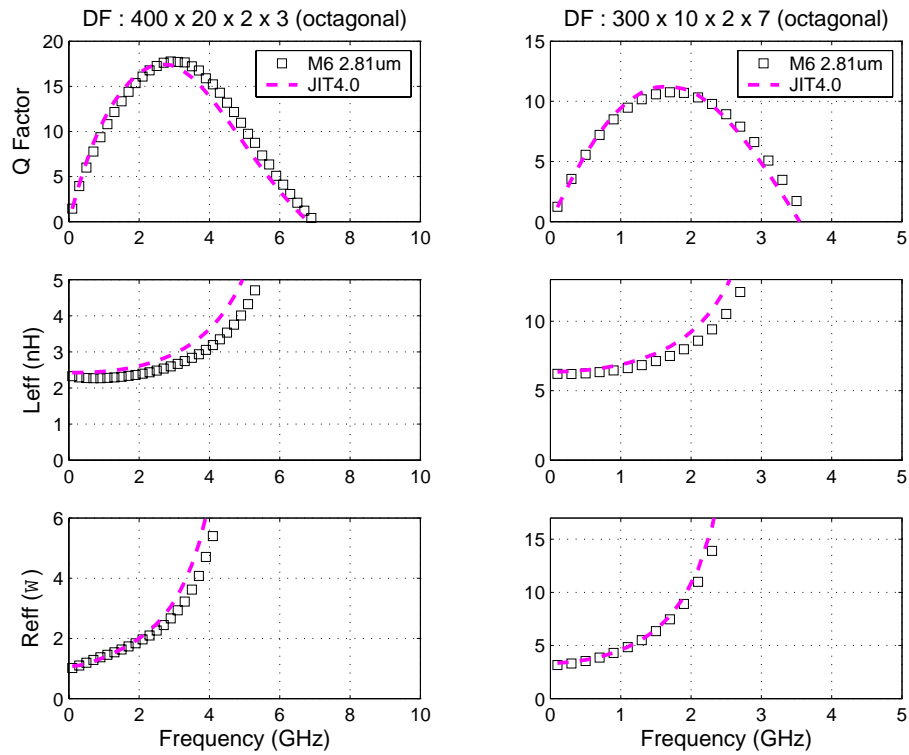


FIGURE 5.46 Inductor Model Verification

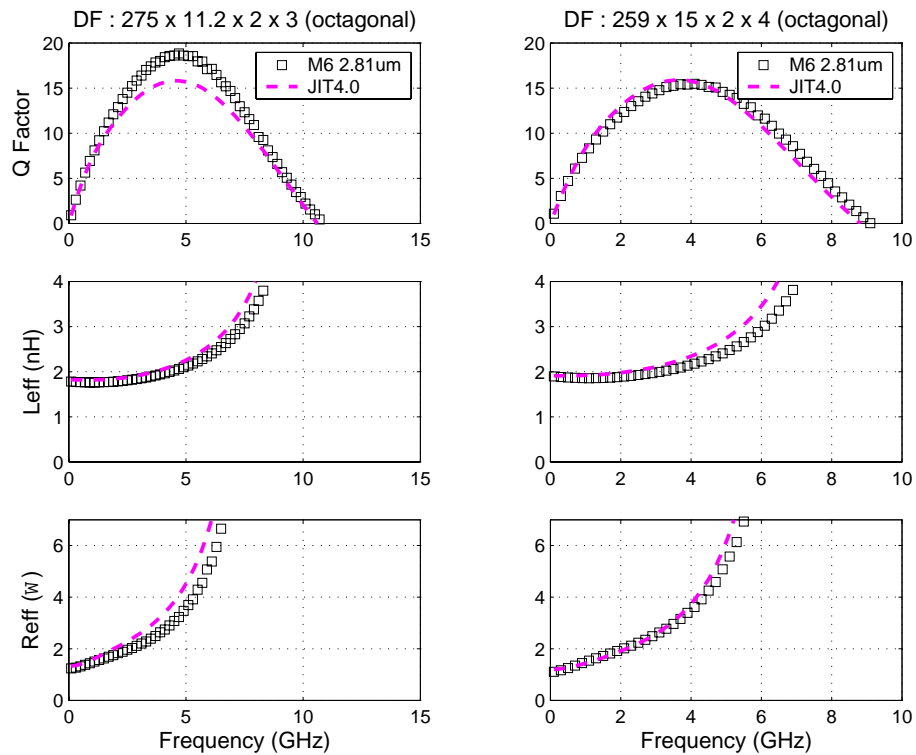


FIGURE 5.47 Inductor Model Verification

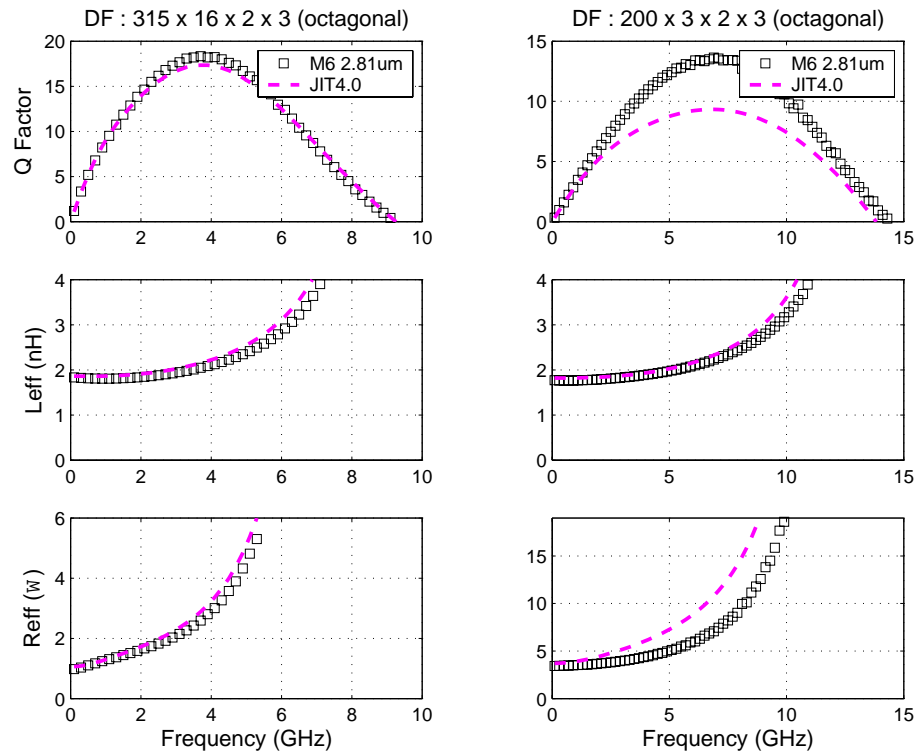


FIGURE 5.48 Inductor Model Verification

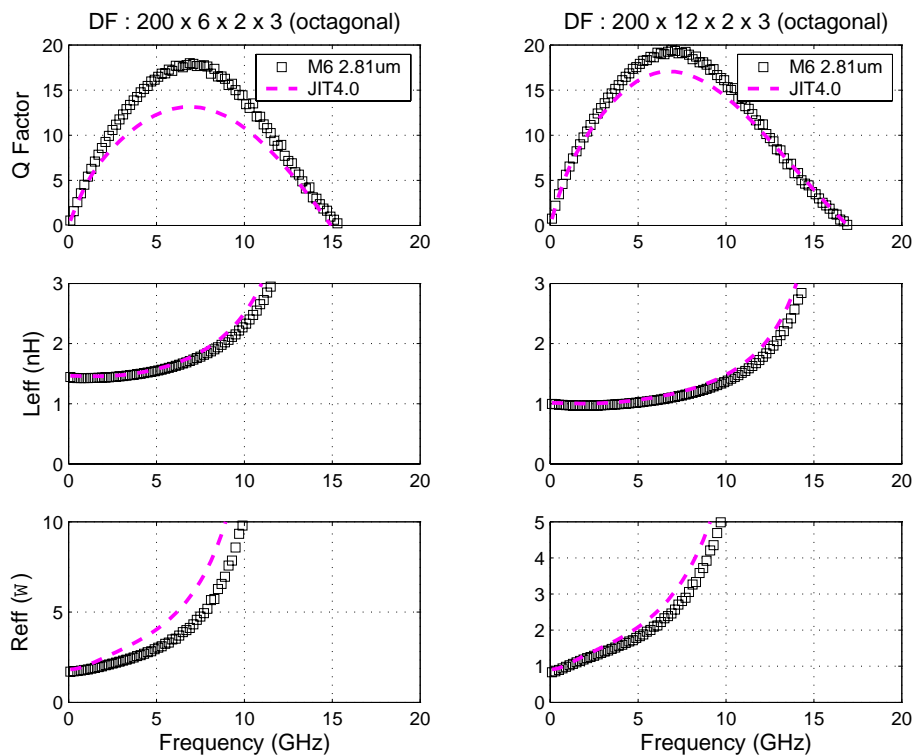


FIGURE 5.49 Inductor Model Verification

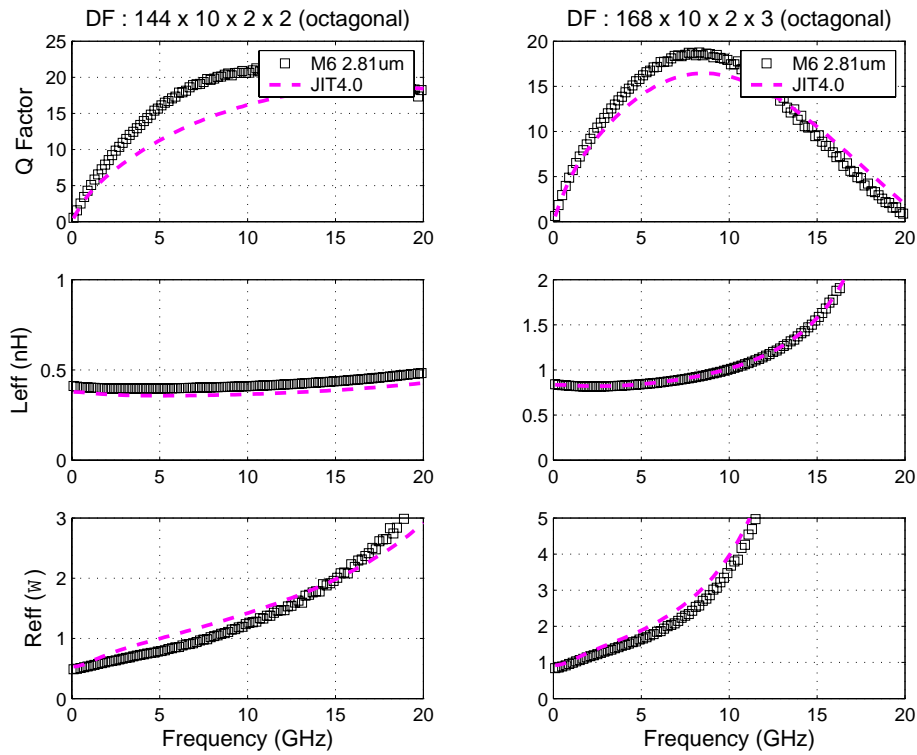


FIGURE 5.50 Inductor Model Verification

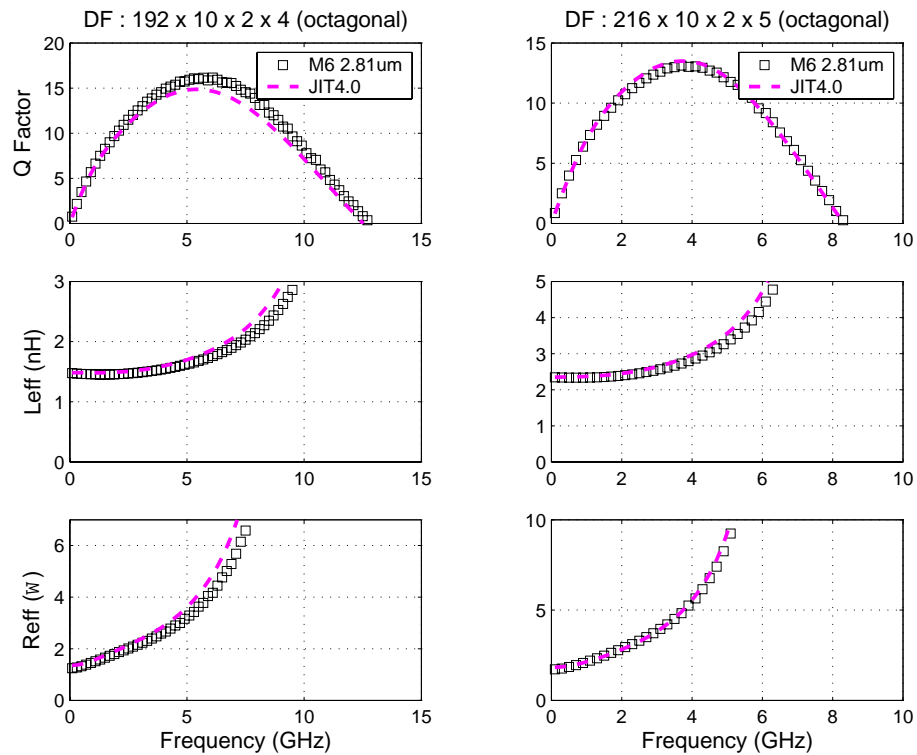


FIGURE 5.51 Inductor Model Verification

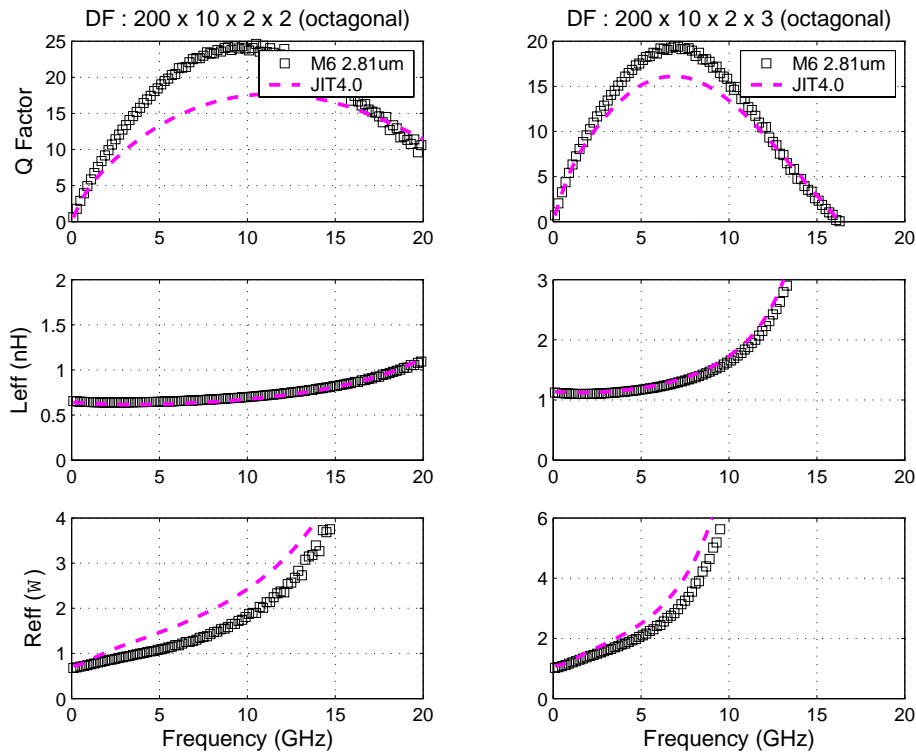
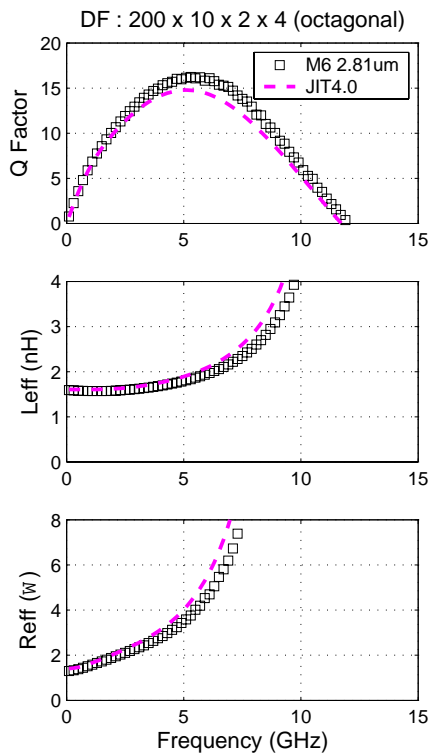


FIGURE 5.52 Inductor Model Verification



5.4 Inductor Statistical and Corner Models

5.4.1 Corner Models

The corner performance is simulated using the corner model card in the design kit. The equivalent circuit component values are provided by the JIT through the CDF with their nominal value. These nominal values are then multiplied by a factor within the model card to obtain the corner case which was optimized to maximize (fast corner) or minimize (slow corner) the peak Q value of the inductor. The multiplier factors are based on the $\pm 3\sigma$ electrical spec limits of the parameters that affect the value of the individual circuit components. The corner case can be simulated by changing the inductor corner from “NOM” to either “SLOW” or “FAST” under the “Set Active Library” menu in the Spectre “Analog Environment”. The multiplier factors are tabulated in Table 5.4.

The component Cx is not represented by an individual element in the sub circuit diagram but is rather a part of the interwinding capacitance Cp. It is representing the capacitance between spiral trace and cross-overs. In its corners, the cross-over and turn-to-turn capacitances move opposite while they are both part of the feed forward capacitance Cp shown in Figure 5.6 and Figure 5.7. The corner value of component Cp is calculated in the sub circuit model card from these 2 parts resulting in an improved corner model.

TABLE 5.4 Corner Component Multipliers

Component	Multiplier	Fast	Nominal	Slow
L_s^2	lsig	0.980	1.00	1.020
R_s^1 (2.81um metal)	rsmsig_3u	0.790	1.00	1.210
C_{ox}^2	coxsig	0.930	1.00	1.070
C_p^2 (2.81 um metal)	cpsig_3u	1.200	1.00	0.800
C_x^2	cxsig	0.740	1.00	1.260
R_{sub}^2	rsbsig	0.710	1.00	1.290
C_{sub}^2	csbsig	0.990	1.00	1.010

PCM notes:

1. The Rs multiplier is consistent with the common PCM and ESPEC limits.
2. There is no PCM monitoring.

5.4.2 X-Sigma Corner Models

X-Sigma corner models allow for process variation settings different than the conventional worst case ± 3 sigma corners. The simulation results with x-sigma set to ± 3 sigma align with the “FAST” and “SLOW” cases of the corner models in section Section 5.4.1, while 0 sigma corresponds to the “NOM” case. The X-Sigma models share model libraries and statistical mappings with the statistical models, with the main difference that the sigma value is user chosen rather than simulator dictated. For more information see also the design manual chapter on X-Sigma.

5.4.3 Statistical Model

The statistical models allow simulation of inductors as affected by the variation of process parameters. These variations are on a global scale affecting the variation of inductors over a larger set of wafers or wafer lots rather than within a given wafer. Generally it is observed that the performance variation between a particular inductor over a wafer is below the resolution of the RF measurements. Therefore, the mismatch of 2 closely located inductor structures is negligible; however mismatch is enabled within the statistical model card and set to an empirical number of 0.1σ . In comparison to the corner model card, the statistical model is not optimized under the constraint of maximizing or minimizing a particular figure of merit such as Q peak. Consequently, the statistical model is more meaningful in exploring the inductor performance space as dictated by the espec.

Since inductors are fairly large devices and their measurement involves a RF network analyzer, inductors don't lend itself to inline process control. Thus these structures are not monitored like process variables that are defined in the espec. Consequently, there is no data available on an inductor population to enable statistical modeling. Instead, the statistical models are based indirectly on the ESPEC via the corner multipliers of the component values described in the previous section. This method corresponds to the forward propagation of variance. The $\pm 3 \sigma$ variations in the component multipliers propagate through the Spectre model to simulate the device electrical behavior [2].

The statistical model cards were verified for the convergence of the average Qpeak to the nominal Qpeak obtained with the corner model card. Convergence to within 0.1σ is typically achieved with a sample size of less than 100 Monte Carlo simulations.

5.5 Model Update History

Table 5.5 lists the model updates with each revision after JIT1.4. Unlisted model revisions indicate that no changes have occurred in that revision. Toolbox JIT4.0 represents a major change over JIT1.4 with added new functionality, simplified corner sub circuits and more accurate models.

TABLE 5.5 Model Updates in JIT4.0

JIT4.0 Update Detail	Devices	Reason	Impact on User
Active ground shield	Single-Ended Inductor	Improve Q.	Inductors with higher Q.
Modeling of packaging compound	All	Improved accuracy.	Model takes into account the capacitance increase through the packaging material.
New substrate resistance model	All	Improved accuracy, models are calibrated to Jazz silicon.	Better models for roll-off section of Q curve.
Cox and Cp account for distributed effect	All	Improved accuracy.	Better models for roll-off section of Q curve and self-resonant frequency.
Additional interwinding capacitance from port to center-tab	Differential Inductor	Improved accuracy.	More accurate prediction of self-resonant frequency.
Interchange of ports 1 and 2	Single-Ended Inductor	Align models with layout PCELL.	Q performance of port1 and port2 shifts. Port2 identifies the outer (non-underpass) port and has the higher Q due to lower Cox.
Proximity effect warning	Differential Inductor	Prevent usage of devices that are not modeled well.	The warning alerts users of dense inductor designs, whose Q is over predicted by the model.

TABLE 5.5 Model Updates in JIT4.0

JIT4.0 Update Detail	Devices	Reason	Impact on User
New subcircuit model cards and optimized corner multipliers	All	Simplify kit maintenance and improve corner accuracy.	Corner results changed. The inductance corner flipped.
New octagonal inductors	All	Improve Q	Inductors with higher Q

5.6 References

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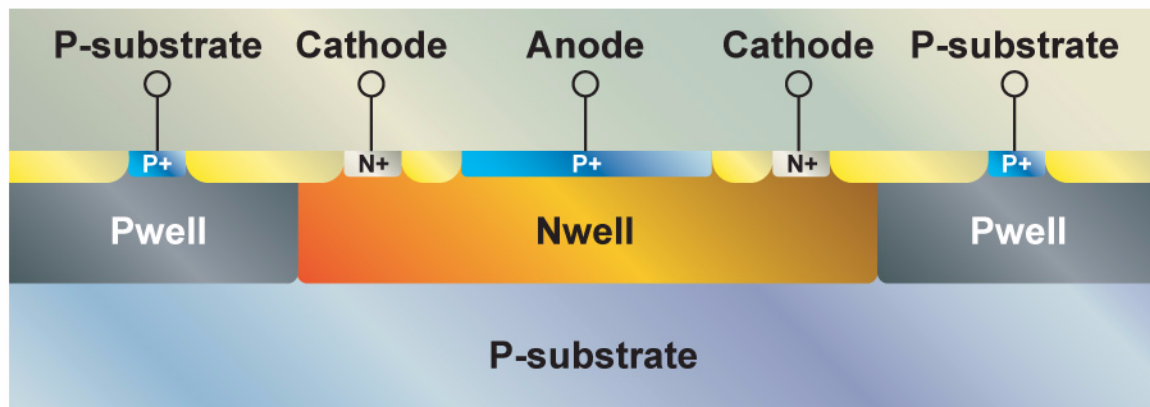
6.0 Varactor Model

6.1 P+ /Nwell Junction Varactor

6.1.1 Device Description

Figure 6.1 displays the cross section of the P+/Nwell junction varactor (device name: **var_ni**). The varactor (voltage controlled capacitance) is formed by the PN junction capacitance between anode (P+) and cathode (Nwell). There is no additional mask required for this varactor. This device is supported in the super-set variants as well as CA18HR and CA18PW54.

FIGURE 6.1 Cross section of the P+/Nwell junction varactor



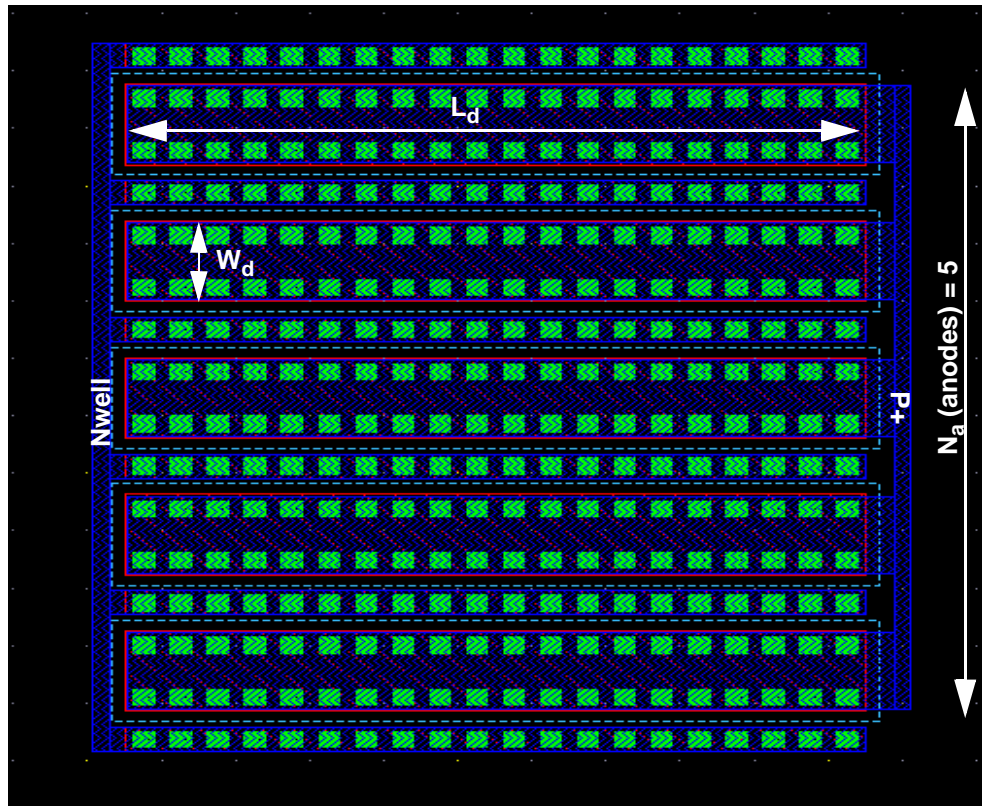
6.1.1.1 Layout Options

The junction varactor pcell offers several design parameters to allow optimization of device performance. Table 6.1 provides detailed information on the pcell variables. The anode width (W_d) and length (L_d) control the capacitance (C) tuning range and quality factor (Q). Increased W_d and L_d provide higher tuning range as the contribution of fixed capacitance is reduced. However, the Q is reduced due to increased Nwell (W_d) and salicide/metal resistance (L_d). Section 6.1.5 provides further validation of C vs. Q trade-off. The C is further scaled through increasing the anodes (N_a).

TABLE 6.1 P+ / Nwell Junction Varactor parameter ranges

Parameter	Description	Typical	Min	Max
W_d	anode width for each var_ni cell	1.4 ~ 2 μm	0.9 μm	5.5 μm
L_d	anode length for each var_ni cell	20 ~ 30 μm	10 μm	50 μm
N_a	number of var_ni anodes connected in parallel	scaled to give C	1	30

FIGURE 6.2 Junction Varactor Layout



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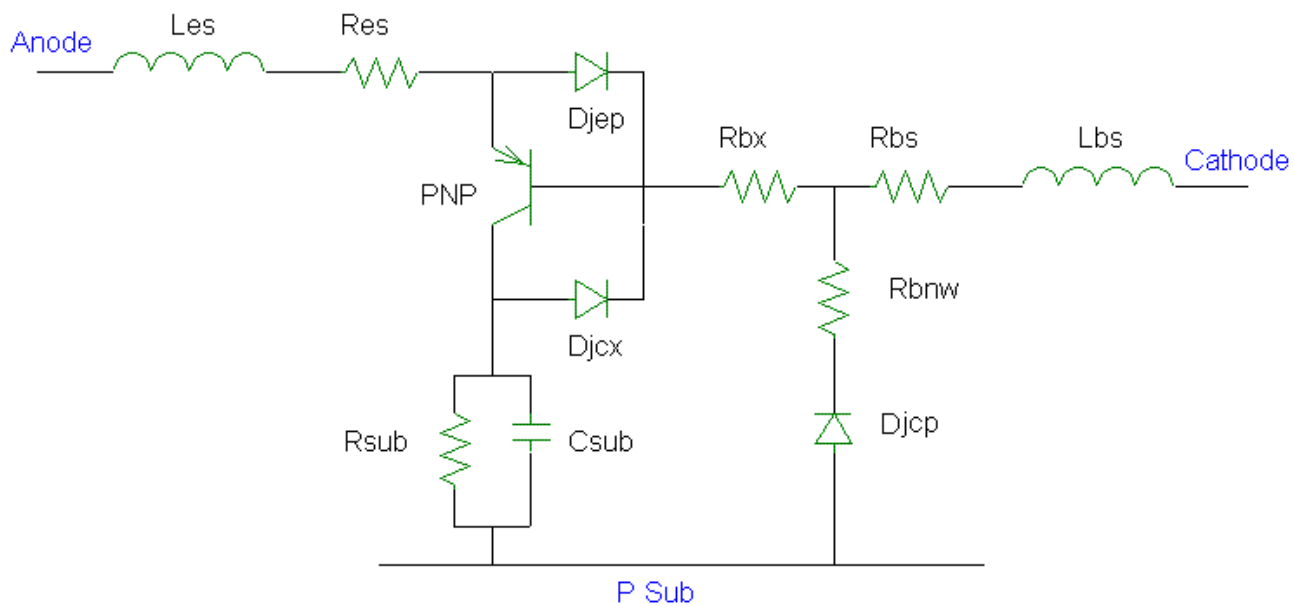
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6.1.2 Model Description

The sub circuit used for the var_ni junction varactor scalable model is shown in Figure 6.3. The varactor capacitance formed by P+/Nwell junction capacitance is split into bottom-side (or area) capacitance (base-emitter of PNP) and perimeter-side capacitance (Djep). The dominant parasitic resistance is associated with the Nwell towards the cathode contact (Rbx). Descriptions of all the sub circuit components are given in Table 6.2.

TABLE 6.2 Junction Varactor Model Sub-Circuit Component Descriptions

Circuit Component Description	
PNP	BE junction forms area component of Varactor junction BC junction forms Nwell to PSUB junction under anode
Djep	Perimeter component of Varactor junction
Rbx	Resistance of Nwell
Djcx	Nwell to PSUB junction not under anode (area component)
Djcp	Nwell to PSUB junction not under anode (perimeter component)
Rbnw	Parasitic resistance between cathode contact towards Djcp
Res, Lres	Parasitic resistance and inductance of anode metal
Rbs, Lbs	Parasitic resistance and inductance of cathode metal
Csub	Substrate capacitance
Rsub	Substrate resistance

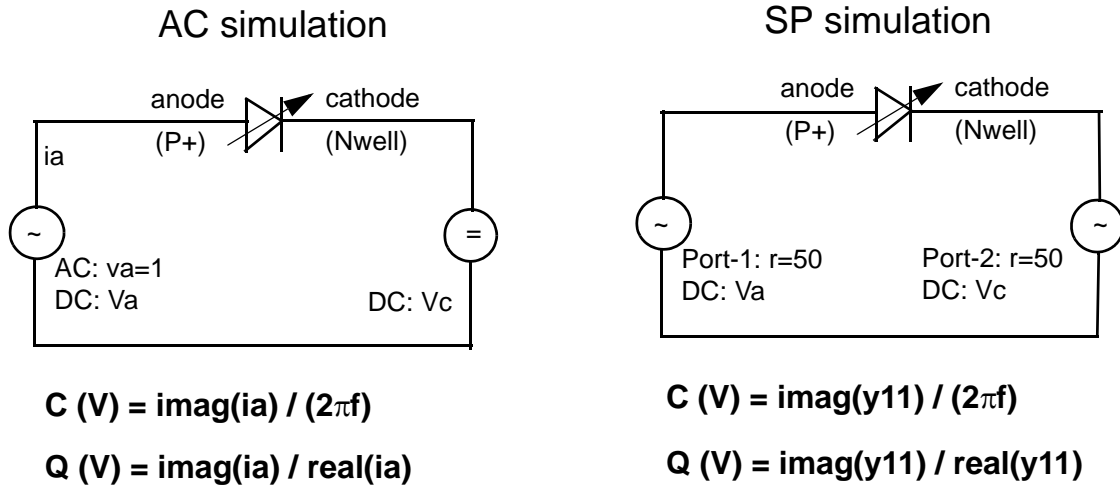
FIGURE 6.3 Subcircuit model for junction varactor


6.1.3 Effective Capacitance and Quality Factor (Q) simulation

There are two methods to simulate and verify junction varactor RF characteristics as shown in Figure 6.4. The key points for correctly simulating junction varactor RF characteristics are:

1. For ac simulation case, ac signal should always be applied at anode (P+) terminal, not at cathode (Nwell) terminal.
2. For s-parameter simulation case, only parameter y11 is used to calculate C and Q.
3. Make sure dc bias across Nwell-Psub diode is always reverse or zero bias.

FIGURE 6.4 Test diagrams for simulating junction varactor



DC bias condition: (1) V_a sweep (0 to 2.5V), $V_c \geq 2.5V$, $V_{sub} = 0V$; or

(2) V_c sweep (0 to 2.5V), $V_a = 0V$, $V_{sub} = 0V$

6.1.4 Parameter Extraction

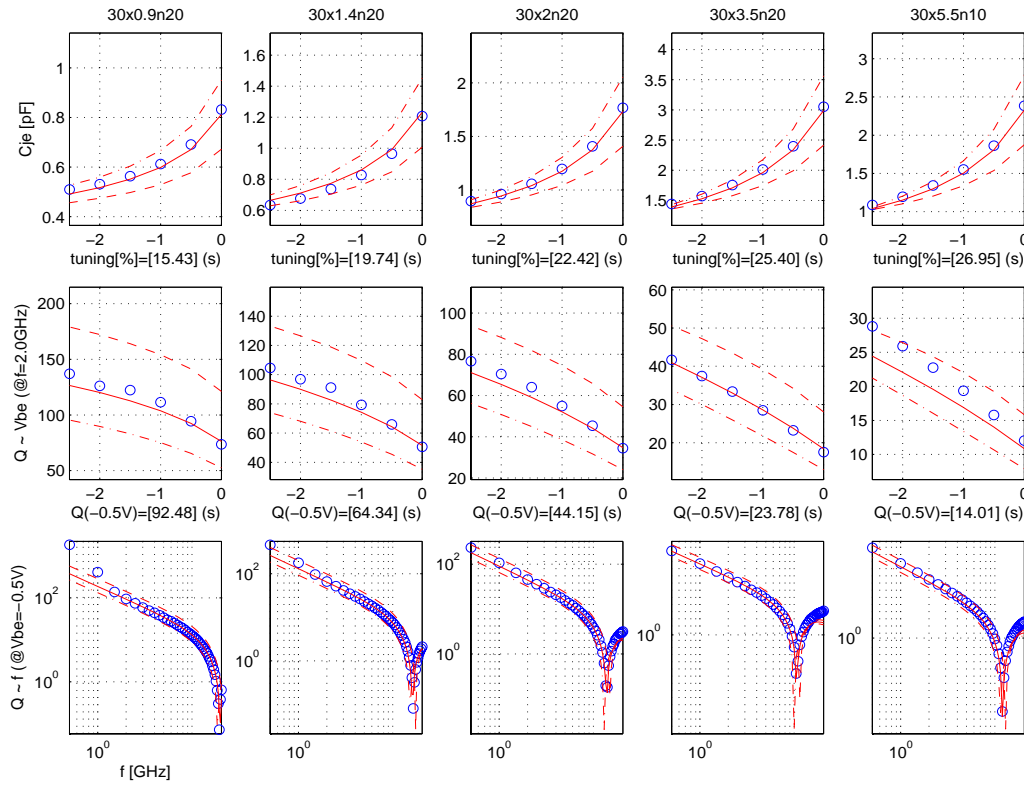
The varactor model parameters are physically extracted based on test devices with varying W_d (0.9 μm to 5.5 μm) at fixed $L_d=30\mu\text{m}$ and $N_a=20$. The bottom and perimeter portions of varactor capacitance can be extracted from the measured CV curves. The parasitic Nwell resistance parameters are extracted from the Quality Factor (Q). Parasitics associated with the metal are based on physical equations. Future characterization will include test devices with varying L_d .

6.1.5 Model Verification

The junction varactor RF data shown in Figure 6.5 uses OPEN de-embedding methodology only (refer to OPEN-THRU de-embedding methodology in MOS varactor section 7.3.5 below). Due to lack of feedline-related test structures at present, a fixed parasitic inductance of 80pH is added intentionally in the model simulation for all test devices for verification purpose only. The OPEN-THRU de-embedding methodology will be implemented in future releases, allowing for improved de-embedding at higher frequencies.

Figure 6.5 displays model and data behavior as the anode width increase at fixed $L_d=30\mu\text{m}$, $N_a=20$. As W_d increases (0.9 μm to 5.5 μm), the capacitance sensitivity (tuning) increases due to higher area/perimeter ratio. The Q is decreased significantly as a result of increased parasitic Nwell resistance. Temperature coefficients are not included in the model at present. Future versions of the model and design manual will contain enhanced temperature verification.

FIGURE 6.5 Verification plot for var_ni data and scalable model

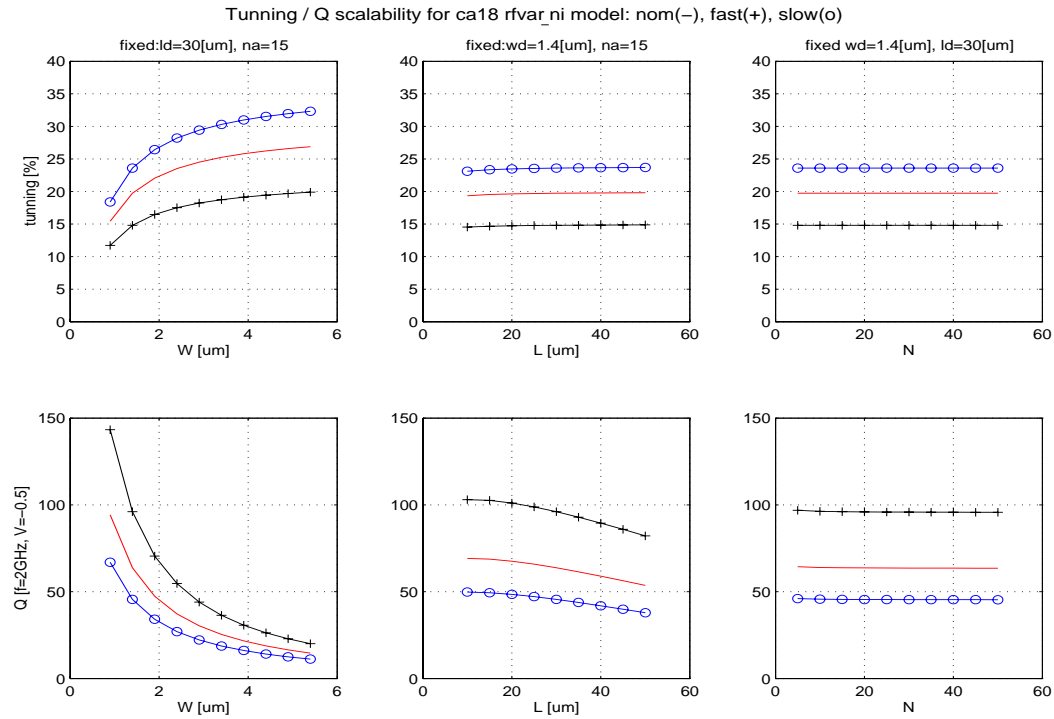


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6.1.6 Model Scalability

Figure 6.6 illustrates the junction varactor model scalability based on the figure displays tuning and quality factor vs. scalable device size (W_d , L_d , and N_a respectively).

FIGURE 6.6 var_ni model scalability plot showing Tuning/Q vs. Wd, Ld or Na respectively



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6.1.7 Junction Varactor Statistical and Corner Models

The junction capacitance variation and parasitic resistance is dominated by the Nwell doping. Thus, the process-related variation in the corner and statistical models are correlated with other devices such as the Nwell resistors. Figure 6.7 displays the corner simulation for the junction varactor. Table 6.3 lists the ESPEC values compared to simulated corner and statistical values for **var_ni** junction varactor.

FIGURE 6.7 Verification plot for var_ni data and scalable corner model at T=25C

TABLE 6.3 Espec, Corner and Statistical model comparison for P+/Nwell *var_ni* junction varactor

Parameters		Slow			Nom			Fast		
device: 1.4x30n78 Wd [μm] x Ld [μm] x Na	unit	Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
Capacitance (-0.5V)	pF	4.41	4.41	4.41	3.85	3.86	3.86	3.29	3.31	3.30
Capacitance sensitivity ^{1,2}	%/V	24.2	23.6	24.0	19.6	19.7	19.6	15.0	14.8	15.2
Q(1.9G,-0.5V) ¹					68	68.8	57.0			
I (leakage current at -3.6V) ¹	pA							165	165	162

PCM/ESPEC notes:

1. There is no PCM monitoring.
2. Capacitance sensitivity definition: $[C(-0.5V) - C(-2.5V)] / [C(-0.5V) + C(-2.5V)] * 100$

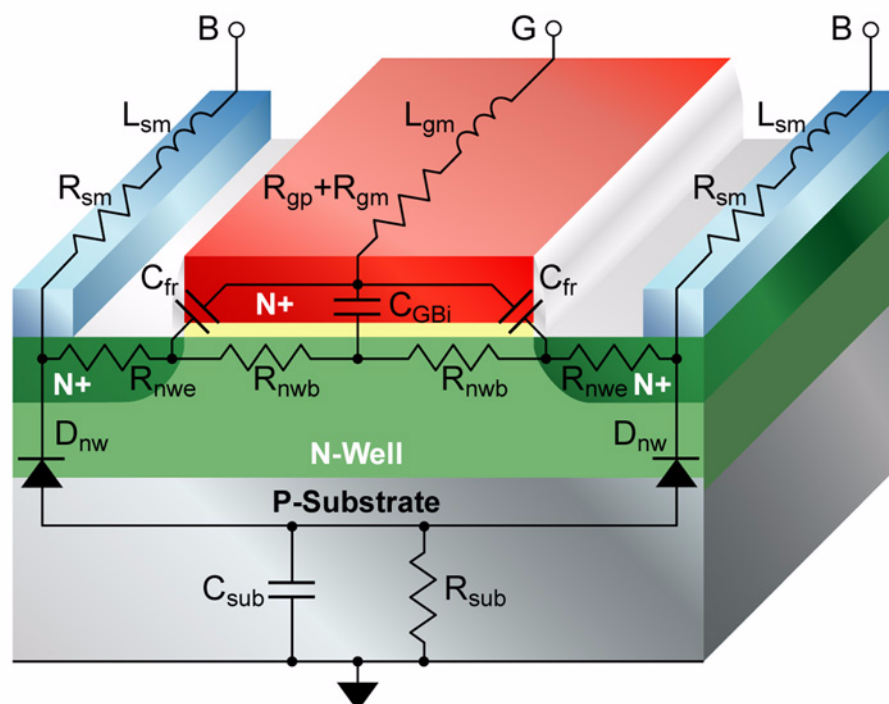
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6.2 MOS Varactor

6.2.1 Device Description

The MOS varactor (device name: **var_mos**) is formed by thin gate-oxide over Nwell, with N+ implant at both source / drain regions to form ohmic contacts with varactor Nwell region. The cross section of this device is shown in Figure 6.8. The device is the same in cross section to the 1.8V poly capacitors available in all CA18 variants. However, the device is supported as a varactor in the super-set variants as well as CA18HR and CA18PW54.

FIGURE 6.8 MOS Varactor Cross Section: n+ poly to Nwell capacitor as MOS Varactor



6.2.2 Layout Options

The MOS varactor pcell offers several design parameters to allow optimization of device performance. Table 6.4 provides detailed information on the pcell variables. The gate width (W_g) and length (L_g) control the capacitance (C) tuning range and quality factor (Q). Increased W_g and L_g provide higher tuning range as the contribution of fixed capacitance is reduced. However, the Q is reduced due to increased Nwell and poly gate resistance. Section 6.1.5 provides further validation of C vs. Q trade-off.

The C is scaled through arraying the device as *slices* (N_s) and *fingers* (N_f). There is no break in the poly or metal 1 between successive slices. There is a break in the active to allow for metal 1 contact to the poly gate in order to minimize the gate resistance. Two different *metal style* options (metal 1 and metal 2) are offered for

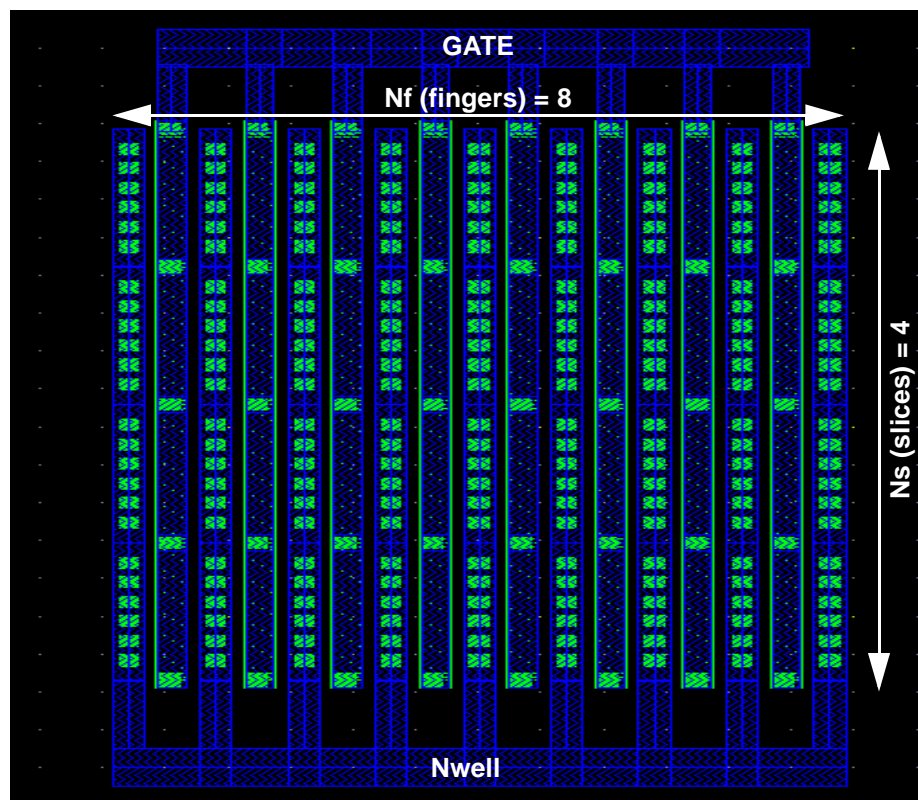
the MOS varactor in the CA18 design kit. The metal one option is shown in Figure 6.9. Metal 1 fingers are drawn parallel to the gate poly and Nwell contacts. The metal 2 option exists as *unconnected* and *connected*. The metal 2 *connected* option is shown in Figure 6.10. In the *unconnected* option, the vertical metal bars are removed. In the metal 2 option, the metal 2 fingers are drawn orthogonal to the metal 1 fingers with vias dropped to connect to the gate and Nwell metal 1 fingers. The metal 2 option provides for lower metal resistance for larger N_s layouts ($N_s > 5$) at the expense of increased parasitic metal 1 to metal 2 capacitance which degrades the tuning range.

TABLE 6.4 MOS Varactor Parameter Description

Variable	Description	Typical	Min	Max
L_g	gate length for each var_mos cell	0.5 μm	0.5 μm	2 μm
W_g	gate width for each var_mos cell	3.0 μm	2 μm	4.0 μm
N_s (slices)	number of slices which controls the number of var_mos cells in series	4	1	10
N_f (fingers)	number of fingers connected in parallel for each slices	scaled to give C	1	40
Metal Style	metal connection type	metal 1, metal 2, metal 2 connected		

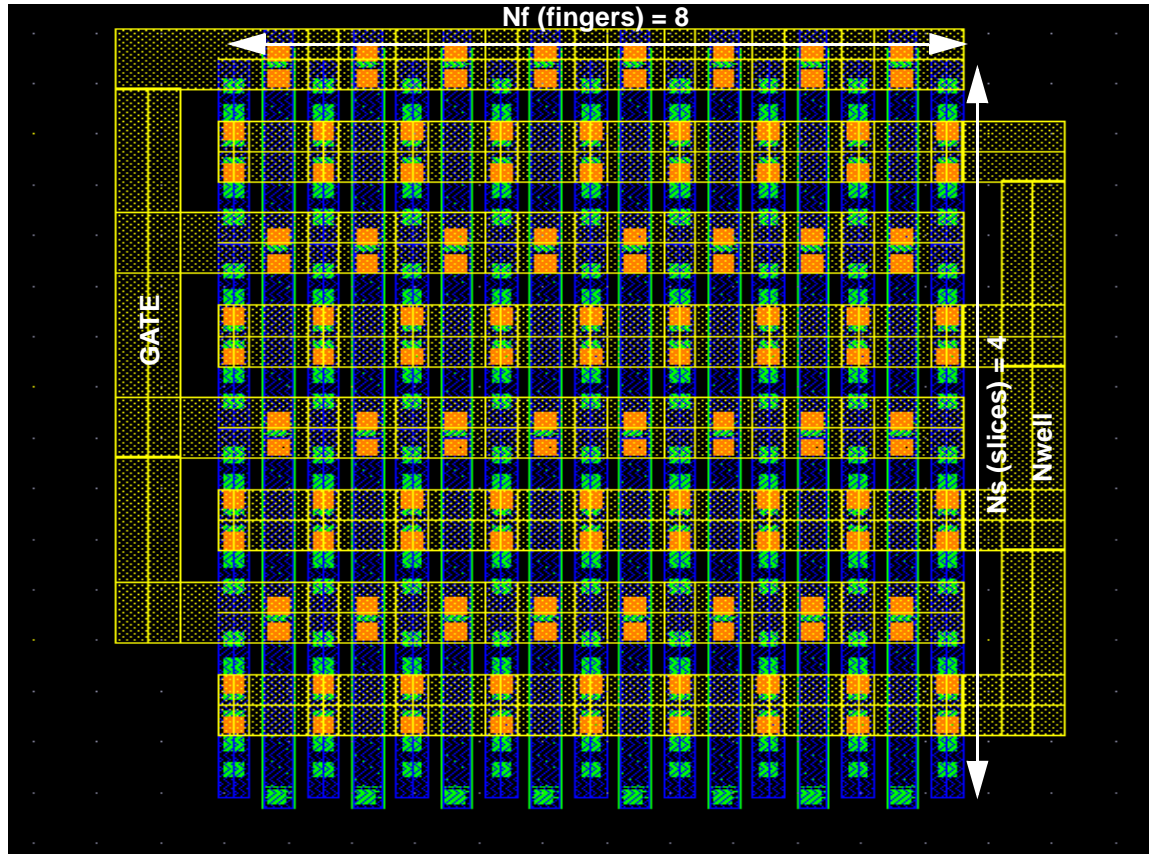
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FIGURE 6.9 MOS varactor - Metal 1 Layout Option



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FIGURE 6.10 MOS varactor - Metal 2 Connected Layout Option



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6.2.3 Model Description

The sub circuit used for MOS varactor scalable model is shown embedded in Figure 6.8. Table 6.5 provides the descriptions of all sub circuit components. The intrinsic capacitance C_{GBi} is the oxide capacitance C_{ox} in series with a voltage dependent depletion capacitance C_d . The total capacitance swings from a maximum of C_{ox} in accumulation for positive V_{gb} to the series combination of C_{ox} and C_d in depletion when V_{gb} is negative. Overlap and fringing capacitances (C_{fr}) are considered to be constant. The parasitic resistance is dominated by the Nwell resistance ($R_{nwb} + R_{nwe}$). The model takes into account the metal style options in calculating parasitic metal capacitance, inductance, and resistance.

TABLE 6.5 MOS Varactor Model Sub-Circuit Component Descriptions

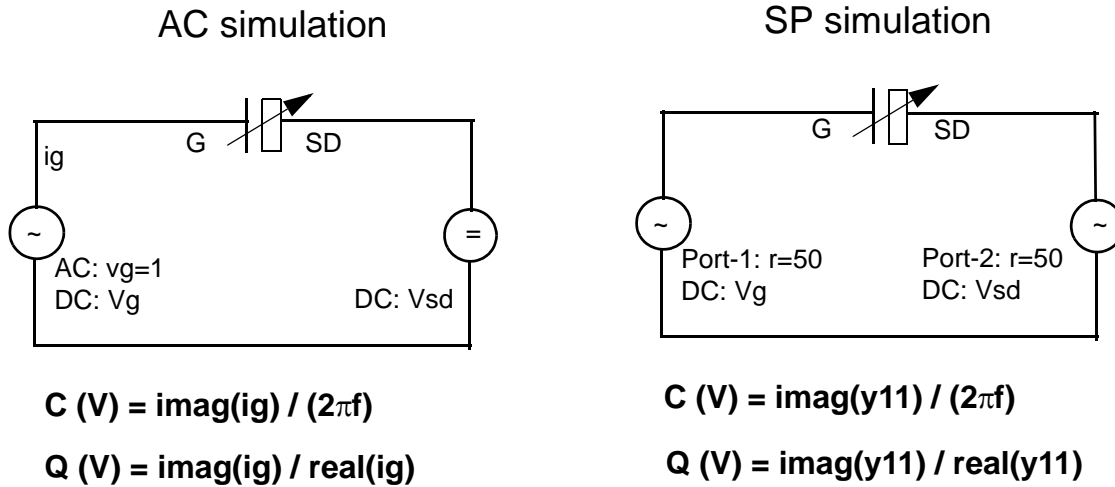
Circuit Component Description	
C_{GBi}	Intrinsic MOS capacitor
C_{fr}	Overlap and fringing capacitance for poly and metal 1
C_{m2}	Metal 1 to metal 2 capacitance (Metal 2 layout option only)
R_{nwb}	Nwell resistance under oxide
R_{nwe}	Nwell end and contact resistance
R_{gp}	Gate poly resistance (see RF MOSFET chapter, Section 3.2 on page 135 for details)
R_{gm}, L_{gm}	Parasitic resistance and inductance of gate metal
R_{sm}, L_{sm}	Parasitic resistance and inductance of Nwell metal
D_{nw}	Nwell-PSUB junction
C_{sub}	Substrate capacitance
R_{sub}	Substrate resistance

6.2.4 Effective Capacitance and Quality Factor (Q) simulation

There are two methods to simulate MOS varactor RF characteristics as shown in Figure 6.11. The key points for correctly simulating MOS varactor RF characteristics for model verification are:

1. For ac simulation case, ac signal should always be applied at gate (G) terminal, not at source/drain (SD) terminal.
2. For s-parameter simulation case, only parameter y11 is used to calculate C and Q.
3. Make sure dc bias across Nwell-Psub diode is always be set to reversed or zero bias, never goes to forward bias.

FIGURE 6.11 Test diagrams for simulating MOS varactor



DC bias condition: (1) V_g sweep (-2V to 2V), $V_{sd} = 0$, $V_{sub} = 0$;

or (2) V_{sd} sweep (-2V to 2V), $V_g = 0$, $V_{sub} \leq -2V$

6.2.5 Parameter Extraction

The MOS varactor model parameters were physically extracted based on the following sets of test devices:

1. Varying gate length L_g ($0.5\mu\text{m}$ to $2\mu\text{m}$) at fixed $W_g = 3\mu\text{m}$, $N_s=2$, $N_f=10$;

$L_g > 2\mu\text{m}$ gives very low Q values with minimal returns in tuning range. $L_g < 0.5\mu\text{m}$ significantly reduces the tuning range at minimal returns in Q improvement.

2. Varying gate width W_g ($2\mu\text{m}$ to $8\mu\text{m}$) at fixed $L_g = 0.5\mu\text{m}$, $N_s=2$, $N_f=10$;

At $W_g = 8\mu\text{m}$ the Q values drops significantly compare to $W_g = 4\mu\text{m}$, the design kit limit. $W_g < 2\mu\text{m}$ will begin to degrade the tuning range at minimal returns in Q improvement since the Nwell resistance dominates.

3. Varying N_s and N_f at fixed $L_g = 0.5\mu\text{m}$ and $W_g = 3\mu\text{m}$.

6.2.6 Model Verification

Prior to extracting model parameters, all measurement data is rigorously de-embedded. A detailed OPEN-THRU de-embedding methodology is used in order to properly de-embed all pad and feedline related parasitic resistance, capacitance and inductance. The THRU de-embedding uses an ABCD matrix to extract transmission line related model parameters such as characteristic impedance (z_0) and propagation constant (γ). Figure 6.12 shows the example of Q vs. frequency data for device: $W_g=3\mu\text{m}$, $L_g=1\mu\text{m}$, $N_s=2$, and $N_f=10$. In this plot, dots represent the raw measured data, circles represents the OPEN de-embedding only data, the solid line represents the data after further THRU de-embedding. The THRU de-embedding technique provides reliable data up to 20GHz.

Figure 6.13 through Figure 6.15 illustrate the MOS varactor model performance. Figure 6.13 displays model vs. data behavior as L_g increases while maintaining $W_g=3\mu\text{m}$, $N_s=2$, and $N_f=10$. As L_g increases ($0.5\mu\text{m}$ to $2\mu\text{m}$), capacitance sensitivity (tuning) increases (~ 68 to ~ 82) due to more oxide capacitance area relative to fixed fringing capacitor. The minimum Q decreases (~ 100 to ~ 30 at 2GHz) as a result of significantly increased Nwell resistance with increasing L_g .

Figure 6.14 displays model vs. data behavior for varying W_g while maintaining $L_g=0.5\mu\text{m}$, $N_s=2$, and $N_f=10$. As W_g increases ($2\mu\text{m}$ to $4\mu\text{m}$), capacitance sensitivity (tuning) increases and Q_{min} decreases slightly. Further increasing W_g to $8\mu\text{m}$, Q starts to drop significantly mainly due to higher gate poly resistance.

Figure 6.15 displays model vs. data behavior for the constant $N_s \times N_f$ at fixed $W_g=3\mu\text{m}$, and $L_g=0.5\mu\text{m}$ for *metal 1 style* layout. As expected, large N_f and small N_s yields highest Q. Large N_s results in Q degradation from long metal fingers resulting in high metal resistance. Data for *metal 2 style* layouts is currently not available.

FIGURE 6.12 Q vs. f for raw data (.), after de-embedding with OPEN (o) and THRU (-)

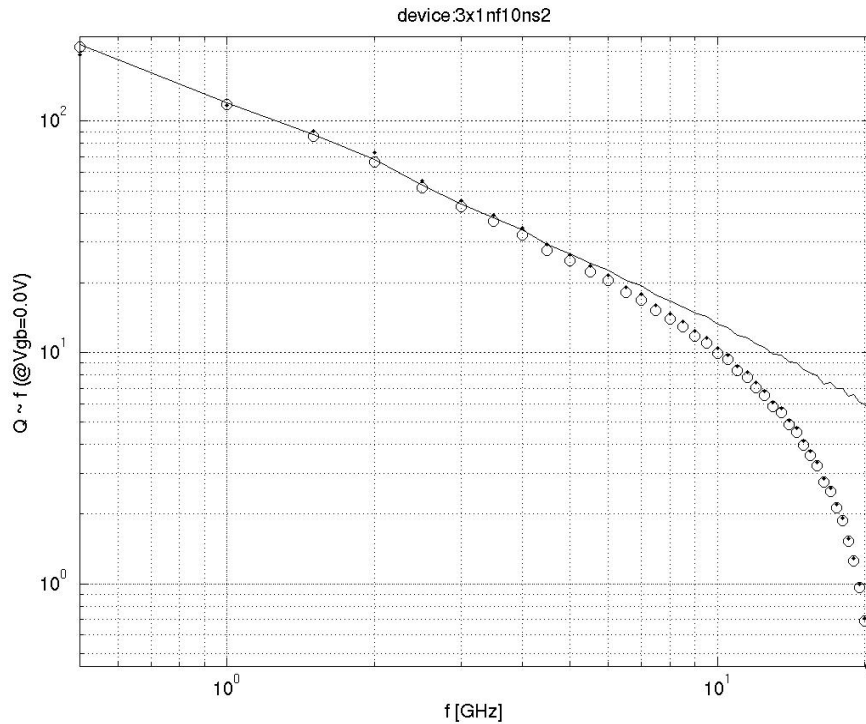
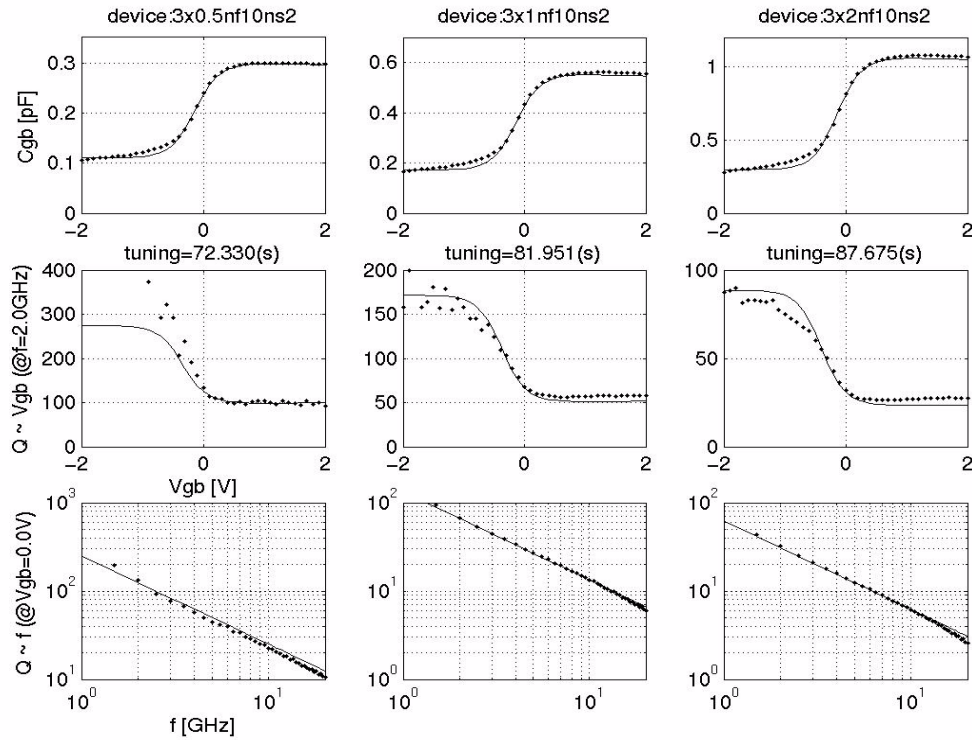


FIGURE 6.13 MOS varactor - Varying L_g



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FIGURE 6.14 MOS varactor - Varying W_g

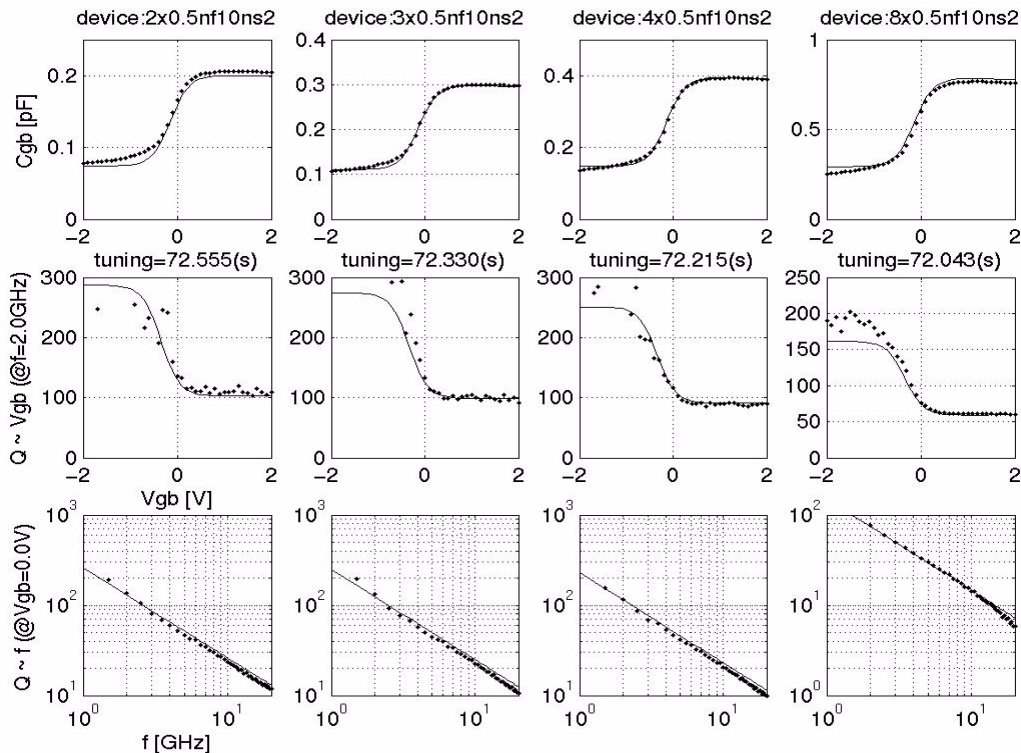
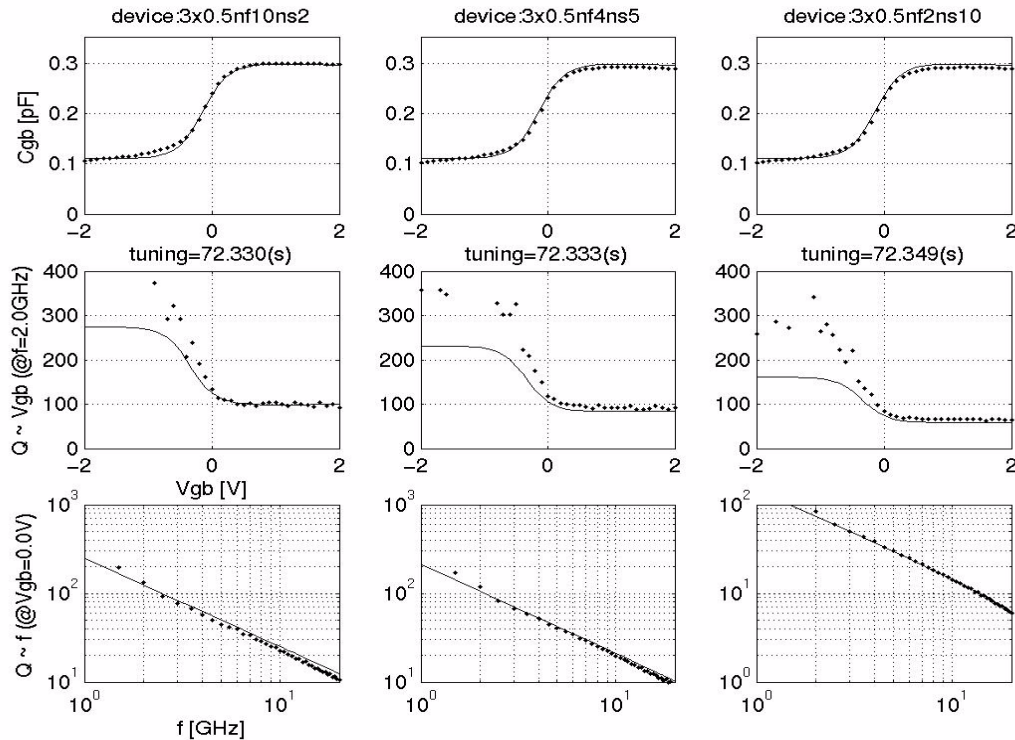


FIGURE 6.15 MOS varactor - Varying $N_s \times N_f$, with constant C_{gb} 

6.2.7 MOS Varactor Statistical and Corner models

For the most part, the MOS varactor is directly correlated with the MOSFET statistical parameters (see Chapter 2 and Appendix A on statistical model correlation). The MOS capacitance is directly correlated with the MOSFETs. The Nwell resistance under the gate is dominated by the surface doping and hence is correlated with the threshold variance of the PFET. For the FAST case, the capacitance increases and the nwell resistance increases from the lower threshold implant. Thus, the fast case yields lowest Q and vice versa for the SLOW case. The poly resistance follows the NWEELL resistance in the MOS varactor corner model to give worst/best case Q. See Appendix A for further explanation of the device interdependence in the corner models. Table 6.6 gives the MOS varactor parameters used in corner and statistical model and the associated process parameters.

TABLE 6.6 Corner and statistical model parameters for mos varactor model

var_mos parameters	Description	associated process parameter
tox (m)	Oxide thickness	1p8PFET_delta_tox
vth0 (v)	long channel threshold	1p8PFET_delta_vth0
k1 ($V^{1/2}$)	body constant	1p8PFET_factor_k1
rsh_nw (ohm/sq)	sheet resistance of Nwell under gate	1p8PFET_factor_nch
rend_nw (ohm-m)	rend resistance of Nwell to contact	rnws_factor_rend
rsh_poly (ohm/sq)	sheet resistance of poly gate	rpoly_factor_rsh

Figure 6.16 displays the corner simulations for the MOS varactor with typical device size of 3x0.5x2x10.

Table 6.7 lists the measured and simulated ESPEC values for MOS varactor. The capacitance value $C(1V)$ in the table shows the highest capacitance value at $V_{gb}=1V$ for a larger device size 3x0.5x15x25 used in the PCM test. The Q values listed in the table show the Q_{min} (at $V_{gb}=1V$) at three different frequencies (1.9G, 5G and 10G) for a typical RF test device size: 3x0.5x2x10.

FIGURE 6.16 MOS varactor - Corner Model

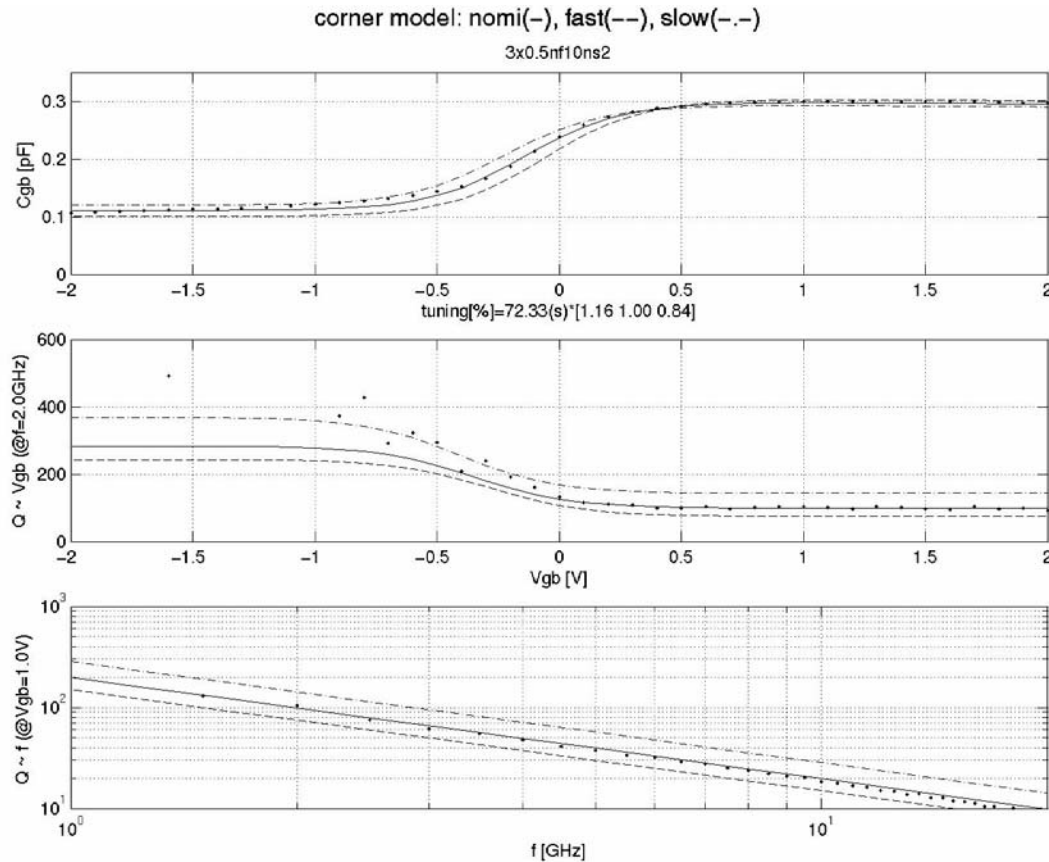


TABLE 6.7 Espec, Corner and Statistical Model Comparison for MOS Varactor Model

Parameter	device WgxLgxNsxNf	unit	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
$C(1V)^1$	3x0.5x5x70	pF	TBD	5.07	5.14	5.00	5.00	5.00	TBD	4.92	4.86
Sensitivity ^{1,2}	3x0.5x5x70	%/V	60.9	60.3	61.9	72.5	72.6	73.1	84.1	82.3	84.2
$Q(1.9G, 1V)^1$	3x0.5x2x10		75	74.9	74.8	100	99.4	99.9			
$Q(5G, 1V)^1$	3x0.5x2x10		30	30	29.9	40	39.8	40.0			
$Q(10G, 1V)^1$	3x0.5x2x10		15	15.0	15.0	20	19.9	20.0			

PCM/ESPEC notes:

1. There is no PCM monitoring.

2. Capacitance sensitivity definition: $[C(0.5V) - C(-0.5V)] / \{[C(0.5V) + C(-0.5V)] / 2\} * 100$

TABLE 6.8 TOX Variation in Corner and Statistical Models

	3- σ Corner		3- σ Stat	
	Espec	Model	Espec	Model
thin tox	+/- 1A	+/- 1A	+/- 1.5A	+/- 1.5A
thick tox	+/- 1.8A	+/- 1.8A	+/- 3A	+/- 3A

6.3 Model update History

6.3.1 v3.4

TABLE 6.9 Varactor model specific updates in model release version 3.4

v3.4 update	Reason	Impact on user
Corner/Statistical model oxide thicknesses	Updated to match new E-spec. with tighter variation	No change in NOMINAL model. Reduced corner/statistical model variation in gate oxide capacitance: corner model: v3.3a +/- 3Å; v3.4 +/- 1Å 1stat. model: v3.3a +/- 3Å; v3.4 +/- 1.5Å
Corner Model Change so that fast gives low Q, slow gives high Q. Q controlled by 1/RC. For FAST MOSFET, means high C (thinner tox) and low surface implant, high resistance, hence high Q varactor.	Provide consistency with MOSFET corners.	FAST and SLOW MOSFET Corners will yield reverse Q results from prior release.
Added salicide-polysilicon contact resistance to the gate resistance	salicide-polysilicon gate resistance is a significant component of gate resistance for narrow width (<3µm) RF FETs with 2-sided gate contacts	No real impact as Wg range for Mos Varactor is 2-4µm. Old model was able to compensate for this effect. New model is more physical and consistent with MOSFET.

6.3.2 v4.1

TABLE 6.10 Varactor model specific updates in model release version 4.1

v3.4 update	Reason	Impact on user
Change temperature coefficient for nwell resistance	Align to nwell resistor model update	Change in Q Vs. temperature dependency

6.3.3 v4.2

TABLE 6.11 Varactor model specific updates in model release version 4.2

v3.4 update	Reason	Impact on user
Updated junction varactor tuning range and junction capacitance	Updated to match new E-spec.	Smaller tuning range. Change in zero bias junction capacitance
Changed corner model correlation between tuning range and junction capacitance	New statistical data that shows reduced tuning range when junction capacitance is reduced	FAST corner: Changed from lower capacitance/higher tuning range to lower capacitance/lower tuning range SLOW corner: Changed from higher capacitance/lower tuning range to higher capacitance/higher tuning range
Updated nwell resistance temp. coefficients in MOS Varactor model	New data	Changes in Q vs. temperature dependency
Changed SLOW corner end resistance in MOS Varactor model	Negative resistance in previous model was causing convergence problems	Improved convergence

6.3.4 References

1. P. Andreani and S. Mattisson, "On the use of MOS varactor in RF VCO's," IEEE JSC, June 2000
2. H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," IEEE PHP, June, 1974

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7.1 Device Description

For all resistors, the resistance can be changed through choice of Finger Width “W”, length “L” and number of fingers “Strips” in the component property window. A CDS calculator updates the resistance value using the nominal electrical specification. For the Nwell resistor, this result corresponds to zero bias at the terminals.

FIGURE 7.1 Cross section of Salicided Poly Resistor; Low Value and High Value Poly Resistor

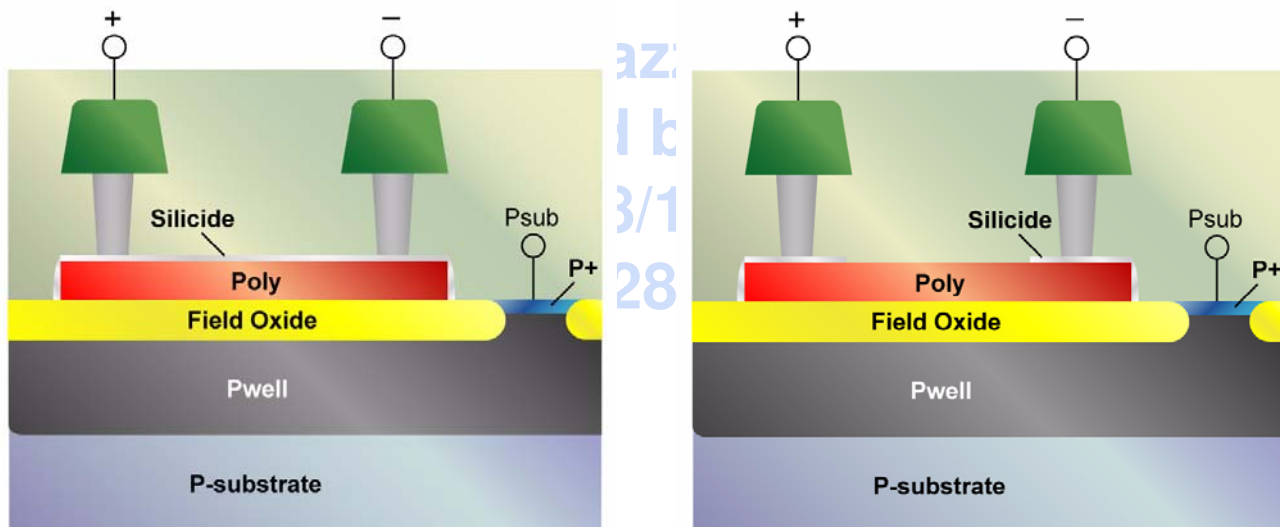
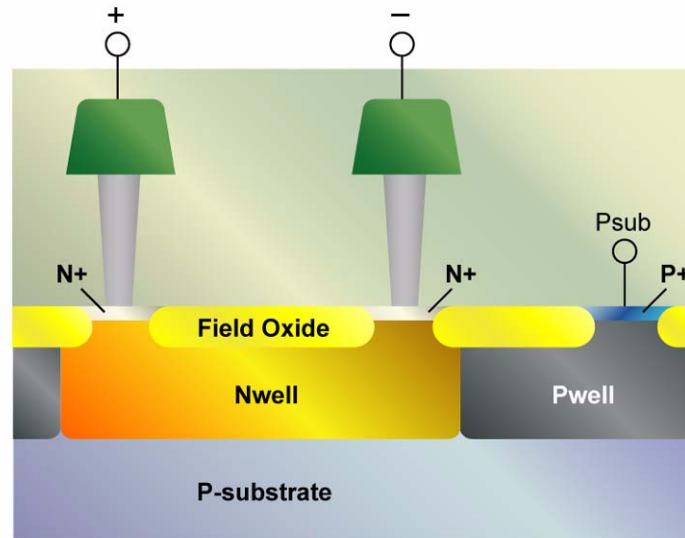


FIGURE 7.2 Cross section of the Nwell Resistor



7.2 Model Description

The equivalent circuit representation of the poly resistors (rf-version) is shown in Figure 7.3. The individual components are based on physical models and are computed using geometrical and electrical process spec information. The base resistance equation is given by

$$R = \frac{\rho_{\square} \cdot L + R_{end}}{W + \Delta W} \quad (\text{EQ 1})$$

where ΔW is the change in effective width, ρ_{\square} is the sheet resistance, and R_{end} is the end resistance. For cases when the rf-behavior of the resistor is not important, a simplified model with fewer components can be used. The dc or low-frequency simulation results of rf-version and dc-version models are identical. This simplified model (dc-version) for the poly resistors is shown in Figure 7.4. The equivalent circuit for an Nwell resistor is shown in Figure 7.10 where Rn is described by a voltage dependent resistance implemented in Verilog-A. Rn is given by (EQ 1) at zero bias.

FIGURE 7.3 Sub-Circuit model for resistor (rf-version)

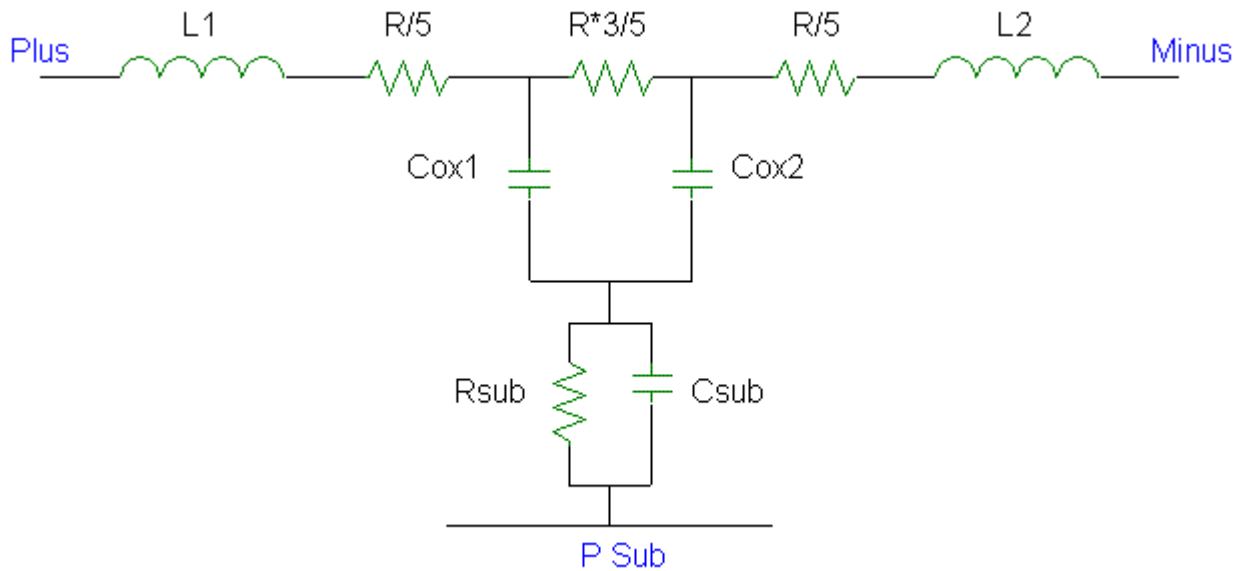
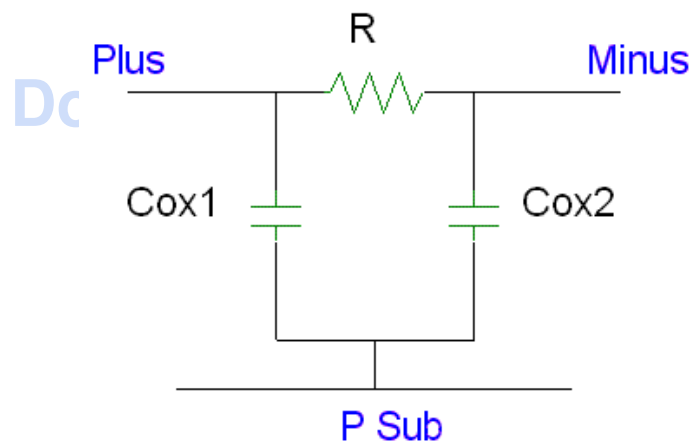


FIGURE 7.4 Sub-Circuit model for resistor (dc-version)



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FIGURE 7.5 Sub-Circuit model for Nwell resistor

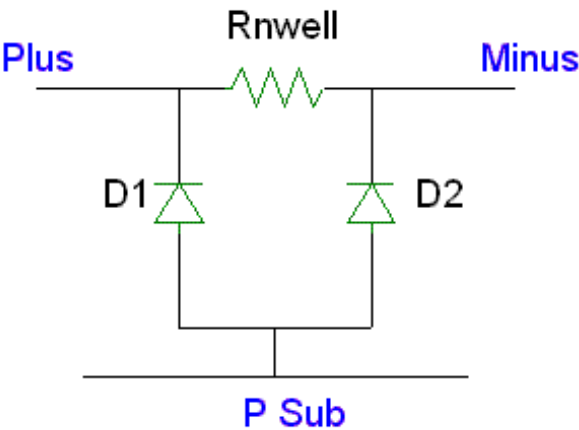


TABLE 7.1 Model Sub-circuit Component Names

Circuit Components	
R	Poly resistance
L1, L2	Resistor self-inductance
Cox1, Cox2	Oxide capacitance
Rnwell	Resistance of Nwell
D1, D2	Diodes associated with Nwell
Csub	Substrate capacitance
Rsub	Substrate resistance

7.3 Model Verification

DC measurements are performed over temperature for the poly and nwell resistors. The temperature coefficients TC1 and TC2 are extracted based from measurements with ranging from -40 to 125 C. The temperature model equation is

$$R(T) = R_{T25} \cdot [1 + TC1 \cdot (T - T25) + TC2 \cdot (T - T25)^2] \tag{EQ 2}$$

Figures Figure 7.6 through Figure 7.8 show the measured data and the simulated results for temperature range from -40C to 125C for poly resistor (*rppoly_lo*), salicide poly resistor (*rppoly_sal*) and nwell resistor (nwell) respectively. Figure 7.9 shows the nwell resistor model validation over voltage.

FIGURE 7.6 rppoly_lo temperature characteristics comparison between data and model

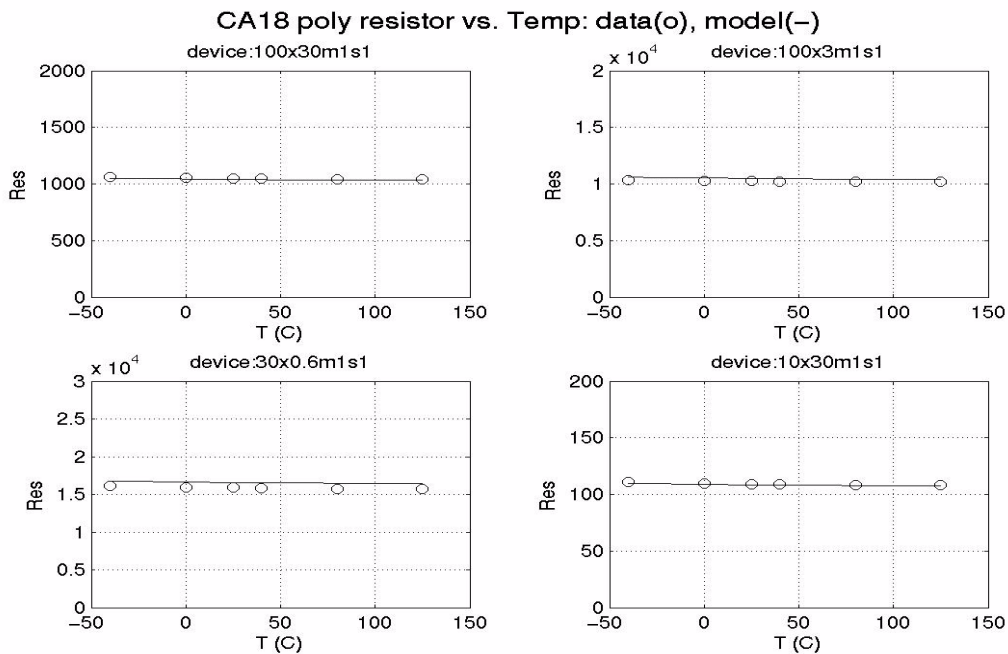


FIGURE 7.7 rppoly_sal temperature characteristics comparison between data and model

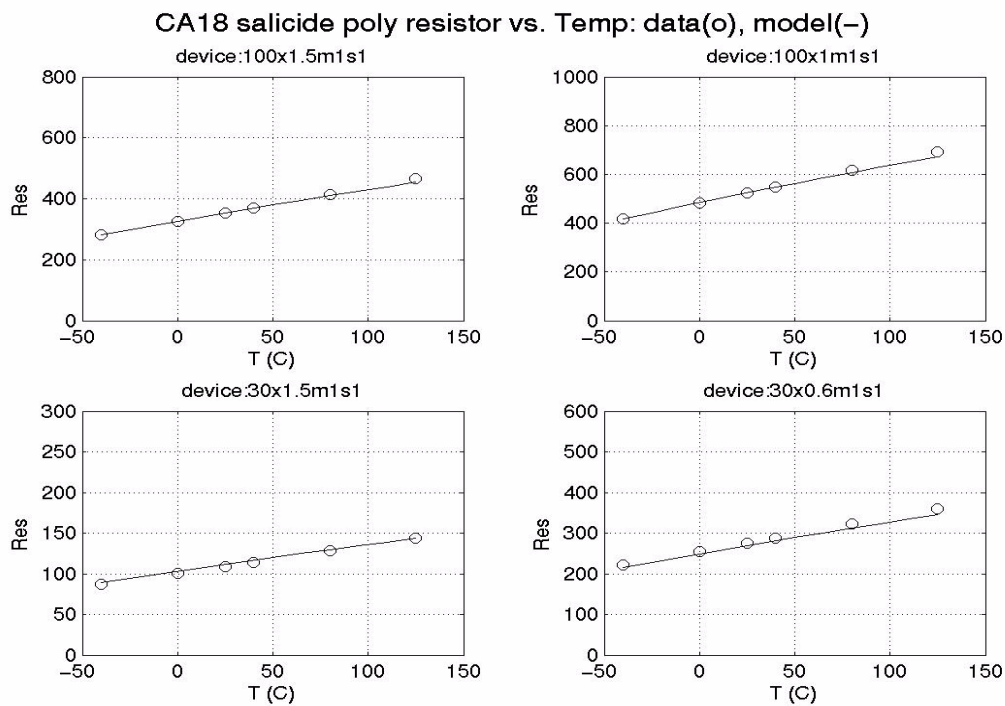
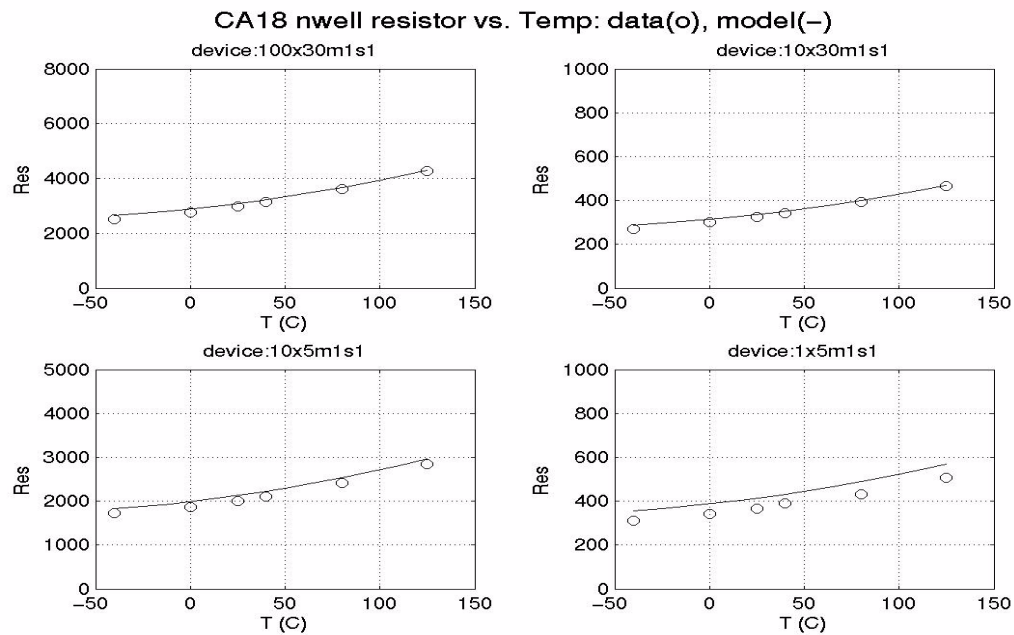
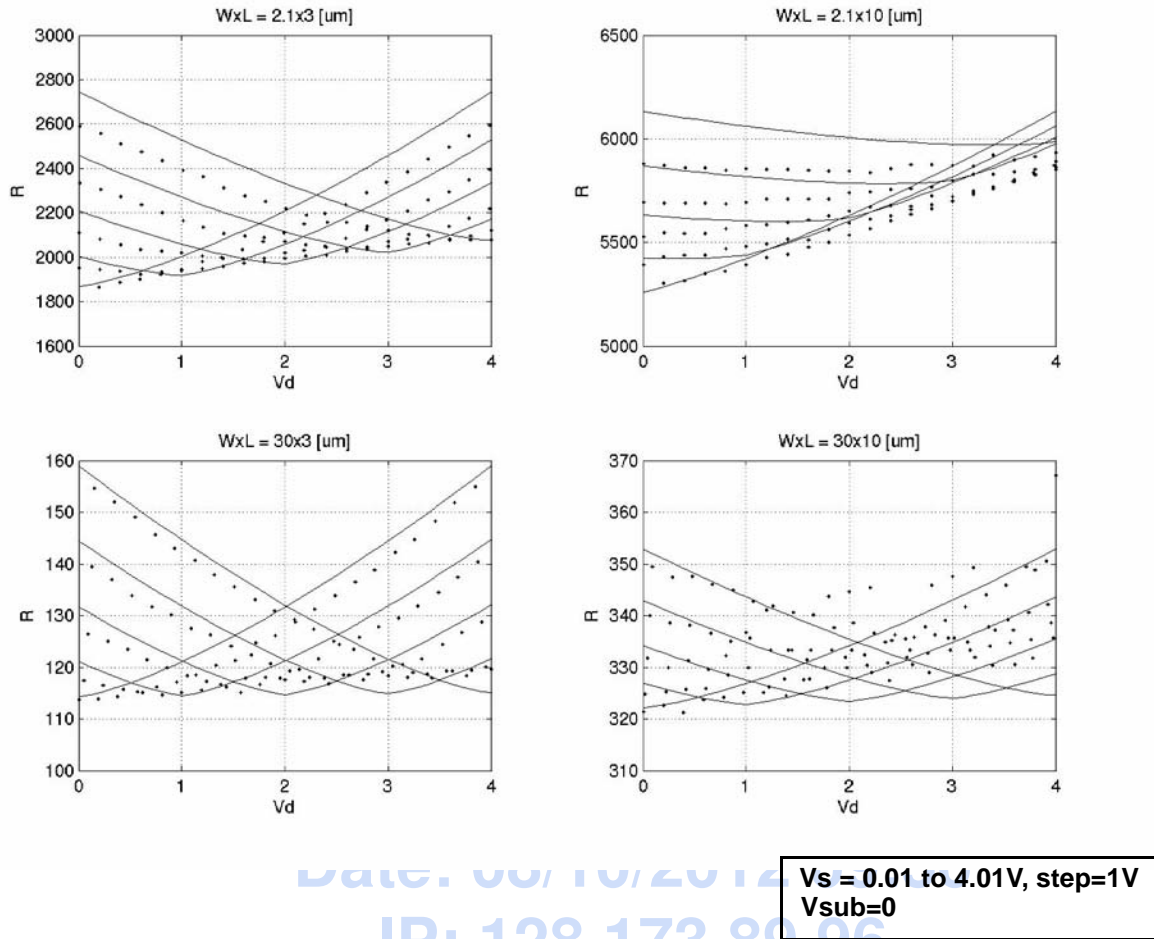


FIGURE 7.8 nwell temperature characteristics comparison between data and model



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FIGURE 7.9 r_{nwell} – over voltage


7.4 Resistor Statistical and Corner Models

The resistor statistical and corner models account for process variation of the ΔW , sheet resistance ρ_q , and resistance R_{end} , and STI thickness derived directly from the process espec. The Resistor model parameters are directly correlated with the process parameters. The corner performance is determined using the min and max values in the espec. Correlation with other device types can be found in Appendix A. Table 7.2 lists the resistor specific espec compared to simulated corner and statistical values.

TABLE 7.2 Corner and statistical resistor model predictions

Device	name	units	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
rppoly_lo	rend ²	ohm-um	240	240	239	190	190	190	140	140	141
	dw ²	um	0.0435	0.0435	0.0424	0.0045	0.0045	0.0039	-0.0345	-0.0345	-0.0346
	rs ¹	ohm/sq	365	365	368	310	310	310	255	255	252

TABLE 7.2 Corner and statistical resistor model predictions

Device	name	units	Slow			Nom			Fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
rppoly_hi	rend ²	ohm-um	1040	1040	1030	865	867	865	692	693	698
	dw ²	um	0.03	0.03	0.03	0.04	0.04	0.04	0.05	0.05	0.05
	rs ¹	ohm/sq	1150	1150	1160	1000	1000	1000	850	852	850
rppoly_sal	rend ²	ohm-um	15.7	15.7	15.4	12.7	12.6	12.5	9.70	9.59	9.62
	dw ²	um	0.03	0.03	0.03	0.04	0.04	0.04	0.05	0.05	0.05
	rs ³	ohm/sq	7.44	7.39	7.40	5.95	5.91	5.92	4.46	4.44	4.43
rnwell	rend ²	ohm-um	1050	1050	1070	875	871	877	700	697	684
	dw ²	um	-0.38	-0.38	-0.36	-0.28	-0.28	-0.272	-0.18	-0.18	-0.183
	rs ¹	ohm/sq	1070	1090	1080	890	909	904	710	727	729

PCM notes:

1. PCM and ESPEC share the same limits.
2. There is no PCM monitoring.
3. Salicided poly sheet rho PCM limits are 1 and 12. The PCM test structures are serpentine structures, susceptible to CD variations which are not accounted for in the sheet rho equation, inducing the larger PCM limits.

7.5 Resistor Mismatch Models**7.5.1 Mismatch Measurements**

A detailed description of resistor mismatch characterization methodology and results are available in the Jazz Semiconductor document NPB PS-0281 titled "Analog Characterization Report for CA18." The basic set-up is a kelvin measurement of 2 matched pairs. Resistor mismatch characterization is only available for poly resistors.

7.5.1.1 Resistor Mismatch Modeling

The resistor mismatch included in the design kit takes into account area and perimeter capacitance mismatch variations. Mismatch due to spacing variation is not included in the model. The mismatch models for the ΔW , sheet resistance ρ_q , end resistance R_{end} are given by

$$\rho_{\square mm} = \rho_{\square nom} \left(1 - \frac{\sigma_A}{\sqrt{LW}} \right) \quad (\text{EQ 3})$$

$$R_{end mm} = R_{end nom} \left(1 - \frac{\sigma_B}{\sqrt{LW}} \right) \quad (\text{EQ 4})$$

$$\Delta W_{mm} = \Delta W_{nom} \left(1 - \frac{\sigma_C}{\sqrt{W}} \right) \quad (\text{EQ 5})$$

where σ_A , σ_B , and σ_C are the mismatch coefficients extracted via a nonlinear least squares global optimization method to best fit the measured data.

7.5.1.2 Mismatch Model Usage Guidelines

The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between resistors. It is implemented inside the “sub-circuit” definition of the resistors allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the resistors. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

7.5.2 Mismatch Model Verification

The mismatch between closely spaced resistor pairs follows a geometric dependence. An extraction process was performed to determine the mismatch coefficients for resistor parameters of ΔW , ρ_{\square} , and R_{end} . These coefficients are used in the statistical model card. The Spectre to measurement mismatch results are shown in Figure 7.10 and Figure 7.11 for low value and salicided poly resistors, respectively. To obtain good matching results, it is preferable to not use minimum dimension but larger size resistors.

FIGURE 7.10 Low-Value Poly resistor mismatch

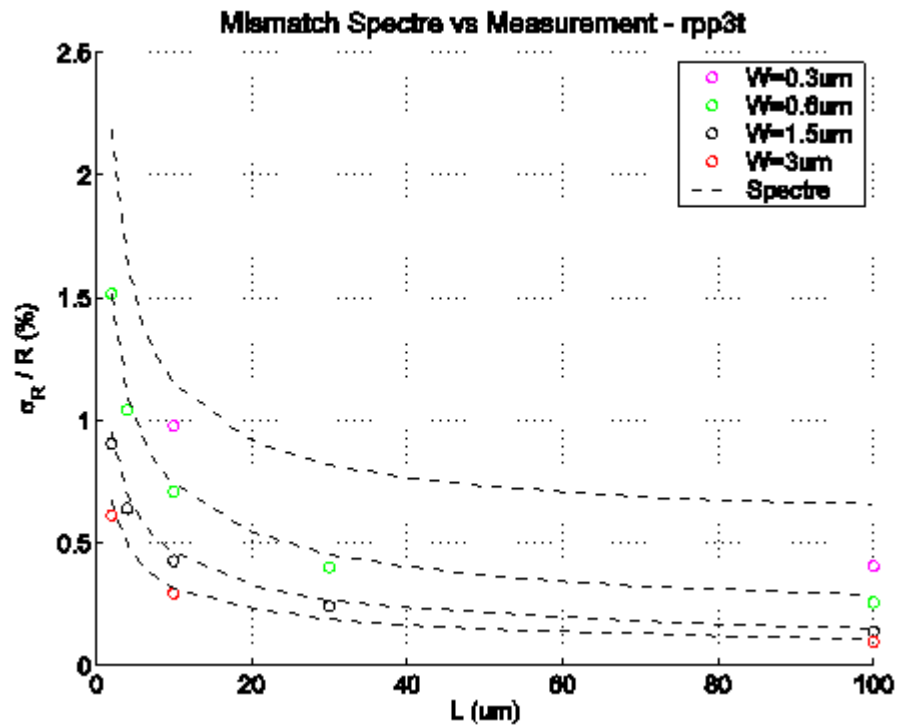
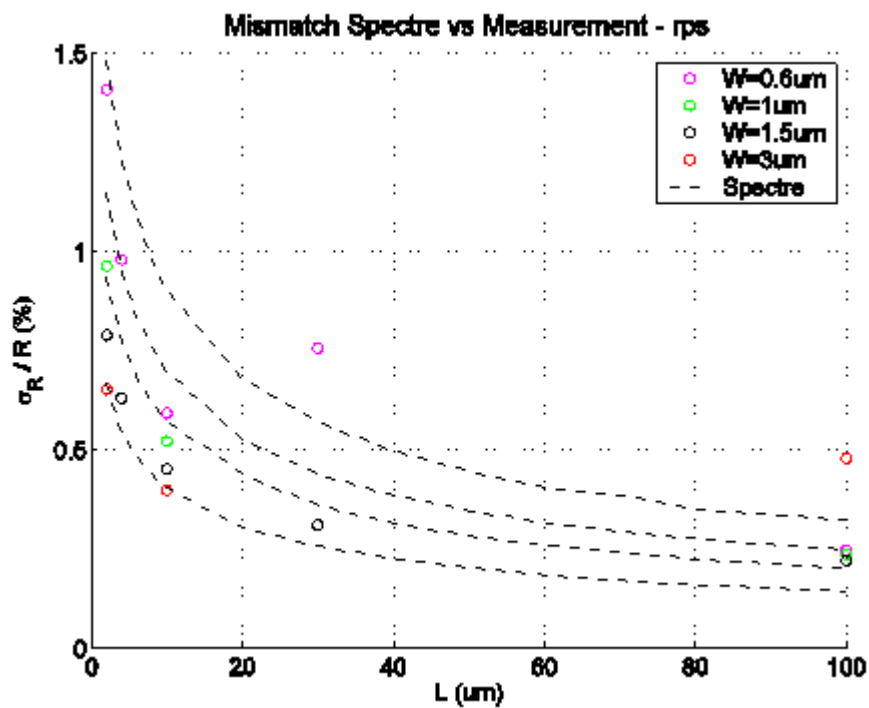


FIGURE 7.11 Salicided Poly resistor mismatch



7.6 Low Value Poly Resistor Flicker Noise (1/f Noise) Model and Verification

Poly-silicon resistors exhibit current noise that is at lower frequencies inversely proportional to frequency and area of the resistor. At higher frequencies the 1/f dependence is replaced by thermal noise which is described by

$$\sqrt{S_{th}} = \sqrt{\frac{4 \cdot k \cdot T}{R}} \quad \left[\frac{A}{\sqrt{Hz}} \right] \quad (EQ 6)$$

The 1/f noise is caused by charge trapping and de-trapping events at the poly-silicon grain boundaries. These events change the energetic barrier and thus modulate the resistance or current over the grain boundary. A physics based equation was proposed in IEEE Transactions on Electron Devices, Vol48, No.6, June 2001 by Brederlow et al.

$$S_I = \frac{I^2}{W \cdot L} \cdot \frac{\alpha}{f} \quad \left[\frac{A^2}{Hz} \right] \quad (EQ 7)$$

where S_I is the noise current per frequency band width and α is the parameter extracted to measured data.

This equation was implemented in the Spectre model cards for **rppoly_lo** device by matching it with the coefficients of the Spectre provided noise equation.

$$\sqrt{S_I} = \sqrt{\frac{KF \cdot I_r^{AF}}{f}} \quad \left[\frac{A}{\sqrt{Hz}} \right] \quad (EQ 8)$$

where $I_r = I$, $AF = 2$, and $KF = \alpha/(WL)$.

The model verification plots for two **rppoly_lo** devices at biases 0.25, 0.5 and 2 V are shown in figures Figure 7.12 and Figure 7.13.

FIGURE 7.12 Flicker Noise (rppoly_lo) – W=3um, L=10um (R=800 Ω)

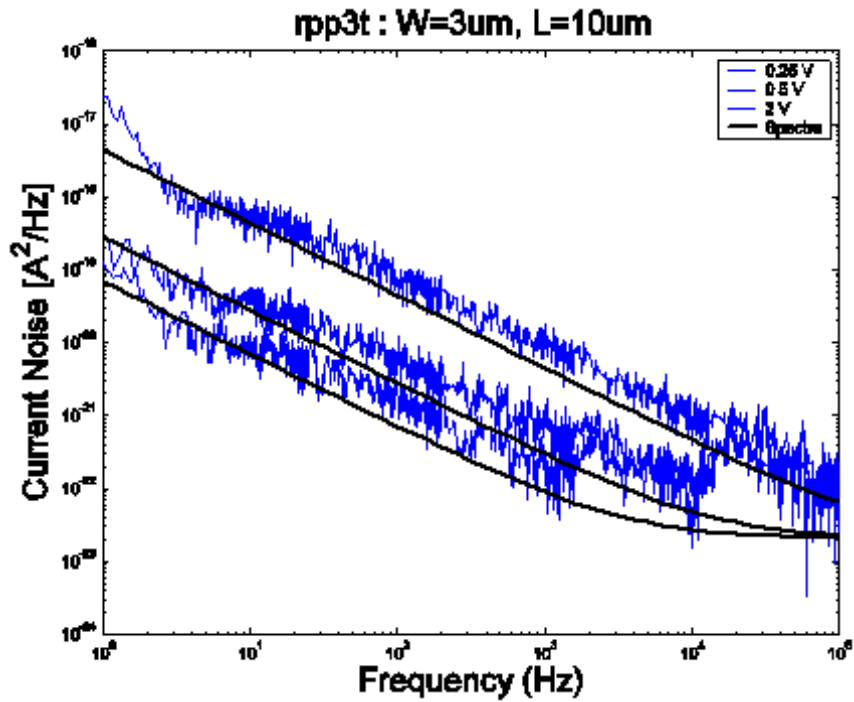
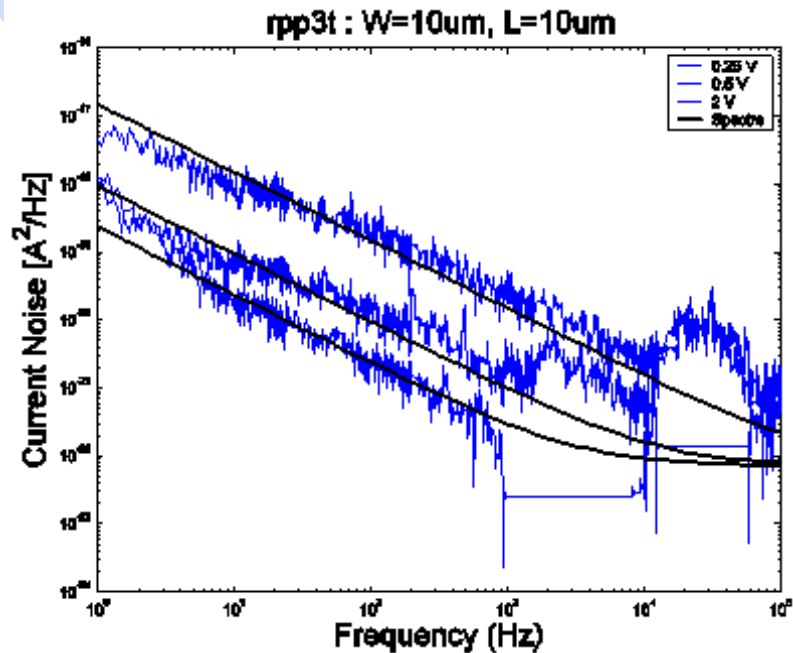


FIGURE 7.13 Flicker Noise (rppoly_lo) – W=10um, L=10um (R=243 Ω)



7.6.1 v4.2**TABLE 7.3** Resistor model specific updates in model release version 4.2

v3.4 update	Reason	Impact on user
Tighten low value poly resistor Rsh corner values	Updated to match new E-spec.	Reduced spread in simulations using corner models

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8.0 Capacitor Models

8.1 MiM capacitor model

8.1.1 Device description

The CA18 technology offers vertical MIM capacitor densities and metal layer configurations given in Table 8.1.

TABLE 8.1 CA18 MIM Capacitors

Process	Metal Layers	MIM Definition	Device Name
CA18QD	4	2fF between M2-M3 2fF between M3-M4 4fF stacked between M2-M4	cmim2, cmimw2, cmimw2_4 cmim2_m3, cmimw2_m3, cmimw2_4_m3 csmim4, csmimw4, csmimw4_4
CA18QW5	4	1fF between M2-M3	c3t_mim, c3t_mimw
CA18PD	5	2fF between M3-M4 2fF between M4-M5 4fF stacked between M3-M5	cmim2, cmimw2, cmimw2_4 cmim2_m4, cmimw2_m4, cmimw2_4_m4 csmim4, csmimw4, csmimw4_4
CR18PW54	5	1fF between M2-M3	c3t_mim, c3t_mimw
CA18HD	6	2fF between M2-M3 2fF between M3-M4 4fF stacked between M2-M4	cmim2, cmimw2, cmimw2_4 cmim2_m3, cmimw2_m3, cmimw2_4_m3 csmim4, csmimw4, csmimw4_4
CA18HR	6	2fF between M2-M3 4fF stacked between M2-M4	cmim2, cmimw2, cmimw2_4 csmim4, csmimw4, csmimw4_4

MIM capacitors can be placed over Nwell ("w" in device name) or over P-substrate. MIM capacitors over Nwell have an additional Nwell to P-substrate junction isolation between the bottom plate and P-substrate which is included in the model. Three terminal devices only are available in CA18QW5 and CR18PW54. For devices over P-substrate, the 3rd terminal is the P-substrate. In CA18HD/PD/QD, four terminal devices ("_4" suffix) are available for devices over Nwell where the 4th terminal is the P-substrate. Table 8.2 provides a description of the terminal connections. In order to obtain better isolation between the MIM capacitors over Nwell and nearby devices, it is recommended to tie the Nwell to AC ground (VDD for example). Figure 8.1 illustrates a cross section of a CA18QD stacked MIM capacitor and base MIM capacitor over Nwell.

FIGURE 8.1 Sample CA18QD Single and Stacked MIM Capacitor cross sections

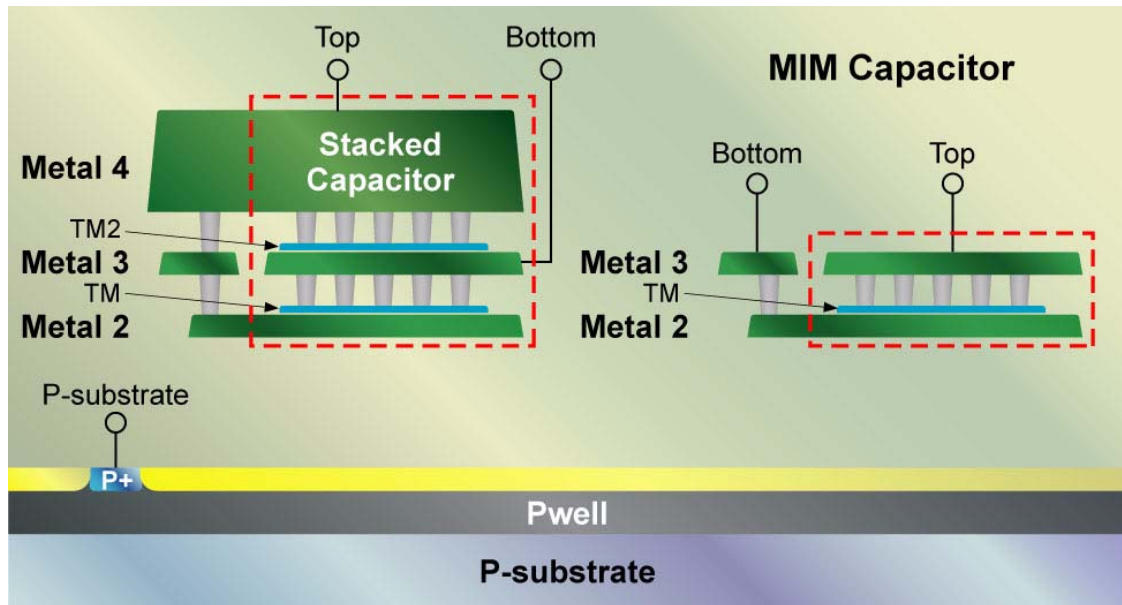


TABLE 8.2 NWell and SUB Terminals

Terminals	OVER NWell?	SUB Terminal	NWell Terminal	Models
3	NO	3rd terminal	none	c3t_mim, cmim2, csmim4
3	YES	No terminal, SUB hard coded to SPICE node 0 in model	3rd terminal	c3t_mimw, cmimw2, csmimw4
4	YES	4th terminal	3rd terminal	cmimw2_4, csmimw4_4

8.1.2 Model Description

Figure 8.2 through Figure 8.5 show the sub circuits used to model the MIM and stacked MIM devices respectively. Please refer to Table 8.3 for sub circuit component names and physical descriptions. The model includes all elements within the dashed box shown in Figure 8.1 including metal and via parasitics. The bottom plate access is not included in the model since its placement is controlled by the pcell with various options available. The model assumes one sided bottom and top plate routing which is a worst case scenario. Accurate simulations of the bottom plate access are achieved through post-extraction (PEX/RCX) simulation. See Appendix A for more information on layout parasitics. The device over Nwell model includes the Nwell/psub diode. All models scale with MIM length (L) and width (W). The MIM device model parameters can be different between the 4, 5, and 6 layer metal technologies. A subset of the parameters are adjusted to match the different back end structure topologies and measured data, when available.

FIGURE 8.2 Sub-circuit and component description of a MIM capacitor over Nwell.

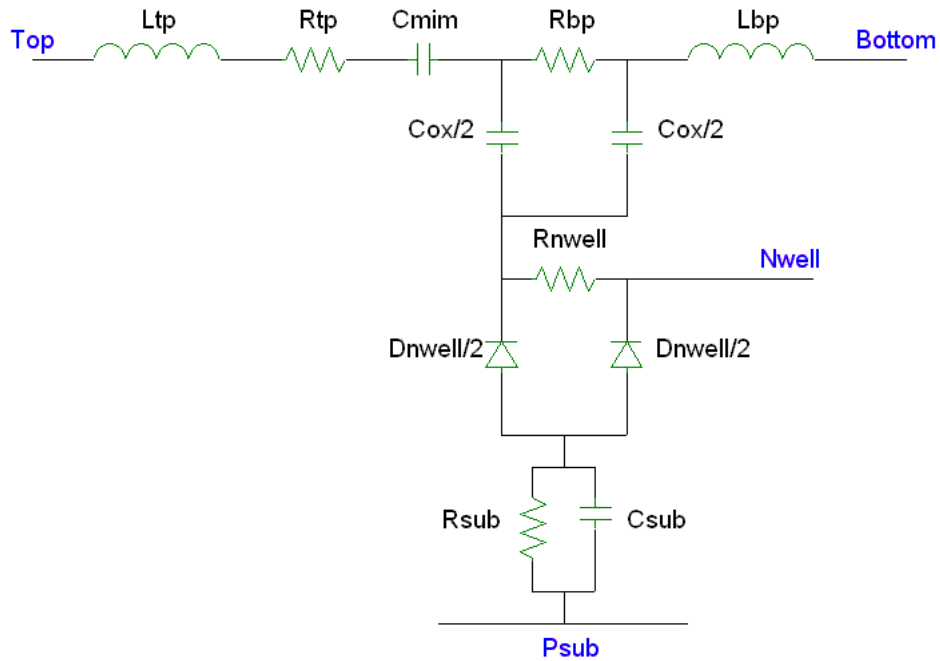


FIGURE 8.3 Sub-circuit and component description of a MIM capacitor over P substrate.

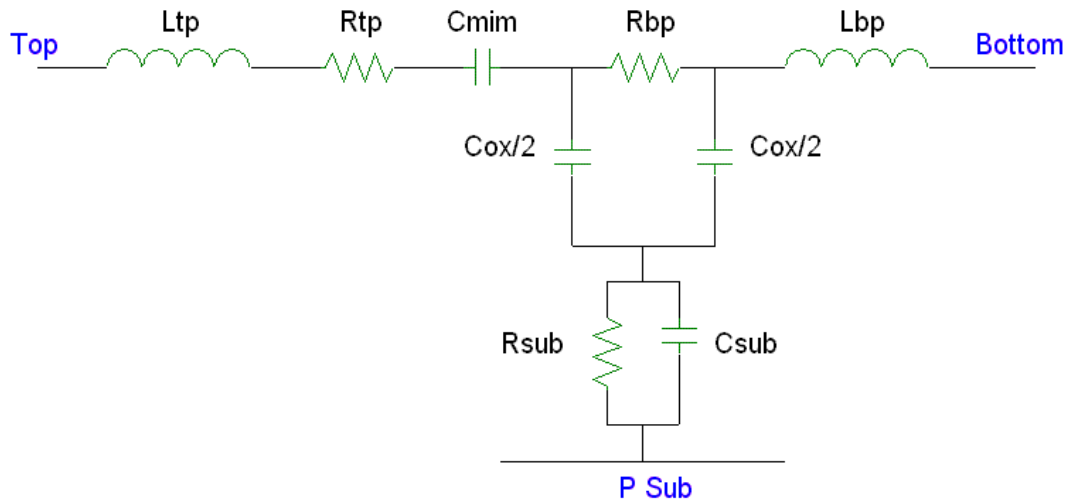


FIGURE 8.4 Sub-circuit and component description of a Stacked MIM capacitor over Nwell.

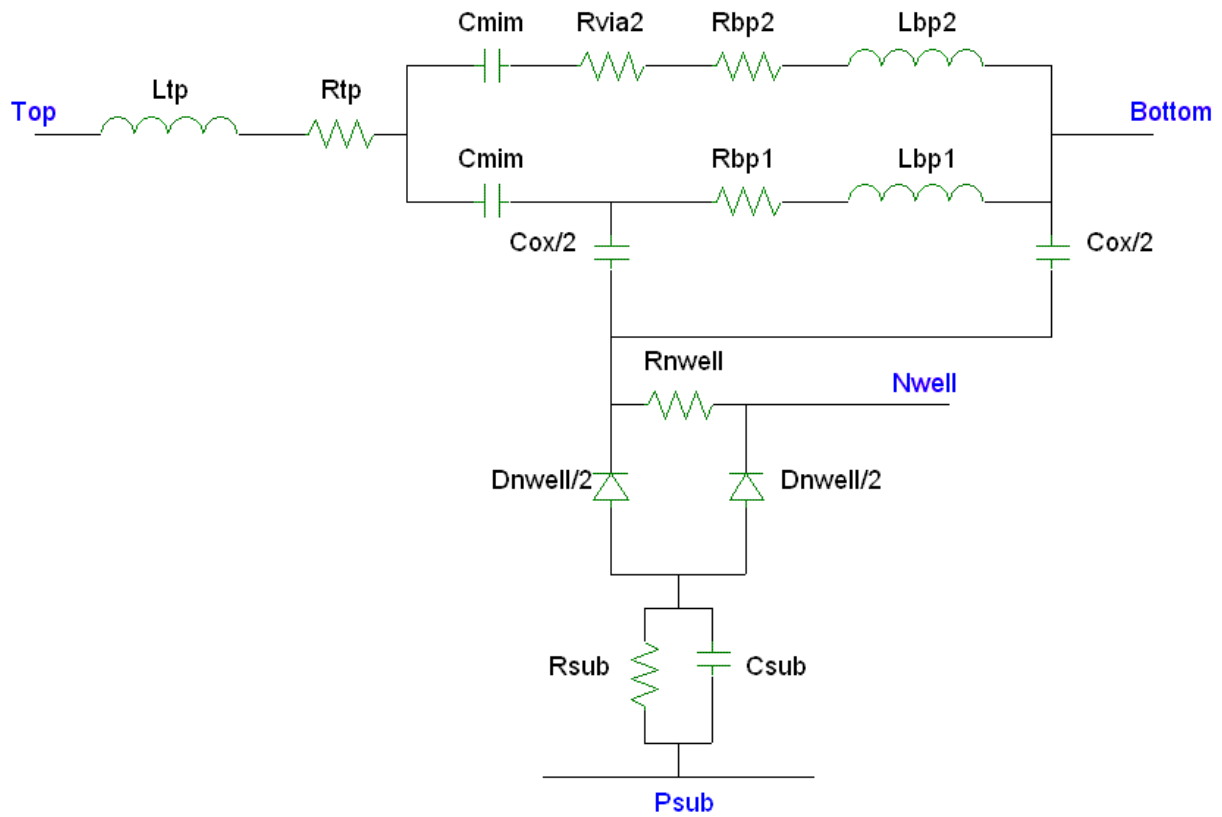


FIGURE 8.5 Sub-circuit and component description of a Stacked MIM capacitor over P substrate.

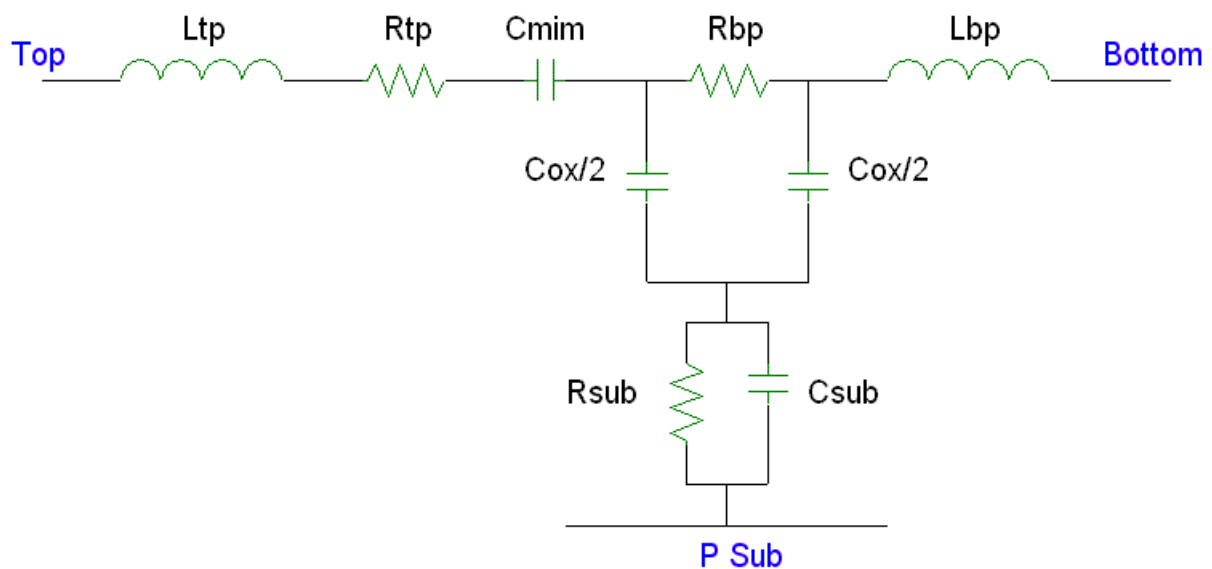
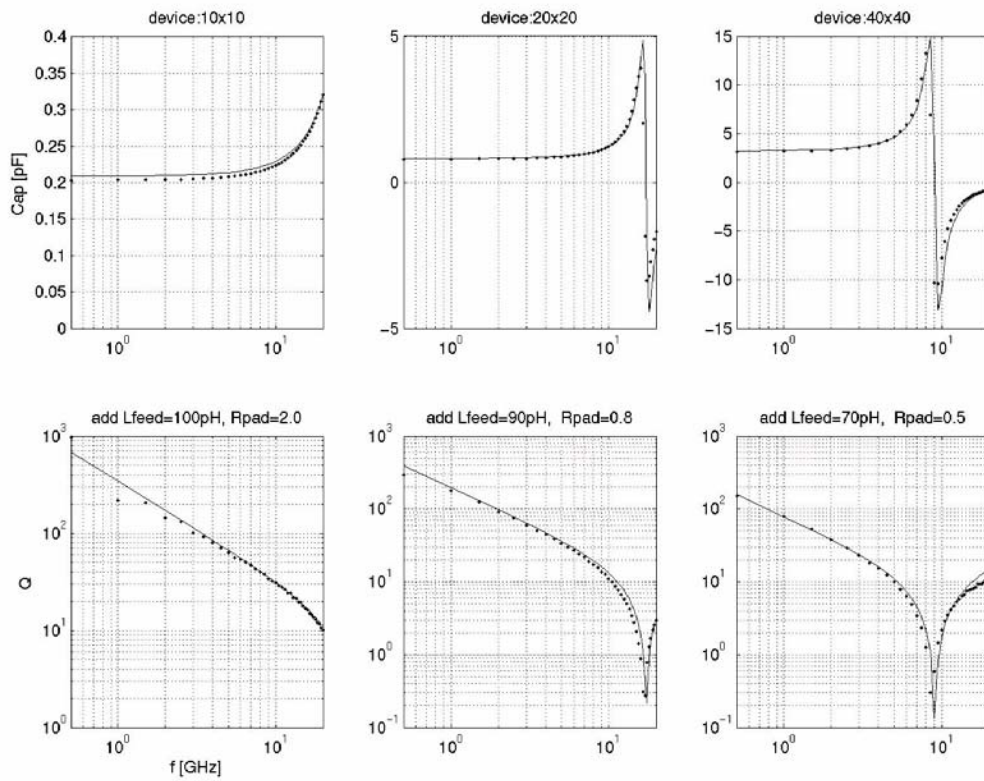


TABLE 8.3 Capacitor Model Sub-circuit component names

Circuit Components	
cmim	MIM Capacitance
Ltp	Top Plate Inductance
Rtp	Top Plate Resistance
Rbp	Bottom Plate Resistance
Lbp	Bottom Plate Inductance
Cox	Oxide Capacitance
RNwell	Nwell Resistance
DNwell	Nwell to P Sub junction diode
Csub	Substrate Capacitance
Rsub	Substrate Resistance
Rvia	Via Resistance

8.1.3 Model Verification

RF measurements are performed on various MIM capacitors. As MIM caps have very small resistance (on the order of a few hundred milliohms and smaller), accurate measurements of the device resistance are difficult. Contact resistance de-embedding errors and repeatability are the limiting factors. Short and thru line de-embedding methods will not yield the true device resistance. Thus, open only de-embedding is performed, requiring simulation of feed line inductance (L_{feed}) and contact resistance (R_{pad}) to match the Q and resonance. These values are indicated directly on the plots. Effective capacitance and quality factor (Q) plots are shown for several geometries of 2fF and stacked 4fF devices in Figure 8.6 and Figure 8.7 respectively. The effective capacitance increases at higher frequencies due to the inductance of the metal plates, eventually approaching a self-resonance. Larger capacitors show this effect at lower frequencies since the large capacitance equates to lower resonance frequency. The MIM capacitors give very high Q due to the low resistive losses of the metal plates and vias. As parasitics of the metal connections to the MIMs in layout will significantly reduce the Q, post layout parasitic extraction simulation is crucial for accurate Q simulation. Figure 8.8 shows a comparison of the 3 MIM densities as a function of device area.

FIGURE 8.6 $2fF/\mu m^2$ MIM capacitance and Q characteristics

Note: 10x10 test device measured contains $3.5\mu m$ via spacing. Design kit pcell and model has $1\mu m$ via spacing. There is a 1Ω discrepancy in the 10x10 via resistance included in the compared to this test device, resulting in the much higher Rpad for the 10x10 device.

FIGURE 8.7 4fF/ μm^2 MIM capacitance and Q characteristics

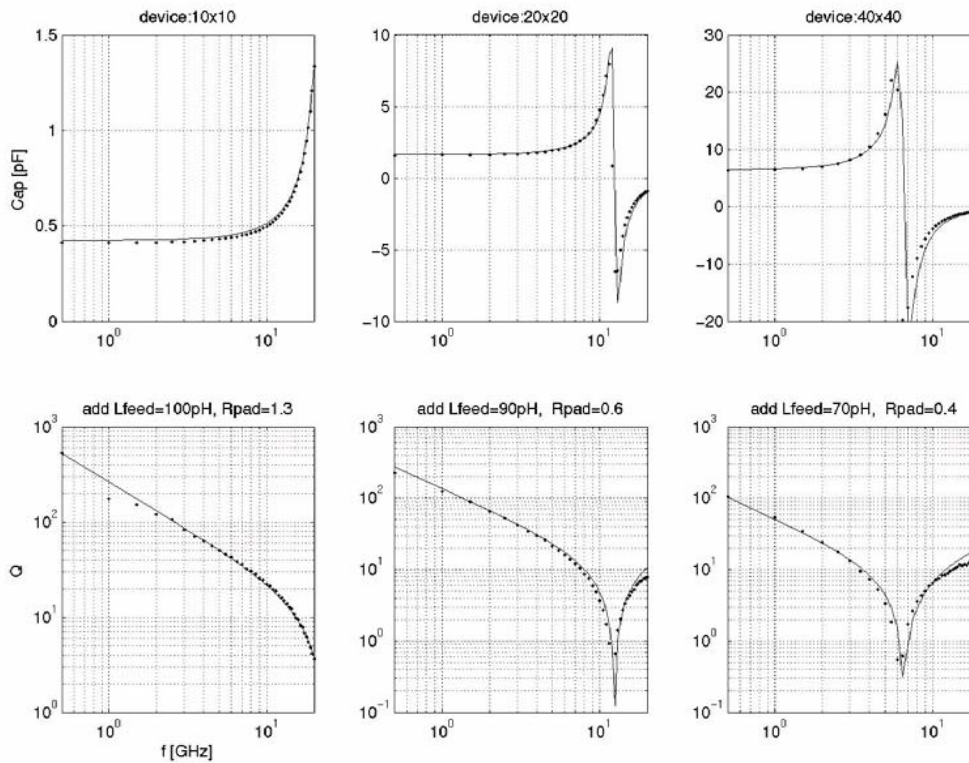
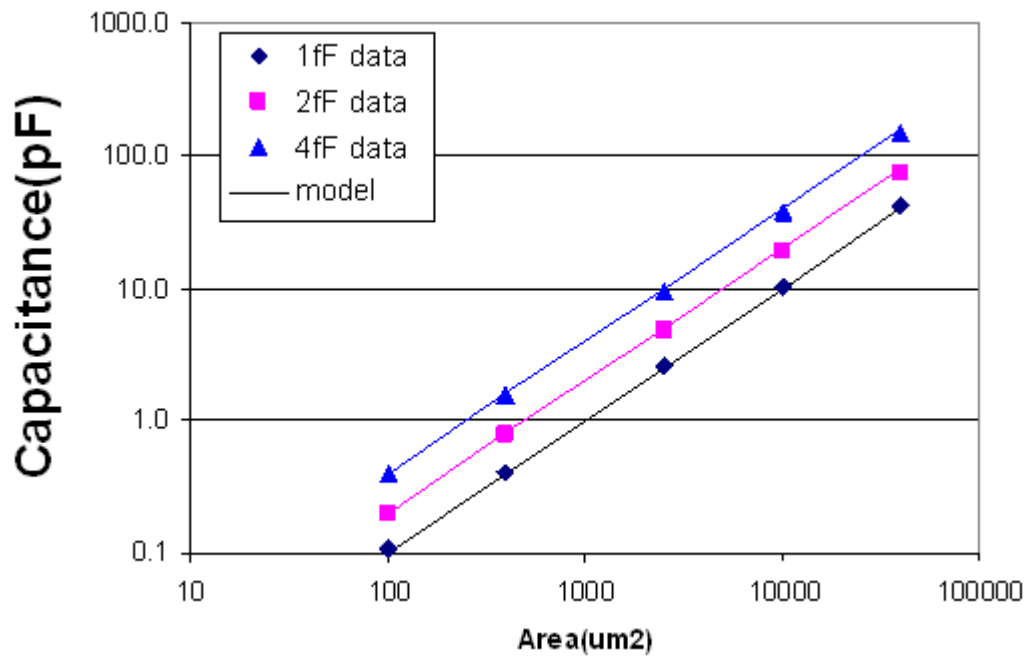


FIGURE 8.8 Comparison between MiM capacitor model and measured data



8.1.4 MiM Statistical and Corner Models

The MiM statistical and corner models account for process variation of the MiM oxide thickness, metal thickness (sheet resistivity), and ILD thickness derived directly from the process espec. The MiM model parameters are directly correlated with the process parameters. Correlation with other device types can be found in Appendix A. Table 8.4 lists the MiM specific espec compared to simulated corner and statistical values for three MiM capacitor devices.

TABLE 8.4 ESPEC, Corner and Statistical Model Comparison for MiM Capacitor Model

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
c3t_mim	cp ²	fF/um	0.13	0.13	0.13	0.1	0.1	0.1	0.07	0.07	0.07
	ca ¹	fF/um ²	1.15	1.15	1.16	1	1	1	0.85	0.85	0.84
	tc ²	ppm/v		20	20	20	20	20		20	20
c3t_mim2	cp ²	fF/um	0.35	0.34	0.34	0.23	0.23	0.23	0.12	0.12	0.12
	ca ¹	fF/um ²	2.3	2.3	2.3	2	2	2	1.7	1.7	1.7
	tc ²	ppm/v		20	20	20	20	20		20	20
c3t_sMIM4	cp ²	fF/um	0.8	0.8	0.8	0.6	0.6	0.6	0.4	0.4	0.4
	ca ¹	fF/um ²	4.6	4.6	4.6	4	4	4	3.4	3.4	3.4
	tc ²	ppm/v		20	20	20	20	20		20	20

PCM notes:

1. PCM and ESPEC share the same limits.
2. There is no PCM monitoring.

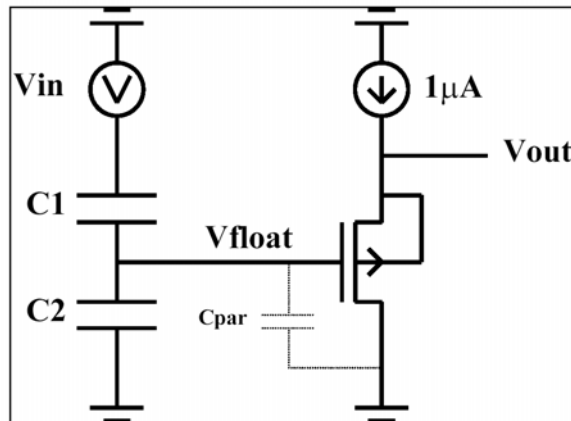
8.1.5 MiM Mismatch Models

8.1.5.1 Mismatch Measurements

A detailed description of MiM mismatch characterization methodology and results are available in the Jazz Semiconductor document NPB PS-0281 titled "Analog Characterization Report for CA18." The basic set-up is a voltage divider circuit as shown in Figure 8.9. By reversing the terminals of the capacitor pairs, the mismatch can be calculated independent of the circuit parasitics, given by

$$\frac{\Delta C}{C} = 2 \cdot \left(\frac{C1 - C2}{C1 + C2} \right) \quad (\text{EQ 1})$$

FIGURE 8.9 MiM Mismatch Measurement Schematic



8.1.5.2 MiM Mismatch Modeling

The MiM mismatch included in the design kit takes into account area and perimeter capacitance mismatch variations. Mismatch due to spacing variation is not included in the model. The mismatch models for area and perimeter effects are given by

$$CA_{mm} = CA_{nom}(1 - \sigma_A[LW]^{\delta_A}) \quad (EQ 2)$$

$$CP_{mm} = CP_{nom}(1 - \sigma_P[LW]^{\delta_P}) \quad (EQ 3)$$

where σ_A , σ_P , δ_A , and δ_P are the area and perimeter coefficients and exponents extracted via a nonlinear least squares global optimization method to best fit the measured data.

8.1.5.3 Mismatch Model Usage Guidelines

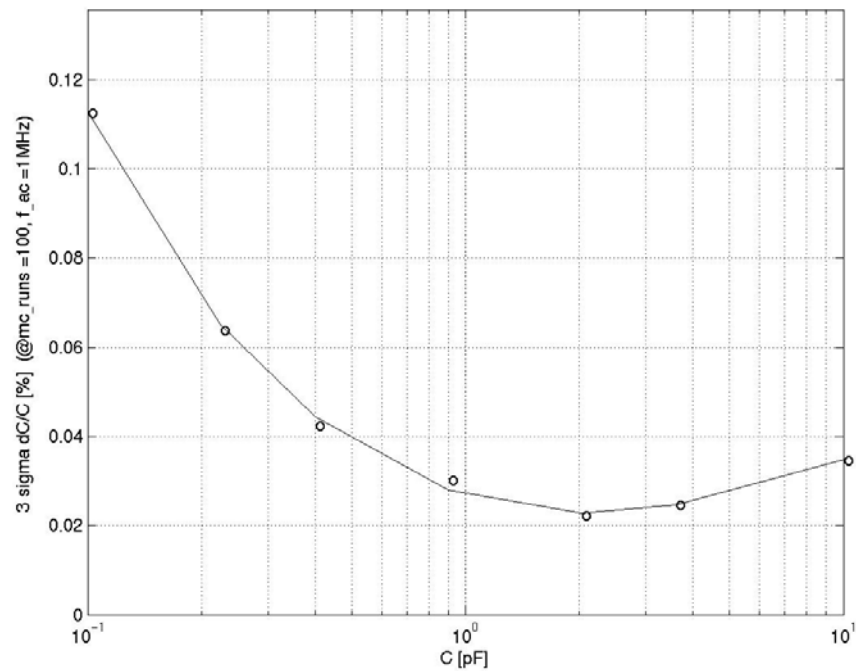
The mismatch model is available in Spectre, which provides the necessary framework to model the local mismatch between capacitors. It is implemented inside the “sub-circuit” definition of the MiMs allowing for “instance to instance” variations in the process parameters. The “variations” variable inside Spectre should be set equal to “mismatch.” Typically, ~100 monte-carlo runs are sufficient to accurately simulate the local-mismatch between the MiMs. The user should, however, increase the “numruns” variable inside Spectre until the improvement in the simulated results is small.

8.1.5.4 Mismatch Model Verification

Figure 8.10 through Figure 8.12 compare the mismatch model prediction of the measured data for the minimum spacing (4μm) 3-σ $\frac{\Delta C}{C}$ vs. capacitance value which is scaled through geometry variation. For smaller devices, the mismatch increases due to perimeter effect dominance. For larger devices, the mismatch

increases due to area effect dominance. The model accurately predicts the trends and can be used to design for minimum mismatch between 2 capacitor pairs. More elaborate mismatch configurations such as common centroid are characterized in the CA18Analog Characterization report.

FIGURE 8.10 1fF MiM Matching Data (circles) vs. Model (solid line) (spacing=4 μ m)



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FIGURE 8.11 2fF MiM Matching Data (circles) vs. Model (solid line) (spacing=4 μ m)

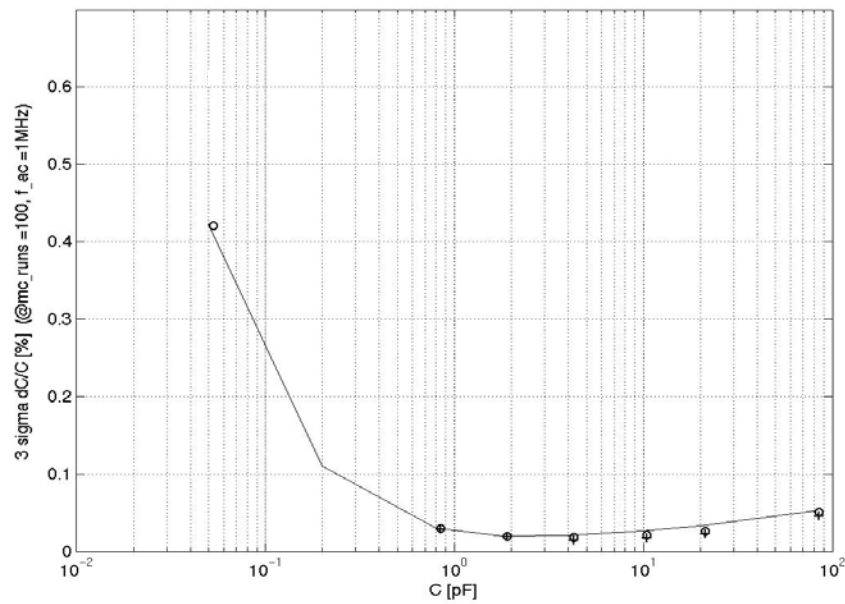
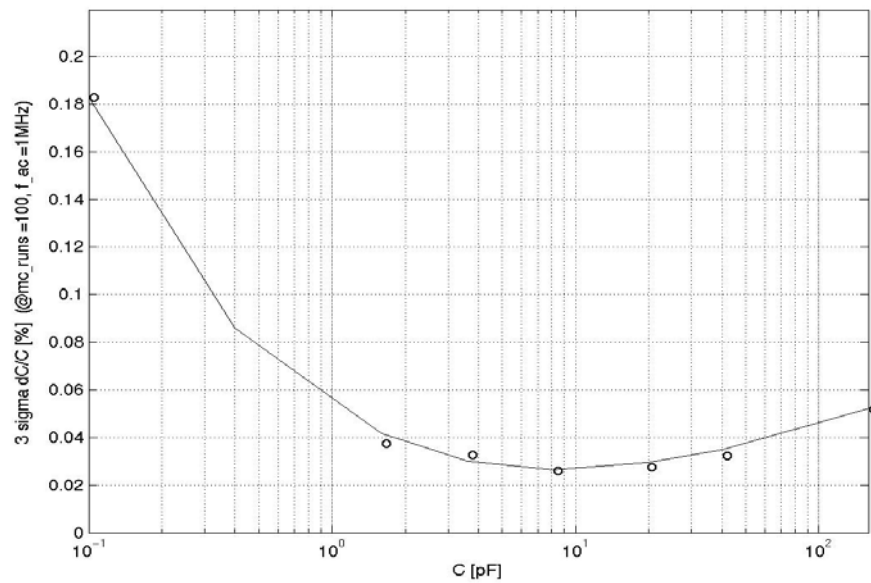


FIGURE 8.12 4fF MiM Matching Data (circles) vs. Model (solid line) (spacing=4 μ m)

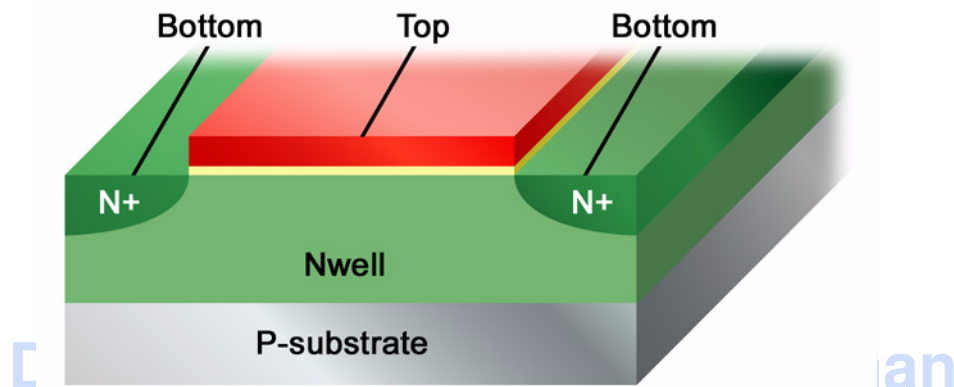


8.2 Poly Capacitor (CPOLY, CPOLY3P3) model

8.2.1 Device Description

Poly capacitors are formed by MOS structures with Nwell beneath the n+ poly gate and n+ Nwell contacts as shown in Figure 8.13. Without p+ source/drains, there is no source for inversion charge, resulting in depletion capacitance in inversion. Maximum capacitance is achieved in accumulation when the poly gate is positively biased with respect to the Nwell. The device is available in thin oxide (library name: **cpoly**) and thick oxide (library name: **cpoly3p3**) versions. The **cpoly** device is exactly the same in cross section to the MOS varactor in section 7.2. The difference between the **cpoly** device and the MOS Varactor is in layout and modeling.

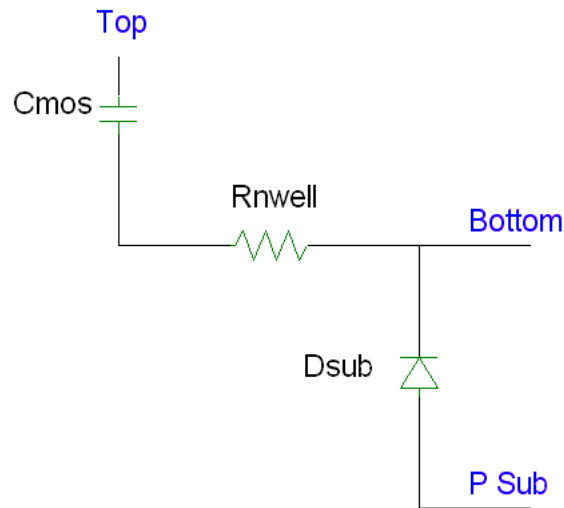
FIGURE 8.13 Poly Capacitor cross-section



8.2.2 Model Description

Figure 8.14 shows the sub circuit model for the **cpoly** device. The **cpoly** model consists of MOS capacitance (emulated through a BSIM element) in series with a Nwell resistance. The parasitic Nwell/Psub junction diode is also included. **The capacitance model is accurate for large plate geometries ($L > 2\mu\text{m}$, $W > 2\mu\text{m}$).** The Nwell resistance is estimated in order to give reasonable simulations of RC effects. **The *cpoly* or *cpoly3p3* devices should not be used in varactor applications.** For varactor applications which require accurate capacitance and parasitic modeling over bias, frequency and geometry, the **varactor_mos** device should be used (see Chapter 5.2).

FIGURE 8.14 Poly Capacitor Sub-circuit description



8.2.3 Model Verification

Figure 8.15 and Figure 8.16 show the measured and simulated CV data for **cpoly** and **cpoly3p3** devices. Parameters are extracted from devices with $W_g=250\mu\text{m}$ and $L_g=110\mu\text{m}$. As a result, ΔL , ΔW , and fringing terms are not accurately extracted. Thus choosing geometries below a few μm may lead to inaccuracies.

FIGURE 8.15 **cpoly** CV curve measurement (Cg.m) vs. simulation (Cg.s)

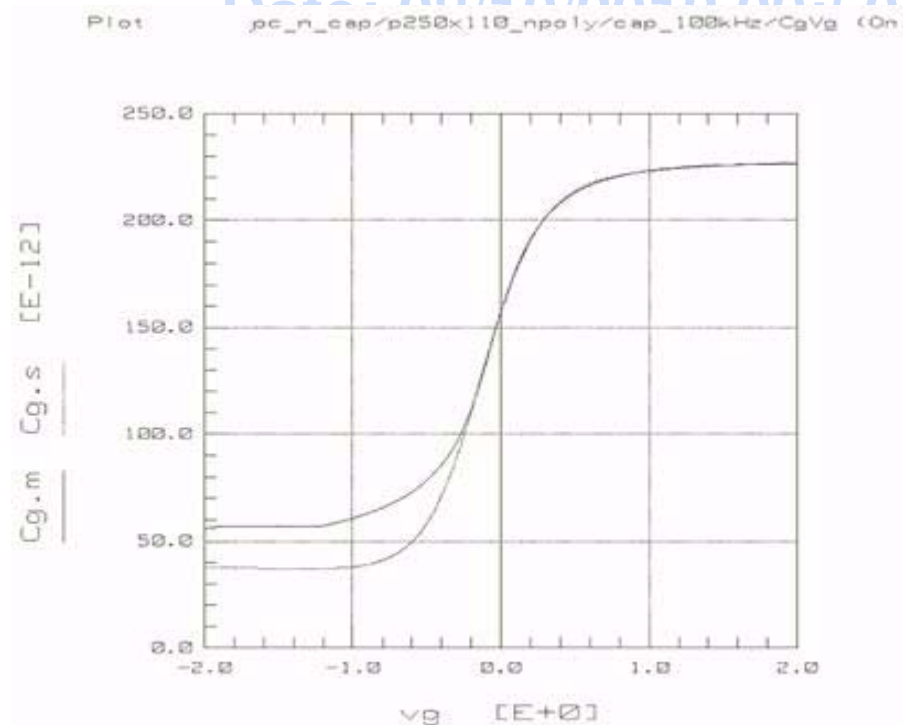
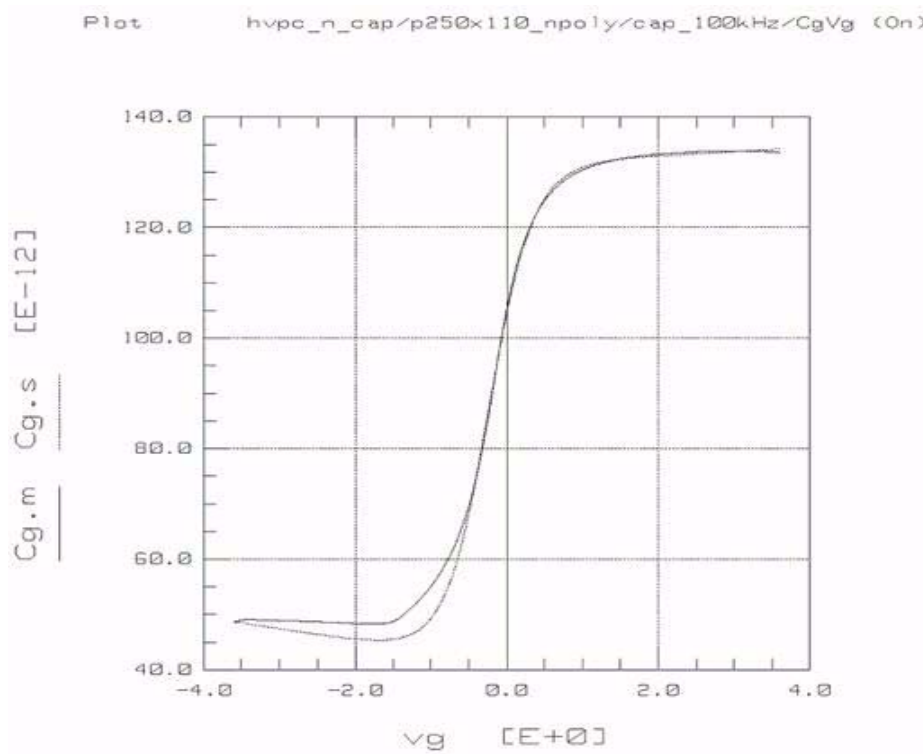


FIGURE 8.16 *cpoly3p3* CV curve measurement (Cg.m) vs. simulation (Cg.s).

8.2.4 Cpoly Statistical and Corner Models

The statistical and corner models for the *cpoly* devices are correlated directly with the MOSFETs through the parameters T_{ox} , V_{TH} , ΔW , and ΔL .

8.2.5 Cpoly MisMatch Models

Mismatch models for *cpoly* and *cpoly3p3* are not supported.

9.0 Vertical PNP

9.1 Device Description

The CA18 process offers a vertical PNP transistor formed by a p+ emitter, Nwell base, and psub collector as shown in Figure 9.1. There are four discrete vertical PNP transistors in the model library given in Table 9.1. These four geometries are accessible through the **vPNP** symbol in schematic entry and as **PNPa/b/c/d** in layout. The top layout view is shown in Figure 9.2.

FIGURE 9.1 Cross Section of the Vertical PNP

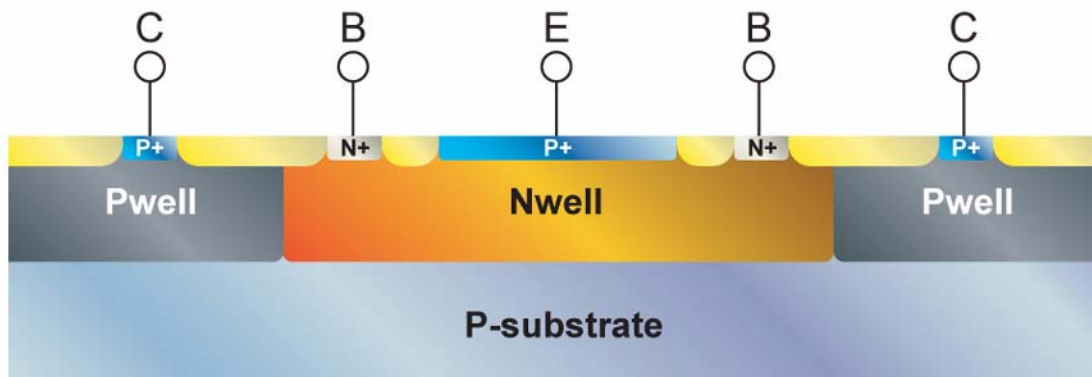
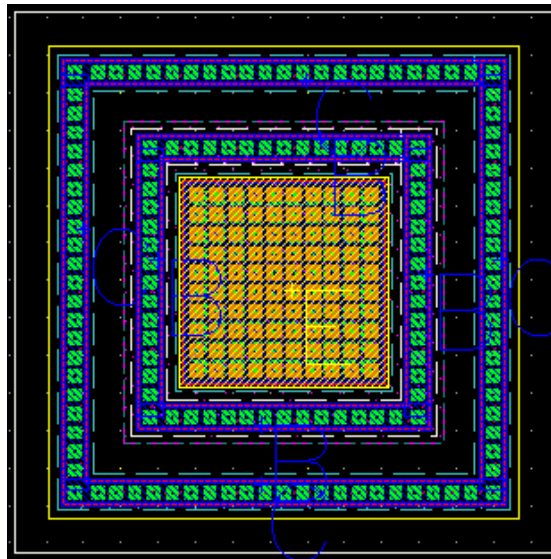


TABLE 9.1 VPNP Devices

Device Name	Emitter Area
PNPa	25x25 μm^2
PNPb	11x11 μm^2
PNPc	5.4x5.4 μm^2
PNPd	3x3 μm^2

FIGURE 9.2 Top view of the vertical PNP transistor

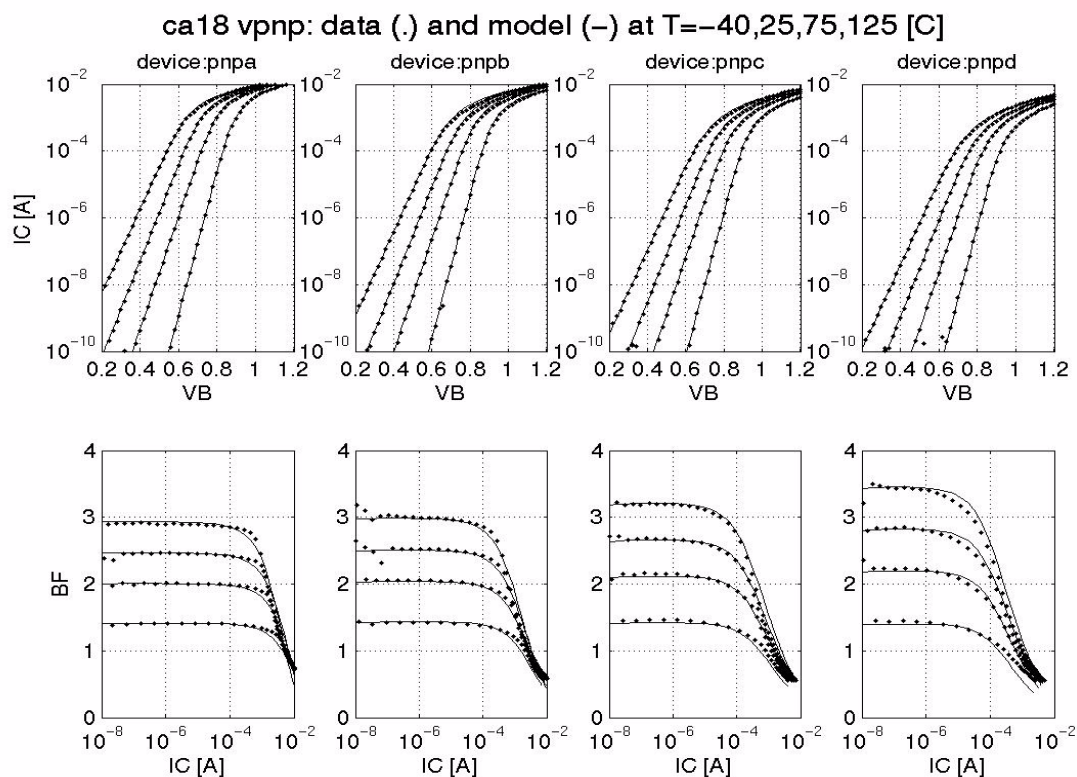
9.2 Model Description

The VPNP is modeled with a standard Gummel-Poon model. Four discrete model cards are extracted for the four different emitter sizes given in Table 9.1.

9.3 Model Verification

Figure 9.3 displays vertical PNP performance across different temperatures. The forward beta (BF) model parameter is shifted from the nominal model by -14% in order to match this measured data. This shift is within the corner specification.

FIGURE 9.3 Verification Plots for VPNP



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9.4 VPNP Statistical and Corner Models

The primary process parameter that controls the statistical behavior of the VPNP is the Nwell doping. The current gain (β), saturation current (I_s), and Early Voltage (V_{AF}) are affected by the Nwell doping. Figure 9.4 illustrates the corner model performance of the vertical PNP under different bias conditions. Table 9.2 lists the VPNP specific espec compared to simulated corner and statistical values.

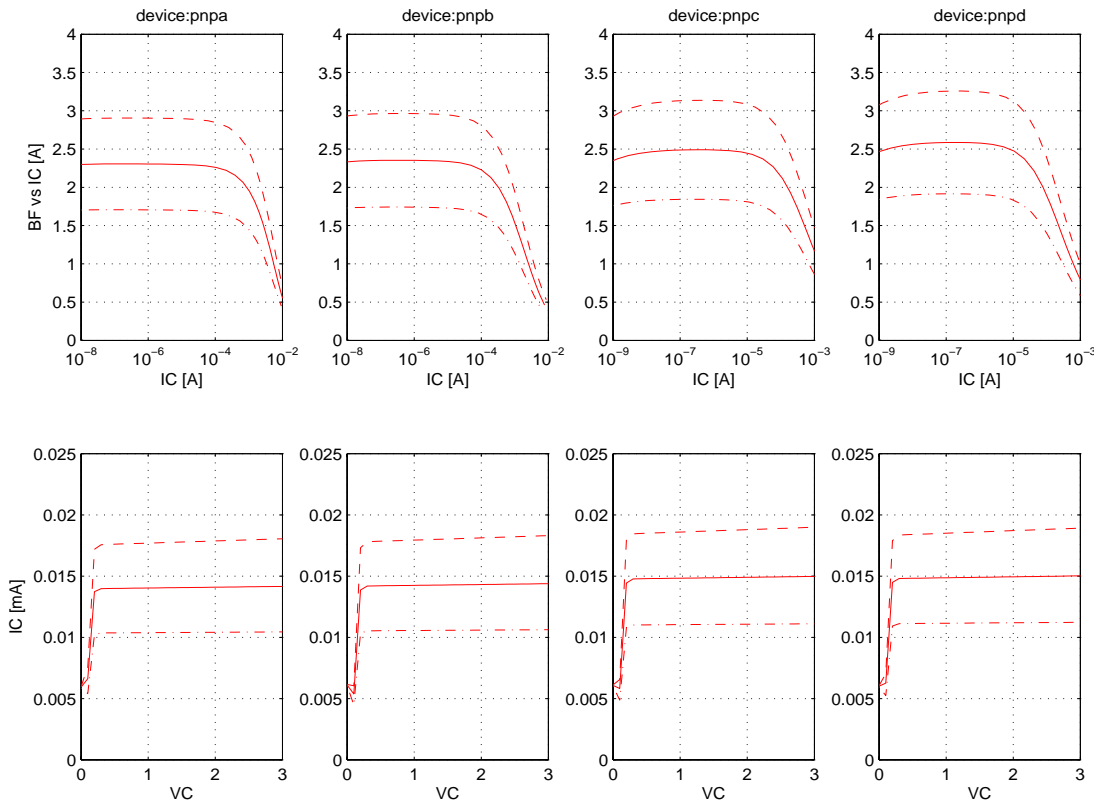
TABLE 9.2 ESPEC, Corner and Statistical Model Comparison for VPNP Model

Device	name	units	slow			nomi			fast		
			Espec	Corner	Stat	Espec	Corner	Stat	Espec	Corner	Stat
PNPa	beta ($I_e=10\mu A$) ¹		1.70	1.70	1.76	2.30	2.30	2.32	2.90	2.90	2.88

PCM notes:

1. PCM and ESPEC share the same limits.

FIGURE 9.4 Vertical PNP Corner Model Performance



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9.4.1 v4.2

TABLE 9.3 VPNP model specific updates in model release version 4.2

v3.4 update	Reason	Impact on user
Reduced peak beta from 2.8 to 2.3	Updated to match new E-spec.	Reduced current gain in simulations

10.0 Diode Models

10.1 Device Description

The CA18 family offers four diodes: **dn** (ndiode), **dn3p3** (n3p3diode), **dp** (pdioes) and **dp3p3** (p3p3diode). Where the names in **bold** refer to the diode device names in CA18QD/PD/HD, while the values in parentheses refer to the naming convention used in all other CA18 variants. Even though the device nomenclature is different, the device physical characteristics are identical. The n(p)diodes and n(p)3p3diodes are sub-circuit extensions of the primitive n(p)diode and n(p)3p3diode diode models for the 1.8v and 3.3v operation, respectively. The sub-circuit extension for the “n”-type diodes consists of a n+ diffusion cathode in a p-well anode with an additional pin for the p-substrate. Similarly, the sub-circuit extension for the “p”-type diodes consists of a p+ diffusion anode in a n-well cathode, along with a third node to contact the p-substrate. It is recommended that the **dp** (pdioes) and **dp3p3** (p3p3diode) sub-circuits, instead of the primitive pdiode and p3p3diode models, be used to ensure correct biasing of the parasitic n-well to p-substrate diodes for the “n”-type diodes. Similarly, it is recommended that the ndioes and n3p3diodes sub-circuits be used for the “p”-type diodes. A schematic illustrating the sub-circuits is shown in Figure 10.1 and a typical layout and cross-section for these diodes is shown in Figure 10.2.

FIGURE 10.1 Schematic illustrating the sub-circuit used to model the junction diodes

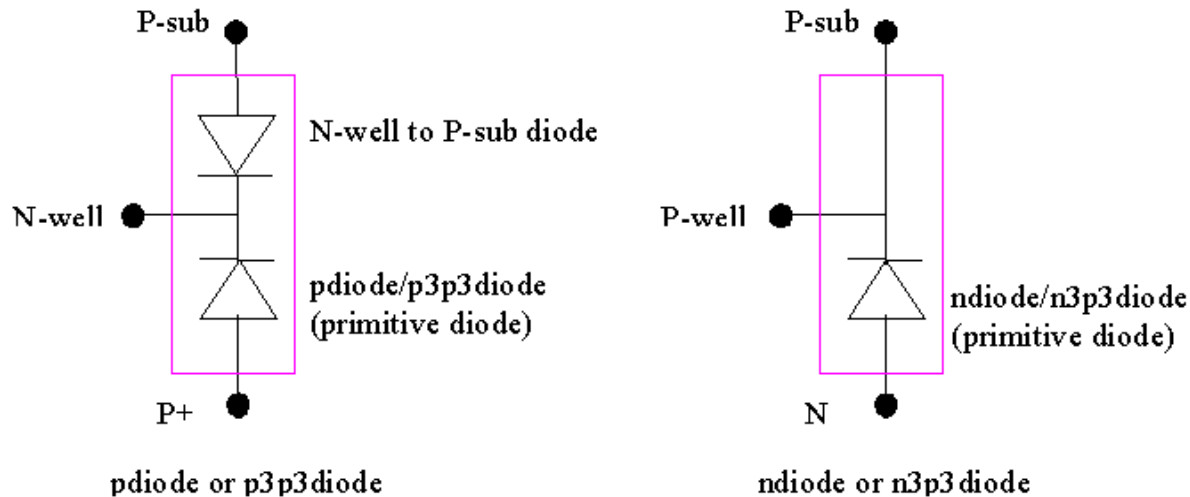
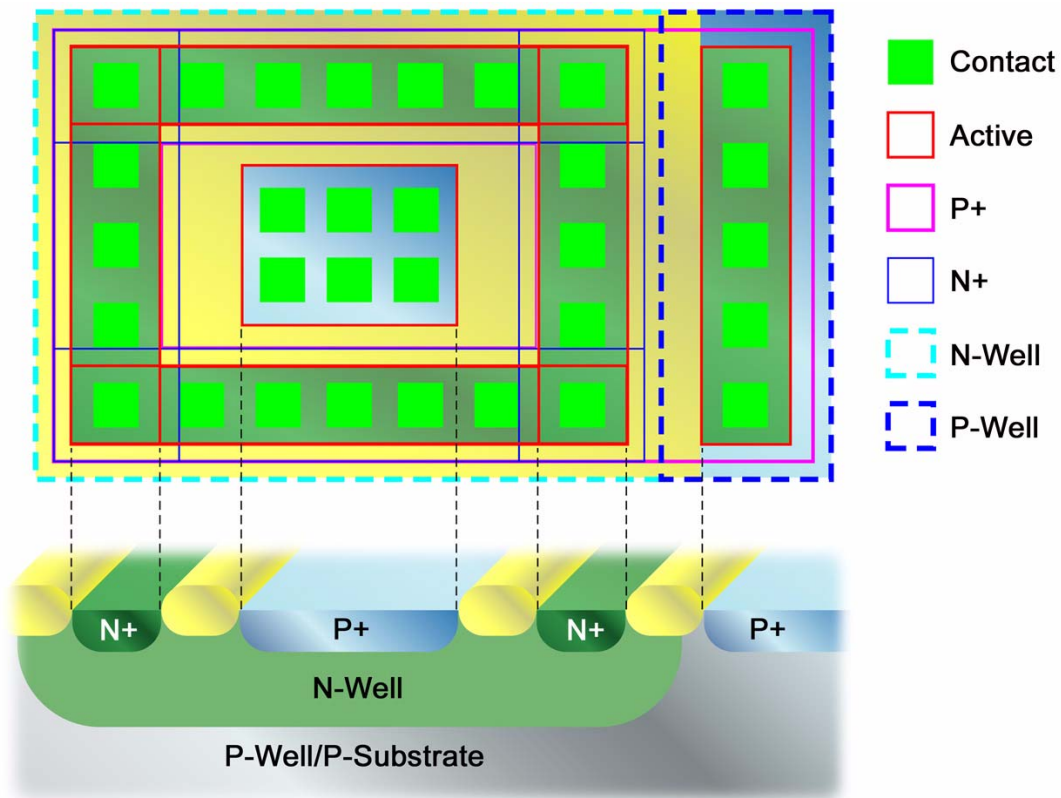


FIGURE 10.2 Layout and cross-section of a typical “p”-type diode



10.2 Model Description and Verification

Spice based diode models are extracted from two different structures. The first is an area intensive structure with $W \times L = 250\mu\text{m} \times 250\mu\text{m}$. The second structure is a perimeter intensive structure with 99 fingers of $W \times L = 1.6\mu\text{m} \times 250\mu\text{m}$. The capacitances were measured via a CV meter @ 100 KHz for reverse biases ranging from 0 to 1.8v for the low-voltage diodes, and from 0 to 3.5v for the high-voltage diodes. The area and perimeter capacitance densities and their bias dependencies were extracted simultaneously from measurements of the two test structures described above. The junction capacitance model is valid for reverse biases from 0 to 1.8v for the low voltage diodes and from 0 to 3.5v for the high voltage diodes, at room temperature. Default temperature coefficients in the diode model allow usage of the model at temperatures ranging from -40 to 125C. The measurements at room temperature along with model playbacks are plotted in Figures 10.3 through 10.6.

Similarly, the diode current as a function of reverse and forward bias was measured for the two flavors of diodes, allowing simultaneous extraction of saturation current densities for the bulk (area) and sidewall (perimeter) components for the forward bias. The junction leakage current for the reverse bias characteristics is not modeled. The dc current diode model is valid up to a 0.6v forward bias and at room temperature. Default temperature coefficients in the diode model allow usage of the model at temperatures ranging from -40 to 125C. The measurements along with model playbacks are shown in Figures 10.7 through 10.10.

10.3 Diode Statistical and Corner Models

The area and perimeter components of the capacitance are varied by to give 3- σ values of +/- 10% based on typical expected variation. The numbers have not been verified through process monitoring or electrical data of ring oscillators. The CA18 ESPEC Document, NPB PS-0173 lists a 20% variation for area components. The junction current is not varied. The junction capacitances nor junction currents are monitored in the PCM.

FIGURE 10.3 Measured junction capacitance and model playbacks for ndiode

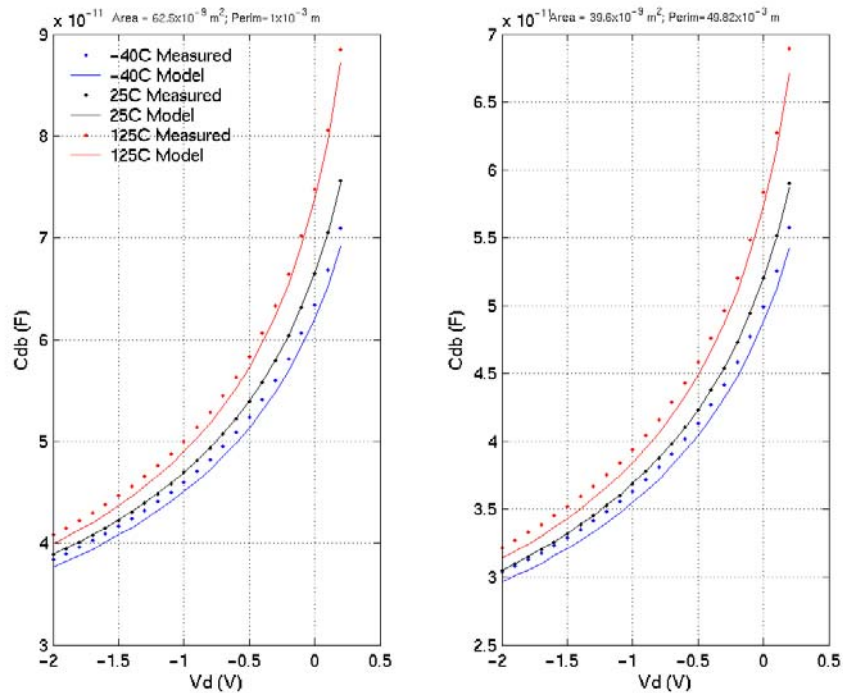


FIGURE 10.4 Measured junction capacitance and model playbacks for pdiode

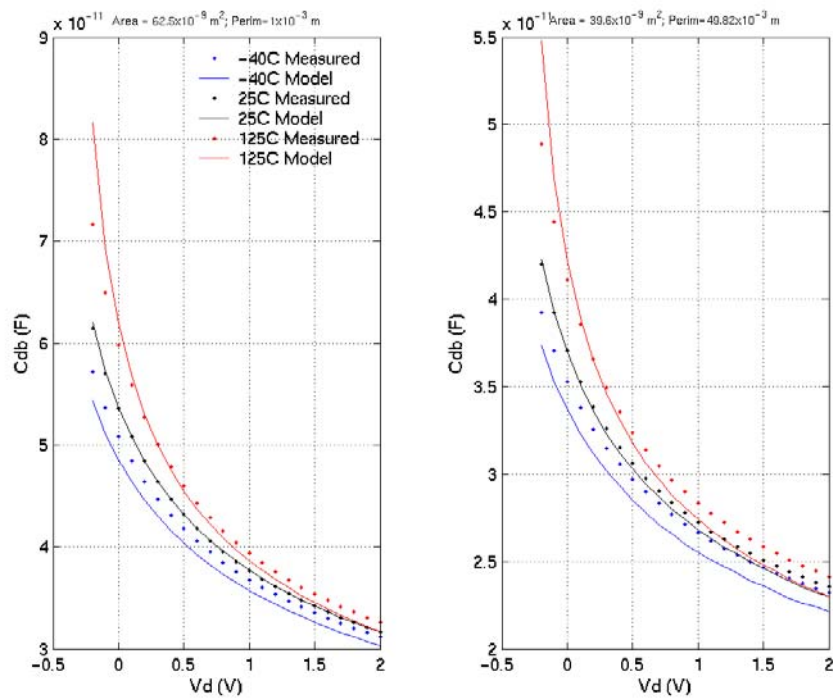


FIGURE 10.5 Measured junction capacitance and model playbacks for n3p3diode

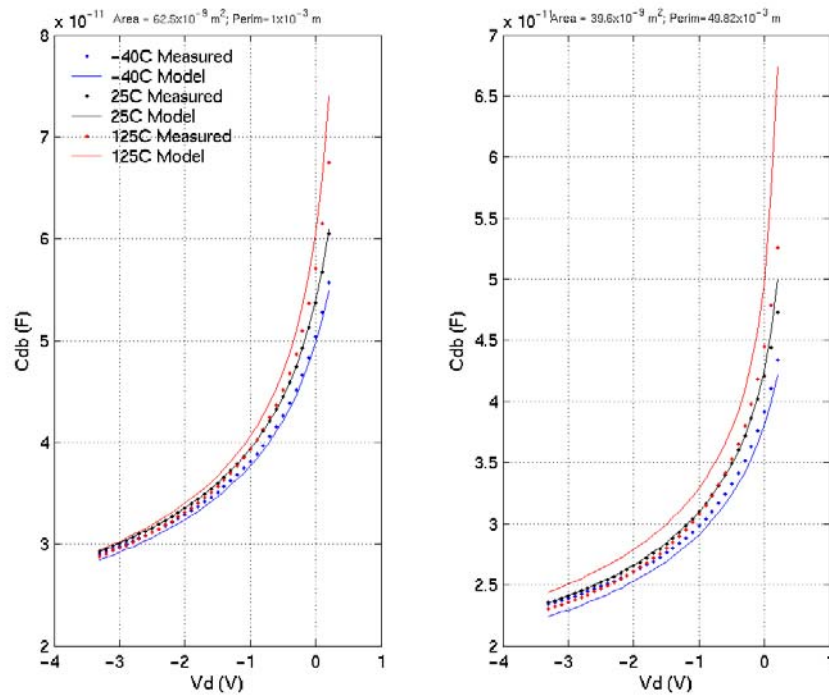


FIGURE 10.6 Measured junction capacitance and model playbacks for p3p3diode

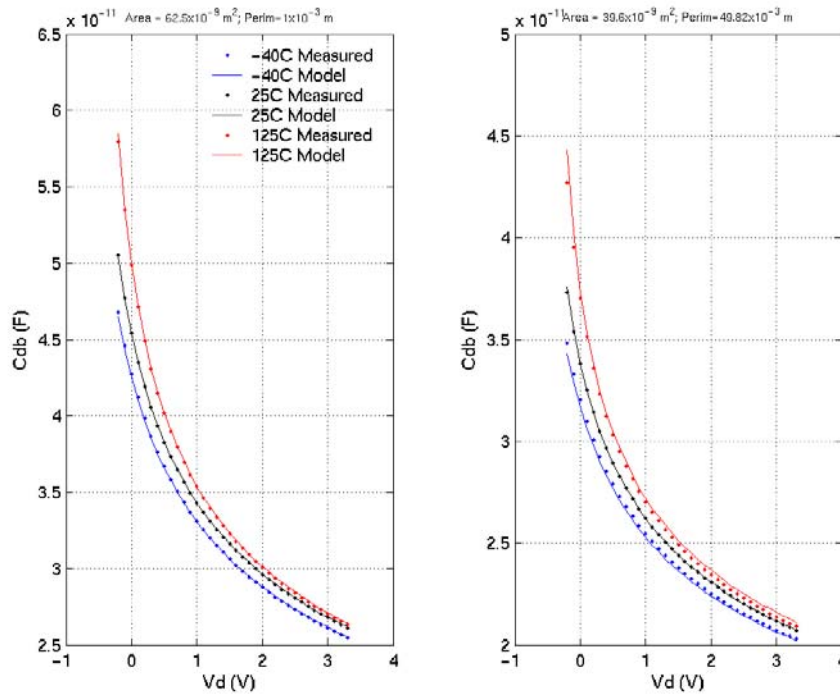


FIGURE 10.7 Measured junction diode current characteristics and model playbacks for ndiode

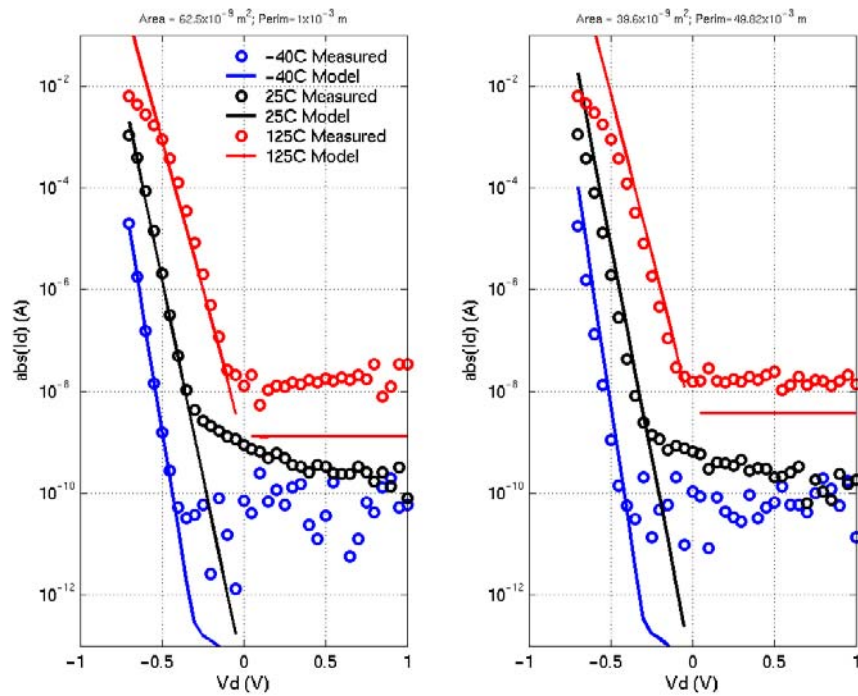


FIGURE 10.8 Measured junction diode current characteristics and model playbacks for pdiode

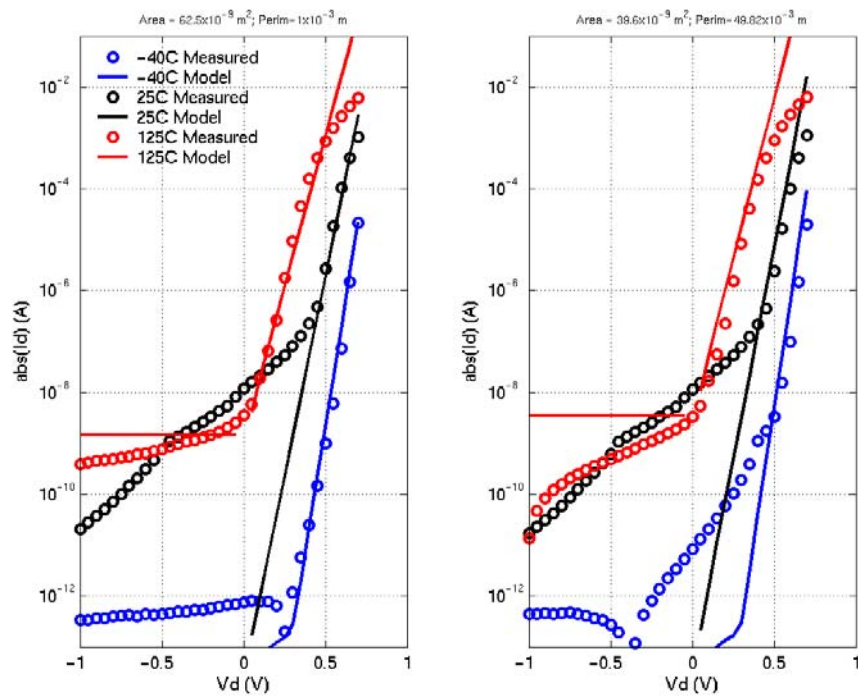


FIGURE 10.9 Measured junction diode current characteristics and model playbacks for n3p3diode

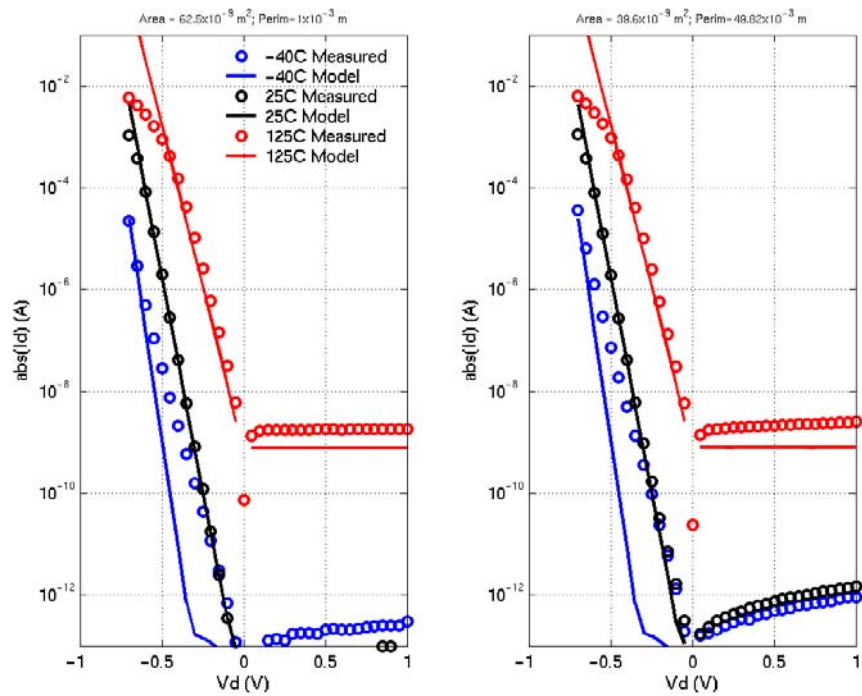
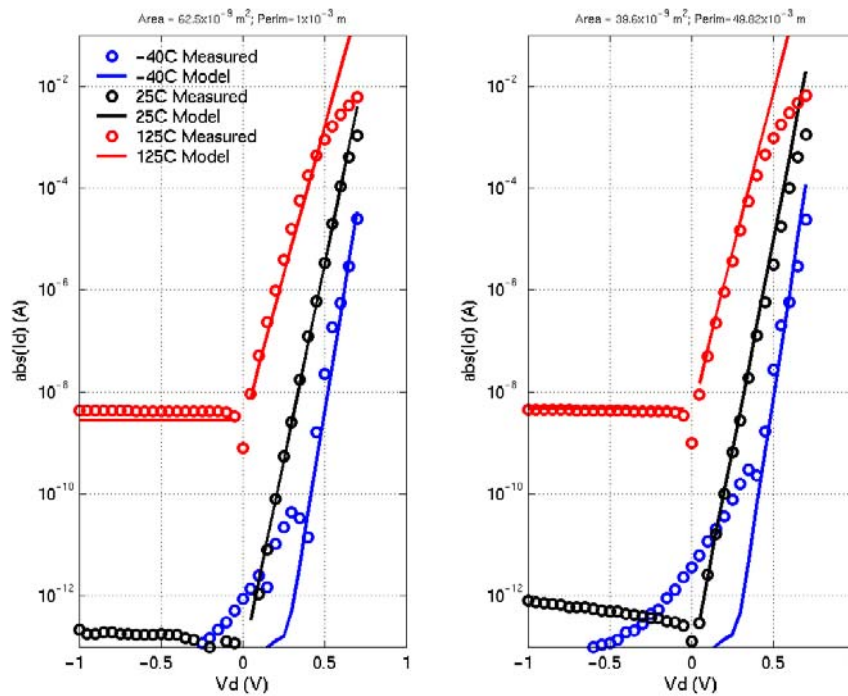


FIGURE 10.10 Measured junction diode current characteristics and model playbacks for p3p3diode



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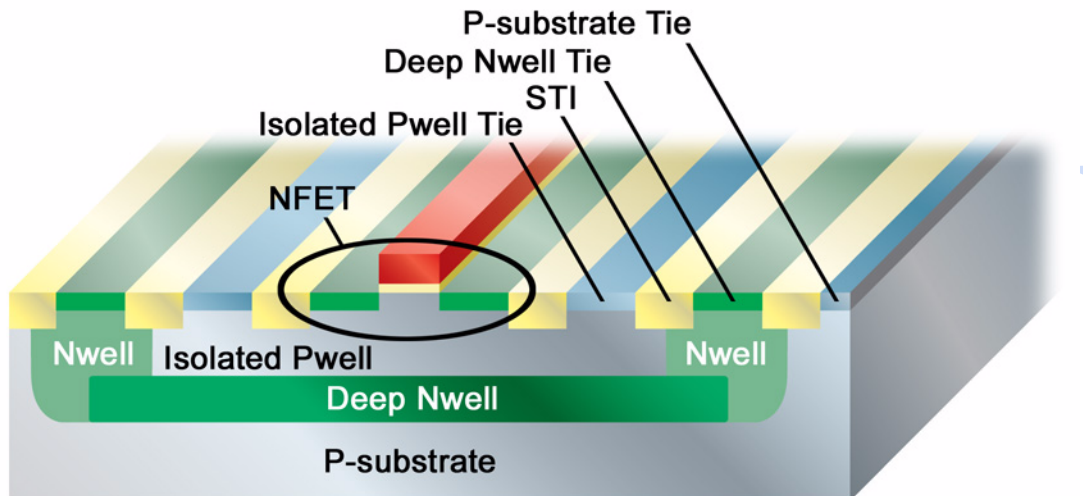
11.0 Deep Nwell

11.1 Introduction

The purpose of this section is to describe the use of the Deep Nwell module to provide additional substrate isolation for nfet_rf library devices. This chapter describes how the Jazz design system accounts for the Deep Nwell process module. This document will cover the modeling, schematic, layout, and verification aspects of this technology. For details on Deep Nwell process availability and specifications please refer to the respective design rules and electrical specification documents.

The current Deep Nwell implementation provides a methodology that allows for robust connectivity and verification and provides a basic model. Among some of the benefits, this methodology allows the designer to bias the isolated Pwell separately from the outer P-substrate. It will also prevent the improper biasing (such as forward bias) of the junctions formed by the Deep Nwell by reporting design rule and LVS violations. Please refer to Figure 11.1 and Figure 11.3 for Deep Nwell silicon cross section, top views, and legend.

FIGURE 11.1 Deep Nwell Silicon Cross Section including isolated NFET.



11.2 Modeling

The addition of Deep Nwell will form two PN junction diodes across the physical circuit area. The Jazz design environment models these junctions as separate diodes **diso** and **ddnw** as seen in Figure 11.2. The first diode **diso** is formed by the Deep Nwell/Nwell to Isolated Pwell junction. The second diode, **ddnw**, is formed by the the P-substrate to Deep Nwell/Nwell junction. Table 11.1 lists the ESPEC and NOM model simulation of the area and perimeter capacitances. Corner and statistical models are not supported. Investigation of the DC and RF effects of the Deep Nwell is given in Section 11.6.

TABLE 11.1 Deep Nwell Diode ESPEC vs. NOM Model

Capacitance	units	Espec	NOM
Pwell to DNW CA ¹	$\mu\text{F}/\text{m}^2$	546.6	546.7
Pwell to DNW CP ¹	nF/m	1.346	1.346
DNW to P-Sub CA ¹	$\mu\text{F}/\text{m}^2$	126.7	126.8
DNW to P-Sub CP ¹	nF/m	3.124	3.122

PCM notes:

1. PCM and ESPEC share the same limits.

11.3 Schematic Entry

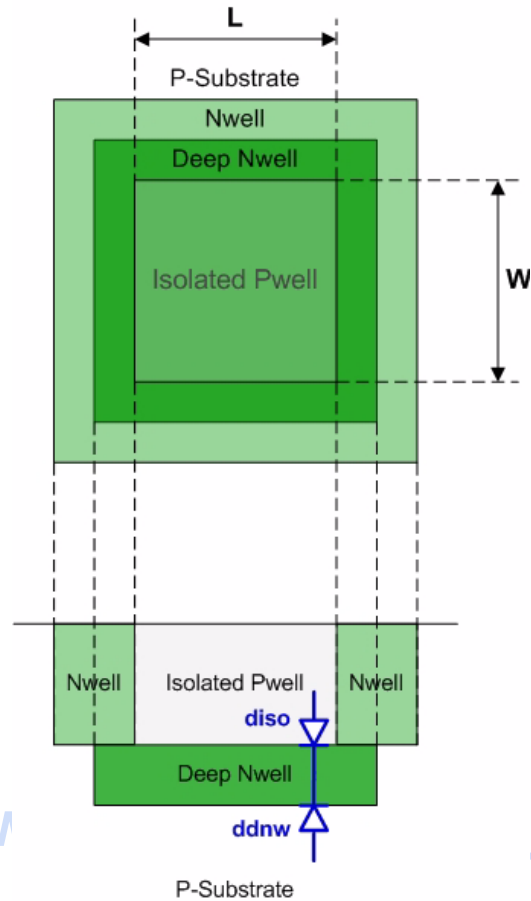
The two diodes, **ddnw** and **diso**, are shown in Figure 11.2.

FIGURE 11.2 ddnw Device Schematic

11.3.1 Device Attributes

The geometry of each of the diodes can be entered by A/P (area and perimeter), L/W (length and width), or A/R (area and aspect ratio). For the **diso**, the geometry is a measure of the isolated Pwell. For the **ddnw**, the geometry is a measure of the drawn deep Nwell layer. Typically these devices can be used during schematic entry and simulation to give an estimate of the Deep Nwell construction.

FIGURE 11.3 Deep Nwell Top view and Cross section



Once layout is completed, the schematic should be updated to reflect the final geometries. Section 10.5.2 will describe how these parameters are included in LVS.

FIGURE 11.4 *ddnw* device attributes

CDF Parameter	Value
Model name	dnw_psub
Specify	<input checked="" type="radio"/> A/P <input type="radio"/> WL <input type="radio"/> A/R
Width	5u M
Length	5u M
Area	25.0p M ²
Perimeter	20u M
Aspect - Ratio	1
Count	1

11.3.2 Connectivity

The **diso** and **ddnw** devices allow the designer to connect and bias the Isolated Pwell and P-substrate independently. By default, the Jazz three terminal FETs come embedded with an inherited substrate connection

“sub_inh” set to “sub”. The value of the sub_inh property may be changed through the object properties page as shown in Figure 11.5. Four terminal FETs allow for more explicit definition of the substrate connection. Finally, for all other devices allowed in deep nwell such as diodes, poly resistors, and capacitors, the user may edit the **Substrate Node** property directly through the CDF.

FIGURE 11.5 How to define a FET substrate name

The screenshot shows the 'Edit Object Properties' dialog box with the following sections:

- Buttons:** OK, Cancel, Apply, Defaults, Previous, Next, Help.
- Apply To:** only current (selected), instance.
- Show:** ☐ system, ☒ user, ☒ CDF.
- Property Table:**

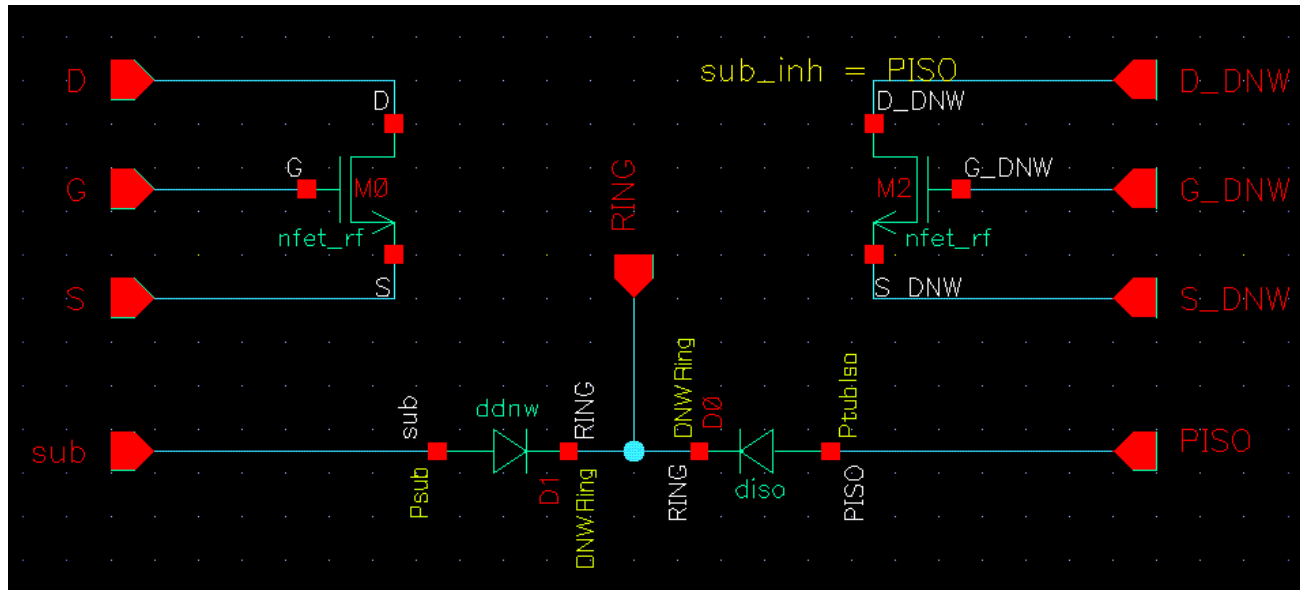
Property	Value	Display
Library Name	sbcl8pt	off
Cell Name	nfet_rf	value
View Name	symbol	off
Instance Name	M2	off
- User Property Table:**

User Property	Master Value	Local Value	Display
sub_inh		PISQ	off
- CDF Parameter Table:**

CDF Parameter	Value	Display
Model Name	nfet_rf	off
Substrate Node	PISQ	off

Figure 11.6 illustrates the schematic view of two NFET transistors. The right hand side NFET (M2) will be placed over Deep Nwell, while the left hand side device (M0) will be placed over P-substrate. The schematic also shows how the ddnw device can be properly connected to each transistor.

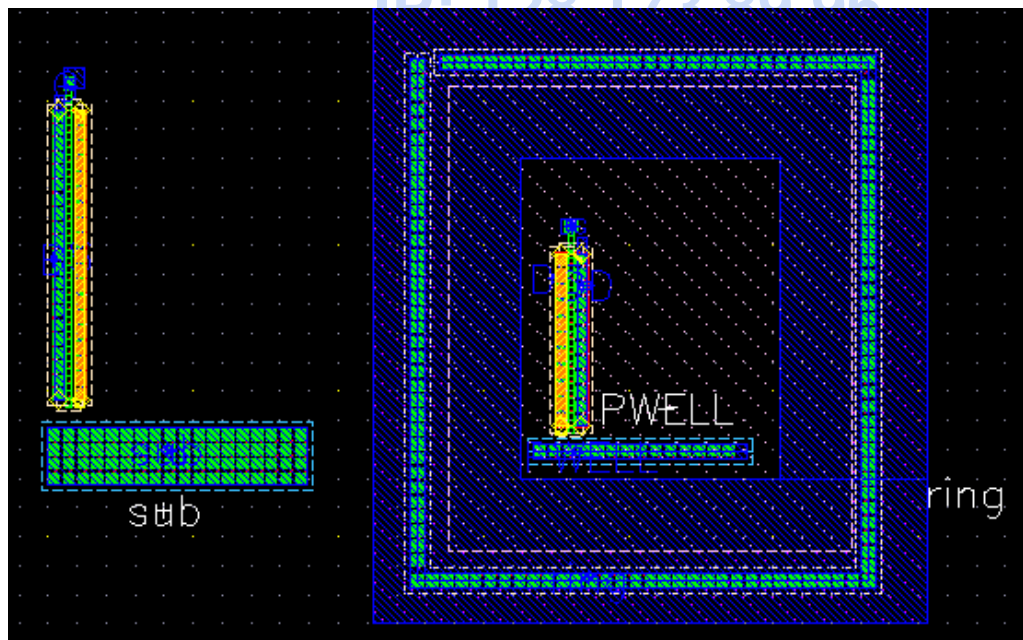
FIGURE 11.6 Deep Nwell connectivity example



11.4 Layout

The Deep Nwell (Cadence layer “dnw”, number 36) can be drawn around a circuit block or an element. At this point, no layout view is provided to generate the Deep Nwell/Nwell ring structure. The user must draw the Deep Nwell, Nwell layers, and ntap and ptap contacts when applicable. The figure below pictures the layout view of the example given in the proceeding section.

FIGURE 11.7 Deep Nwell layout example



11.5 Verification

11.5.1 Design Rules

Please refer to the design rule document for complete details.

11.5.2 LVS

The LVS routine will check for accurate connectivity matching. In addition, the LVS deck provides the “**CompareDnwDiode**” switch. Once enabled, this switch will trigger the comparison of the **Area** and **Perimeter** properties defined in the **ddnw** and **diso** schematic elements with the physical properties, as defined by layout, of the Isolated Pwell.

11.6 RF and DC Measurement Validation

The deep n-well structure can greatly improve the device isolation from substrate. On the modeling side, in order to provide an accurate RF SPICE model, the impact on both DC and RF performance from the deep n-well must be studied. This section focuses on the impact of deep n-well on the CMOS transistor using the **nfet** device in the Jazz 0.18 μ m CMOS as a test case.

11.6.1 Test Structure and Experiment Description

Test structures are fabricated in order to compare the DC and RF performance of deep nwell and standard devices. Table 11.2 lists the 4 types of tests along with test structure description and WELL connections. For all tests, the *gate* is port 1, the *drain* is port 2, and the *source* is connected to ground of the GSG probe.

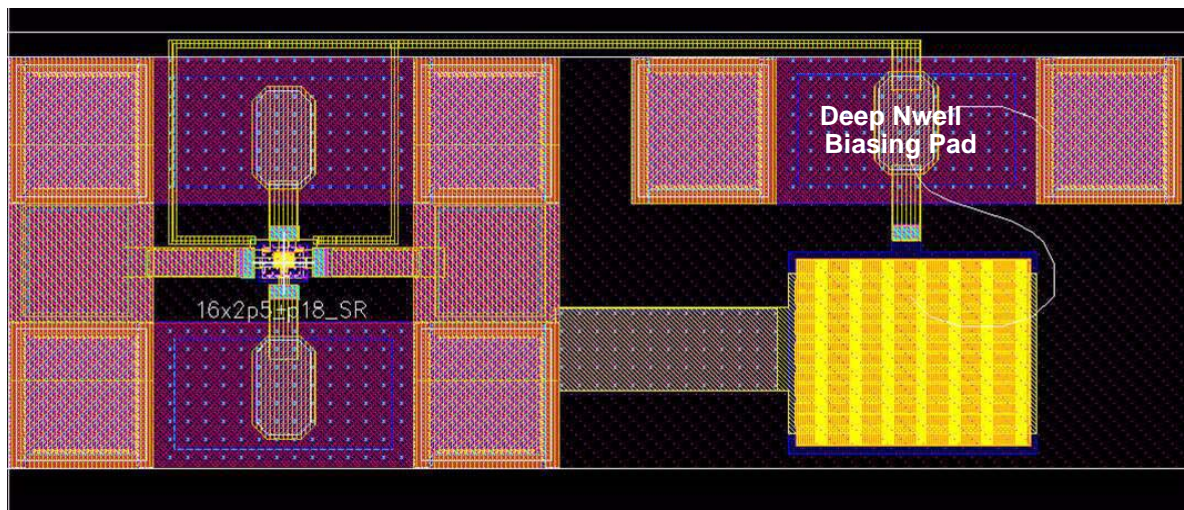
TABLE 11.2 Test Descriptions

Test Name	Test Structure Description	PWELL	Deep Nwell	P-Sub
<i>NDNW</i>	standard device in P-Substrate	G (of GSG)	NA	G
<i>DNWA</i>	deep Nwell device with isolated PWELL, deep Nwell, and P-Substrate all tied to ground of GSG.	G	G	G
<i>DNWB</i>	deep Nwell device with isolated PWELL and P-Substrate all tied to ground of GSG. Deep Nwell connected to separate DC bias with large de-coupling capacitor.	G	0 V	G
<i>DNWB3</i>	deep Nwell device with isolated PWELL and P-Substrate all tied to ground of GSG. Deep Nwell connected to separate DC bias with large de-coupling capacitor.	G	3 V	G

The DC and S-parameters are measured at different bias conditions. For the RF characterization, the measured raw S-parameters are de-embedded from the *Open* and *Short* S-parameters. After the de-embedding,

the Y-parameters are plotted against frequency. We compared Y-parameters with *NDNW* vs. *DNWA*, *DNWA* vs. *DNWB*, and *DNWB* vs. *DNWB3*. The purpose of the *DNWA* vs. *DNWB* comparison is to verify that the DC biasing scheme for the deep Nwell is correct. The Y-parameters for these two cases should be identical since the deep Nwell is grounded in both. The purpose of the *DNWB3* test is to investigate any “pinching” effects of the depletion region into the isolated PWELL. In normal circuit operation, the deep Nwell is biased to the VDD of the circuit. This test will illuminate any requirement to modify the substrate network in the RF MOSFET model for deep Nwell devices. Figure 11.8 shows the layout for the *DNWB* and *DNWB3* measurements. A GSGGSG probe is used to contact the deep Nwell and *drain* at port 2, assuring consistent DC and AC grounding.

FIGURE 11.8 DNWB Layout



11.6.2 DC Measurements and Analysis

In all 4 cases the DC Output characteristic are measured. The bias conditions are listed Table 11.3.

TABLE 11.3 DC Measurement Conditions

Sweep	Start	Stop	Step
VD	0	1.8	0.05
VG	0	1.8	0.3
VS	0	0	0
VB	0	0	0

In the case of *DNWB* and *DNWB3*, additional DC biases of $V_{dnw}=0$ and $V_{dnw}=3V$ are applied respectively to the Deep Nwell to monitor the change of the drain current I_d and output conductance g_{ds} . The output conduc-

tance g_{ds} is derived numerically from the drain current data where a small step = 50mV is applied to keep the g_{ds} smooth. The DC measurement is performed by the Agilent E5270A parametric Measurement Unit.

Figure 11.9 compares the *NDNW* and *DNWA* drain current I_d and output conductance g_{ds} . Figure 11.10 shows a zoom in of the output conductance. The differences seen are on the same order of measurements on exact devices (both without deep Nwell) in different die. Therefore the differences can be attributed to process variation. Furthermore, comparisons of *DNWB* and *DNWB3* yield the same results as expected.

FIGURE 11.9 NDNW vs. DNWA Drain Current I_d

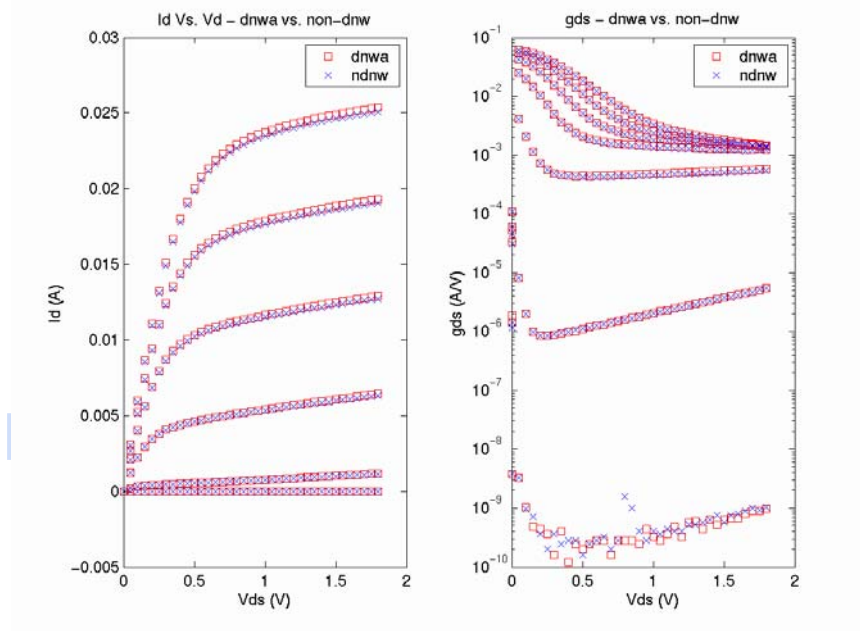
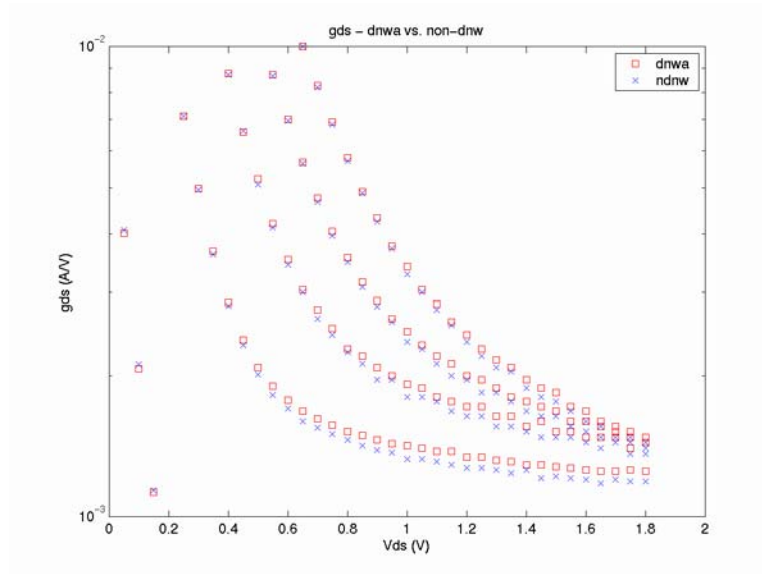


FIGURE 11.10 NDNW vs. DNWA Output Conductance gds



At $V_G=0.9$, $V_D=1.8$, $\Delta g_{ds}=15\%$

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11.6.3 Y-parameter Measurements and Analysis

S-parameter measurements are performed by the Agilent network analyzer E8376B with the frequency sweep from 100MHz to 10.1 GHz. Two step, open-short de-embedding is performed and the results converted to Y-parameters. The DC bias conditions are listed in Table 11.4. Figure 11.9 through Figure 11.10 display the *NDNW* vs. *DNWA* comparisons for a device with $NF_xW_{gx}L_g=16 \times 2.5 \times 0.18$. The expected potential difference is in $Real(Y_{22})$ where the bulk resistance affects the high frequency data. At low frequencies, $Real(Y_{22})$ is proportional to g_{ds} . The shifts in $Real(Y_{22})$ can be attributed to the difference in the DC output conductance shown in Figure 11.11. Similarly, shifts in the $Real(Y_{21})$ are a result of small differences in the transconductance g_m . The Y-parameters are all close in value and frequency dependence except for $Real(Y_{11})$ and $Real(Y_{12})$ whose values are all close to the dynamic range limit of the NWA¹. It was also discovered that there are minor differences between the gate connection in the layout between the *NDNW* and *DNWA* which can be amplified when operating close to the dynamic range limit. Figure 11.13 through Figure 11.15 show the Y-parameter *NDNW* vs. *DNWA* comparisons for a device with $NF_xW_{gx}L_g=16 \times 2.5 \times 0.3$. All the Y-parameters

1. Improved test structures are under development to eliminate measurement error seen in $Real(Y_{11})$ and $Real(Y_{21})$.

match, including $Real(Y_{11})$ and $Real(Y_{12})$, whose values are now well above the dynamic range limit due to the increased channel resistance.

To investigate the effects of applying a DC bias to the deep Nwell, the test structures previously described in Figure 11.8 are measured. The first step is to ensure the measurements are accurate. This is achieved by comparing a 0V bias applied to the deep Nwell (*DNWB* test) with the hard wired ground applied to the deep Nwell (*DNWA* test). Figure 11.16 shows the comparison where the Y-parameters are the same except for slight differences in conductances due to different devices. The scale of the plot is very small, thus the differences are very small. The next step is to apply a DC bias of 3V to the deep Nwell (*DNWB3*). Figure 11.17 shows the *DNWB* vs. *DNWB3* comparison where the Y-parameters are exact (no DC difference since the measurements are performed on the same device).

TABLE 11.4 DC Measurement Conditions for S-parameter Sweeps

	VG	VD
<i>sweep 1</i>	1.8	0
<i>sweep 2</i>	0.9	1.8
<i>sweep 3</i>	1.8	1.8

11.6.4 Conclusions

The experiments performed show that the deep Nwell has no influence on the DC or RF performance of the *nfet* devices. Therefore, the MS and RF models are not altered in the presence of deep Nwell. The junction isolation effects of the deep Nwell and added terminals are modeled by the *ddnw* component as described in Section 11.2.

FIGURE 11.11 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=0$, $V_g=1.8\text{V}$

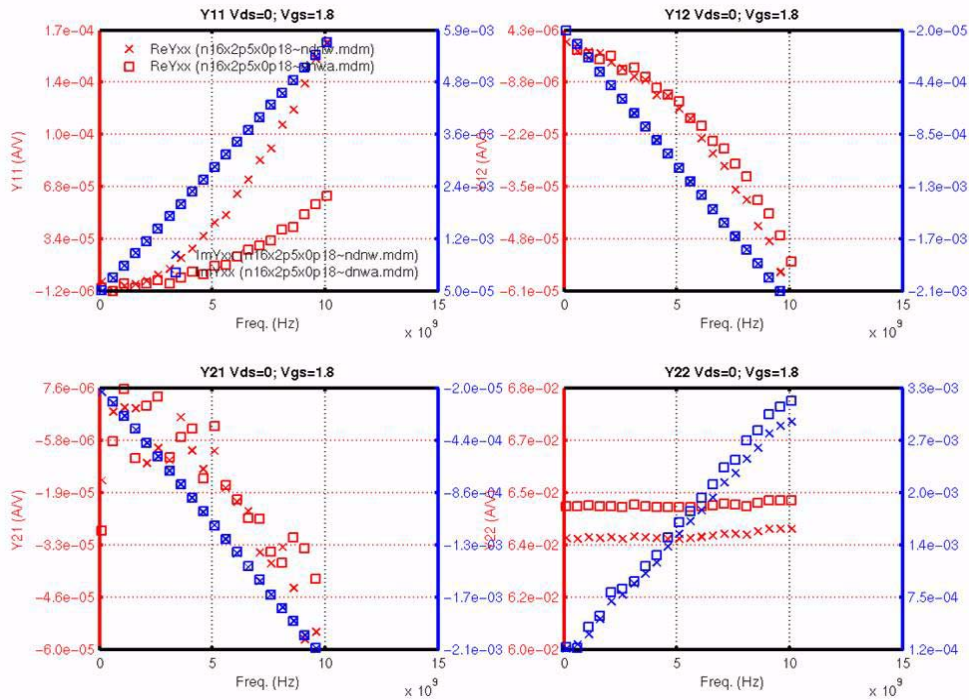


FIGURE 11.12 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$

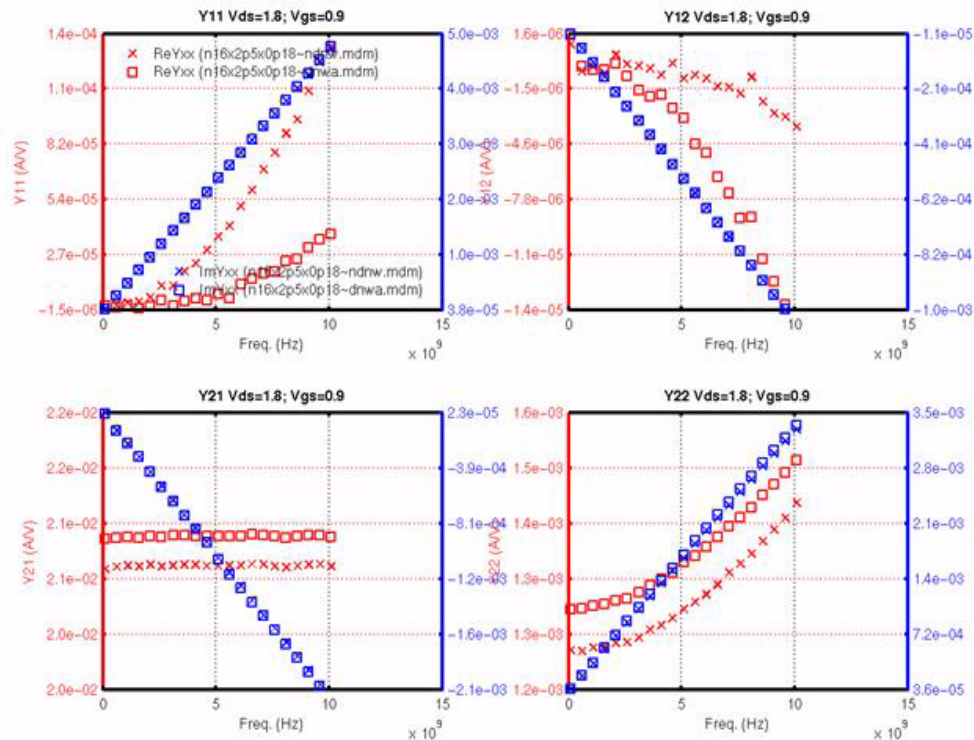


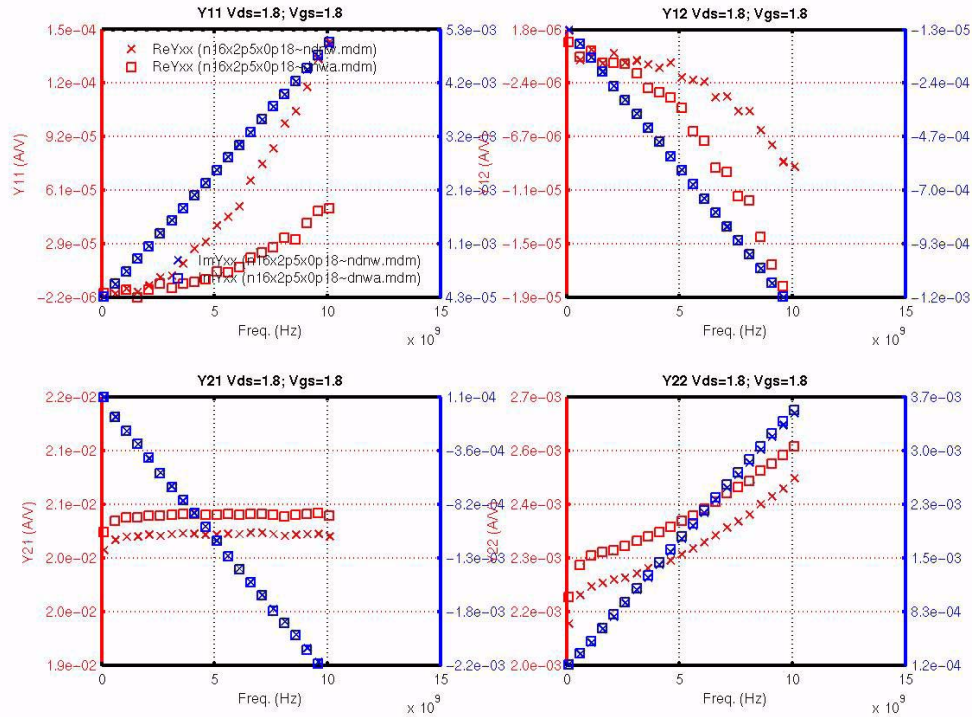
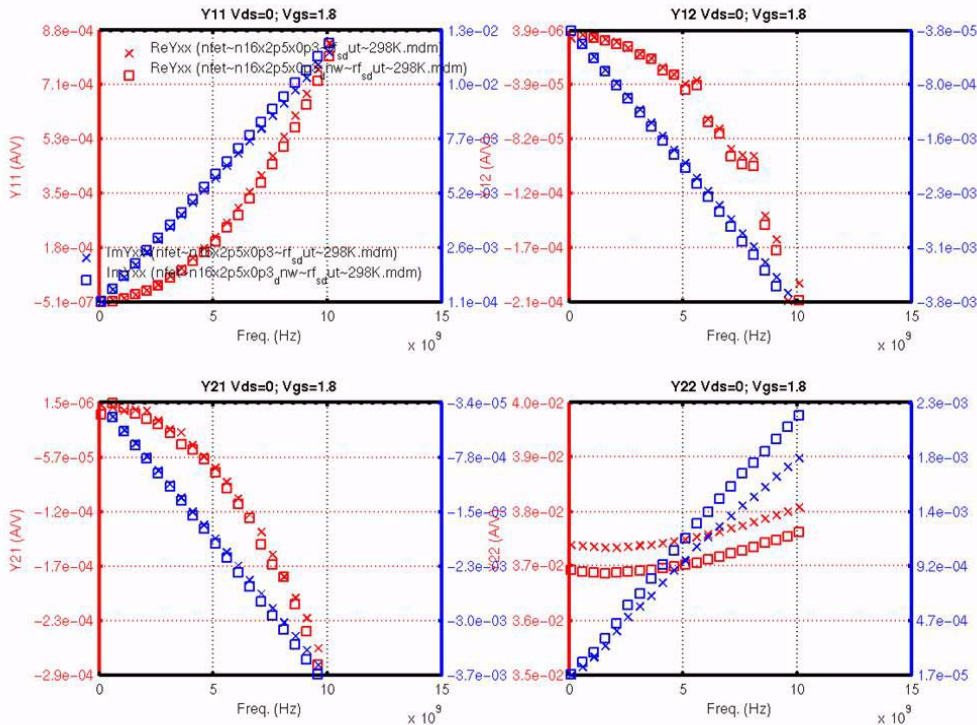
FIGURE 11.13 $W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=1.8\text{V}$ FIGURE 11.14 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=0$, $V_g=1.8\text{V}$ 

FIGURE 11.15 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$

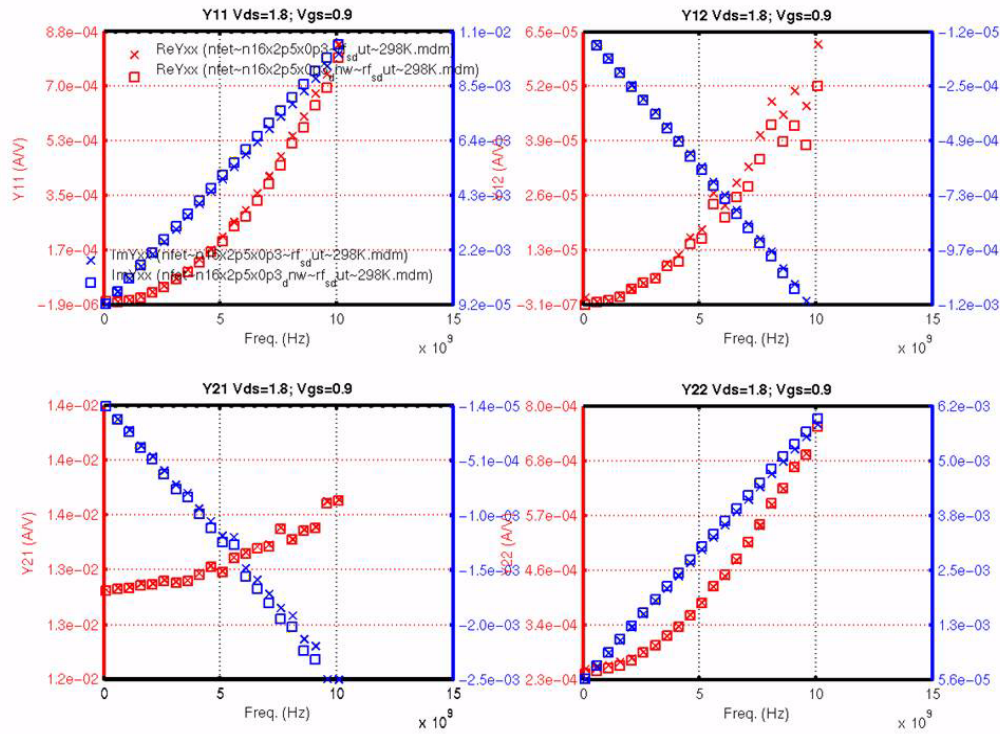


FIGURE 11.16 $W_g=2.5\mu\text{m}$, $L_g=0.3\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=1.8\text{V}$

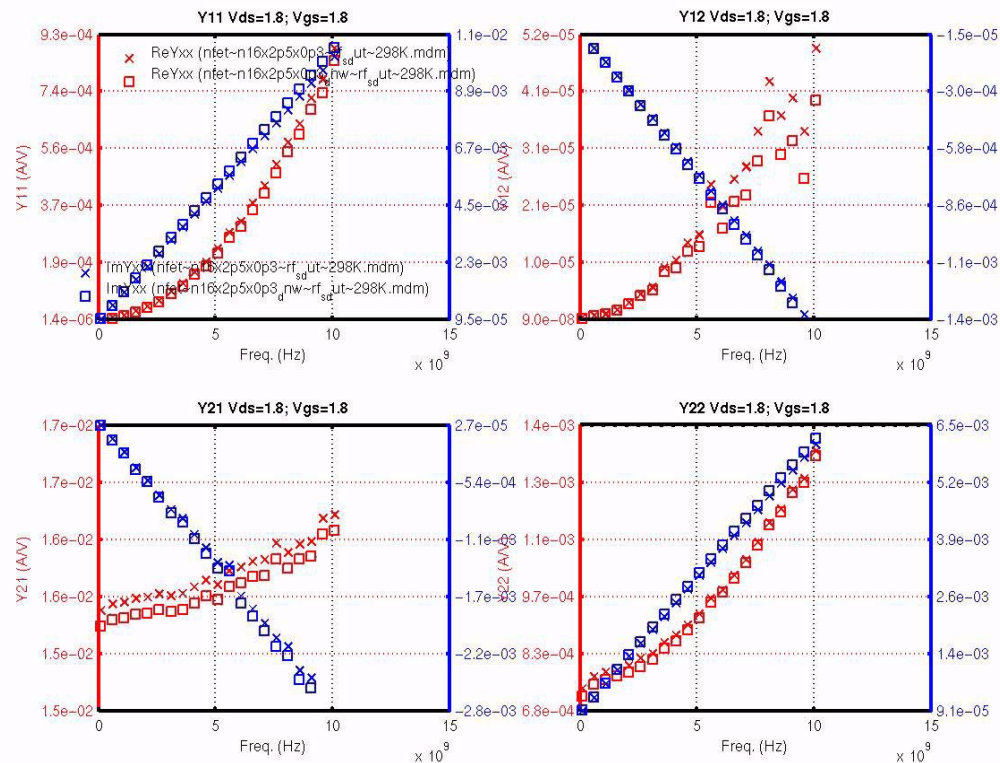
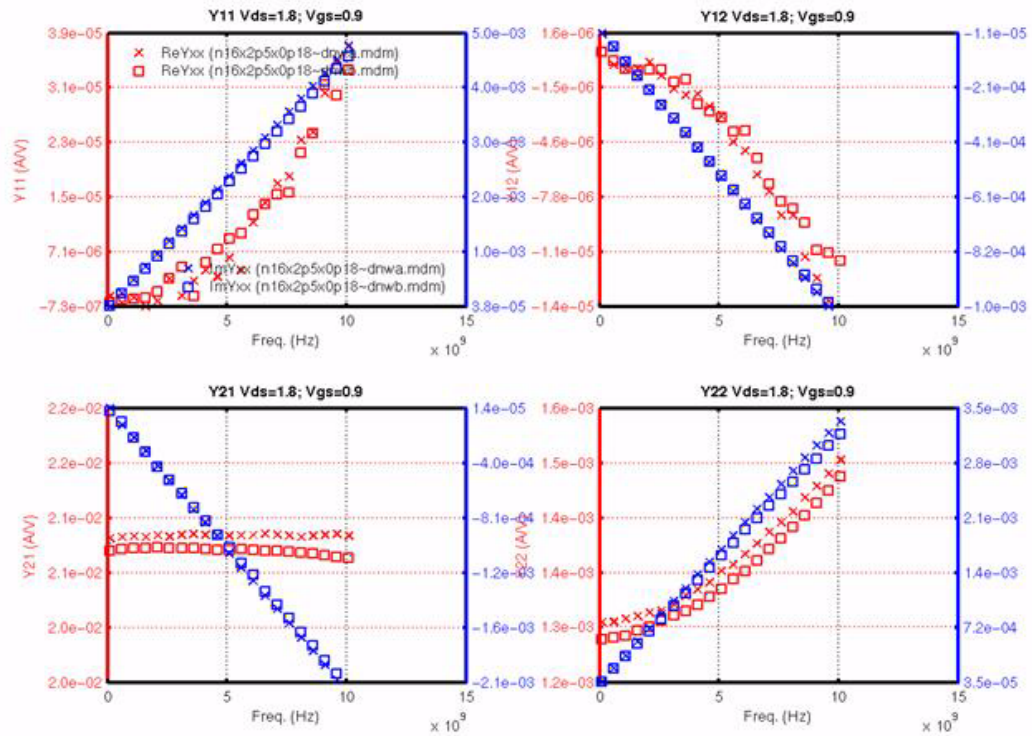
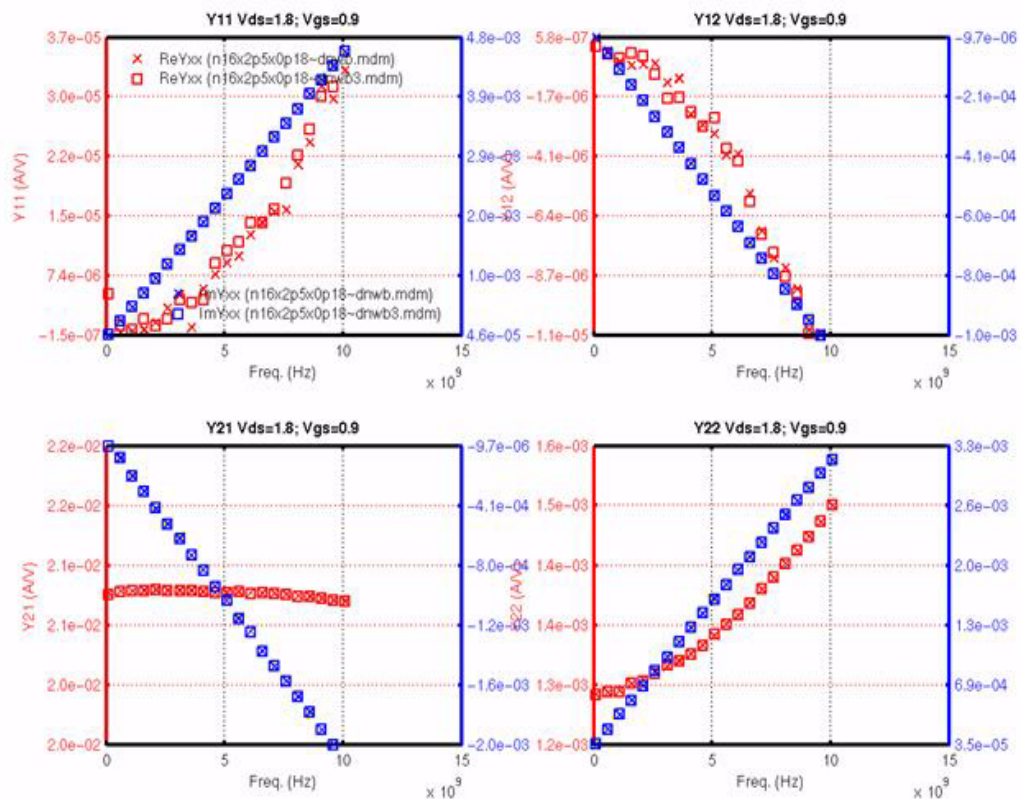


FIGURE 11.17 DNWA vs. DNWB ($W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$)FIGURE 11.18 DNWB vs. DNWB3 ($W_g=2.5\mu\text{m}$, $L_g=0.18\mu\text{m}$, $NF=16$, $V_d=1.8\text{V}$, $V_g=0.9\text{V}$)

12.0 X-Sigma Corner and Statistical Models

12.1 X-Sigma Corner Models

X-Sigma corner models allow for process variation settings different than conventional corner models which typically set the process variation to worst case ± 3 sigma. Process sigmas, classified into device classes, are variable inputs. In their limits, the X-Sigma models align to the limits of the ESPECs. The ESPECs limits are mostly aligned with the PCM limits. Typically, the process may run tighter than the PCM limits. Combined with PCM data tracking, the X-Sigma models allow design to a more aggressive process variation than is predicted by the ESPECs. The added flexibility provides for direct insight into circuit sensitivities previously hidden by the fixed corner settings.

12.1.1 Device Correlation

The X-Sigma models provide 100% correlation among device types. Table 12.1 shows the device class groupings and the related independent process variables which fall under their control. The individual devices are listed in the horizontal axis of the table. Table entries indicate variation caused by the given process variable on the particular device. When a process variable affects more than one device type, a judgement is made on the relative significance of the process variable. This in turn determines which class controls the sigma variation. A master slave approach is used where the secondary device, or slave device, follows the variation determined by the master device.

The GLOBAL device class contains dominant process variables which affect a variety of devices. The variables move according to FET conventions. In order to see the full process swing on some devices, a combination of device class sigmas must be set. For example to achieve the slowest NFET, one would set GLOBAL and NFET X-Sigma to -3. Table 12.2 provides the X-Sigma numbers by device class to achieve worst case performance for each individual device. To achieve best case performance, the X-Sigma numbers are multiplied by -1.

12.1.2 Design Kit Implementation

Figure 12.1 shows the Cadence analog environment implementation of the X-Sigma models. Entry fields for the sigma number are given for each device class. The legacy corner model buttons are listed for backward compatibility and can not be used in unison with the X-Sigma or STAT models. Once X-Sigma is selected for a device class, all device classes are switched to X-Sigma. When the X-Sigma models are chosen, the device class sigma variables become design variables as shown in the Figure 12.1. Users are then free to access these variables within the environment, enabling custom parametric sweeping for example. Figure 12.2 shows an example VCO circuit and plots resulting from a sweep of the FET global sigma with a parametric CAP global sigma sweep.

TABLE 12.1 X-Sigma Model Matrix

Device Class	Independent Process Variables	Device																
		N F E T	P F E T	5 / 1 2 N L D M O S	5 / 1 2 P L D M O S	5 / 4 0 N L D M O S	5 / 4 0 P L D M O S	H V P O L Y R E S	L V P O L Y R E S	S A L P O L Y R E S	N W E L L R E S	M O S V A R	J U N C V A R	M I M	I N D	L P N P	V P N P	H V N P N
GLOBAL (+ values give Fast Fets)	active CD	✓	✓	✓	✓	✓	✓											
	tox	✓	✓	✓	✓	✓	✓					✓						
	poly CD	✓	✓	✓	✓	✓	✓	✓	✓	✓								
	substrate doping			✓		✓							✓					
NFET	NFET channel doping	✓		✓		✓												
	NFET flatband voltage	✓		✓		✓												
	NFET short channel body effect	✓																
	NFET short channel Vt	✓																
	NFET body constant	✓																
	NFET narrow width effect on VT	✓																
	NFET body effect of k3	✓																
	NFET Idd impact on Leff	✓		✓		✓												
	NFET Idd impact on Rds	✓																
	NFET low field mobility	✓		✓		✓												
	deep nwell doping				✓		✓											
	pwell doping				✓													
PFET	PFET channel doping		✓		✓		✓					✓						
	PFET flatband voltage		✓		✓		✓					✓						
	PFET 2nd order body constant		✓															
	PFET narrow width effect on VT		✓															
	PFET body effect of k3		✓															
	PFET Idd impact on Leff		✓		✓		✓											
	PFET Idd impact on Rds		✓															
	PFET low field mobility		✓		✓		✓											
	PFET short channel Vt		✓															
	nwell doping			✓							✓		✓			✓	✓	
	nwell cd										✓							
	nwell end resistance										✓	✓	✓					
HV NLD MOS	HV nwell doping					✓											✓	
HV PLD MOS	HV pwell doping						✓										✓	

TABLE 12.1 X-Sigma Model Matrix

Device Class	Independent Process Variables	Device																
		N F E T	P F E T	5 / 1 2 N L D M O S	5 / 1 2 P L D M O S	5 / 4 0 N L D M O S	5 / 4 0 P L D M O S	H V P O L Y R E S	L V P O L Y R E S	S A L P O L Y R E S	N W E L L R E S	M O S V A R	J U N C V A R	M I M	I N D	L P N P	V P N P	H V N P N
HVRES	high value poly doping							✓										
	high value poly end resistance							✓										
LVRES	low value poly doping								✓									
	low value poly end resistance								✓									
SALRES	salicide sheet resistance									✓								
	salicide end resistance									✓								
CAP	sti thickness							✓	✓	✓								
	MiM tox (area cap)													✓				
	MiM peripheral cap													✓				
IND	ILD thickness													✓	✓			
	metal thickness													✓	✓			

Notes:

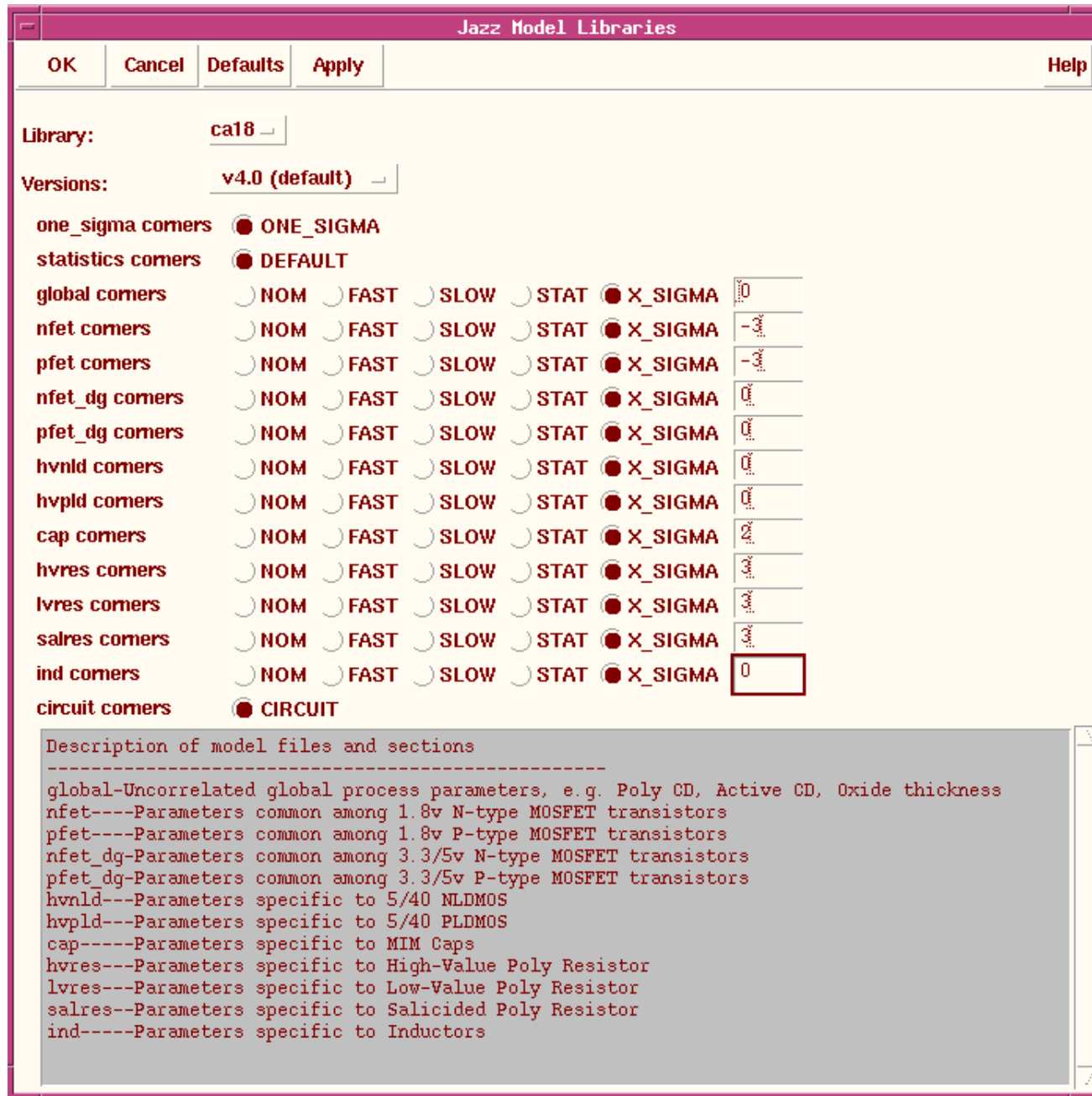
1. X-sigma support for the 5/12 LDMOS is not currently supported, but will be added in model v4.1. There is no x-sigma or statistical model support for 1.8v native fet, 3.3v LDMOSs (nfet3p3_id, pfet_3p3_id), and high performance pnps (vpnp_hp)
2. Details for 3.3v and 5.0v (DG) N and PFETs are not explicitly shown, but qualitatively follow the 1.8v N and P FETs shown in the Table 12.1

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TABLE 12.2 X-Sigma Numbers to Achieve Worst Case Devices

		Device Class									
Device	Figure of Merit	GLOBAL	NFET	PFET	HV NLD MOS	HV PLD MOS	HV RES	LV RES	SAL RES	CAP	IND
NFET	low I_{dsat} , high V_t	-3	-3								
PFET	low I_{dsat} , high V_t	-3		-3							
5/12 NFET	low I_{dsat} , high V_t , high R_{DSon}	-3	-3	-3 Rdrift, low nwell doping							
5/12 PFET	low I_{dsat} , high V_t , high R_{DSon}	-3	-3 Rdrift low pwell doping	-3							
5/40 NFET	low I_{dsat} , high V_t , high R_{DSon}	-3	-3		-3 Rdrift, low hvnwell doping						
5/40 PFET	low I_{dsat} , high V_t , high R_{DSon}	-3		-3		-3 Rdrift, low hvpwell doping					
HV Poly Res	High Res	3					-3				
LV Poly Res	High Res	3						-3			
Sal Poly Res	High Res	3							-3		
Nwell Res	High Res			3							
MOS Var	High Cap	-3	-3	-3							
Junction Var	High Cap			-3							3
VPNP	Low I_c , Low Beta				3 high hvnwell doping						
LPNP	Low I_c , Low Beta			-3							
HVNPN	Low I_c , Low Beta					3 high hvpwell doping					
MIM Cap	High Cap									-3	
Inductor	High Inductance and low Q										-3

FIGURE 12.1 JAZZ Design Kit Model Library Selection Form



Jazz Model Libraries

OK Cancel Defaults Apply Help

Library:

Versions:

one_sigma comers ☒ ONE_SIGMA

statistics comers ☒ DEFAULT

global comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

nfet comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

pfet comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

nfet_dg comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

pfet_dg comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

hvnld comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

hvpld comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

cap comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

hvres comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

lvres comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

salres comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

ind comers ☐ NOM ☐ FAST ☐ SLOW ☐ STAT ☒ X_SIGMA

circuit comers ☒ CIRCUIT

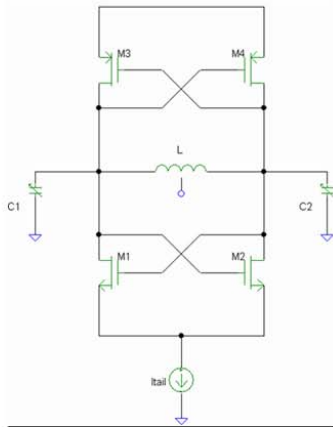
Description of model files and sections

```

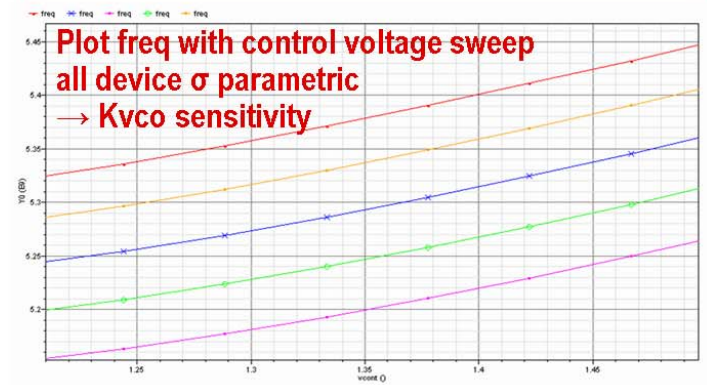
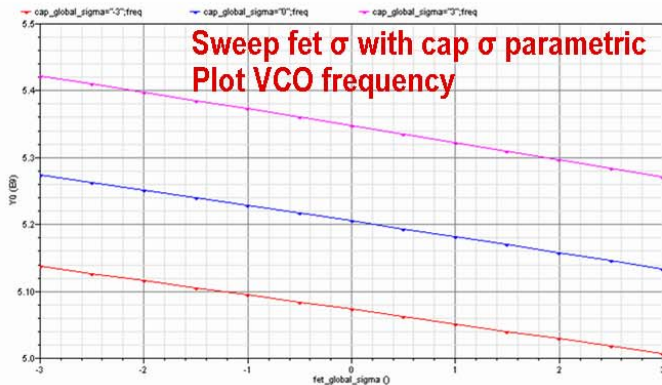
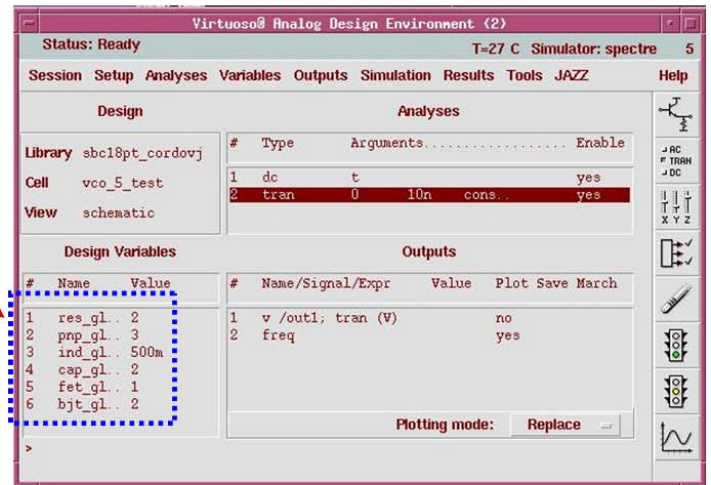
-----
global-Uncorrelated global process parameters, e.g. Poly CD, Active CD, Oxide thickness
nfet----Parameters common among 1.8v N-type MOSFET transistors
pfet----Parameters common among 1.8v P-type MOSFET transistors
nfet_dg-Parameters common among 3.3/5v N-type MOSFET transistors
pfet_dg-Parameters common among 3.3/5v P-type MOSFET transistors
hvnld---Parameters specific to 5/40 NLD MOS
hvpld---Parameters specific to 5/40 PLD MOS
cap-----Parameters specific to MIM Caps
hvres---Parameters specific to High-Value Poly Resistor
lvres---Parameters specific to Low-Value Poly Resistor
salres--Parameters specific to Salicided Poly Resistor
ind-----Parameters specific to Inductors
  
```

FIGURE 12.2 X-Sigma Parametric Sweep Example

Simple VCO Example



Access σ_s as
design variables



IP: 128.173.89.96

12.2 Statistical Models

Statistical models provide the most accurate simulation of the process variation at the expense of simulation time. The random nature of Monte-Carlo simulation emulates the true process variation. The statistical and X-Sigma models use the same model libraries and statistical mappings. Thus, Table 12.1 applies fully to the statistical models. Isolated statistical simulation provides more direct access to circuit sensitivities to particular devices. Statistical simulation of one device (or multiple) device class can be combined with X-Sigma simulation of another (or multiple) device class. Thus, for example, one can run a statistical simulation on the NFET device class while the X-Sigma of the other device classes can be set to anywhere in the process space. The statistical models are centered around the NOM case. The difference lies in the amount of sigma variation (simulator defined for statistical simulation, user defined for the X-Sigma model simulation).

12.3 Verification

Tables for each device type showing the corner and statistical simulation match to the technology ESPECs are contained in the relevant device chapters of this design manual.

13.0 Appendix A: Layout Parasitics

Jazz supports Assura and Calibre parasitic extraction in the CA18 design kit. Table 13.1 gives a detailed device by device breakdown of what parasitics are included in the model compared to parasitics extracted by Assura or Calibre.

TABLE 13.1 Parasitic Extraction Reference Table

Device Model	Included in Model	Included in Extraction Deck
MS MOSFET	<ul style="list-style-type: none"> ✓ When the mos primitive is used alone (i.e. NFET instead of NFETs), it represents a single “finger” of a device with nominal source/drain area/perimeter. HDIF parameter helps estimate multiple finger scaling. ✓ When the subcircuit wrapper is used (i.e. NFETs), the source/drain is calculated to be shared between the fingers and also scaled based on the “current” parameter. The default source/drain size uses the minimum design rule size for the gate/source/drain. ✓ No gate or contact resistance is modeled. 	<ul style="list-style-type: none"> ✓ Gate resistance, contact resistance, etc. even in active region ✓ Each finger is extracted separately with the proper shared source/drain also calculated. ✓ All metal interconnect.
RF MOSFET	<ul style="list-style-type: none"> ✓ all source/drain area and perimeter calculations ✓ gate poly and metal interconnect over active 	<ul style="list-style-type: none"> ✓ source, drain, and gate connections on the ends of the fingers ✓ number of gate fingers extracted and passed to the model
Resistors	<ul style="list-style-type: none"> ✓ Head resistance/capacitance on poly. This is an Espec value that includes a “nominal” contact resistance. Head resistance scales inversely with width because more contacts are included with a wider resistor. ✓ Body resistance/capacitance on poly. ✓ Well-to-sub resistance and diode. 	<ul style="list-style-type: none"> ✓ All metal and interconnect except contact. Contact is part of the head resistance and is NOT extracted.

Device Model	Included in Model	Included in Extraction Deck
MIM Capacitor	<ul style="list-style-type: none"> ✓ bottom metal resistance and capacitance ✓ topmm resistance and capacitance ✓ top metal resistance including via to topmm ✓ Well-to-sub resistance and diode. 	<ul style="list-style-type: none"> ✓ bottom metal access resistance (see Section 8.1.2 on page 312)
Varactor_NI	<ul style="list-style-type: none"> ✓ All M1 and contacts on fingers ✓ fingers (nf) 	<ul style="list-style-type: none"> ✓ Number of fingers extracted and passed to the model
Varactor_MOS	<ul style="list-style-type: none"> ✓ All M1, M2, via1, poly, and contacts over device area inside Nwell ✓ fingers (nf) and slices (ns) included ✓ 1 Nwell per device which scales with w,l, ns and nf. 	<ul style="list-style-type: none"> ✓ nf and ns extracted and passed to the model ✓ metal interconnect of end regions connecting up fingers outside of Nwell
Poly Capacitors	<ul style="list-style-type: none"> ✓ poly to nwell capacitance ✓ nwell resistance 	<ul style="list-style-type: none"> ✓ All M1, M2, and poly to metal capacitance ✓ All M1, M2, poly, via, and contact resistance
Inductors	<ul style="list-style-type: none"> ✓ All metal parasitics 	<ul style="list-style-type: none"> ✓ Any interconnect outside of the inductor marking layer LCELL ✓ Connection metal not included with pcell but drawn on LCELL is ignored.
VPNP	<ul style="list-style-type: none"> ✓ Primitive PNP 	<ul style="list-style-type: none"> ✓ All metal interconnect ✓ All contact resistance

14.0 Appendix B: Additional CA18 Process Variants

14.1 Alternate Device Names

In addition to the CA18QD/PD/HD super set process variants, Jazz offers other 0.18um CMOS technology flavors. These additional process variants do not share the same naming conventions as CA18QD/PD/HD. The following list details the device names in these variants. Please notice that while the device nomenclature is different, the device performance and characteristics is identical.

FETs:

- nfet (analog NFET, thin oxide, 3-terminal with implicit bulk pin, sub-circuit model NFETs)
- nfet4 (analog NFET, thin oxide, 4-terminal with explicit bulk pin, sub-circuit model NFETs)
- pfet (analog PFET, thin oxide, 4-terminal with explicit bulk pin, sub-circuit model PFETs)
- pfet3 (analog PFET, thin oxide, 3-terminal with implicit bulk pin, sub-circuit model PFETs)
- n3p3fet (analog NFET, thick oxide, 3-terminal with implicit bulk pin, sub-circuit model n3p3fets)
- n3p3fet4 (analog NFET, thick oxide, 4-terminal with explicit bulk pin, sub-circuit model n3p3fets)
- p3p3fet (analog PFET, thick oxide, 4-terminal with explicit bulk pin, sub-circuit model p3p3fets)
- p3p3fet3 (analog PFET, thick oxide, 3-terminal with implicit bulk pin, sub-circuit model p3p3fets)
- nfet_rf (RF NFET, thin oxide, 4-terminal with explicit bulk pin, sub-circuit model NFET_rf)
- pfet_rf (RF PFET, thin oxide, 4-terminal with explicit bulk pin, sub-circuit model PFET_rf)
- n3p3fet_rf (RF n3p3fet, thick oxide, 4-terminal with explicit bulk pin, sub-circuit model n3p3fet_rf)
- p3p3fet_rf (RF p3p3fet, thick oxide, 4-terminal with explicit bulk pin, sub-circuit model p3p3fet_rf)
- passgate (thin oxide passgate, schematic based)*
- passgate3p3 (thick oxide passgate, schematic based)*

Junction Diodes:

- ndiode (n+/sub junction diode, thin oxide, 2-terminal, primitive model ndiode)
- pdiode (p+/well junction diode, thin oxide, 2-terminal, primitive model pdiode)
- n3p3diode (n+/sub junction diode, thick oxide, 2-terminal, primitive model n3p3diode)
- p3p3diode (p+/well junction diode, thick oxide, 2-terminal, primitive model p3p3diode)

Resistors:

- rw3t (Nwell resistor, 3-terminal, sub-circuit model rw3t)
- rpp3t (unsalicated poly resistor, 3-terminal, sub-circuit model rpp3t)
- rps (salicated poly resistor, 3-terminal, sub-circuit model rps)

Capacitors:

- pc (poly cap over well, thin oxide, 3-terminal, sub-circuit model pc)
- pc3p3 (poly cap over well, thick oxide, 3-terminal, sub-circuit model pc3p3)
- c3t_mim (MIM capacitor over substrate, 3-terminal, sub-circuit model c3t_mim)
- c3t_mimw (MIM capacitor over well, 3-terminal: plus-minus-well (no substrate pin available), sub-circuit model c3t_mimw)

Pnps:

- vPNP: 4 discrete devices available through pcell: PNPa (25x25), PNPb (11x11), PNPe (5.4x5.4), PNPd (3x3) (thin oxide, 3-terminal, primitive model)

Varactors:

- varactor_ni (non-implanted varactor, 3-terminal, sub-circuit model rfvar_ni)

Inductors:

- l3t (top metal planar inductor, 3-terminal, sub-circuit model l3t)
- ldiff (top metal differential inductor, 4-terminal, sub-circuit model ldiff)

Fuse:

- fuse (metal fuse, 2-terminal, sub-circuit resistor model fuse) *

ESD FETs

- NFET_esd (esd NFET with well resistor and guard ring, schematic based)*
- PFET_esd (esd PFET with guard ring, schematic based)*
- n3p3fet_esd (esd n3p3fet with well resistor and guard ring, schematic based)*
- p3p3fet_esd (esd p3p3fet with guard ring, schematic based)*

* Data not available