namely, the PEC loop BW is primarily set by the LPF BW and larger LPF BW would inject more in-band noise from the PEC path to the LC tank, disturbing in-band noise characteristic of the injection-locked tripler. While the SiGe HBT-based design, which shows ~10x better flicker noise performance than CMOS-based design in the PI’s preliminary simulations, can mitigate the noise issue, a comprehensive study on the phase noise requirement and the PLL/PEC loop parameters will be conducted after an integral review on the E-band wireless channel interference environment and system speed requirement. Given that the E-band wireless system standard has not been firmly established yet, the PI will initiate the study by referring to Gigabit speed microwave point-to-point system standards [xx-xx], which will be updated in accordance with the progress of the FCC E-band wireless system standardization in the course of the Career program.

**Component Research (3): E-Band Distributed RF Front-End Receiver Element**

The phase shifter is an indispensable element to realize beamforming and beam-steering, and significant efforts have been made to improve the performance of integrated phase shifters in silicon technology by the PI and others [1-5]. Passive phase shifters exhibit good linearity but suffer from performance tradeoffs between phase resolution, loss and chip area: namely, increasing phase resolution requires cascading more passive networks, claiming larger chip space and higher loss because of a finite quality factor of the passive components [6-11]. While active phase shifters can achieve virtually unlimited phase resolution with signal gain by interpolating quadrature phases in a continuous way [11-16], nonlinearity and power consumption are of major concern. The PI has recently proposed a distributed phase shifting approach to leverage the benefits of both active and passive phase shifters with a minimum tradeoff, and test chip at 94 GHz has been taped out under a DARPA program (Fig. 14) [xx].

 **Fig. 14.** Block diagram of RF front-end element that merges LNA and phase shifter in a distributed way (upper) and its layout in IBM 0.13-m SiGe BiCMOS technology at 94 GHz (lower). Layout size: 1830x600 m2.

Because of a finite gain per stage in silicon at mm-wave (> 60 GHz), a multi-stage LNA is preferable to achieve sufficient gain to suppress noise from the following receiver path. In the proposed (Fig. 14: upper), the passive 90o- and 180o-hybrids are interposed in between the cascaded LNA stages, and the input signal will be split into I/Q vector signals (2 phases) in the first 90o-hybrid. One of the I/Q phases will be selected in the pre-selection stage and the 180o-hybrid generates differential phases based on each set of the I/Q vectors (4 phases), which are fed to the variable gain amplifiers (VGAs) for further fine phase processing. The second 90o-hybrid plays as a phase interpolator: i.e., it takes independently weighed differential inputs, changes the differential phases into quadrature phases, and finally adds the quadrature-phased signals at the outputs. A continuous gain control in the VGAs will result in two-quadrant continuous phases at each output of ⑤ and ⑥, respectively. The cascading of the post-selection stage completes 360o of phase rotation at the final output.

Note that in the proposed approach, LNA and phase shifter functionalities are merged together in a distributed way, where majority of phase shifter function is accomplished by the passive hybrids while LNA provides necessary amplitude weighting for the fine phase interpolation. This topological innovation provides number of benefits: *1. the merged configuration allows to use minimum number of hardware and removes the performance tradeoff in passive phase shifter, while achieving the same degree of high phase resolution as in active phase shifter; 2. overall linearity will be set by the LNAs and the integration of phase shifter functionality does not degrade the linearity performance; 3. further, the cascade of 180o-hybrid, VGAs and 90o-hybrid constitutes a conventional microwave balanced amplifier configuration [17,18], benefitting an increase of IIP3 by 3 dB more; and 4. the hybrids provide a good isolation between amplifiers, improving stability issue in cascading multiple amplifier stages.*

From the PI’s preliminary EM simulations based on a 0.18-m SiGe BiCMOS process, typical loss per each hybrid network is about 1-1.5 dB at the E-band up to 95 GHz, causing negligible impact on the overall system performance (Fig. 15 (a)). In the 94 GHz design, the overall system shows 26 dB gain, 8.5 dB NF, and –14 dBm IIP3 (+12 dBm OIP3) with 4-bit phase resolution in a discrete control, one of the-state-of-the-art performance at the mm-wave frequency (Fig. 15 (b), (c) and (d)).



(b) (c) (d)

**Fig. 15.** Simulated performance of the 94 GHz distributed RF front-end receiver: (a) EM simulation results of 90o-hybrid, (b) gain and NF, (c) input referred 1-dB compression point (P-1dB), and (d) 16 discrete phase responses.

**Proposed Work**: The 90o- and 180o-hybrids in the preliminary design are based on /4-transmission lines (/4=250 m @ 80GHz) and take ~50% of chip space. To reduce the chip size in Phase I (years 1 & 2), the transmission line based hybrid networks will be replaced by lumped-hybrid networks [19, 20] which can be integrated compactly at the E-band because required inductance is on the order of 10’s pH. The number of LNA stage is also a design parameter to be engineered dependent of required system gain, NF, and linearity. It is likely that an optimal system budget allocation could replace the last stage post-selection amplifiers in Fig. 14 with a SPDT switch with a minimal compromise in overall system gain and NF performance. Therefore, a performance comparison work is planned in Phase I by replacing the pre- and post-amplifier stages with the switch networks, leveraging recent advancement in integrated SPDT switch [21-23]. While single-ended topology is preferable to differential one in the front-end receiver element design because of simpler layout (hence smaller layout parasitics thereof), lower power consumption, and greater facility to interface with antenna, a differential version of the receiver is also planned to be taped out to investigate any performance difference including common-mode noise effect.

Reference: Component Research (3)

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