W-band 65-nm CMOS and SiGe BiCMOS Transmitter and Receiver with Lumped I-Q Phase Shifters

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***Abstract*—This paper describes 80-94 GHz and 70-77 GHz I-Q phase shifters and the corresponding transmitter and receiver ICs, fabricated in 65-nm CMOS and SiGe BiCMOS technologies, respectively. Lumped inductors and transformers are employed to realize small-form factor 90° hybrids as needed in high density phased arrays. The CMOS transmitter operates with a saturated output power of +3 dBm and exhibits maximum absolute phase and amplitude errors of 14° and 5.5 dB, respectively, when the phase is varied from 0° to 360° in steps of 22.5°. The absolute phase error in the SiGe BiCMOS receiver is less than 8°, with a maximum gain imbalance below 3 dB over its 3-dB bandwidth of 70-77 GHz. The peak gain and power consumption are 3.8 dB and 142 mW from 1.2 V supply for the CMOS transmitter, and 17 dB and 128 mW from 1.5 V and 2.5 V supplies for the SiGe BiCMOS receiver.**

***Index Terms*—mm-wave phase shifter, phase interpolation, CMOS weighted adder, BiCMOS variable gain amplifier.**

I. Introduction

SiGe BiCMOS technology and CMOS technologies at the 65-nm node and beyond are ideally suited for highly integrated and low-power W-band phased arrays, opening up the path for new system architectures based on electronic beam-forming and beam-steering. These can provide increased range, resolution and zooming functions for applications such as automotive and industrial sensors, active and passive imaging.

This paper describes the highest frequency phase shifters in silicon, with 3-dB bandwidths of 70-77 GHz and 80-94 GHz, respectively. Two different 90° hybrids, based on lumped inductors and transformers, and new mm-wave CMOS and BiCMOS phase rotators are employed to achieve the most compact transmit and receive lanes, less than 150μm $\times$ 800 μm, allowing for tens of thousands of transceivers or receivers to be integrated on a single 300-mm wafer.

II. Phase shifter topology

Both phase shifters employ the phase interpolation architecture (Fig. 1) consisting of a 90° hybrid, which splits the input signal into two equal-amplitude paths in quadrature, and a phase rotator [1]. The latter features two variable gain amplifiers (VGAs), one for each path, and an adder. The phase error and amplitude imbalance of the hybrid and the gain-to-PM conversion of the VGAs dictate the overall performance of the phase shifter. In both the CMOS (Fig. 2) and the BiCMOS (Fig. 3) designs, the VGAs are realized as telescopic-cascode Gilbert cells, with the current summer implemented as a differential-to-single-ended balun. The latter also performs impedance matching to 50Ω. Unlike in other Gilbert cell based

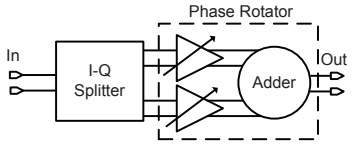

Fig. 1: I-Q phase shifter architecture

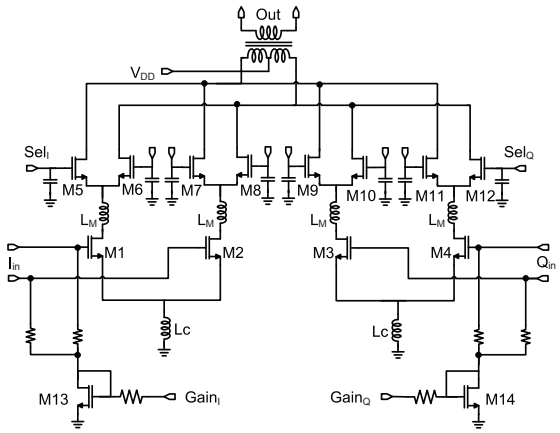

Fig. 2: Schematics of the 94-GHz phase rotator. All MOSFETs have the minimum drawn gate length of 60 nm.

phase shifters operating below 50 GHz [2], the mm-wave signal is applied at the gates of the common-source devices, thus maximizing gain, isolation and bandwidth.

The two phase shifters differ in the choice of 90° hybrid and in the gain control mechanism. The latter directly reflects in the phase and gain error performance.

The 94-GHz, 65-nm CMOS phase shifter features a quadrature all-pass filter based on the schematic in [2] and realized with spiral inductors (Fig. 4). Differential cascode buffers are used at the outputs of the filter to ensure good isolation between the two signal paths. Careful attention was paid in optimizing the characteristic impedance and inductor values such that the phase and amplitude errors are minimized in the presence of the parasitic capacitances presented by the buffers. The simulated performance of this filter is illustrated in Fig. 5, showing a bandwidth that exceeds 20% and a phase error below $\pm 1.5^\circ$. Its major disadvantage is the relatively high loss of 6-6.5 dB.

In the CMOS phase rotator of Fig. 2, the 2-bit quadrant selection is performed by the top CMOS switches of the two VGAs. In each quadrant, the phase is controlled in analog

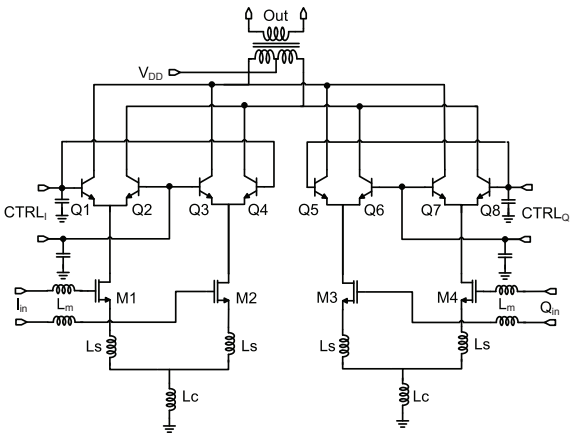

Fig. 3: Schematics of the 77-GHz phase rotator. All MOSFETs/HBTS have 130-nm gate length/emitter width.

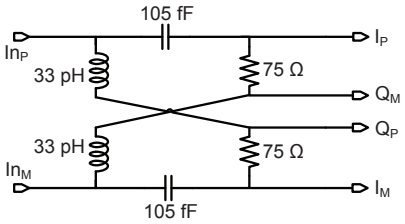

Fig. 4: All-pass polyphase filter schematics.

fashion by changing the bias currents of the common source MOSFETs in the I and Q Gilbert-cells. A multi-bit DAC could replace the analog control in an all-digital control version. This gain control mechanism is not optimal since, at current densities below 0.15 mA/μm, when the power gain changes, the phase is also affected by the change in transistor gate-source capacitance and transconductance.

The gates of transistors M5-M12 are decoupled to ground through $0.5pF$ capacitors in order to prevent instability [3], while inductors Lc provide common mode rejection. The 94-GHz CMOS phase shifter consumes 43 mW, of which 20 mW are in the rotator, from 1.2 V supply.

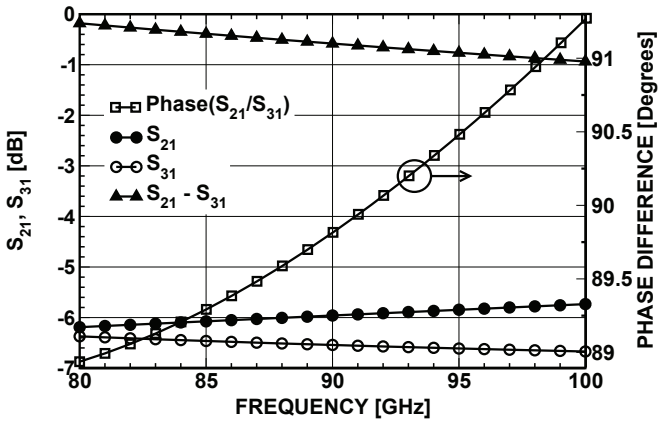

Fig. 5: Simulated performance of the all-pass polyphase filter.

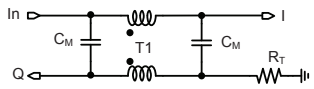

Fig. 6: Implemented lumped quadrature hybrid schematics.

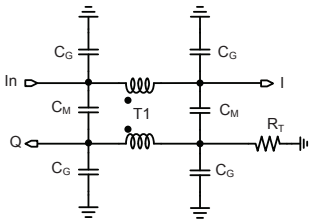

Fig. 7: Lumped quadrature hybrid as in [4].

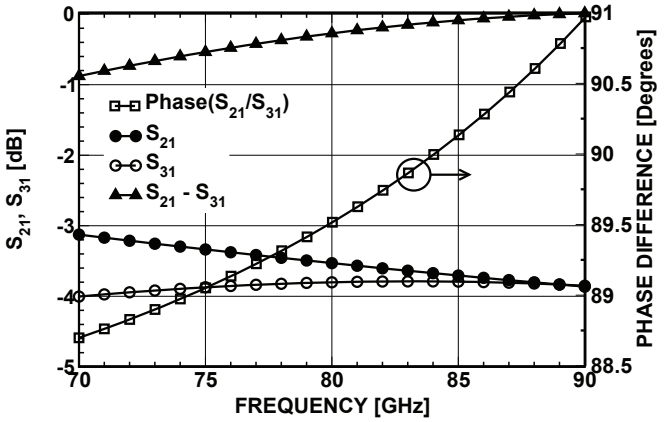

Fig. 8: Simulated performance of the quadrature hybrid.

The 77-GHz SiGe BiCMOS phase-shifter utilizes a single-ended, transformer-based, quadrature hybrid [4] illustrated in Fig. 6 which is a modified version of the one depicted in Fig. 7 [4]. The main challenge in designing a lumped hybrid coupler in the W-band is posed by the very small capacitance values which cannot be realized as MiM capacitors. To overcome this problem, a three step procedure was followed. First, the coupling coefficient and coil inductance of transformer T1 were designed to be as close as possible to the target values predicted by theory [4]. In order to achieve the required tight coupling in a thick metal back-end, a laterally (as opposed to vertically) coupled transformer structure was employed with minimum allowed spacing between the coils. The resulting total size of the transformer is $17\mu m \times 17\mu m$. In a second step, the values of the capacitors in the hybrid are optimized by accounting for the parasitic capacitances and resistances of T1. Finally, the capacitors C_G shown in Fig. 7 that cannot be realized as MiM capacitors are omitted and the values of the remaining capacitors are fine tuned. In the final structure of Fig. 6, C_{M1} and C_{M2} are equal to 27 fF and 40 fF, respectively, and are realized as MiM capacitors.

The simulation results for the transformer-based quadrature hybrid are shown in Fig. 8. The phase error is less than 1°, while the gain imbalance remains below 1 dB over the entire 70-90 GHz range. The simulated loss is 3 dB at 70 GHz and 4 dB at 90 GHz, 1-2 dB better than that of the all-pass quadrature filter.

The BiCMOS phase rotator shown in Fig. 3 employs MOS-HBT cascodes [5] due to their stability, high bandwidth,

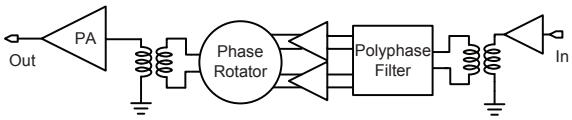

Fig. 9: Block diagram of the transmitter IC.

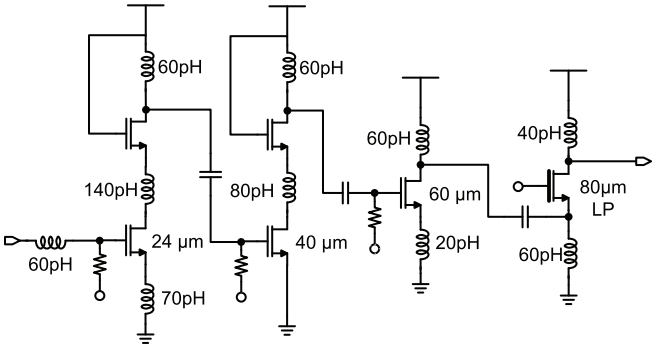

Fig. 10: Power amplifier schematics. All MOSFETs have 60-nm drawn gate length.

linearity and lower supply voltage when compared to an HBT-only cascode. Gain control is achieved through the analog voltages $CTRL_I$ and $CTRL_Q$ by steering the current through each of the pairs Q1-Q2, Q3-Q4, Q5-Q6 and Q7-Q8 [6]. Under this gain control scheme, the bias current in M1-M4 and the impedance seen at their drains remain constant over all gain states. As a result, the gain-to-PM conversion is improved over the VGAs presented in Fig. 2.

Spiral inductors L_s along with line inductors L_m are used to match the input impedance of the VGA to the 40Ω reference impedance of the hybrid. The SiGe phase shifter, including bias and control circuitry, consumes 27mA from a $2.5V$ supply.

III. Receiver and Transmitter ICs

The CMOS phase shifter was integrated along with an input buffer and a medium power amplifier in an 80-94 GHz transmitter IC (Fig. 9). The measured gain of the stand-alone PA was 7 dB, centered at 90 GHz, and the P_{SAT} is +3 dBm. As illustrated in Fig. 10, the PA consists of two telescopic cascode stages for high-gain and lower power consumption, followed by an AC-coupled cascode stage that maximizes the signal swing at the output node. To ensure reliable operation, the final common-gate stage is implemented with a low-power (LP) transistor, which has a thicker gate oxide than the general purpose (GP) MOSFETs used elsewhere, making it more immune to degradation due to large voltage swings.

The 94-GHz transmitter was fabricated in a 65-nm GPLP CMOS technology with 7 metal backend. The die microphotograph is shown in Fig. 11. The output of the power amplifier is connected to a pad through a $\lambda/4$ transmit/receive SPDT switch [7], which is not shown in Fig. 11. The total power consumption is 142 mW from 1.2 V supply while occupying an area of $800\mu m \times 150\mu m$ (not including the switch and the pad).

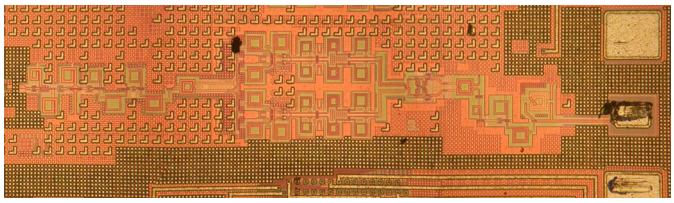

Fig. 11: 65-nm CMOS transmitter die microphotograph.

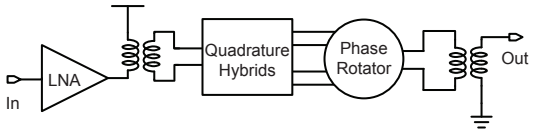

Fig. 12: Block diagram of the receiver IC.

The SiGe phase shifter was integrated along with a 3-stage LNA with 22-dB gain and 4-dB noise figure [8] in a 70-77 GHz receiver, illustrated in Fig. 12. The receiver IC was fabricated in a 130-nm SiGe BiCMOS technology with 6 levels of copper metallization [9]. The die microphotograph is shown in Fig. 13. The total size is $660\mu m \times 690\mu m$ ($150\mu m \times 500\mu m$ without pads) and the power consumption is $128mW$ from 1.5 V and 2.5 V power supplies.

IV. Measurement Results

On-wafer S-parameter measurements were carried out in the 55-94 GHz range using a Wiltron 360B VNA and 110-GHz Cascade Infinity probes. The analog control voltages of the phase shifters were provided by an Agilent 4155 semiconductor parameter analyzer.

A. 80-94 GHz Transmitter

Fig. 14 illustrates the measured phase versus frequency characteristics for the 16 different phase settings in the 80-94 GHz range, whereas Fig. 15 depicts the phase error of each state versus frequency. The phase error was calculated by assuming constant phase shift across frequency and reaches a minimum of 4° at 90 GHz, at the center of the PA bandwidth.

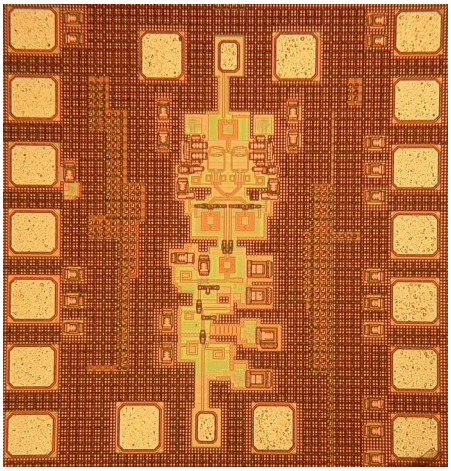

Fig. 13: SiGe BiCMOS receiver die microphotograph.

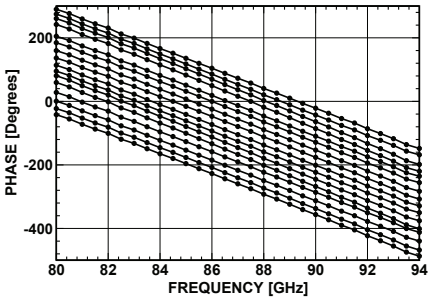

Fig. 14: Measured phase vs. frequency characteristics of the 94-GHz transmitter.

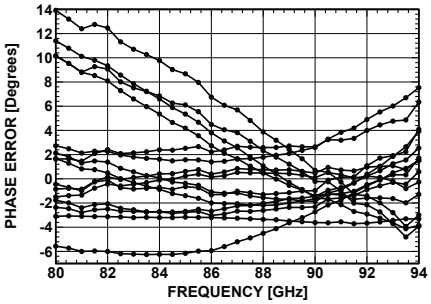

Fig. 15: Transmitter phase error vs. frequency.

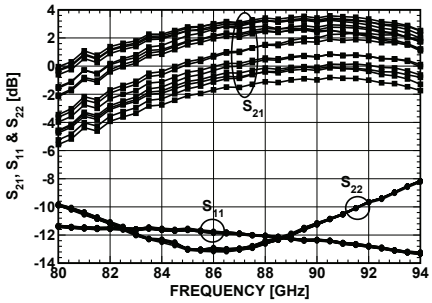

Fig. 16: Measured S-parameters of the transmitter IC.

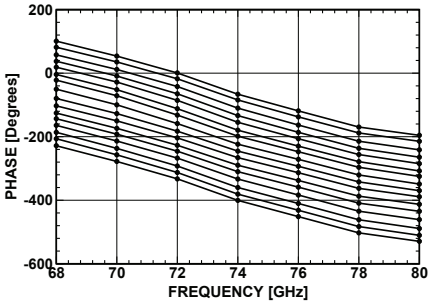

Fig. 17: Measured phase vs. frequency characteristics of the 77-GHz receiver.

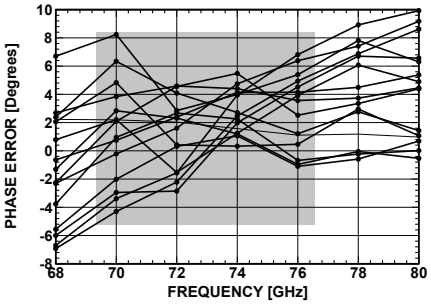

Fig. 18: Receiver phase error vs. frequency.

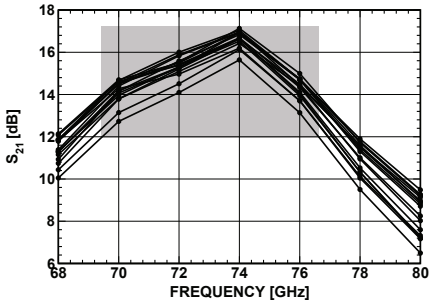

Fig. 19: Measured receiver S_{21} vs. frequency.

Fig. 16 shows the measured S_{21}, input and output return loss versus frequency for the 16 different phase settings. A maximum small-signal gain of 3.8 dB is demonstrated, with a maximum peak-to-peak gain variation among all states of less than 4 dB, at 90 GHz.

B. 70-77GHz Receiver

Fig. 17 reproduces the measured phase versus frequency characteristics for the 16 different phase settings in the 68-80 GHz range. Fig. 18 shows that the phase error remains below 6° in the 72-76 GHz range and below 8° in the shaded area which highlights the 70-77 GHz 3-dB bandwidth of the entire receiver.

Fig. 19 illustrates the measured S_{21} versus frequency for all 16 settings. The maximum gain is 17 dB with less than 2 dB of peak-to-peak gain imbalance. The improved results over those in Figs. 15 and 17 are attributed to the superior gain-to-PM characteristics of the BiCMOS VGAs.

V. Conclusions

A 65-nm CMOS 94-GHz transmitter and a 77-GHz SiGe BiCMOS receiver have been demonstrated. Both circuits employ phase interpolation architectures to achieve 360° of controllable phase shift. The transmitter exhibits a peak gain of 3.8 dB with a maximum gain imbalance of 5.5 dB and a maximum phase error of less than 14° over a bandwidth exceeding 14 GHz. The receiver achieves a maximum gain of 17 dB with an outstanding peak-to-peak gain imbalance of less than 3 dB and an in-band phase error below 8°. By employing lumped inductors and transformers in the matching networks and in the 90° hybrids, the footprint of both ICs was minimized, making them ideal for integration in high-density phased arrays with electronic beam-steering.

VI. Acknowledgments

The authors thank Bernard Sautreuil, Christophe Garnier and STMicroelectronics for technology access, NSERC for funding, CMC and Jaro Pristupa for CAD support.

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