A 76–84 GHz SiGe Power Amplifier Array Employing Low-Loss Four-Way Differential Combining Transformer

Mury Thian, Marc Tiebout, *Member, IEEE*, Neil B. Buchanan, Vincent F. Fusco, *Fellow, IEEE*, and Franz Dielacher, *Senior Member, IEEE*

***Abstract*—This paper presents holistic design of a novel four-way differential power-combining transformer for use in millimeter-wave power-amplifier (PA). The combiner with an inner radius of 25 μm exhibits a record low insertion loss of 1.25 dB at 83.5 GHz. It is designed to simultaneously act as a balanced-to-unbalanced converter, removing the need for additional BALUNs typically required in differential circuits. A complete circuit comprised of a power splitter, two-stage differential cascode PA array, a power combiner as well as input and output matching elements was designed and realized in SiGe technology with $f_{\mathrm{T}}/f_{\mathrm{max}}$ 170/250 GHz. Measured small-signal gain of at least 16.8 dB was obtained from 76.4 to 85.3 GHz with a peak 19.5 dB at 83 GHz. The prototype delivered 12.5 dBm output referred 1 dB compression point and 14 dBm saturated output power when operated from a 3.2 V dc supply voltage at 78 GHz.**

***Index Terms*—Cascode, differential circuit, *E*-band, heterojunction bipolar transistor (HBT), integrated circuit (IC), millimeter-wave, power amplifier, power combiner, silicon germanium (SiGe), transformer.**

I. Introduction

MOST wireless radio communications operate at frequencies below 10 GHz where bandwidth is priceless due to already congested frequency spectrum. As demand for ultra high-speed data transfer unprecedentedly increases, large bandwidth is required. One of the trivial solutions to this issue is through a migration to millimeter-wave frequency regime. To name a few, the unlicensed 60 GHz frequency band allocated for indoor applications and the newly licensed, yet inexpensive 71–76 GHz and 81–86 GHz E-band intended for backhaul applications provide a generous bandwidth of several gigahertz worldwide. Despite this bandwidth advantage, the path loss incurred at millimeter-wave frequencies is substantially high. As an illustration, the loss due to oxygen absorption reaches its peak 15 dB/km at around 60 GHz. Consequently, to enable long-range distance data transmission, high effective isotropic radiated power (EIRP) is required. Given the gain of the antenna array, the EIRP would in turn dictate the output power level of the power amplifier (PA).

Meanwhile, breakthroughs in nanotechnology and optics have enabled the production of high-performance high-speed transistors in low-cost highly-integrated silicon technology. As a direct result, the III-V based technologies such as GaAs and InP that have in the past decade been dominating the market for millimeter-wave wireless products are being greatly challenged. For instance, the 60/77/79 GHz PAs reported in [1]–[7] and [8]–[15] were triumphantly implemented in CMOS and SiGe processes, respectively.

Recently, there have been significant research efforts on millimeter-wave silicon PA that attempt to achieve output power at least 20 dBm derived from the EIRP specification for long-range radios. This high power level cannot realistically be achieved by merely relying on the capability of the largest device that even the most advanced silicon IC process can offer. This stems from the inevitable natural trade-off that as the f_{T} of the transistors increases the breakdown voltage $\mathrm{BV}_{\mathrm{CEO}}$ decreases, limiting the signal swing and hence reducing the output power. In addition, thermal dissipation due to typically poor efficiency of the millimeter-wave PAs eventually reduces the output power further down. In SiGe process, an increase in temperature from 25 °C to 85 °C typically results in 2–3 dB power reduction.

In order to relax the design specifications for the PAs, given the challenges described above, power-combining techniques utilizing passive structures can be adopted. Traditionally, output power from the PAs can be combined in phase using the Wilkinson structure [11] illustrated in Fig. 1(a). The Wilkinson combiner is formed by two $\lambda/4$ transmission lines (TLs) with characteristic impedance $Z_{\mathrm{T}} = Z_0\sqrt{2}$ (Z_0 is the system characteristic impedance) and a ballast resistor of $2Z_0$ that provides an excellent isolation between the input ports. In cases where three or more PAs ($n \geq 3$) are combined, the Wilkinson structure is no longer planar since the ballast resistors will cross over one another. Besides, the value of Z_{T} will increase. For example, for $n = 4$, Z_{T} will be $2Z_0$. For a 50-Ω system, this means 100 Ω. In SiGe process [16], the maximum realizable Z_{T} is about 70 Ω, associated with the smallest metal width allowed by the technology. To get around this issue, Z_0 can be set to 35 Ω rather than 50 Ω.

However, in this scenario a matching element to transform 35Ω back to 50 Ω is required, adding more complexity and

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M. Thian was with the ECIT Institute, Queen's University of Belfast, Belfast BT3 9DT, U.K.. He is also with Infineon Technologies, Villach A9500, Austria (e-mail: m.thian@qub.ac.uk).

M. Tiebout and F. Dielacher are with Infineon Technologies, Villach A9500, Austria.

N. B. Buchanan and V. F. Fusco are with the ECIT Institute, Queen's University of Belfast, Belfast BT3 9DT, U.K.

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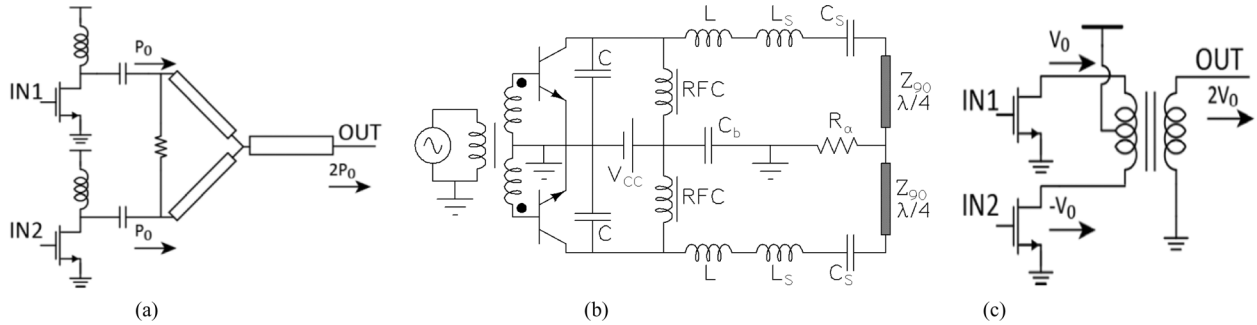


Fig. 1. Power-combining techniques. (a) Wilkinson. (b) $\lambda/4$ transmission-line. (c) Transformer.

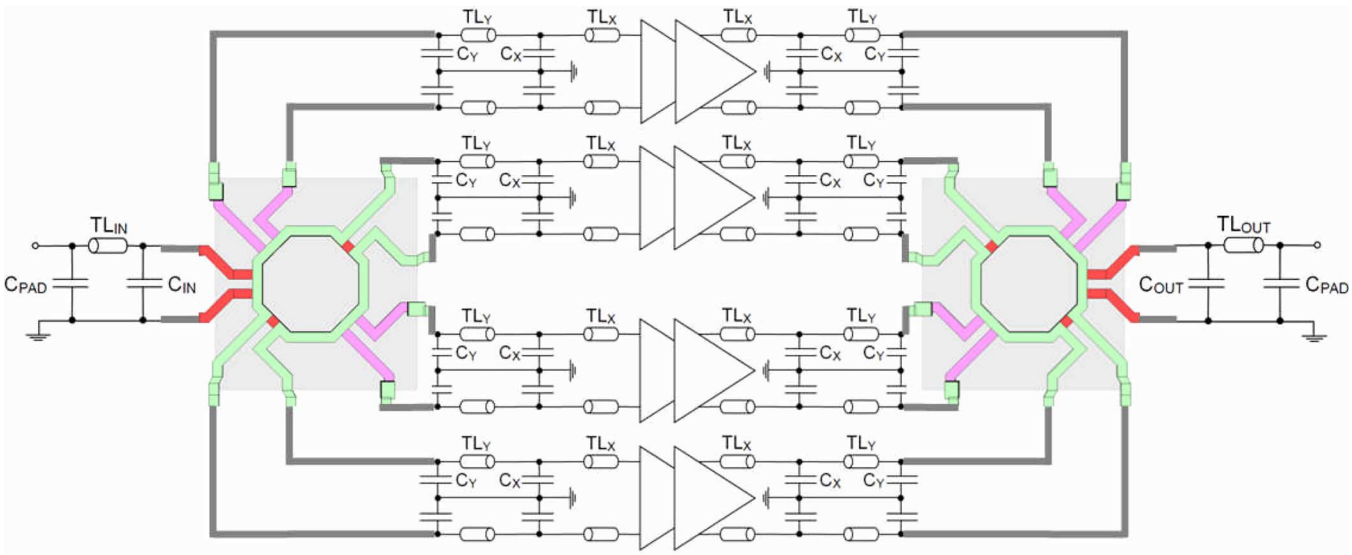


Fig. 2. Schematic of the proposed four-way differential combining PA.

losses. Alternatively, multiple two-way Wilkinson structures to combine 4 or 8 PAs can be used, but the insertion loss of the combining network will soon be greater than the added power of additional amplifiers. Also, the interconnections can be daunting and any mismatches introduced by these interconnections will degrade the overall performance.

As in the Wilkinson structure, the high-efficiency Class-E PA reported in [17], [18] employs $\lambda/4$ TLs to combine power but without the ballast resistor, Fig. 1(b). This leads to a rather poor isolation, but it can be tolerated if the leakage energy injected from one port to another does not substantially affect the circuit's operation.

Another power-combining strategy proposed in [1]–[4], [10] and [12] is based upon transformers, Fig. 1(c). While the $\lambda/4$ TL combiners are bulky and lossy, particularly if implemented in low-resistivity silicon substrate, the transformer-based combiners offer very compact geometry. To give an illustration, the inner diameter of the power-combining transformer designed at 80 GHz center frequency is only 50 μm in contrast to 465μm electrical length of the $\lambda/4$ TL at the same frequency. Importantly, these transformers can also simultaneously provide an impedance transformation (the higher the number of input ports, the higher the impedance transformation ratio) and balanced-to-unbalanced conversion roles, thus dispensing the need for additional matching elements as well as for BALUNs typically required in differential circuits.

To date, there are only a few publications reporting on millimeter-wave transformers with combining capability of more than two single-ended paths. For example, the transformers demonstrated in [2]–[4] and [10] realized in CMOS and SiGe, respectively, are able to combine four single-ended paths efficiently. This paper will discuss the design of a novel compact eight-way power-combining transformer and its implementation in SiGe technology. The loss of the combiner is only 1.25 dB at 83.5 GHz center frequency of 81–86 GHz E-band. For practical validations, a complete circuit comprised of a power splitter, two-stage differential cascode PA array, a power combiner as well as input and output (I/O) matching networks is built. The circuit schematic is depicted in Fig. 2 and the circuit component values are given in Table I.

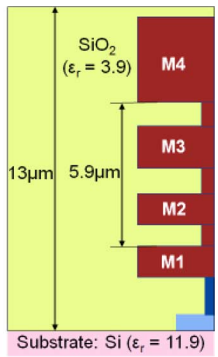
II. Technology

Active and passive circuits presented in this paper are designed and implemented using Infineon B7HF200 SiGe process [16]. The HBT transistors are fabricated with a double-polysilicon self-aligned emitter base configuration with

TABLE I
CIRCUIT COMPONENT VALUES

Fig. 2		Fig. 4	
TL_X	265 × 5 μm²	TL_1	30 × 5 μm²
TL_Y	275 × 5 μm²	$TL_{2,3}$	70 × 5 μm²
$TL_{IN,OUT}$	330 × 2.4 μm²	TL_4	60 × 5 μm²
C_X	60 fF	TL_5	50 × 5 μm²
C_Y	85 fF	TL_6	30 × 5 μm²
C_{IN}	35 fF	C_1	50 fF
C_{OUT}	45 fF	C_2	55 fF
C_{PAD}	25 fF	R_1	250 Ω
		T_1–T_4	0.35 × 40 μm²

Technology	B7HF200
Lithography node	0.35 μm
Eff. emitter width	0.18 μm
Substrate	p⁻, 20 Ω cm
f_{max}	250 GHz
f_T at j_C = 5 mA/μm²	170 GHz
BV_{CEO}	1.7 V
BV_{CBO}	6.5 V
Active devices	UHS/HS/HV npn Vertical pnp
Varactor	Yes
MIM capacitor	Yes
Resistor	Poly p⁺ and p⁻ TaN
Cu metallization	M1 – M4
Bonding pads	Au



(a) (b)

Fig. 3. (a) Core features of the Infineon B7HF200 technology and (b) cross section of the metal layer stack.

a selectively grown SiGe:C base. High-speed (HS) rather than ultra-high-speed (UHS) transistors are chosen since they offer higher $\mathrm{BV_{CEO}}$ and $\mathrm{BV_{CES}}$ values, 1.7 and 6.5 V, respectively. The peak $f_{\mathrm{T}} = 170$ GHz and the peak $f_{\max} = 250$ GHz occur at a collector current density 5 mA/μm^2. These parameters are obtained from the measurements of transistors with emitter mask size 0.35×2.8 μm^2 or effective emitter size $(0.35–0.17) \times (2.8–0.17)$ μm^2.

Four copper metal layers (M1–M4) are available for interconnections as well as for implementation of passive elements. The microstrip lines are realized using the top metal M4 and M2 as the ground plane. The width of the ground plane is set three times larger than the width of the signal line. The smallest available pad measures 68×68 μm^2 and has a parasitic capacitance C_{PAD} 25 fF. Metal-insulator-metal (MIM) capacitors as well as TaN and polysilicon resistors are also provided in B7HF200 process. The key features of the technology and the cross section of the metal layer stack are presented in Fig. 3.

III. ACTIVE CIRCUITS: POWER AMPLIFIER AND DRIVER

Illustrated in Fig. 4 is the circuit schematic for the driver and the PA. For simplicity, the biasing circuits that enable the amplifier to operate from a single dc supply voltage VCC are excluded in the schematic. To provide sufficient power gain as well as output power and to isolate the output from the input in order to minimize the Miller effect, the amplifier employs the classic cascode topology, i.e., a common-emitter (CE) $\mathrm{T_1}$–$\mathrm{T_2}$ followed by a common-base (CB) $\mathrm{T_3}$–$\mathrm{T_4}$ in a differential fashion. The differential architecture is preferred to the single-ended one as it removes all even-mode harmonics

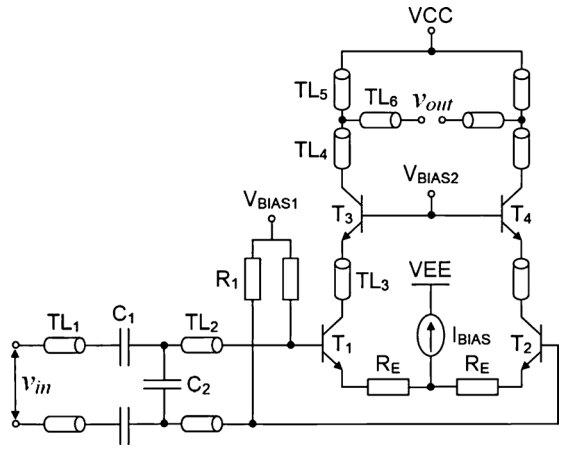


Fig. 4. Simplified schematic of a single-stage cascode PA including the input and output matching networks.

and offers high common-mode rejection ratio (CMRR) for a better noise immunity. The cascode stage is emitter degenerated in order to improve bandwidth and to avoid thermal runaway. Input matching elements $(\mathrm{TL_1}$–$\mathrm{TL_2}, C_1$–$C_2)$ and output matching elements $(\mathrm{TL_4}$–$\mathrm{TL_6})$ are also incorporated in the amplifier cell. Their values are given in Table I. The series capacitance C_1 also functions as a dc-blocking capacitance. The differential input and output ports are matched to 50 Ω rather than 100 Ω, so as to allow higher current swing to achieve the same output power level. This is aimed to prevent the transistors entering the avalanche breakdown region that is not included in the present transistor's model. The tail current I_{BIAS} is set to 50 mA in the PA cell and to 16.7 mA in the driver cell. The biasing circuits consume 17 and 10.7 mA in the PA and driver cells, respectively. For optimum thrust operation, the transistors $\mathrm{T_1}$–$\mathrm{T_4}$ should be biased at 5 mA/μm^2 collector current density, resulting in a tail current 70 mA, i.e., $(0.35–0.17) \times (40–0.17) \times 5$.

Note that in this first design attempt, the PA and the driver including the biasing circuits as a whole are not fully optimized for high-efficiency performance. For example, the output referred 1 dB compression point, $OP_{-1\mathrm{dB}}$, of the driver cell is 3–4 dB higher than what is needed to drive the PA cell into saturation and therefore consume more currents. Equally important, the current consumption of the biasing circuits that stands at 42% as much as that of the PA and driver core circuits combined could be effectively reduced so as to maximize the overall PAE.

Fig. 5 shows the simulated S-parameter of the driver cell cascaded with the PA cell. The input and output return losses are higher than 10 dB from 81 to 94.5 GHz and from 79 to 90 GHz, respectively. The small-signal gain of at least 18 dB is obtained within 66.7–88.6 GHz bandwidth and it reaches the peak 23 dB at 80.5 GHz. The isolation is higher than 60 dB across the simulated frequencies.

IV. PASSIVE STRUCTURES: POWER-SPLITTING/COMBINING TRANSFORMER AND ROUTING LINE

The design of a power-combining transformer involves a number of iterative optimization procedures with the primary aim to obtain the lowest insertion loss possible. There are two

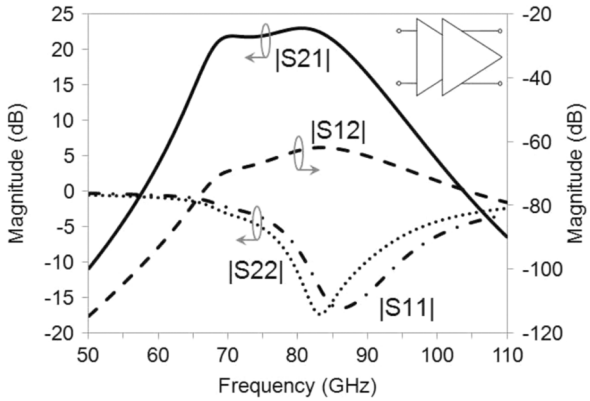


Fig. 5. Simulated S-parameter of the two-stage cascode PA.

key factors that contribute to the loss of the combiner, namely, magnetic coupling factor (k) and port mismatch.

The proposed eight-way single-ended or four-way differential combining transformer (4WDCT) is illustrated in Fig. 6. The vertical broadside-coupled structure is adopted here since it offers higher k than the horizontal edge-coupled counterpart. Two input windings are realized on M2 and M4 while M3 is used for the output winding. Each input winding has two pairs of differentially excited ports while the output winding has only one pair. If one of these output ports is grounded, the combiner will simultaneously exhibit as a BALUN. RF currents coming out from the PA array will circulate in the input windings producing a set of magnetic flux. This magnetic flux is induced to the output winding, generating an RF current that will flow to the load. Four differential ports in the input windings are arranged perpendicular to one another so as to prevent energy being transferred between them. Since the number of turns of the output winding is twice that of the input winding, the impedance seen at each input port should ideally be one quarter of the load impedance. This means that the output PA connected to the input of the power-combining transformer can be matched to lower impedances, relaxing the voltage stress on the transistors.

Design parameters that are typically optimized include the transformer radius and the trace width. The transformer radius is a strong function of the input susceptance and therefore it critically contributes to the port mismatch. In addition, shunt capacitance $C_{\rm Y}$, Fig. 2, is added to the input transformer ports to further improve the port mismatch. The transformer radius also determines the self-resonance frequency (SRF), i.e., the smaller the radius, the lower the inductance, the higher the SRF. It is important to make sure that the SRF is sufficiently far above the operating frequency. Meanwhile, the trace width determines the unloaded Q-factor of the metal winding self-inductance, i.e., the wider the trace, the lower the parasitic electrical series resistance (ESR), the higher the Q. Ideally, the trace width is set to the maximum metal width allowed by the technology but this may require larger chip area. Further, in cases where the combining transformer is also intended to provide dc access, i.e., to bias the PAs, it is vital that the trace width complies with the maximum current density of the metal winding. The inner diameter of the octagon-shaped 4WDCT in Fig. 6 is 50 μm and the trace width is 5 μm.

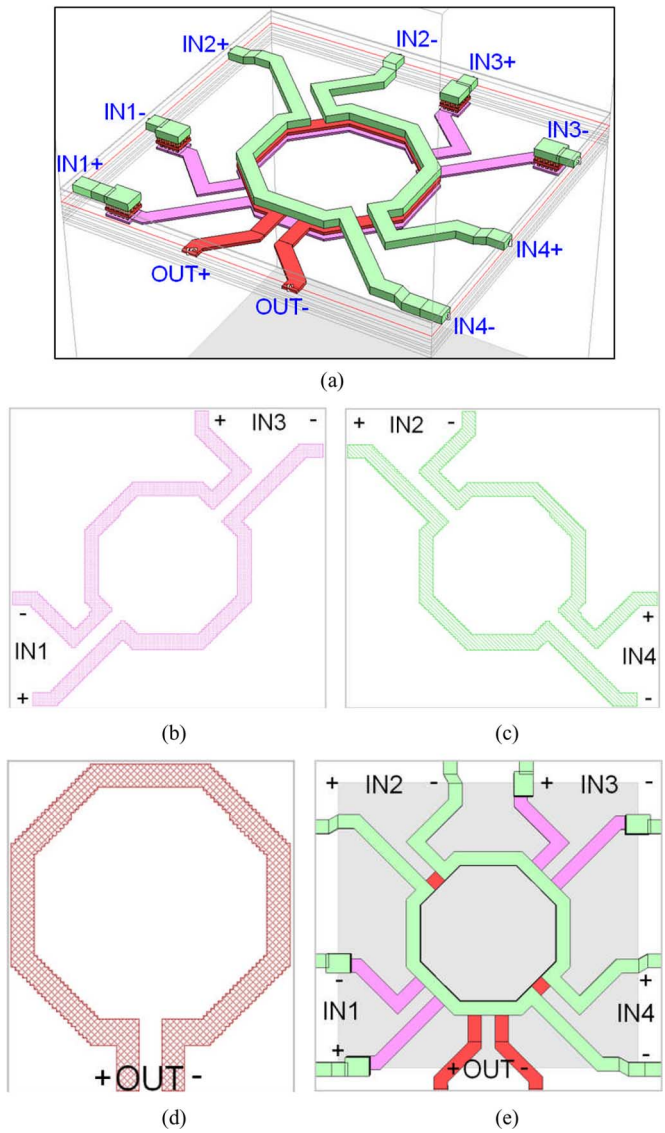


Fig. 6. Proposed four-way differential combining transformer (4WDCT). (a) 3-D view. (b) Input winding #1 on M2. (c) Input winding #2 on M4. (d) Output winding on M3. (e) Top view.

Due to the symmetry of the structure, the input impedances seen at port 1 and 3 are identical. The same applies to the impedances at port 2 and 4. On the other hand, since the electrical properties of M2 and M4 are not equivalent, it is expected that $\{Z_{\rm IN1} = Z_{\rm IN3}\} \neq \{Z_{\rm IN2} = Z_{\rm IN4}\}$. The S-parameters of the 4WDCT simulated in SONNET are plotted in Fig. 7. Here, the differential ports of the input transformers are terminated with the shunt capacitance $C_{\rm Y}/2$ in parallel with 50 Ω resistance. One of the ports of the output transformer is grounded whereas another one is terminated with $C_{\rm PAD}$ in parallel with 50Ω resistance. The output return loss $|{\rm S55}|$ is higher than 10 dB from 70 to 92 GHz. As predicted, it is observed that $\{|{\rm S51}| = |{\rm S53}|\} \neq \{|{\rm S52}| = |S54|\}$ across the frequency band of interest. At 83.5 GHz, $|{\rm S51}| = |{\rm S53}| = -6.9$ dB, $|{\rm S52}| = -7.7$ dB, and $|{\rm S54}| = -7.5$ dB. This means that if 0 dBm RF power is injected at port 5, the combined power appear at port 1–4 will be $10 \times \log(10^{-0.69} + 10^{-0.69} + 10^{-0.77} + 10^{-0.75}) = -1.25$ dBm, implying a loss of 1.25 dB or equivalent to 75%

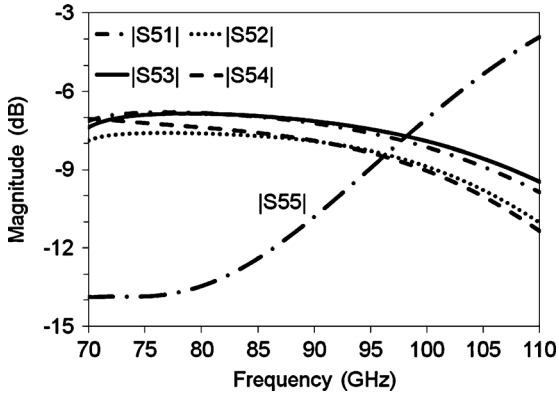


Fig. 7. Simulated insertion loss and output return loss of the 4WDCT.

TABLE II
COMPARISON WITH STATE-OF-THE-ART MILLIMETER-WAVE POWER COMBINERS

Reference	Tech.	Type	Freq. (GHz)	N-way (single-ended)	Loss (dB)
[1]	CMOS	Transformer	60	2-way	0.9
[2]		Transformer	60	4-way	0.63
[3]		Transformer	60	4-way	1.2
[4]		Transformer	77-81	4-way	0.8
[10]	SiGe	Transformer	77/79	4-way	1.2
[11]		Wilkinson	77	2-way	0.46
[12]		Transformer	77	2-way	6.6
This work		Transformer	83.5	8-way	1.25

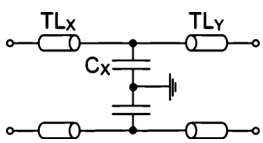


Fig. 8. Routing lines with capacitive compensators.

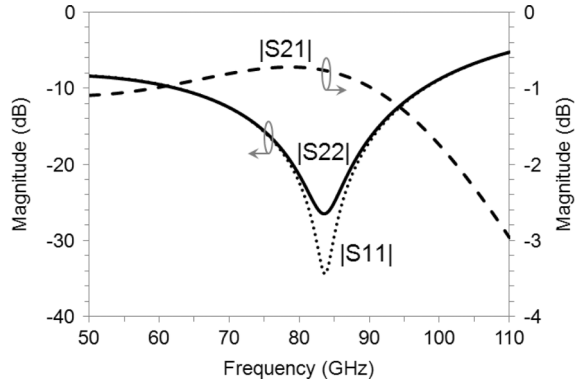


Fig. 9. Simulated return loss and insertion loss of the routing-line element.

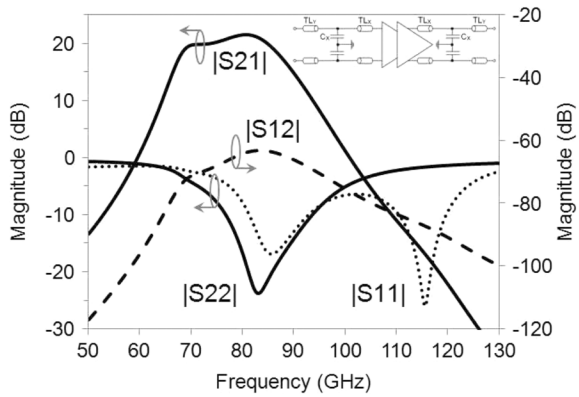


Fig. 10. Simulated S-parameter of the two-stage cascode PA with routing-line elements connected at its input and output.

efficiency. This result is also confirmed by the harmonic-balance (HB) simulation in ADS and SPECTRE. The insertion loss of the proposed 4WDCT is compared to state-of-the-art millimeter-wave power combiners in Table II.

Up to this point, the designs of the driver and PA cells as well as the 4WDCT have been discussed independently. One of the remaining challenges is associated with the technique to connect the output of the PAs to the input of the 4WDCT. Used as routing lines are the series microstrip lines, $\mathrm{TL_X}$ and $\mathrm{TL_Y}$, which together with the shunt capacitance C_X form a low-pass filter. This is depicted in Fig. 8 and their values are given in Table I. These routing lines have to be designed accurately with attentive care as any presence of amplitude and/or phase imbalance among the eight paths would cause the signals not being combined constructively and therefore would deteriorate the overall circuit performance. Fig. 9 shows the simulated return loss and insertion loss of the routing-line element. Broadband input and output matching are achieved. Insertion loss is lower than 0.8 dB from 70.5 to 85 GHz.

Simulated S-parameters of the two-stage cascode PA with routing-line element attached to both its input and output are plotted in Fig. 10. Compared with Fig. 5, the I/O matching and the reverse transmission are not substantially altered although it appears from the $|\mathrm{S11}|$ plot that the routing-line elements introduce a new higher-frequency pole at around 115 GHz. The small-signal gain of at least 18 dB is obtained within 68–87 GHz bandwidth and it reaches the peak 21.4 dB at 80.5 GHz. This peak is 1.6 dB lower than that in Fig. 5 due to 0.8 dB loss introduced by each routing-line element.

Simulated power gain versus output power of the two-stage cascode PA with and without the routing-line elements are presented in Fig. 11. The 1.6 dB reduction in small-signal gain agrees well with the S-parameter results. The routing-line element at the output of the PA reduces $OP_{-1\ \mathrm{dB}}$ to 12 from 12.9 dBm.

V. MEASUREMENT RESULTS

The chip microphotograph of the complete PA is shown in Fig. 12. It occupies $675 \times 1264\ \mu\mathrm{m}^2$ active die area. Each PA/driver cell including the biasing circuits measures $130 \times 260\ \mu\mathrm{m}^2$. The amplifier was characterized through on-chip measurements with 100 μm pitch GSG probes used to probe both input and output ports.

For the S-parameter measurements, the circuit was operated from a single dc supply voltage $\mathrm{VCC} = 3.2$ V. The measured and simulated S-parameter results are compared in Fig. 13 with good agreements observed. The simulation is able to accurately predict the small-signal gain $|\mathrm{S21}|$ of the PA up to about 86 GHz, above which the measured gain rolls off more rapidly than the simulated one. Broadband characteristic is observed in

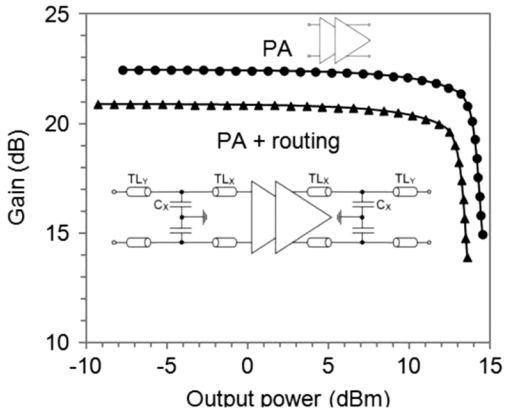


Fig. 11. Simulated power gain versus output power of the two-stage cascode PA with and without the routing-line elements.

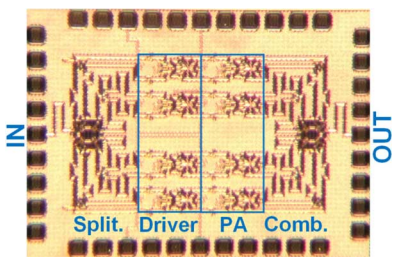


Fig. 12. Chip microphotograph of the complete PA including the 4WDCT.

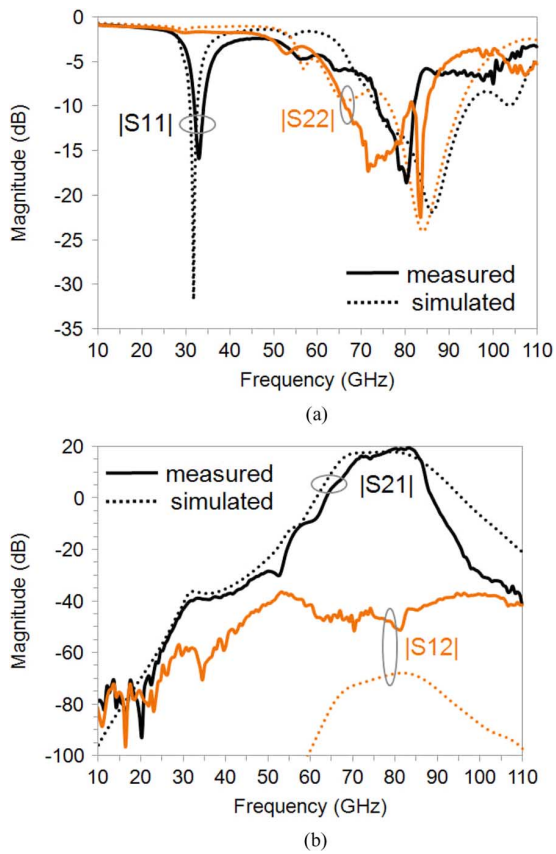


Fig. 13. Measured and simulated (a) return loss, (b) small-signal gain, and reverse transmission.

the simulation where gain of at least 15 dB is obtained from 67.5 to 85.4 GHz. It reaches a peak 17.9 dB at 80.3 GHz. On the other hand, narrower characteristic but with higher peak is observed in the measurement. Measured small-signal gain of at least 16.8 dB is obtained from 76.4 to 85.3 GHz with a peak 19.5 dB at 83 GHz. The simulated peak gain of the complete PA, 17.9 dB, is 3.5 dB lower than that in Fig. 10 at the same frequency around 80.5 GHz. This is due to $2 \times 1.25 = 2.5$ dB loss in the power splitter and combiner as well as $2 \times 0.5 = 1$ dB loss in the I/O matching elements. Excellent isolation |S12| higher than 68 dB is achieved in the simulation. However, due to parasitic coupling through substrate, the measured isolation is about 20 dB lower than the simulated one.

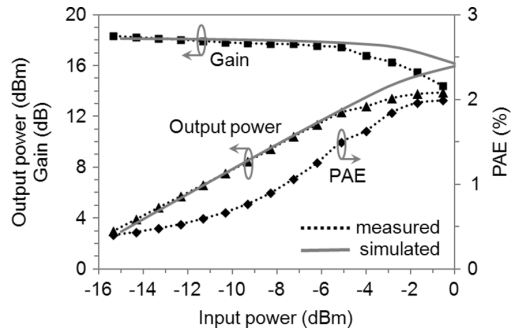


Fig. 14. Output power, power gain, and PAE versus input power at 78 GHz for VCC = 3.2 V.

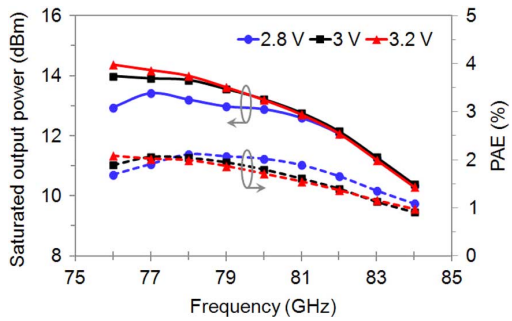


Fig. 15. Measured saturated output power and PAE versus frequency for VCC = 2.8, 3, and 3.2 V.

TABLE III
COMPARISON WITH RECENTLY PUBLISHED MILLIMETER-WAVE PAS

Ref.	Tech. f_T/f_{max} (GHz)	Freq. (GHz)	V_{DC} (V)	Gain (dB)	OP-1dB (dBm)	P_{sat} (dBm)	Peak PAE (%)	P_{DC} (mW)	Area (mm²)
[1]	90 nm CMOS	60	1.0	5.6	9	12.3	8.8	-	0.25
[6]	65 nm CMOS	77	1.2	13.7	6.7	10.5	8.4	115	-
[7]	90 nm CMOS	77	1.2	12.4	4.8	9.1	7.6	68.4	0.6
[8]	0.12 μm SiGe 207/285	77	2.5	6.1	11.6	12.5	2.5	325	1.58
[9]	0.13 μm SiGe 200/-	85	-2.5/ +0.8	8	-	21	3.4	2475	2.4
[11]	0.25 μm SiGe 180/200	75-80	3.5	>17	-	3.4	1	210	2.25
[12]	0.13 μm SiGe 230/280	77	2.5	25	9	14.5	9	250	0.24
[13]	0.13 μm SiGe 160/175	77	2.5	18.5	11	12	4.7	350	-
[14]	0.13 μm SiGe 230/280	77	1.8	13.5	6.2	13	2.2	270	1.12
This work	0.18 μm SiGe 170/250	78	3.2	18.3	12.5	14	2	1325	0.85

Output power, power gain, and PAE of the PA at 78 GHz for VCC = 3.2 V are plotted against input power in Fig. 14. The

simulated and measured power gain slightly over 18 dB are in a good agreement. The measured $OP_{-1\mathrm{dB}}$ is 12.5 dBm compared to 15 dBm in the simulation and the measured saturated output power, P_{sat}, is 14 dBm, almost 2 dB lower than that predicted in the simulation. This disagreement is primarily due to inaccurate modeling of the active device, for instance, the avalanche breakdown is not accounted in the present model. Further, presented in Fig. 15 are the measured P_{sat} and PAE of the PA across the frequency band of interest 76–84 GHz for a set of VCC values. With $\mathrm{VCC} = 3.2$ V, the PA is able to deliver output power of at least 10.3 dBm. The performance matrix of the proposed PA is summarized and compared with other recently published millimeter-wave PAs in Table III.

VI. Conclusion

The working principle of the novel four-way differential power-combining transformer for use in millimeter-wave PAs has been demonstrated. The combiner was implemented in SiGe technology and it exhibits a record high efficiency of 75% equivalent to 1.25 dB loss at 83.5 GHz. The combiner was validated through small-signal and large-signal measurements of the complete circuit that includes four driver cells and four medium-power PA cells. Design strategy to connect the PA and the combiner without causing substantial performance degradation has also been discussed in a great detail.

References

[1] D. Chowdhury, P. Reynaert, and A. M. Niknejad, "A 60 GHz 1 V + 12.3 dBm transformer-coupled wideband PA in 90 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2008, pp. 560–561.

[2] J. Chen and A. M. Niknejad, "A compact 1 V 18.6 dBm 60 GHz power amplifier in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2011, pp. 432–433.

[3] D. Zhao, S. Kulkarni, and P. Reynaert, "A 60 GHz outphasing transmitter in 40 nm CMOS with 15.6 dBm output power," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2012, pp. 170–172.

[4] K.-Y. Wang, T.-Y. Chang, and C.-K. Wang, "A 1 V 19.3 dBm 79 GHz power amplifier in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2012, pp. 260–261.

[5] T.-Y. Chang, C.-S. Wang, and C.-K. Wang, "A 77 GHz power amplifier using transformer-based power combiner in 90 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, San Jose, CA, Sep. 2010, pp. 1–4.

[6] Y. A. Li, M. H. Hung, S. J. Huang, and J. Lee, "A fully integrated 77 GHz FMCW radar system in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2010, pp. 216–217.

[7] J. Lin, K. To, D. Hammock, B. Knappenberger, M. Majerus, and W. Huang, "Power amplifier for 77-GHz automotive radar in 90-nm LP CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 5, pp. 292–294, May 2010.

[8] U. R. Pfeiffer, S. K. Reynolds, and B. A. Floyd, "A 77 GHz SiGe power amplifier for potential applications in automotive radar systems," in *IEEE Radio Freq. Integr. Circuits (RFIC) Symp. Dig.*, Fort Worth, TX, Jun. 2004, pp. 91–94.

[9] E. Afshari, H. Bhat, X. Li, and A. Hajimiri, "Electrical funnel: A broadband signal combining method," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, San Francisco, CA, Feb. 2006, pp. 751–760.

[10] Y. Zhao, J. R. Long, M. Spirito, and A. B. Akhnoukh, "A +18 dBm, 79–87.5 GHz bandwidth power amplifier in 0.13 μm SiGe-BiCMOS," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meeting (BCTM)*, Atlanta, GA, Oct. 2011, pp. 17–20.

[11] L. Wang, J. Borngraeber, W. Winkler, and C. Scheytt, "A 77 GHz MMIC power amplifier driver for automotive radar," in *IET Int. Conf. Radar Syst.*, Edinburgh, U.K., Oct. 2007, pp. 1–4.

[12] V. Giammello, E. Ragonese, and G. Palmisano, "A transformer-coupling current-reuse SiGe HBT power amplifier for 77-GHz automotive radar," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1676–1683, Jun. 2012.

[13] V. Giammello, E. Ragonese, and G. Palmisano, "Transmitter chipset for 24/77-GHz automotive radar sensors," in *IEEE Radio Freq. Integr. Circuits (RFIC) Symp. Dig.*, Anaheim, CA, May 2010, pp. 75–78.

[14] N. Demirel, E. Kerherve, D. Pache, and R. Plana, "Design techniques and considerations for mm-wave SiGe power amplifiers," in *Proc. IEEE Int. Microw. Optoelectron. Conf. (IMOC)*, Belem, Brazil, Nov. 2009, pp. 37–41.

[15] Y. Zhao and J. R. Long, "A wideband, dual-path, millimeter-wave power amplifier with 20 dBm output power and PAE above 15% in 130 nm SiGe-BiCMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 1981–1997, Sep. 2012.

[16] J. Böck, H. Schäfer, K. Aufinger, R. Stengl, S. Boguth, R. Schreiter, M. Rest, H. Knapp, M. Wurzer, W. Perndl, T. Böttner, and T. F. Meister, "SiGe bipolar technology for automotive radar applications," in *Proc. IEEE Bipolar/BiCMOS Circuits Technol. Meet.*, Montreal, QC, Canada, Sept. 2004, pp. 84–87.

[17] M. Thian and V. Fusco, "Power combining techniques into unbalanced loads for class-E and inverse class-E amplifiers," *IET Microw. Antennas Propag.*, vol. 2, no. 6, pp. 529–537, Sep. 2008.

[18] M. Thian, V. Fusco, and P. Gardner, "Power-combining class-E amplifier with finite choke," *IEEE Trans. Circuits Syst. I., Reg. Papers*, vol. 58, no. 3, pp. 451–457, Mar. 2011.

Mury Thian received the B.Sc. degree from the Atma Jaya Catholic University, Jakarta, Indonesia, the M.Sc. degree from the Delft University of Technology, the Netherlands, and the Ph.D. degree from the Queen's University of Belfast, U.K., all in electronics engineering.

He was with Astra International ISUZU, Jakarta, Indonesia; NXP Semiconductors, Nijmegen, the Netherlands; the University of Birmingham;, and the ECIT Institute, Belfast, U.K., before joining Infineon Technologies, Villach, Austria. He has authored over 30 journal and conference papers and coauthored a book chapter.

Dr. Thian was a session Cochair during the *2010 Asia Pacific Microwave Conference* in Yokohama, Japan, and was the 2008 finalist of the British Association for the Advancement of Science.

Marc Tiebout (S'90–M'93) was born in Asse, Belgium, in 1969. He received the M.Sc. degree in electrical and mechanical engineering from the Katholieke Universiteit Leuven, Leuven, Belgium, in 1992, and the Ph.D. degree in electrical engineering from the Technical University of Berlin, Berlin, Germany, in 2004.

In 1993, he joined Siemens AG, Corporate Research and Development, Microelectronics, Munich, Germany, designing analog integrated circuits in CMOS and BiCMOS technologies. In 1997, he started the design of radio frequency devices and building blocks in subμm CMOS technologies. From 1999 to 2005, he was with Infineon Technologies AG, Munich, Germany, where he worked on RF CMOS circuits and transceivers for cellular wireless communication products and conducted highest frequency RF CMOS research for 17 and 24 GHz applications. Since 2006, he is with Infineon Technologies, Villach, Austria, where his work includes Wimedia-UWB CMOS SoC development (system architect) and highest frequency phased-array radar applications. He has authored and coauthored more than 60 IEEE publications and holds more than 10 patents. His interest goes into RFIC design in Silicon Technologies.

Neil B. Buchanan received the B.Eng.(Hons.) degree from the Queens University of Belfast, Belfast, U.K., in 1993, and the Ph.D. degree with a dissertation entitled "Phase locked millimeter-wave HEMT oscillators" from the same university in 2000.

He is currently employed as a Senior Engineer within the High Frequency Electronics Group, Queen's University of Belfast. He has published over 40 papers in refereed journals and conferences and has provided consultancy to a number of companies. His research interests include self-steered (retro-directive) antennas, super regenerative detectors, injection-locked oscillators, and millimeter-wave MMIC design.

Dr. Buchanan has acted as Technical Manager for a number of research/industrial projects and has refereed IEE/IEEE journals and conferences.

Vincent Fusco (S'82–M'82–SM'96–F'04) received the Bachelor's degree in electrical and electronic engineering (first class honors) and the Ph.D. degree in microwave electronics from the Queen's University of Belfast, Belfast, U.K.

Since 1995, he has held a personal chair in high frequency electronic engineering. The main focus for this research is in the area of wireless communications. At present, he is Technical Director of the High Frequency Laboratories, ECIT (www.ecit.qub.ac.uk), where he is also Director of the International Center for Research for System on Chip and Advanced Microwireless Integration (SoCaM). He has published numerous scientific papers in major journals and in referred international conferences, and is the author of two text books. He holds several patents and has contributed invited chapters to books in the field of active antenna design and EM field computation. His research interests include nonlinear microwave circuit design, and active and passive antenna techniques.

Prof. Fusco is a Fellow of the Royal Academy of Engineering, a Fellow of the Institution of Engineering and Technology (IET), and of the Royal Irish Academy. In 1986, he was awarded a British Telecommunications Fellowship, and in 1997, was awarded the NI Engineering Federation Trophy for outstanding industrially relevant research.

Franz Dielacher (M'92–SM'09) received the M.S. and Ph.D. degrees in electrical engineering from the Graz University of Technology, Graz, Austria, in 1981 and 1990, respectively. His doctoral research was directed towards the modeling, simulation and design of oversampled analog-to-digital converters.

From 1981 until 1999, he worked for Siemens Semiconductor Group in circuit development and system integration for wireline and wireless communications. Since 1999, he has been with Infineon Technologies, Villach, Austria, in various positions in circuits and systems for communications like DSL, high-speed transceivers, wireless infrastructure, wireless connectivity and telecom standardization. Currently, he is a Senior Principal Engineer and Chief Scientist in the RF-Power Group. He is the author and coauthor of many scientific papers and several book chapters and holds many patents with several more pending. He has contributed to numerous conference and workshop presentations and is a lecturer at advanced engineering courses.

Dr. Dielacher's international involvement includes ISSCC TPC member from 2001 to 2011, ISSCC wireline subcommittee Chair, ESSCIRC TPC member, ESSCIRC technical program committee Chair in 2001, ESSCIRC steering board member since 2005, IEEE JSSC Guest Editor in 2002, SSCS AdCOM member since 2011 and conference Chair for Advances in Analog Circuit Design (AACD) in 1995. In 2000, he and his team received the Austrian Innovations Award.