22.6 On-Chip Interconnect for mm-Wave Applications Using an All-Copper Technolgy and Wavelength Reduction

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Silicon-based technologies with f_T's above 200GHz [1] promise to enable new broadband applications. Interconnects with comparable operating bandwidth are needed to complement high performance active devices. Presently, energy coupled into the semiconducting substrate at mm-wave frequencies (i.e., $\lambda < 10$mm or $f > 12$GHz on silicon) via the interconnect impairs circuit performance. This paper describes a new design that requires less chip area than other methods, has attenuation limited mainly by metal losses, and works well into the mm-wave range.

Resonant tanks, impedance matching networks, signal splitters, couplers and balun transformers are implemented with transmission lines. A wide range of characteristic impedance ($30\Omega < Z_0 < 300\Omega$), attenuation of 0.1-0.3dB/mm and compact physical size are needed for monolithic components. The length needed to realize a particular phase shift (e.g., $\lambda/4$ or $\lambda/2$) is defined by phase velocity (v) and frequency (f) of the travelling wave, since $\lambda = v/f$.

A top conductor over dielectric, silicon substrate and ground plane (MISM) is the simplest implementation. A true microstrip line consists of a conductor over a ground sheet (MIM) that is above the silicon substrate. Spacing between signal and return path greater than 50μm is required to realize Z_0 above 100Ω. This is not possible with an MIM line where the dielectric separating signal and ground is 3-10μm thick in most technologies. For the all-copper technology used here, a 6μm wide, 2.3μm thick top conductor gives Z_0 of 50Ω. To raise Z_0 further, the signal conductor must be narrowed which increases attenuation. A coplanar waveguide (CPW, Fig. 22.6.1) consists of a center conductor and adjacent grounds in the same plane. Wider conductors can be used with MISM and CPW lines to lower copper losses, but energy coupled to the silicon substrate increases overall attenuation [2]. For MIM, MISM and conventional CPW the wavelength on-chip is about one-half the free space wavelength, so millimeter wavelengths still require millimeter dimensions.

The new slow-wave coplanar configuration (S-CPW in Figs. 22.6.1 and 22.6.2) overcomes many of the limitations of existing designs. It consists of CPW top conductors where the gap between signal and ground is wide enough to achieve an inductance/unit length (L) comparable to an MISM line. Floating metal strips placed beneath the top conductors are oriented to minimize induced currents caused by current flow in the top-metal. This results in a capacitance/unit length C, similar to the MIM line. As a result, wave speed ($v = 1/\sqrt{LC}$) and wavelength are lower than for the other configurations, so distributed S-CPW devices use less chip area. Also, the signal conductor is wider for a given Z_0, thereby reducing copper losses. In addition, only a fraction of the electric field enters the silicon substrate via the floating strips, further reducing attenuation.

Four transmission line configurations are compared experimentally: MISM, MIM, CPW, and S-CPW. IBM's all-copper single damascene process on 10Ω-cm substrates is used for fabrication [3]. Top level (2.3μm AM) and second level (1μm LY) interconnected by 4μm vias (AV) are the elements from the wiring scheme of Fig. 22.6.3 used here. A 6μm thick oxide isolates the first wiring level (LY) from the semiconducting substrate. A novel low-erosion process for planarization of the copper reduces erosion to below 0.03μm in a 1μm thick solid copper (LY) film wider than 400μm. The S-CPW testline uses 420μm wide floating LY strips with minimum length and spacing (1.6μm). Coplanar AM grounds are placed 20μm away from a 16μm wide center conductor.

A 50Ω CPW consisting of a 55μm signal and 200μm wide grounds separated by a 20μm gap and fabricated using 2.5μm thick gold conductors on a polished alumina substrate, is used as a reference for comparison.

All transmission lines, except the MISM line are designed for a Z_0 of 50Ω. Measured Z_0 is plotted in Fig. 22.6.4 and is close to the design target except for the MISM line. Both MIM and S-CPW lines have Z_0 with little frequency variation comparable to the CPW reference on alumina.

Wave velocity ($v = 3x10^8/(\sqrt{\varepsilon_r})$, in m/s) and wavelength are inversely proportional to the square root of the relative permittivity, ε_r of the transmission line. Figure 22.6.5 shows ε_r versus frequency. The relative permittivity of the MIM line is approximately 4 over the entire frequency range, as expected (i.e., SiO_2 dielectric). The increase in the wave velocity with frequency for the MISM line causes dispersion of a broadband signal. The S-CPW line shows less variation and an ε_r as large as 20, indicative of wavelength reduction. Thus, an on-chip $\lambda/4$ line at 30GHz shrinks from 1.25 to 0.56mm when using S-CPW.

Quality (Q) factors are compared in Fig. 22.6.6. Q for the reference CPW (gold on alumina) increases almost continually with frequency, and peak Q's of 30-100 are typical for this technology. For the MISM line, Q is severely affected by energy lost to the silicon, limiting it to a peak of 8 at 3.5GHz. The MIM structure stores relatively little energy in the magnetic field resulting in a low Q-factor. The S-CPW configuration allows the magnetic field to fill a larger volume, and Q is improved by 2x compared to the MIM line over most of the range, and 3x in the mm-wave range between 31 and 33GHz.

Attenuation per mm of length (Fig. 22.6.7) is consistent with the Q-factor data. Results for MISM fabricated in aluminum from a production 0.35μm BiCMOS technology are also shown. The all-copper MISM interconnect has lower attenuation below 20GHz but shows a stronger frequency dependence at mm wavelengths. This may be related to substrate thickness, as a 400μm thick substrate is used for the copper vs. 200μm for the aluminum devices.

Acknowledgements
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[3] A. Joseph et al, "A 0.18mm BiCMOS technology featuring 120/100 GHz fT/fMAX HBT and ASIC-compatible CMOS using copper interconnect," IEEE BCTM, Minneapolis MN, September 2001, pp. 143-146.
[4] J. D. Jackson, "Classical Electrodynamics," Problem 5.29, 3rd ed., John Wiley & Sons, Inc., 1998.

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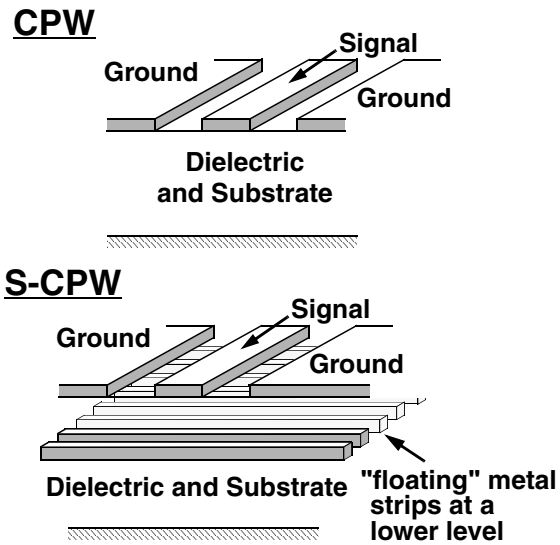

Figure 22.6.1: On-chip transmission lines.

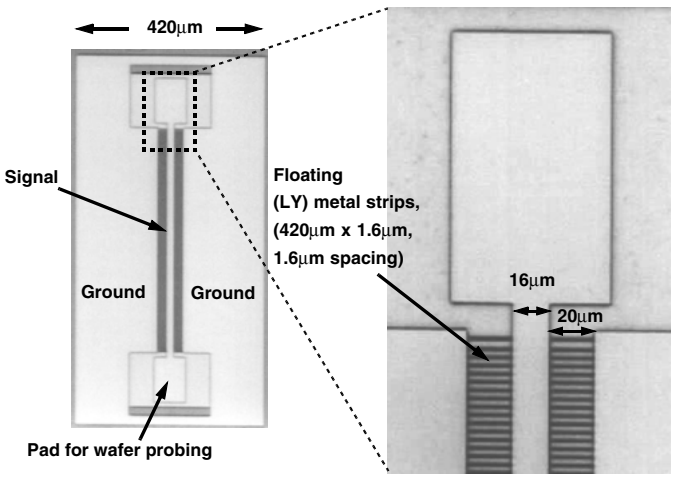

Figure 22.6.2: S-CPW (gap=20μm, width=16μm) micrograph.

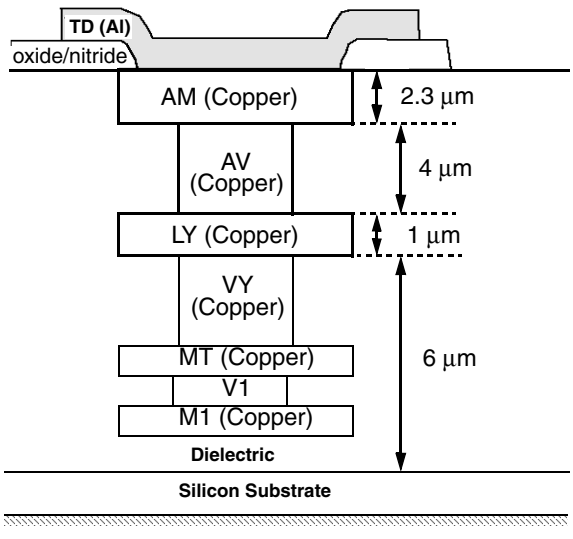

Figure 22.6.3: Cross-section of all-copper wiring scheme.

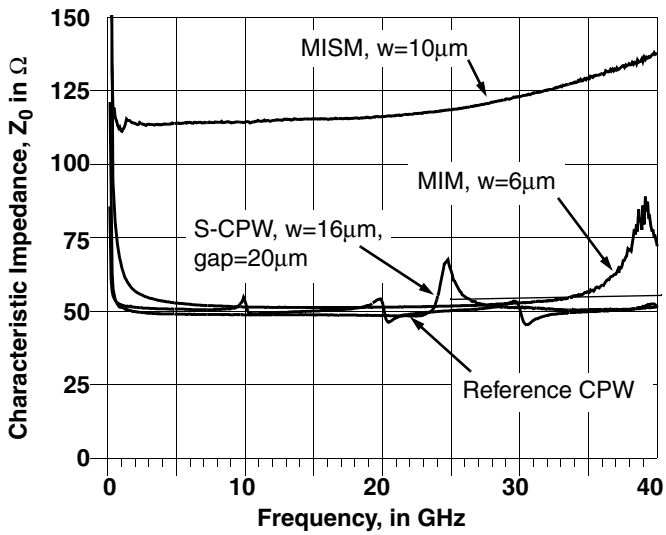

Figure 22.6.4: Measured characteristic impedance (Z_0).

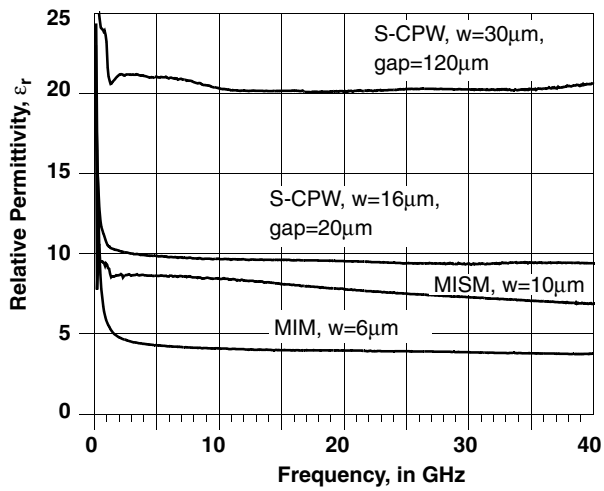

Figure 22.6.5 : Measured relative permittivity (ε_r).

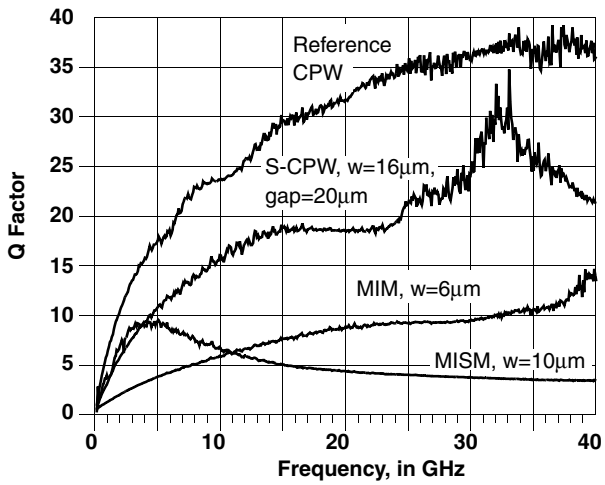

Figure 22.6.6: Measured transmission line Q factor.

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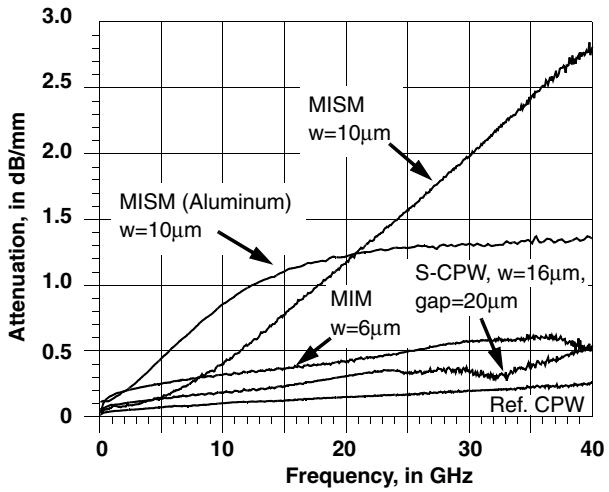

Figure 22.6.7: Measured attenuation per millimeter length.

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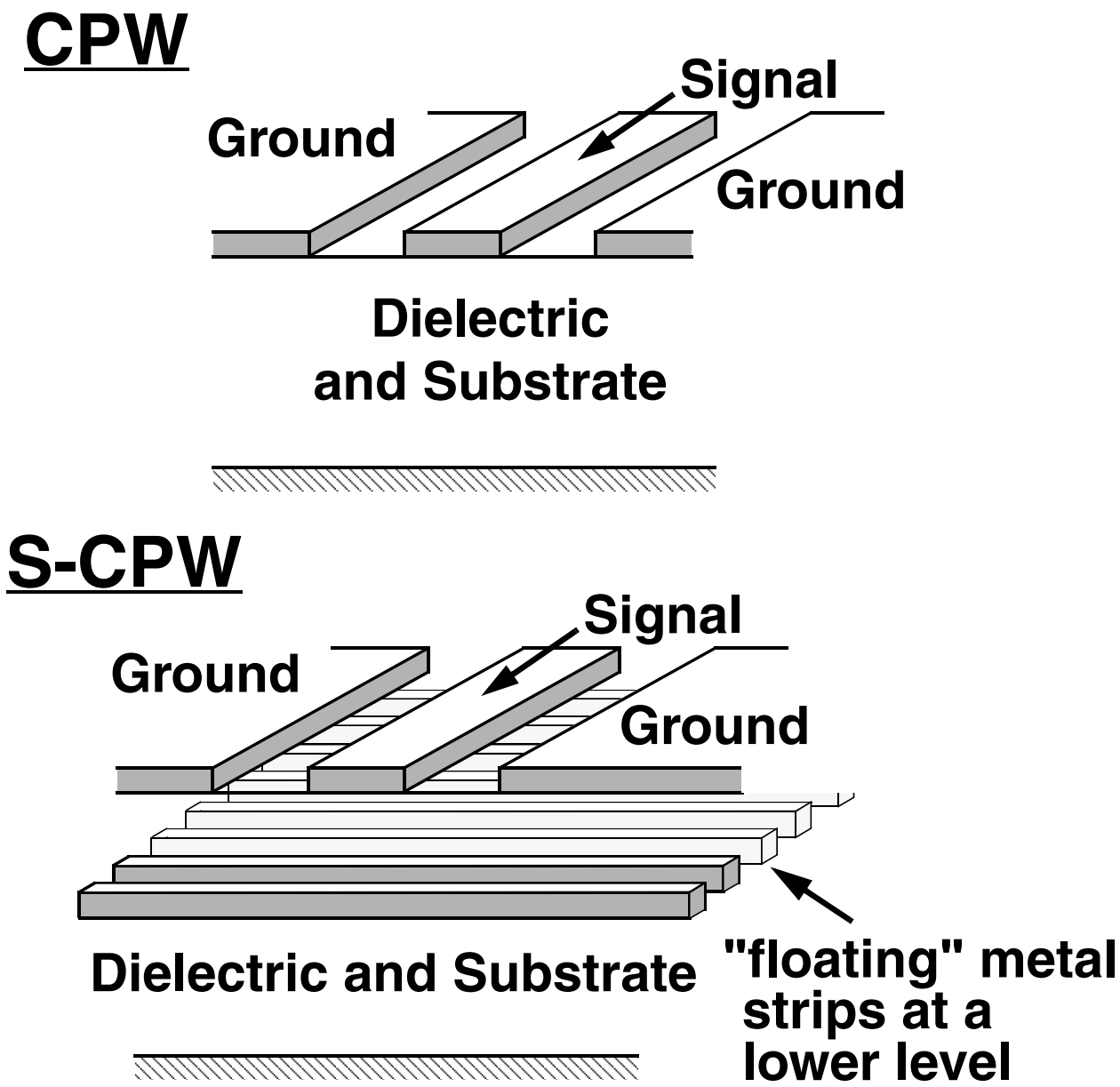

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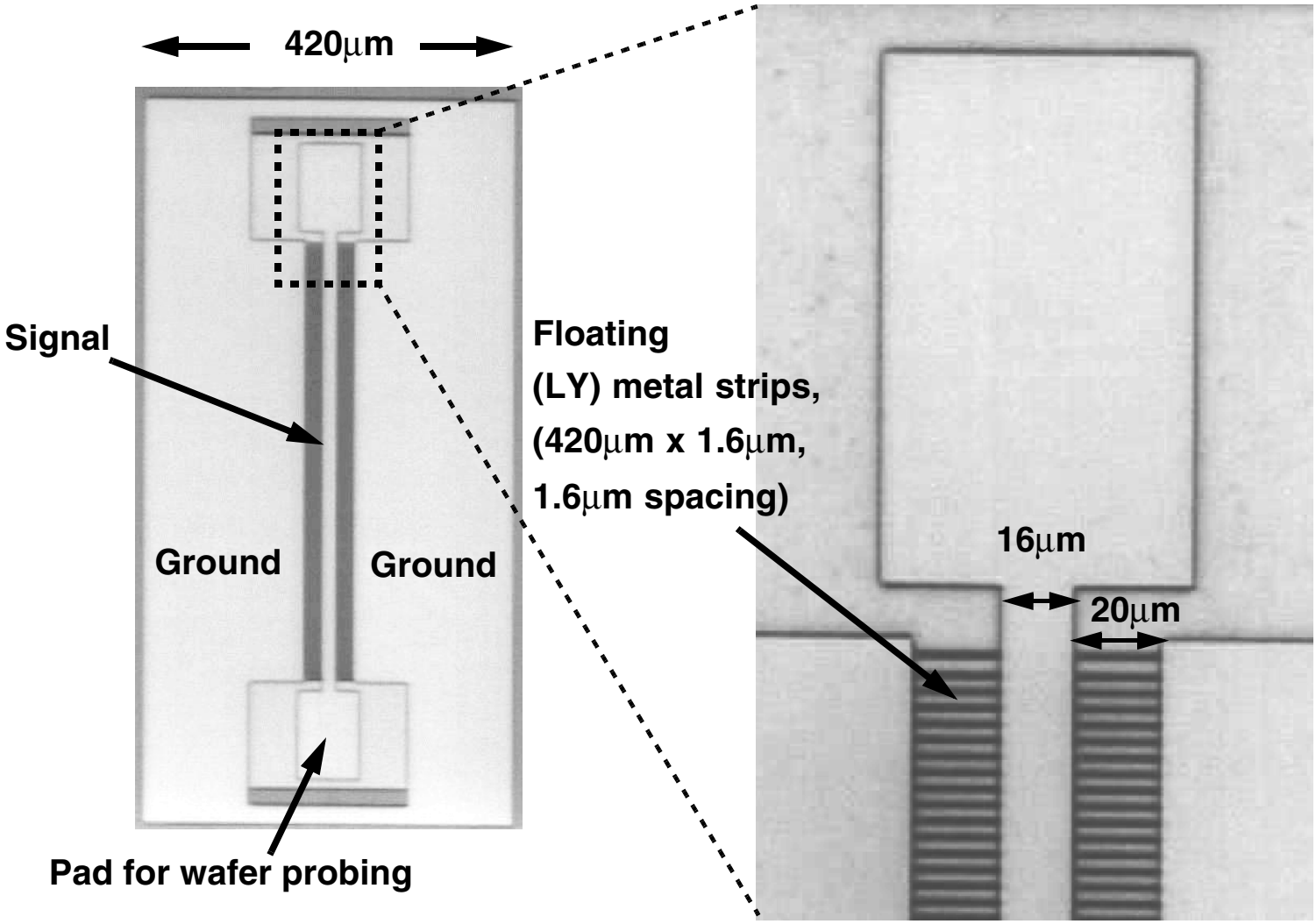

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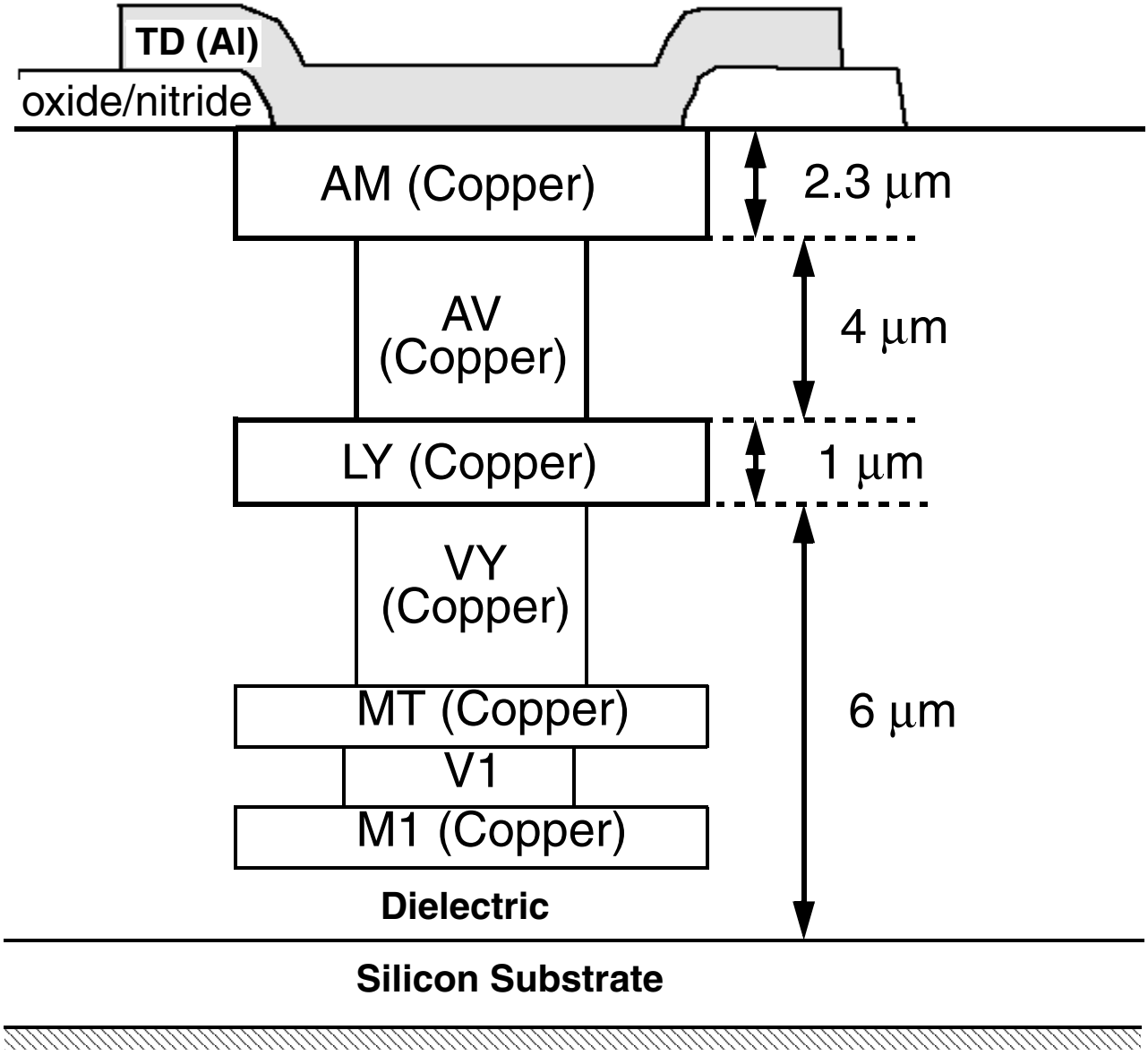

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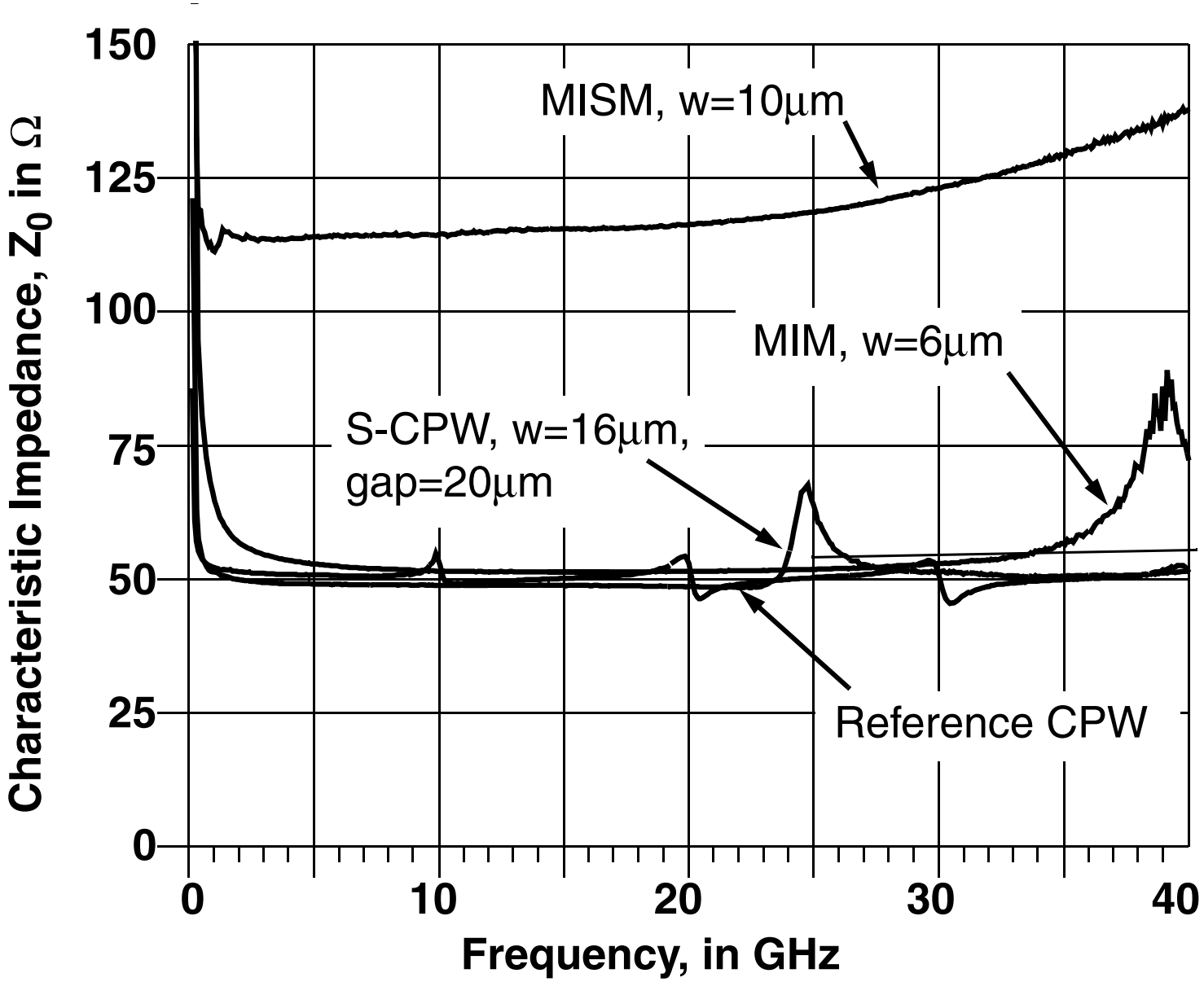

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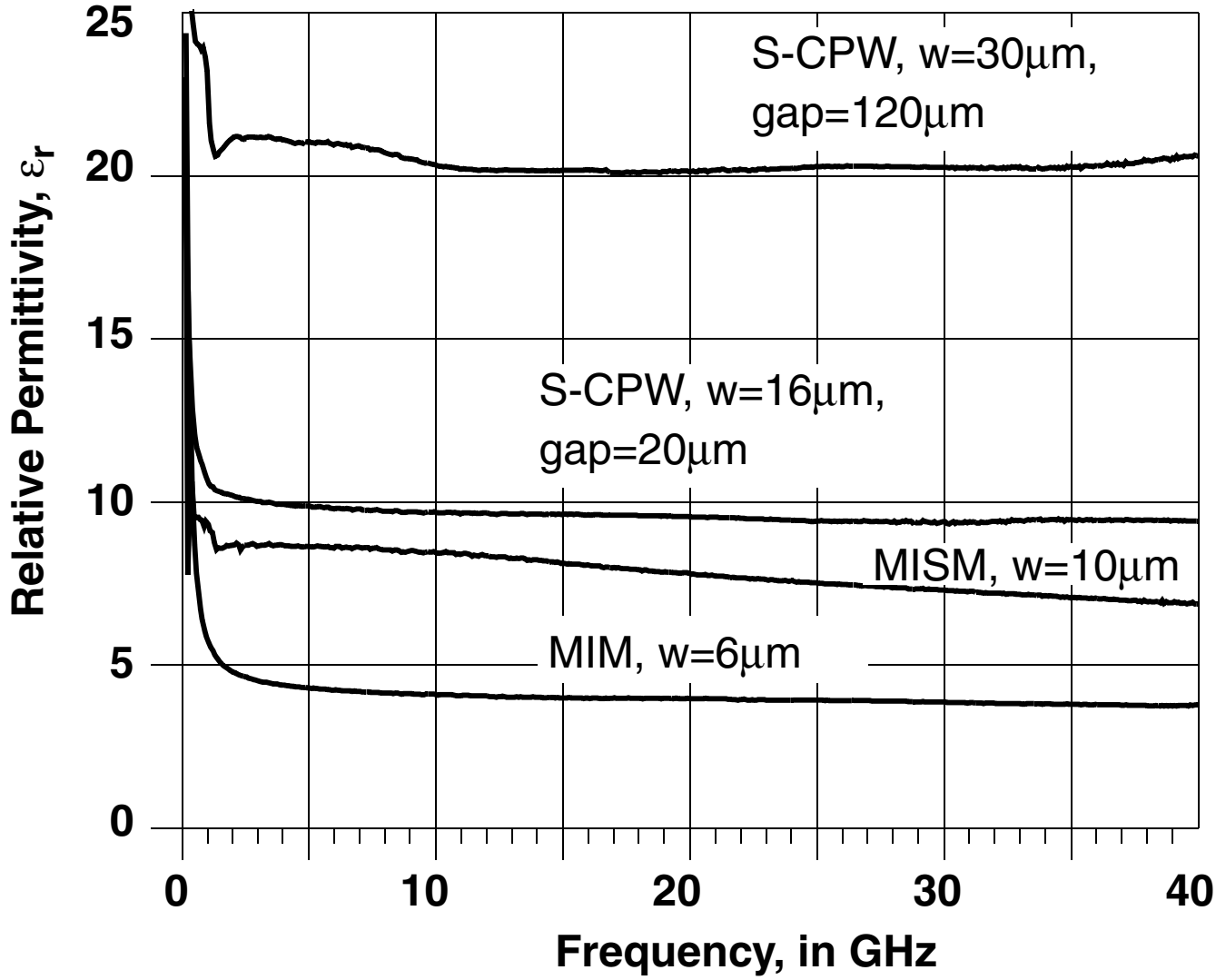

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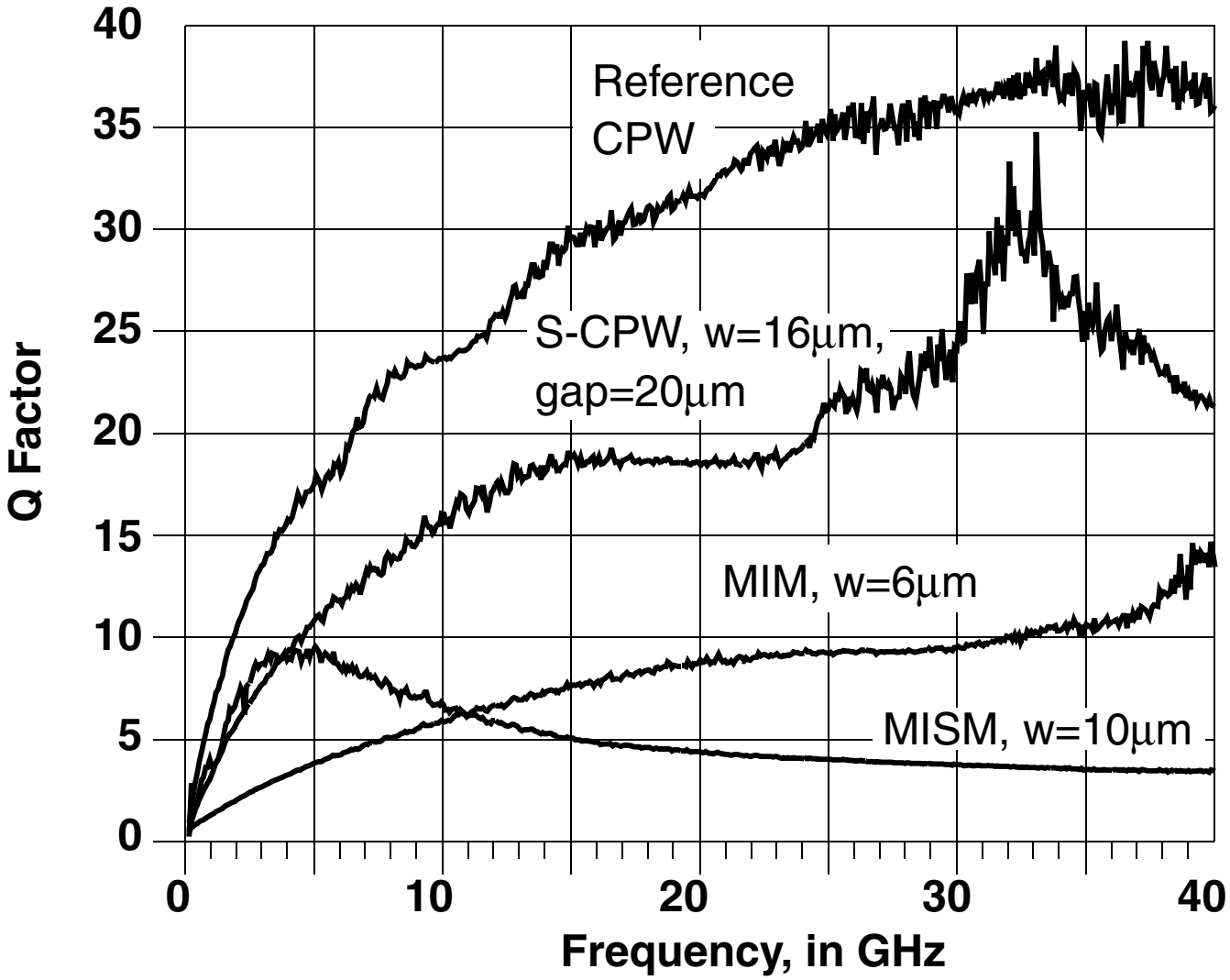

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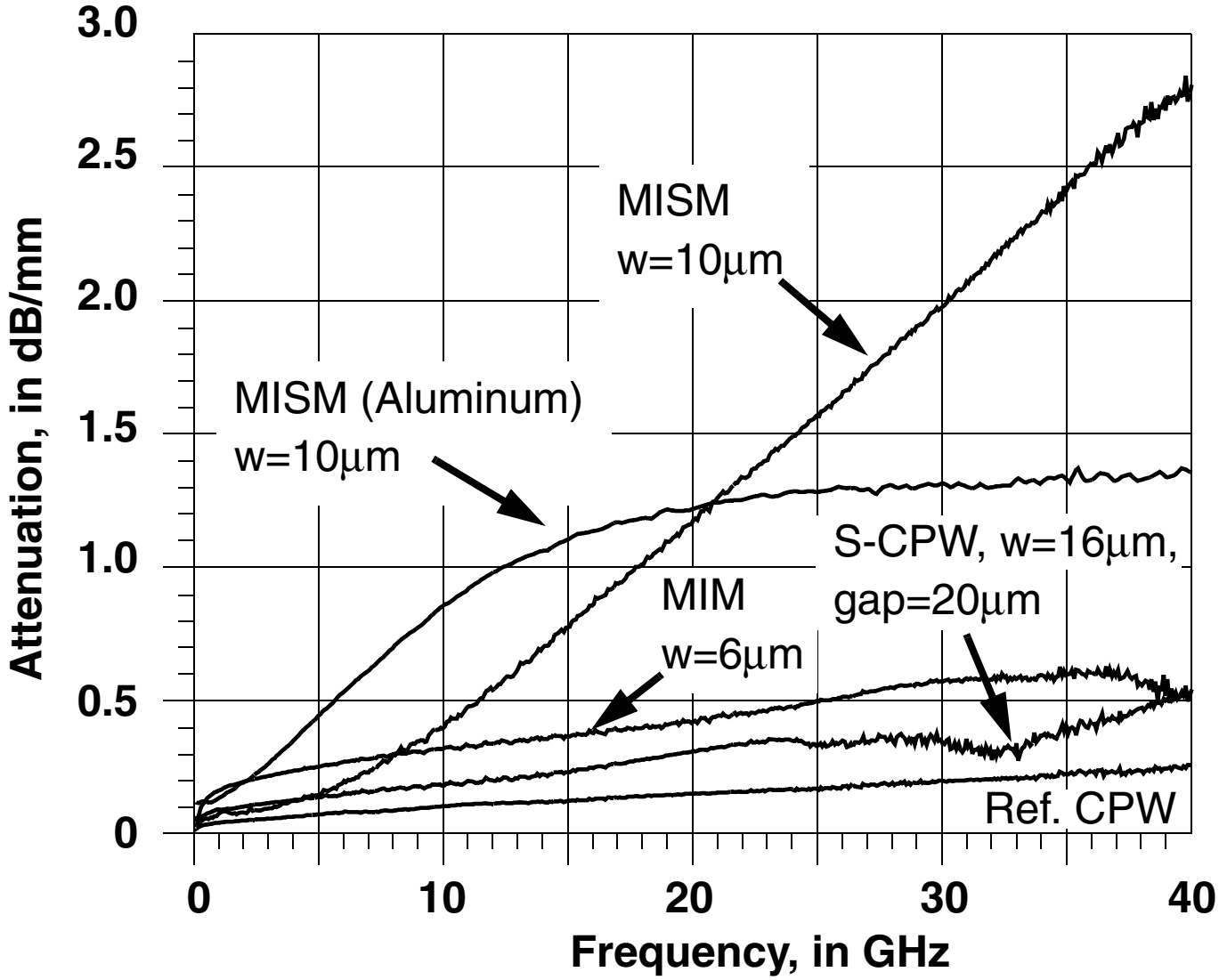

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