Millimeter-Wave and Terahertz Wireless RFIC and On-Chip Antenna Design: Tools and Layout Techniques

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***Abstract*—This invited contribution provides insights for implementation of millimeter-wave and terahertz wireless systems on a chip (MTWSOC). We present an overview of important software and simulation tools and key layout issues and design rules for millimeter-wave (mmWave) circuits. An example of a recently fabricated 0.18μm CMOS integrated circuit by the Wireless Networking and Communications Group (WNCG) at The University of Texas at Austin is presented. The example chip includes 60 GHz on-chip antennas, an array of transmission lines, and IMPATT diodes.**

***Index Terms*—60 GHz, millimeter-wave, on-chip antenna, IMPATT diode, CPW, Transmission Lines, RFIC, CMOS, WPAN, SOC, MTWS**

I. Introduction

Over the past 40 years, wireless carrier frequencies have increased only by an order of magnitude or so, from 400 MHz in early Improved Mobile Telephone Systems (IMTS) and analog cellular, to 5.8 GHz in today's IEEE 802.11a WiFi networks. Yet, due to improved semiconductor capabilities, over the next few years the carrier frequencies of wireless personal area network (WPAN) devices will exceed 60 GHz, most likely to surpass several hundred GHz, and moving into the terahertz range by 2020 [1]. Just as clock speeds and memory sizes have increased exponentially over the past two decades, wireless carrier frequencies are poised to see a similar increase, bringing massive bandwidths to the edge of the network. Communications researchers wishing to design and develop system prototypes at these millimeter-wave (mmWave) frequencies will need to be able to fabricate their own devices and integrate various communication circuit components due to the massive cost of mmWave discrete components, test equipment, and the interconnect losses that occur at such high frequencies. For example, imagine the cost and physical size involved with trying to build an RF channel sounder or MIMO test-bed using discrete test equipment at a 100 GHz carrier frequency. In order to rapidly fabricate and test prototypes and systems, researchers will need to make their own integrated RFICs for such exploration, since wavelengths are so small and discrete external exponents are extremely expensive and cumbersome as compared to eventual real-world implementation.

We envision on-board or on-chip antennas using socket solutions to avoid extensive runs of coaxial cables, thereby reducing bill of material costs and power consumption. Instead of using adaptive phased arrays with individual power amplifiers that drain battery life, as is currently being proposed by companies such as SiBEAM [2], we envision simple stand-alone on-chip antennas, that may be either active or passive, sprinkled throughout the case of a laptop or throughout a printed circuit board, and passively phased using transmission lines on simple printed circuit boards for switching/phasing to achieve a particular radiation pattern. As shown in [3, 4], such low cost, low power switchable antennas will become possible with antenna on a chip technology, and will offer greater degrees of freedom to the handheld device manufacturer in placing antennas and integrating them with the packaging of the handheld device.

This paper teaches the basic tools and techniques used to design and fabricate radio frequency integrated circuits (RFICs) with a focus on on-chip antennas, and provides some examples of actual ICs created at The University of Texas Wireless Networking and Communications Group (WNCG). While the communications research community has seldom crossed over to the circuit design community, the upward explosion of carrier frequencies will make such interdisciplinary interaction vital for wireless research at the edge of the network over the coming decades. Particularly as the wireless post-it note emerges, where content is moved from printed or magnetic media to semiconductor/chip form, and content is beamed wirelessly across a room or building, communications researchers and circuit designers/semiconductor process researchers will need to collaborate in order to create solutions for the future, both in research and product development.

II. RFIC Simulation and Design

Millimeter-wave and terahertz wireless systems (MTWS) on a chip are most inexpensively created in CMOS technology as opposed to more expensive SiGe or GaAs processes. To properly design and layout RFICs, simulation tools are required to predict performance of the physical layout. Transistor-level circuit simulators like Cadence Virtuoso Analog Design Environment (ADE) or Ansoft's Nexxim are important for

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analog/RF design, but electromagnetic (EM) field solvers are necessary in on-chip antenna design and structures such as feedlines and novel 3-D components. EM solvers predict important parameters such as impedances, losses, and, in the case of antennas, radiation patterns, and radiation efficiency. These tools attempt to accurately apply Maxwell's equations to solve for electromagnetic fields given a particular excitation such as a current or voltage source. These simulators use bounding volumes and other computationally efficient methods to trade off simulation time versus accuracy. The three main types of EM solvers are the Finite-Difference Time-Domain (FDTD) Method, the Finite Element Method (FEM), and the Method of Moments (MOM). Each method has particular advantages/disadvantages such as computational time, memory cost, scalability, etc., and a whole realm of research and implementation issues are well known [5, 6]. Typically, 3-D structures tend to be solved using the FEM method, whereas predominately planar structures such as those common on integrated circuits, tend to be solved using the MOM algorithm. Table I shows a list of various commercially available solvers and their respective methods. The particular solvers employed at UT's WNCG are Ansoft's HFSS (FEM), Sonnet's EM software, and Agilent's ADS MOMENTUM package (MOM).

TABLE I
LIST OF COMMERCIAL EM SOLVERS TO HELP DESIGN ON-CHIP ANTENNAS. TABLE RECREATED FROM [7].

Software Name	Theoretical Model	Company
Ensemble (Designer)	Moment method	Ansoft
IE3D	Moment method	Zeland
Momentum	Moment method	HP
EM	Moment method	Sonnet
PiCasso	Moment method/genetic	EMAG
FEKO	Moment method	EMSS
PCAAD	Cavity Model	Antenna Design Associates, Inc.
Micropatch	Segmentation	Microstrip Designs, Inc.
Microwave Studio (MAFIA)	FDTD	CST
Fidelity	FDTD	Zeland
HFSS	Finite element	Ansoft

When setting up EM simulations for a RFIC design, the first step is to build a physical model of the device to be fabricated. Knowing the materials that are being used, their electrical properties, and the sizes/thicknesses of each material in the semiconductor process is critical. Each foundry may have different processes, where each process may have their own list of materials and dimensions. For on-chip antennas and RF devices in the mmWave regime, foundries often do not have reliable or exact characterizations, so researchers must extract and learn the precise behavior of a particular fabrication process. The most important materials in the semiconductor fabrication process are the "interconnect" layers which contain several metal layers sandwiched between layers of dielectric. For example, a 0.18μm CMOS process can have as many as six metal layers sandwiched between dielectric, with only half a micron of spacing between each metal layer. Vias are created during fabrication of the RFIC to tunnel through the dielectric and connect one metal layer to another (ex: Via12, Via23, Via34, etc.). The interconnect is mainly used in digital circuits to connect transistors that are buried in the semiconductor. However, in analog/RF circuit design, the interconnect is also used to create passive components such as capacitors and inductors via sandwiches of metal or planar loops of metal, or in the case of MTWS, on-chip antennas. Rough physical layouts of various layers and dimensions, as shown in textbooks such as [8], can be used for preliminary simulations, and general material properties can be found from textbooks and/or previous literature. More accurate simulations require material characterization and dimensions provided in the Process Design Kit (PDK) supplied by the foundry. Unfortunately, with MTWS fabrication, this information still may not be sufficient. The material electrical properties and losses may be frequency dependent and unknown for mmWave and terahertz operation within the PDK.

When using EM simulators to model the RFIC physical layout, several common parameters must be provided. For dielectrics, simulators require permittivity and loss tangent. When simulating metal, conductivity needs to be provided to the simulator to account for proper conduction losses. Surface roughness and thickness of the metal are also important parameters in MTWS since current is concentrated at the surface due to the skin effect. As frequencies increase, more current is concentrated at the surface and the roughness can significantly impede electron mobility and increase the resistance along the metal line. As an example, the thicknesses of some metal layers are roughly one skin depth at 60 GHz (approximately 0.4 μm). Unfortunately, PDKs may not have information related to surface roughness. Additionally, the material properties such as permittivity, loss tangent, and conductivity may be frequency dependent and the PDK information will likely be different for mmWave and terahertz wave frequencies, or for different fab plants or wafer runs. Experimental test structures and parameter extraction from measured data are needed to ascertain these parameters. According to [9], p. 66, a custom tailored profile with various losses is needed to accurately fit simulation to measured data so that accurate simulations may be used in future designs.

Aluminum (Al) is a common metal used in CMOS processes, and the push towards higher conductivity metals such as copper (Cu) is common in newer processes, such as 65 nm and below [8]. A combination of AlCu may be used, where Cu is used in the thinner metal layers (usually the lower layers close to the semiconductor) and Al will be used in the thicker metal layers towards the top. The thickest metal layers, which have lower ohmic losses, are located on top and are usually used as power lines (Ex: Vdd) or as "pads" for bond wire attachments to send signals to and from the chip. The number of metal layers can also vary, but can range from three to six layers and even upwards to nine layers in new processes such as 45 nm. Predictions such as those of the International

Technology Roadmap for Semiconductors (ITRS) have shown the possibility of reaching up to 15 metal layers by 2016 [8].

A fabrication facility may provide options such as a "super thick top metal" which is designated 7+1, where the "+1" signifies a very thick top metal layer compared to the 7 lower layers. Ultimately, the PDK defines what is available. The insulating dielectric that sits between the metal layers is typically Silicon Dioxide (SiO_2) in CMOS processes. The thickness of this dielectric is roughly the same as the thickness of the metal layers. In some cases, more than one type of dielectric layer will be used between each metal layer, and therefore two different permittivities/loss tangents will exist between the metal layers. Note that newer processes are pushing towards "low-k" dielectrics and trying to drive permittivities down from 3.9 of SiO_2 to less than 2 [8]. Vias that connect from one metal layer to another are typically rectangular and can be made of tungsten. By summing up the thicknesses of all metal layers and dielectrics useable in MTWS design, one can estimate a 10 μm thick interconnecting layer from semiconductor surface to air. Fig. 1 from [8] shows an excellent cross section example of the interconnect in an IC.

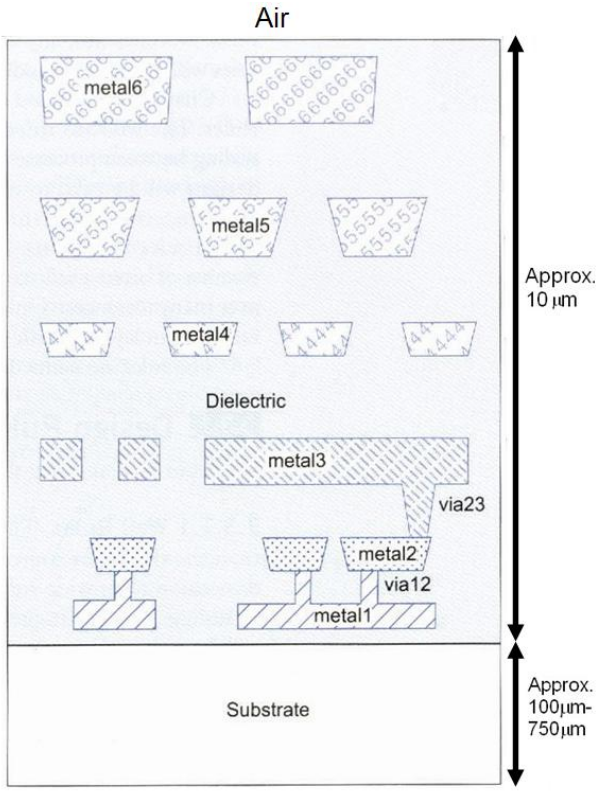

Fig. 1. Example metallization cross section (side view) of an IC (not to scale). Figure taken from [8].

After creating a circuit and physical model of a MTWS device, and after running EM simulations to satisfy expected design performance, the next step is to transition the circuit to a layout. Layout is the process of turning circuit schematics and physical antenna designs into transistors and interconnecting metal with vias. Much like a drawing or schematic tool, layout tools allow circuit designers to draw metal traces, drop-in via contacts and transistors, and create the RFIC layer-by-layer from semiconductor to air. While the software tools for layout are mostly automated for digital logic designers, analog circuit designs must do layouts "by hand" due to the specific geometries implemented and optimized in EM simulation. Once a layout is complete and satisfies the physical design rules (requirements imposed by foundries such that an IC can withstand manufacturing with many other ICs from other customers; these rules are discussed in Section III), the layout is converted to a file format called "Graphic Data System II" (GDSII). The GDSII stream format is an industry standard file type for storing and exchanging IC layout information which all foundries accept for fabrication. A common tool used for layout, which we used for UT's on-chip antennas, is Cadence's Virtuoso. Mentor's Calibre was used to perform the "design rules check" to verify layouts that satisfy the foundry's design rules. This tool may be integrated directly into the Virtuoso environment. When fabricating a circuit, simply passing the design rules set by the foundry will not guarantee intended circuit function. An additional verification tool is needed called LVS (layout versus schematic). The LVS tool compares the layout against a circuit schematic to ensure agreement. Passing LVS will verify that a layout will match the connections of a desired circuit schematic. Mentor's Calibre is also capable of performing LVS.

III. Tape-out Precautions and Guidelines

Once layout is complete, the MTWS is ready for *tape-out*. Tape-out is the term used for creating the final GDSII file that the foundry uses to manufacture an IC. This section highlights some precautions and guidelines for a successful tape-out. Associated with any tape-out are a set of rules that foundries provide ahead of time. These are known as the *design rules*, which describe the physical capabilities of wafers that the foundry can support. Any layout submitted to the foundry for fabrication must satisfy the Design Rules Check (DRC). DRC can be one of the main limiting factors for RFIC and antenna circuit ideas/designs, since certain layout ideas may not pass the DRC, which in turn means they cannot be manufactured by the foundry. Thus, understanding the design rules and knowing how or if they may be modified, is critical throughout the entire design flow from circuit ideas, through simulation, and to final layout.

One of the limiting factors of the design rules in on-chip antenna design is the metal-percentage rule. Depending on the foundry or process, a certain percentage of chip area must have metal. For example, if using six metal layers, each metal layer may be required by the foundry to occupy at least 35% of the area of the design. This provides mechanical stability to the IC but also to surrounding ICs on the wafer. Another design rule that can limit antenna or MTWS design is the wide-metal rule. If any metal area is larger or wider than a certain threshold, a foundry's design rules may require small slots or holes to be

inserted in the metal at a minimum density. For example, if a metal layer occupies an area larger than 50μm x 50μm, a small hole roughly 10μm^2 might need to be removed from the metal, and the density of holes might need to be at least 5% of the area. Older technologies such as 0.18μm have the possibility of metal traces bending diagonally (45° bend), but with newer 45 nm processes, the smaller metal traces are now restricted to perpendicular angles (90° bend). These sharp bends can add capacitance along the metal line and must be considered in MTWS layouts [10].

Via sizes are typically small compared to a wavelength, at roughly half a micrometer, and tend to be rectangular. Vias are set in size (both minimum and maximum) and large arrays are created in the layout tool such as Cadence's Virtuoso. Via sizes can be different from one metal layer connection to another. For example, the vias that connect M5 to M6 (Via56) might be larger and spaced further apart than Via12. It is good practice to place multiple vias on critical metal-to-metal connections. In case a via connection is faulty and a critical connection between two metal layers is opened, other parallel vias can serve as alternate connections. In addition, multiple vias in parallel can reduce the contact resistance between metal layers.

One important feature of an IC process is the "passivation" layer (also known as the "overglass"). This insulating layer is the top most layer above the top metal and acts as a protective layer to shield the wafer from the outside environment. This passivation layer must be etched away if one plans on placing probes directly on the IC or placing pads for bond wire connections. The passivation layer may have a different permittivity compared to the dielectric layers between the metal. The thickness of the passivation layer is comparable to the thickness of the top most metal layer. To etch away the passivation layer, simply draw rectangles on the appropriate layer (i.e. "PAD" layer) to determine which areas of the top metal layer to expose to air. When designing a chip with probe pads for direct probe measurements, the pad area should consist of all metal layers interconnected with as many stacked vias as possible. This provides mechanical stability when the probe tips touch down on the IC. Additionally, the manufacturers of probe tips may have additional rules and guidelines for creating pads on ICs and these should be consulted during chip design. Typically, smaller pad areas are desired to reduce parasitic capacitance. The unwanted parasitic capacitance of the pads must be measured and removed from the overall measurements of the device under test (DUT) [11, 12].

Another precaution in making RFICs that can impact on-chip antennas are "pad rings" and "scribe lines." A pad ring, which is a ring of pads located around the perimeter of the chip, may be used to connect the active circuitry, such as transistors, to the protective chip package via bond wires. This pad ring could possibly be an obstacle in some on-chip antenna designs and must be accounted for in simulation. A scribe line is a thin "wall" of metal with vias located around the perimeter of the chip just beyond the pad ring. The scribe line acts as a barrier to prevent contaminants from entering the semiconductor after the wafer is diced with a diamond saw. If the scribe line is not present, contaminants could enter the chip from the side and corrupt proper transistor function. This ring of metal around the chip may need to be accounted for in on-chip antenna design and simulated as well.

To summarize, the PDK and DRC determine the physical capabilities the foundry can support. The design rules must be studied and regularly consulted throughout the entire design process from initial ideas, through simulations, and into layout.

IV. Example Tape-out for 60 GHz Research

This section describes the RFIC tape-out designed at UT's WNCG. As stated previously, certain material properties such as permittivites and conductivities are relied upon by the EM simulators, and these properties (despite being listed by the PDK) are often inaccurate at mmWave and terahertz frequencies. The goal of our first tape-out was to create on-chip test structures so that material properties can be extracted from measurements. The Wireless Networking and Communications Group (WNCG) has invested in a state-of-the-art probing facility with Cascade Microtech probe tips and various Agilent equipment such as signal generators, a vector network analyzer, and a spectrum analyzer up to 67 GHz. This gear is used to probe and measure the fabricated on-chip test structures [4].

A. Material Property Extraction

Extracting material properties, through measurement of test structures, is essential to run accurate EM simulations in future designs. The main properties to be extracted are dielectric permittivity between metal layers, the loss tangent of the dielectric, and conductivity of the metal layers. Additionally, the substrate conductivity is also an important parameter to extract if metal shields are not used to isolate signals from the lossy substrate. Surface roughness is also a desired parameter, however, the test procedure to extract this parameter can be quite complex. One possibility to account for surface roughness is to adjust the extracted conductivity [13]. A common procedure to extract these material properties is the use of transmission lines [11, 14–19]. Due to the planarity of transmission lines (T-Lines), these structures can be easily implemented in the IC interconnect with minimal effort. The advantage of using T-Lines is that there are well known frequency-dependent equations which rely on material properties and characteristics of the T-Line, such as the characteristic impedance and the propagation constant. These characteristics can be directly measured via a Time-Domain Reflectometer (TDR) or a Vector Network Analyzer (VNA). By varying the geometry of T-Lines as well as the frequency of the measurements, a series of curve-fittings between the simulations and measurements can determine the material properties.

Two common T-Lines used in RFICs are microstrip lines (MS) and co-planar waveguides (CPWs). A discussion on the comparison of MS vs. CPW in RFICs can be found in [15]. However, from a probing/measurement perspective,

CPWs allow direct access to both the signal and ground lines as seen in Fig. 2.

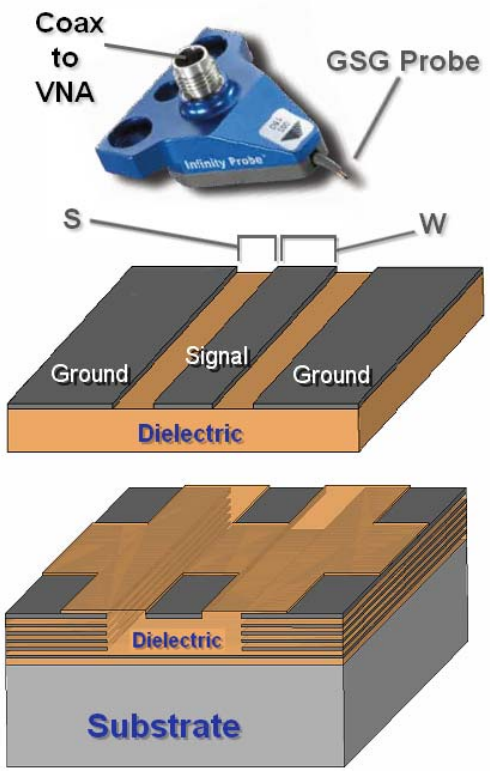

Fig. 2. Top: the Ground-Signal-Ground (GSG) probe tips used for direct IC probing at 60 GHz. Middle: an example of a general co-planar waveguide (CPW). Bottom: the implemented CPWs on IC with multiple metal layers. Stacks of vias connect the multiple metal layers. These CPWs are sometimes referred to as conductor-backed CPWs (CB-CPWs) or Grounded CPWs (GCPWs).

The equipment at UT's WNCG allows for direct probing using a Ground-Signal-Ground (GSG) configuration. An array of CPWs were constructed with various spacings and lengths, as seen in Fig. 3. In direct probing, probes require certain distance to slide after initial contact with the IC pad. This sliding is known as *skating* and a minimum of 25μm of skate is necessary for UT's probe tips. Probe pad dimensions were 40μm x 60μm as recommended by Cascade Microtech. The 60μm length is in the direction of the probe skate motion. The distance between the GSG probe tips, also known as *probe pitch*, is 150μm. Most CPWs on our RFIC were constructed for 2-port measurement. One CPW was altered for 1-port measurement by placing a "short" across one end, which connected the signal line to the surrounding ground lines. Preliminary simulations using PDK information predicted a wavelength at 60 GHz would be approximately 2200μm on chip (dielectric permittivity reduces the wavelength as compared to free space), and both quarter wavelength (550μm) and half wavelength (1100μm) T-Lines were built on the chip.

To satisfy design rules, the CPW ground planes were constructed to include all metal layers, and an array of vias was

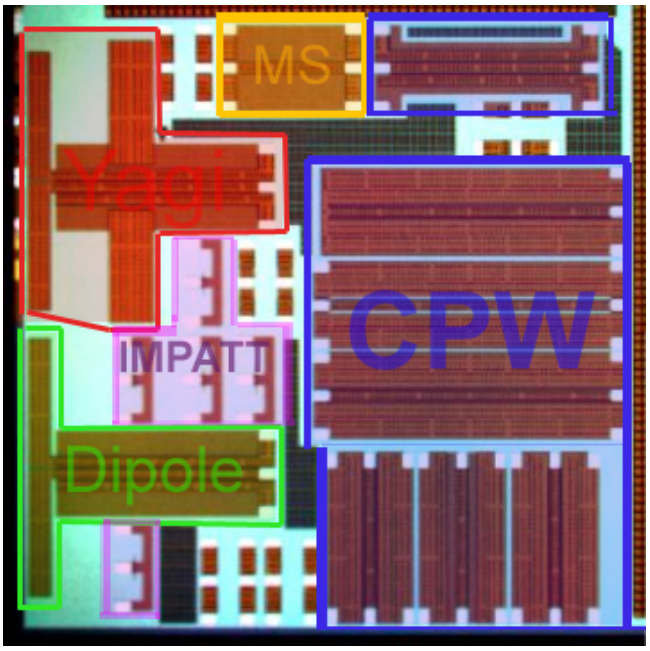

Fig. 3. Die photo of WNCG's RFIC with various transmission lines, antennas, and IMPATT diodes. Chip size is 2.5mm x 2.5mm. Transmission lines were implemented as co-planar waveguides (CPWs). The 60 GHz antennas were implemented as a dipole and 2-element Yagi-Uda antenna. De-embedding structures were also added for the transmission lines and IMPATT diodes.

used to connect each metal layer to one another. The signal line of the CPW was made only from the top metal. According to [15], an unwanted "odd CPW mode" needs to be suppressed by physically connecting the two ground planes of the CPW underneath. This connection was accomplished with M1 as seen in Fig. 2. M1 served as both a connection between the two ground planes of the CPW, but also as a shield to help isolate the lossy substrate from the CPW signal on the top metal. These types of connections should be simulated before tape-out. Additionally, the probe pads and landing structures introduce some measurement errors which must be accounted for. Different de-embedding techniques exist to model the pads and remove their effects [11, 12]. These de-embedding structures were also added in our RFIC layout which included open and shorted versions of the pads.

Characteristic impedance of a GCPW/CPW is a function of the dielectric permittivity and the geometry of the line [20]. If the geometry/dimensions of the T-Line are known, dielectric permittivity can be extracted if the characteristic impedance is known. A separate way of determining dielectric permittivity is measuring the time delay of an impulse and knowing the length of the T-Line. Both methods require measuring the two main properties of a transmission line, the complex propagation constant (usually denoted as γ) and the characteristic impedance (usually denoted as Z_o or Z_c). The characteristic impedance can be measured by a VNA using the reflection coefficient and the scattering matrix (S-parameters). Using the equations in [19], the S_{11} and S_{12} parameters can be used to directly determine the propagation constant and the

characteristic impedance. Once these two values are known, dielectric permittivity can be extracted using the general CPW equations in [20].

According to [15], transmission line losses are well modeled when the shunt loss (usually denoted as G in the Telegrapher's equation model) is due to a constant loss tangent, and the conductor loss (usually denoted as R for the series loss) is only caused by the skin effect losses. Since skin effect is a function of conductivity, both loss tangent and conductivity can be extracted from R and G. R and G can be calculated from Equation 1 and 2 (taken from [19]) which is a function of Z_o and γ. Once R is found, conductivity can be calculated via RF surface resistance, Equation 3, and a conductor loss equation for a CPW from [17].

$$G = \Re\{\gamma\ /Z_o\}, \tag{1}$$

$$R = \Re\{\gamma\ Z_o\}, \tag{2}$$

$$R_{SURF} = (\pi f \mu_o \mu_r / \sigma)^{1/2}, \tag{3}$$

The spacing of the CPWs, S in Fig. 2, was varied for three different values while keeping all widths identical. This variation was done for quarter wavelength and half wavelength CPWs. One CPW variation was identically replicated with the M1 shield removed to help quantify the substrate losses and conductivity. A microstrip (MS) line was also constructed on this tape-out for additional verification of material properties.

B. 60 GHz Feedlines and On-Chip Antennas

Two 60 GHz on-chip antennas were fabricated on this tape-out. Due to size limitations, a classic half wave dipole and two element Yagi-Uda antenna were chosen. A high gain rhombic antenna shall be the subject of future tape-outs, as described in [21]. Design dimensions were selected based upon [21]. In [21], various on-chip antennas were simulated and several guidelines were provided. The dipole antenna was bulked up in thickness to include all metal layers and an array of vias was used to interconnect the layers. The dipole elements are 500μm in length and 90μm in width and the element spacing was identical to [21] at 7μm. Using this configuration, the impedance of the dipole was simulated to be 58-13j and resonated well across the entire 57-64GHz band when fed with a 50Ω source impedance. The two element Yagi antenna has an identical dipole, but also contains an additional undriven reflector. This "floating" reflector also included many metal layers. The additional usage of metal layers helps satisfy design rules. The reflector width was 174μm. Simulations done in [21] show minimal antenna gain improvement for reflector widths greater than 15μm. This particular width was chosen to help satisfy design rules requiring more metal. The reflector was 1100μm long and located 220μm away from the dipole elements.

Using GSG probe tips, a CPW transmission line can be used to feed the antenna with the signal line feeding one element of the dipole, and a co-planar ground feeding the other element of the dipole. To avoid the feedline and Yagi reflector from intersecting, the CPW feed line was constructed on the top most metal layer while the Yagi reflector occupied the other metal layers underneath. The spacing, S, of the CPW was identical to the element spacing of the dipole (7μm), and the width of the signal and ground planes, W, was kept identical to the probe pad width of 40μm. This consistent spacing and width throughout the T-Line avoids any sudden and sharp transitions between feedline and antenna which can lead to parasitic capacitance [10]. Since antenna impedance was simulated at 58-13j, a small series inductance is needed for matching, which can be accomplished by adding a stub tuner to the T-Line. However, if the T-Line length is chosen appropriately, the reactance can be minimized without any additional structure [22]. It is important to note, the T-Line length should be as long as possible if using probes to excite the on-chip antenna. This helps to reduce any interference effects the nearby probes may have on the radiating structures. A T-Line length of 875μm was used to match to the 50Ω source impedance based upon preliminary simulations. Antenna gains of the dipole and Yagi antenna are projected from simulation to be -7 dBi and -3.5 dBi, respectively [21].

C. IMPATT diodes

IMPact ionization Avalanche Transit-Time (IMPATT) diodes provide a possibility of generating an on-chip 60 GHz source in standard CMOS [23]. The diodes produce a negative differential resistance which can be used for amplification or oscillation as well as the possibility of tuning RFIC antennas. Several IMPATT diodes with width variations were constructed on this tape-out. Three diodes were fabricated in 0.18μm CMOS technology using 80, 100, and 120μm widths and using the minimum length of the given 0.18μm CMOS technology, as seen in Fig. 4. These three diodes (and two de-embedding structures), as shown in the Fig. 3, will be used to measure the breakdown voltage, the junction capacitance, the DC resistance, the avalanche frequency, the negative resistance, and the diode reactance. Using CPWs and GSG probes, measurements will give accurate models to be used in further simulations. Besides being able to create an inexpensive, non-invasive mmWave signal source, the IMPATT diodes can be used to help tune antennas since diode impedance and avalanche frequency are strongly dependent on bias voltage. Capacitive or resistive loading on a microstrip patch antenna has been shown to tune resonant frequency or increase the bandwidth, respectively. With IMPATT diodes connected to a planar antenna such as a microstrip patch antenna, the capacitive and resistive loading can be done by a single device which allows tuning of on-chip antennas.

V. Conclusion

This paper has provided important guidelines and precautions for fabricating millimeter-wave and terahertz wireless systems (MTWS) on a chip. Such fabrication will be required as carrier frequencies explode upward in the coming decade. When designing and fabricating on-chip antennas, a few key design rules such as a wide-metal rule or a metal-percentage

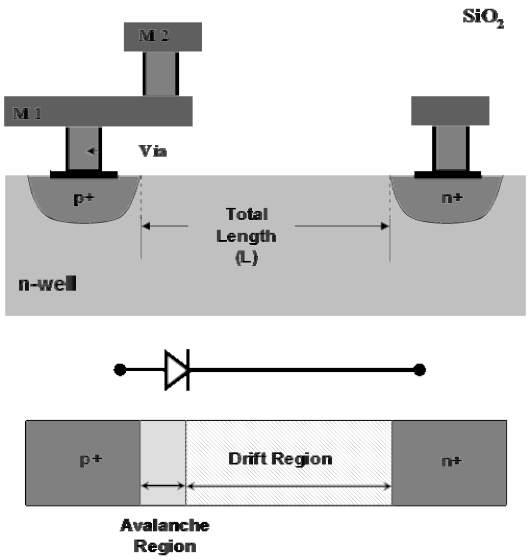

Fig. 4. Cross section of a CMOS IMPATT diode. By simply using n+ and p+ diffusion, an on-chip mmWave signal source can be created. Length of the diodes is the distance between the p+ and n+ diffusions and width is the distance into the page.

rule must be satisfied. It is extremely important that design rules provided by the foundry within the Process Design Kit (PDK) be consulted regularly throughout the entire design cycle, from idea to layout. Being able to characterize the frequency-dependent materials, such as loss tangents and permittivities, in any fabrication process, is extremely important at mmWave and terahertz frequencies. This information is often not available or accurate from the foundry, in which case such data must be extracted using measurements of test structures such as transmission lines.

An example of an RFIC tape-out in 0.18μm CMOS was presented in this paper, and was developed at The University of Texas at Austin. The tape-out provides on-chip test structures for material property extraction, and also has two mmWave on-chip antennas. IMPATT diodes, which promise the ability to create and tune mmWave/terahertz signals were also included, with the idea that they may serve as inexpensive, non-invasive on-chip signal generators or antenna tuning elements.

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