A 40-GHz Low-Noise Amplifier With a Positive-Feedback Network in 0.18-μm CMOS

Hsieh-Hung Hsieh, *Member, IEEE*, and Liang-Hung Lu, *Member, IEEE*

***Abstract*—A novel circuit topology for a CMOS millimeter-wave low-noise amplifier (LNA) is presented in this paper. By adopting a positive-feedback network at the common-gate transistor of the input cascode stage, the small-signal gain can be effectively boosted, facilitating circuit operations at the higher frequency bands. In addition, LC ladders are utilized as the inter-stage matching for the cascaded amplifiers such that an enhanced bandwidth can be achieved. Using a standard 0.18-μm CMOS process, the proposed LNA is implemented for demonstration. At the center frequency of 40 GHz, the fabricated circuit exhibits a gain of 15 dB and a noise figure of 7.5 dB, while the return losses are better than 10 dB within the 3-dB bandwidth of 4 GHz. Operated at a 1.8-V supply, the LNA consumes a dc power of 36 mW.**

***Index Terms*—Coplanar waveguide (CPW), cutoff frequencies, LC ladders, low-noise amplifier (LNA), millimeter wave, positive feedback.**

I. Introduction

DUE TO the superior high-frequency device characteristics, III–V compound semiconductors were generally utilized for the implementation of millimeter-wave integrated circuits. With the advances in the fabrication technology, transistors with a cutoff frequency (f_T) and a maximum oscillation frequency ($f_{\max}$) beyond 100 GHz have been commercially available in a deep-submicrometer CMOS process, motivating RF integrated circuit designs towards higher frequencies. Unfortunately, the development of CMOS millimeter-wave circuits has been long impeded by the inherent shortcomings such as device parasitics, lossy substrate, and low carrier mobility. It is still a challenging task for the designers to realize high-performance CMOS RF circuits at tens of gigahertz frequencies.

Being the first active component in a wireless receiver front-end, the low-noise amplifier (LNA) is typically used to provide a sufficient gain for the incoming signals while maintaining minimum additive noise for the desirable signal-to-noise ratio at the output. In the past few years, CMOS LNA circuits operating at millimeter-wave frequencies have been successfully demonstrated [1]–[6]. As the gain and noise figure (NF) of the LNAs are strongly influenced by the high-frequency capabilities of the MOSFETs, these amplifier designs are exclusively fabricated in deep-submicrometer technologies, leading to higher implementation costs. To alleviate the frequency limitations, an LNA topology is presented in this study. By employing a positive feedback to compensate for the gain rolloff at elevated frequencies, enhanced performance in terms of gain and NF can be achieved in the LNA design at a frequency close to the f_T and $f_{\max}$ of the transistors. Using a standard 0.18-μm CMOS process, a prototype circuit is demonstrated at the 40-GHz frequency band.

This paper is organized as follows. In Section II, the influence of the positive feedback on a common-gate transistor is discussed, while the proposed LNA architecture with a positive-feedback network is illustrated in Section III. Circuit implementation and experimental results of the 40-GHz LNA are presented in Section IV and V, respectively. Finally, a conclusion is provided in Section VI.

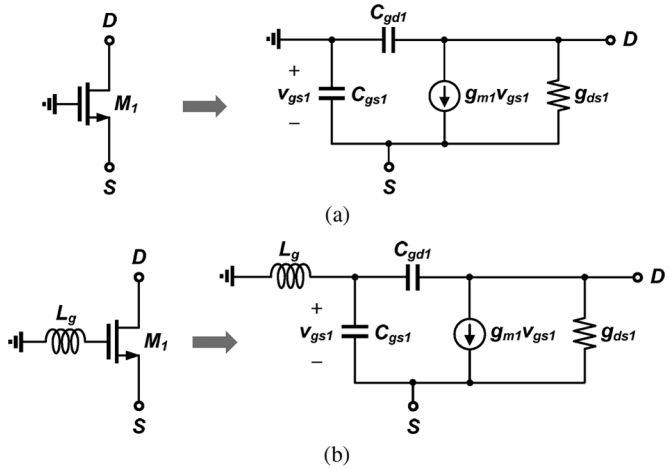

Fig. 1. Common-gate transistor: (a) without and (b) with the gate inductor.

II. Common-Gate Transistor With a Positive-Feedback Network

Conventionally, a cascode stage is preferred for the implementation of the LNA circuits by incorporating a common-gate MOSFET in the signal path. With the gate terminal grounded as shown in Fig. 1(a), the Miller effect is thus eliminated, leading to enhanced reverse isolation and circuit stability. At multigigahertz frequencies, the LNA gain also benefits as the output resistance is boosted by the cascode stage. However, for LNA circuits operating at millimeter-wave frequencies, the gain of the cascode stage is decreased drastically due to the limitations from carrier mobility and device parasitics. In order to compensate for the gain rolloff at higher frequency bands, a positive feedback established by an inductor L_g can be adopted in the common-gate stage [7]–[9], as illustrated in Fig. 1(b).

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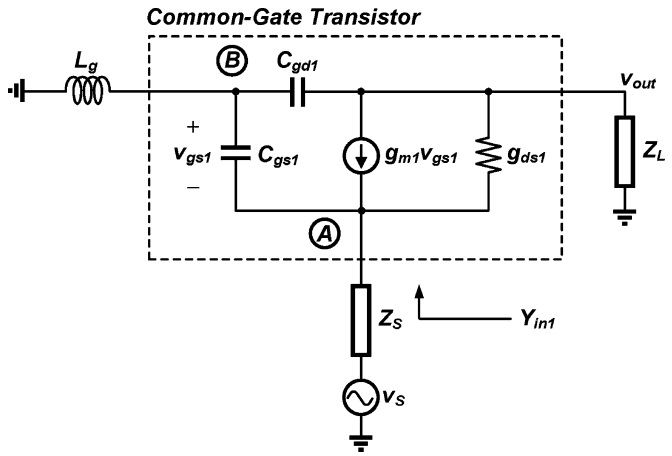

Fig. 2. Small-signal equivalent circuit of the common-gate transistor with the gate inductor.

For further investigation of the gain-boosting technique by the positive feedback, an equivalent circuit of the common-gate stage with the gate inductance is illustrated in Fig. 2. Based the small-signal analysis, the voltages at point A and B can be represented by

$$v_A = \frac{1-(\omega_0/\omega_t)^2}{[1-(\omega_0/\omega_t)^2]+(g_{m1}+j\omega_0 C_{\rm gs1})Z_S} v_S \quad (1)$$

$$v_B = \frac{-(\omega_0/\omega_t)^2}{1-(\omega_0/\omega_t)^2} v_A \quad (2)$$

where ω_0 is the operating frequency and ω_t is given by

$$\omega_t = \frac{1}{\sqrt{L_g C_{\rm gs1}}}. \quad (3)$$

It is noted that the values of the gate-to-drain capacitance $C_{\rm gd1}$ and the channel conductance $g_{\rm ds1}$ are relatively small. Therefore, they are neglected in the analysis for simplification. From (1) and (2), the voltage difference across the gate-to-source capacitance can be expressed as

$$v_{\rm gs1} = \frac{-1}{[1-(\omega_0/\omega_t)^2]+(g_{m1}+j\omega_0 C_{\rm gs1})Z_S} v_S. \quad (4)$$

According to (2), v_A and v_B are out-of-phase if ω_0 is less than ω_t. Consequently, the amplitude of $v_{\rm gs1}$ is thus increased, leading to enhanced effective transconductance and boosted gain for the cascode stage.

In millimeter-wave circuit designs, the maximum stable gain (MSG) is a useful figure-of-merit to evaluate the active device's capability for signal amplification. Based on the device models of a 0.18-μm CMOS process, the simulated MSG of a common-gate transistor with $({\rm W/L}) = 40$ μm/0.18 μm and $V_{\rm GS1} = V_{\rm DS1} = 0.8$ V versus frequency is illustrated in Fig. 3. For a gate inductance of 0.05 and 0.1 nH, the MSG at 40 GHz is improved by 1.06 and 1.6 dB, respectively. In order to provide useful design guidelines for the choice of the gate inductance, the simulated MSG and minimum NF of an n-channel MOSFET with $({\rm W/L}) = 40$ μm/0.18 μm and $V_{\rm GS1} = V_{\rm DS1} = 0.8$ V are depicted in Fig. 4. By introducing the positive feedback with

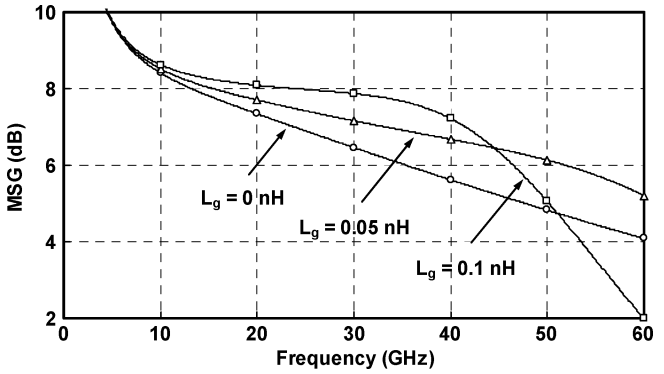

Fig. 3. Simulated MSG of the common-gate transistor with and without the gate inductance L_g.

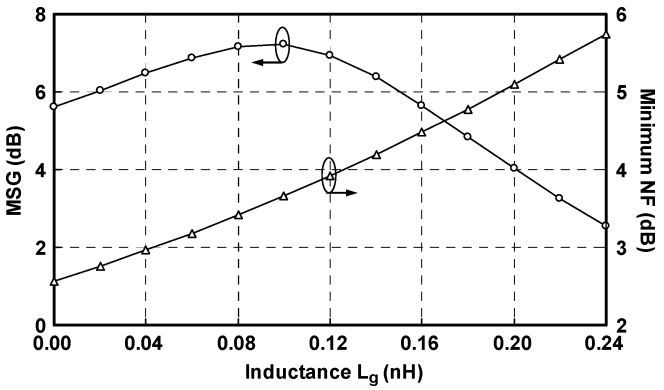

Fig. 4. Simulated MSG and minimum NF of the common-gate transistor at 40 GHz.

a gate inductance L_g, the MSG is effectively increased, indicating enhanced high-frequency capability of the common-gate transistor. However, for excessively large inductance at the gate, the MSG decreases as the condition $\omega_0 < \omega_t$ is no longer valid. It is noted that, with the inductor L_g, the impedance at the gate of the common-gate transistor increases. Consequently, the noise voltage at the gate terminal is elevated, resulting in a higher minimum NF. Therefore, the design value of L_g has to be determined by taking the tradeoff between the gain and NF into consideration.

The gate inductance in the proposed technique is considered a positive feedback and the circuit stability becomes an essential issue. Fig. 5 shows the simulated input stability circles, which are widely utilized in millimeter-wave amplifier designs for various values of L_g. By adopting the gate inductance, the stable region in the impedance plane is restricted. The reason can be explained by deriving the input admittance $Y_{\rm in1}$ in the equivalent circuit in Fig. 2 as

$$Y_{\rm in1} = \frac{g_{m1}}{1-(\omega_0/\omega_t)^2} + \frac{j\omega_0 C_{\rm gs1}}{1-(\omega_0/\omega_t)^2}. \quad (5)$$

For excessively large L_g, ω_t becomes less than ω_0, leading to a negative conductance in $Y_{\rm in1}$. Therefore, in practical circuit implementations, the value of L_g has to be chosen such that the condition of $\omega_0 < \omega_t$ holds. With the proposed technique, the gain of the common-gate stage can be boosted without compromising the circuit stability.

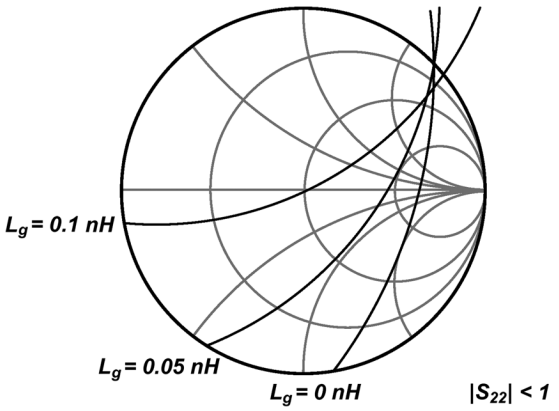

Fig. 5. Simulated input stability circles of the common-gate transistor at 40 GHz.

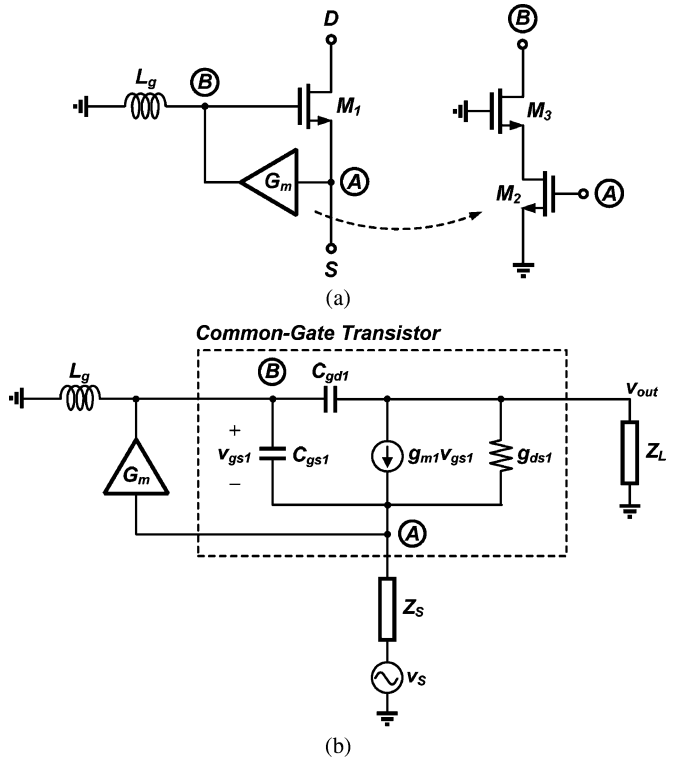

Fig. 6. (a) Common-gate transistor with the gate inductance and the transconductance stage. (b) Its equivalent circuit.

For further gain enhancement at elevated frequencies, a transconductance stage can be inserted between the source and gate of the common-gate transistor, and the conceptual illustration is shown in Fig. 6(a) [10], [11]. In this particular case, the transconductance stage is simply realized by a coscode amplifier. Based on the equivalent circuit, as illustrated in Fig. 6(b), the expressions of v_A, v_B, and $v_{\rm gs1}$ can be derived by small-signal analysis

$$v_A = \frac{1-(\omega_0/\omega_t)^2}{[1-(\omega_0/\omega_t)^2]+(1+j\omega L_g G_m)Z_S} v_S \tag{6}$$

$$v_B = \frac{-(\omega_0/\omega_t)^2 - j\omega L_g G_m}{1-(\omega_0/\omega_t)^2} v_A \tag{7}$$

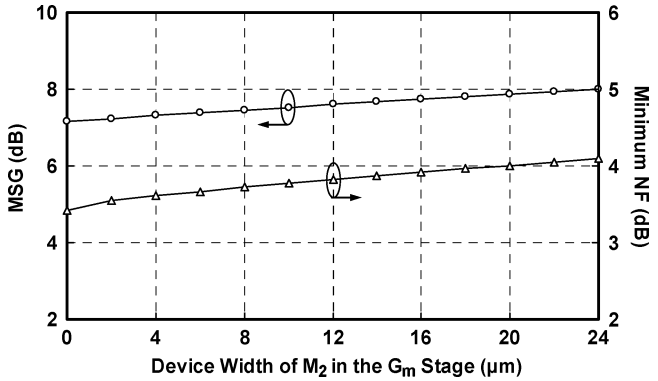

Fig. 7. Simulated MSG and minimum NF of the common-gate transistor for a fixed L_g.

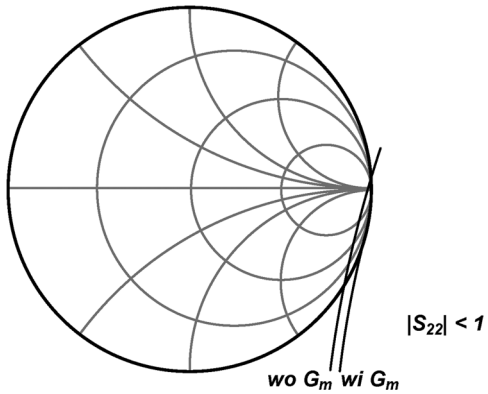

Fig. 8. Simulated input stability circles of the common-gate transistor at 500 MHz.

$$v_{\rm gs1} = \frac{-1-j\omega L_g G_m}{[1-(\omega_0/\omega_t)^2]+(1+j\omega L_g G_m)Z_S} v_S. \tag{8}$$

To have a better understanding on the influence of the transconductance stage, simulated MSG and minimum NF of the common-gate transistor versus the channel width of M_2 in Fig. 6(a) are depicted in Fig. 7 where a common-gate transistor with $(\mathrm{W/L}) = 40$ μm/0.18 μm and $V_{\rm GS1} = V_{\rm DS1} = 0.8$ V is employed and the gate inductance is 0.08 nH. It is clear that, due to the use of the additional G_m stage, the gain can be further boosted. However, the minimum NF is at stake as extra noise sources are contributed by the transistors M_2 and M_3.

An interesting fact is observed in the simulation results. As the additional transconductance stage is introduced, the inherent low-frequency stability issue due to the positive feedback is alleviated. Fig. 8 shows the simulated stability circle of the common-gate stage at 500 MHz. By properly choosing the circuit parameters of the G_m stage, a potentially unstable device can be transferred into a nearly unconditionally stable one. As the G_m stage provides a shunt path for the reverse transmission, the value of $|S_{12}|$ at lower frequencies is decreased and the stability is improved.

III. Proposed LNA Topology

The circuit schematic of the proposed millimeter-wave LNA is shown in Fig. 9, where three cascode stages are cascaded to provide the required signal amplification. By employing the

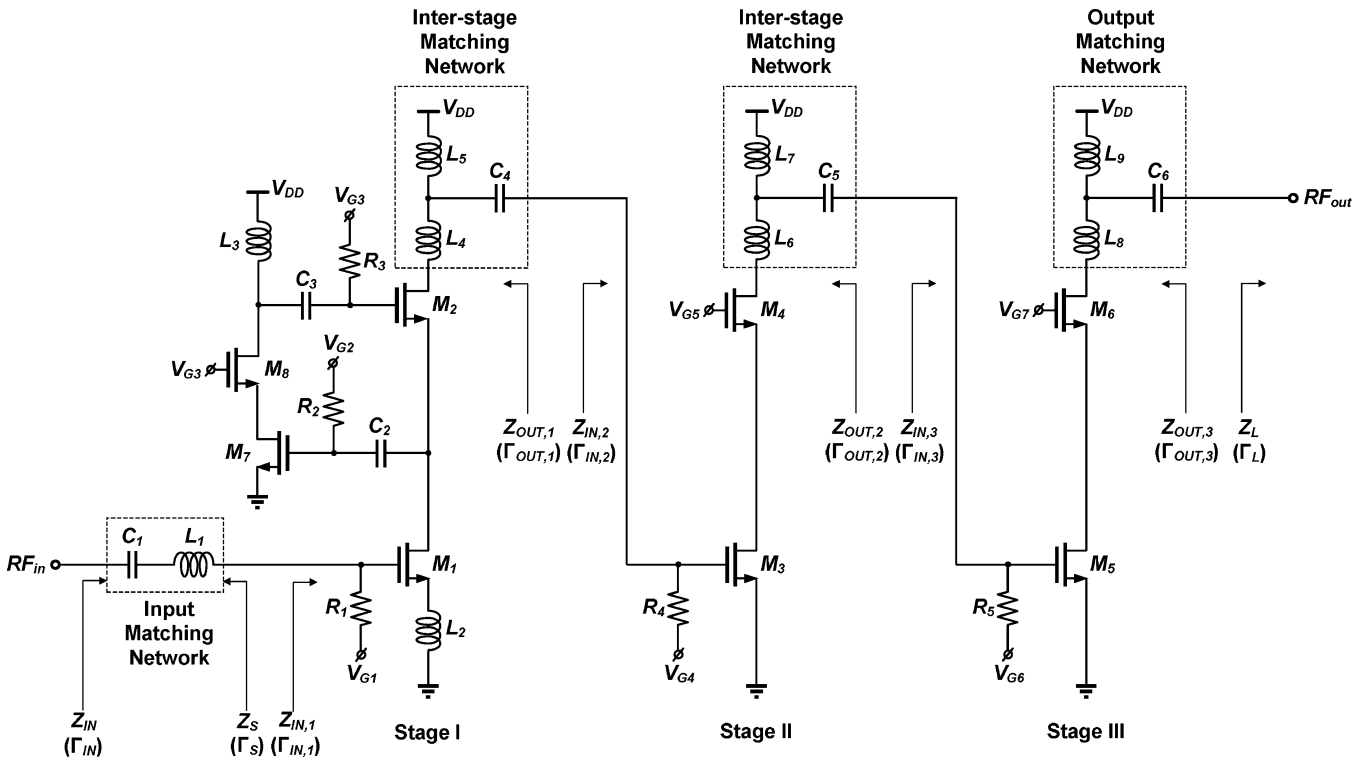

Fig. 9. Circuit schematic of the proposed three-stage CMOS LNA.

gate inductance and G_m cell at the common-gate transistor, the gain of the input stage is boosted by the positive feedback such that the noise contribution of the following stages can be effectively suppressed. In addition, LC ladders are extensively used for inter-stage matching, leading to broadband operations at the higher frequency bands. The design considerations of the proposed LNA circuit are presented as follows.

A. Device Size and Gate Bias

In order to achieve a high gain and low NF, the aspect ratio and dc bias of the MOSFETs have to be chosen carefully, especially when the LNA operates at a frequency near the transistors' cutoff. For the ease of circuit analysis and design optimization, the aspect ratios of the common-source and the common-gate transistors are identical in this particular case. Meanwhile, the gate terminals of the common-gate stages are biased at the supply voltage to provide sufficient headroom for the cascode topology. Based on a 0.18-μm CMOS process, the simulated MSG and minimum NF for the cascode stage at 40 GHz are shown in Fig. 10, where V_G represents the gate voltage of the common-source transistor. It is indicated that the MSG is strongly influenced by the gate bias than the aspect ratio of the MOSFETs. On the other hand, the minimum NF depends on the bias condition, as well as the size of the transistors. By taking the gain, NF, and power consumption into consideration, the circuit parameters of the active devices can be optimized at the frequencies of interest.

B. Small-Signal Characteristics

Once the transistor sizes and bias conditions are determined, the matching networks are implemented to achieve a maximum

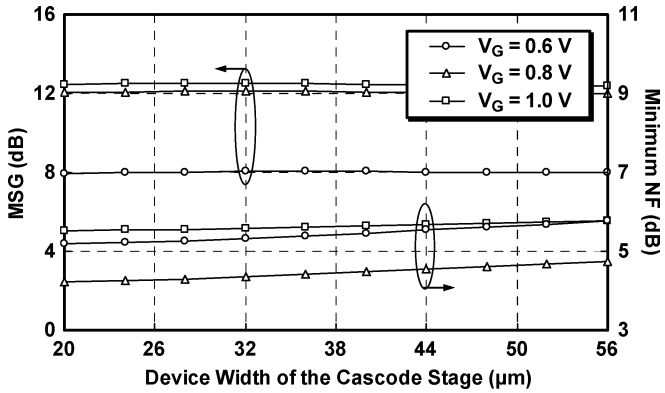

Fig. 10. Simulated MSG and minimum NF of the cascode stage at 40 GHz.

available gain of the LNA. Assuming that the losses from the matching elements are negligible, the conjugate matching conditions for the three-stage LNA are given by [7]

$$Z_S = Z_{\mathrm{IN},1}^* \tag{9}$$

$$Z_{\mathrm{OUT},1} = Z_{\mathrm{IN},2}^* \tag{10}$$

$$Z_{\mathrm{OUT},2} = Z_{\mathrm{IN},3}^* \tag{11}$$

$$Z_{\mathrm{OUT},3} = Z_L^*. \tag{12}$$

In addition to the amplifier gain, the NF is also an important specification for the design of the matching networks. For minimum NF in cascaded stages, the matching conditions are given by

$$Z_S = Z_{\mathrm{opt},1} \tag{13}$$

$$Z_{\mathrm{OUT},1} = Z_{\mathrm{opt},2} \tag{14}$$

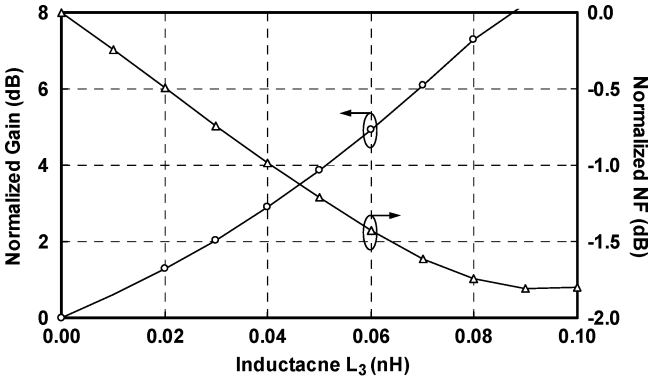

Fig. 11. Simulated gain and NF of the three-stage LNA at 40 GHz.

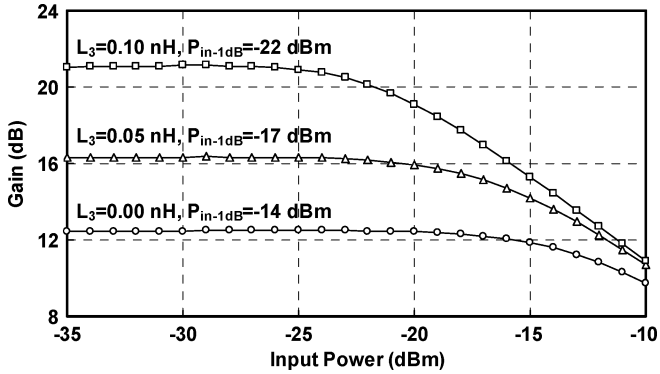

Fig. 12. Simulated gain of the LNA versus the input power level.

$$Z_{\mathrm{OUT},2} = Z_{\mathrm{opt},3} \tag{15}$$

where $Z_{\mathrm{opt},1}$, $Z_{\mathrm{opt},2}$, and $Z_{\mathrm{opt},3}$ are the optimum noise source impedances for the first, second, and third stages, respectively. In typical LNA designs, it is difficult to achieve simultaneous gain and noise matching as specified in (9)–(15). However, due to the use of the source degeneration in the input cascode stage, simultaneous power and noise matching becomes feasible [12]. In order to facilitate broadband circuit operations and to have better tolerance against process variations, LC ladders are employed for inter-stage and output matching. With the proposed positive-feedback technique for the common-gate transistor, the gain of the input stage is sufficiently large such that the noise contribution from the following stages is negligible. Therefore, the inter-stage matching networks are thus designed for maximum power transfer.

As for the design of the feedback network, the transconductance stage is realized by the cascode amplifier $M_7 - M_8$, while L_3 is adopted as the gate inductance. Based on circuit simulations, the normalized gain and NF of the LNA at 40 GHz are depicted in Fig. 11. It is indicated that, as the value of L_3 increases, the LNA gain is boosted due to the positive feedback while the overall NF is decreased. However, the value of L_3 is generally limited by the stability issues in practical circuit implementations.

C. Linearity

As the MOSFETs in the cascode stages are biased in strong inversion for high gain and low NF, the LNA typically exhibits good circuit linearity in terms of gain compression and intermodulation distortion. However, with the positive feedback at the input stage, the linearity of the proposed LNA is further investigated. Fig. 12 shows the simulated gain versus the input power level for various values of L_3. It is noted that a degraded gain compression point $P_{\mathrm{in}-1\ \mathrm{dB}}$ is observed as the value of the gate inductance L_3 increases. For the cascaded LNA, the input stage with the feedback network is optimized for gain and NF. As far as circuit linearity is concerned, the output stage is designed to meet the requirements of $P_{\mathrm{in}-1\ \mathrm{dB}}$ and IIP_3 in this particular design by properly choosing the device sizes and dc bias of M_5 and M_6.

IV. Circuit Implementation

Based on the proposed circuit topology, a 40-GHz LNA is implemented in a standard 0.18-μm CMOS process, which provides a single poly layer and six metal layers. For small-signal circuit operations at millimeter-wave frequencies, the minimum channel length of 0.18 μm is utilized while the transistors are designed in a multifinger layout to reduce the gate resistance. With the device layout optimized for the RF characteristics, the n-channel MOSFET in a deep n-well exhibits a cutoff frequency and a maximum oscillation frequency of approximately 55 and 70 GHz, respectively. As for the on-chip passive components, the process offers polysilicon resistors and metal–insulator–metal capacitors with oxide intermetal dielectric. In order to minimize the chip area, a planar spiral structure is utilized for large on-chip inductances including L_1, L_4, L_6, and L_8. On the other hand, small inductances such as L_2, L_3, L_5, L_7, and L_9 are realized by coplanar waveguides (CPWs) for better accuracy. To effectively reduce the conductor losses, the spiral inductors and transmission lines are fabricated using the top metal layer with a thickness of 2 μm [13].

By investigating the high-frequency device characteristics in this particular CMOS technology, transistors with a gate-to-source bias voltage of 0.9 V and a channel width ranging from 40 to 48 μm exhibit optimum MSG and minimum NF in the vicinity of 40 GHz and are employed in the LNA design. As for the gate inductance L_3, a design value of 0.05 nH is utilized for gain enhancement while maintaining a sufficient margin for circuit stability. Based on the results from circuit simulations, the gain and NF of the LNA are improved by 4.0 and 0.96 dB, respectively, due to the use of the proposed positive feedback. In the 4-dB gain enhancement, the contributions of the gate inductance and the transconductance stage are estimated at 3 and 1 dB, respectively. The circuit parameters of the 40-GHz LNA are tabulated in Table I for clear illustration.

V. Experimental Results

Fig. 13 shows the microphotograph of the fabricated LNA with a chip area of 1.19×0.56 mm^2. The circuit performance was characterized by on-wafer probing while the losses from the measurement setup were calibrated and deembedded in the experimental results. Operated at a 1.8-V supply voltage, the fabricated LNA consumes a dc power of 36 mW.

TABLE I
DESIGN PARAMETERS OF THE 40-GHz LNA

Parameters	Design Values
M_1, M_2	40 μm/ 0.18 μm
M_3, M_4, M_5	48 μm/ 0.18 μm
M_6	44 μm/ 0.18 μm
M_7, M_8	8 μm/ 0.18 μm
L_1	0.3 nH
L_2	0.12 nH
L_3	0.05 nH
L_4, L_6	0.24 nH
L_5, L_7	0.08 nH
L_8	0.26 nH
L_9	0.1 nH
C_2, C_3	0.25 pF
C_4, C_5	0.21 pF
C_6	0.19 pF
R_1, R_2, R_4, R_5	10 kΩ
R_3	2 kΩ

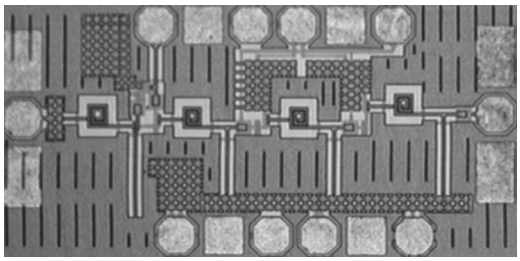

Fig. 13. Microphotograph of the fabricated LNA.

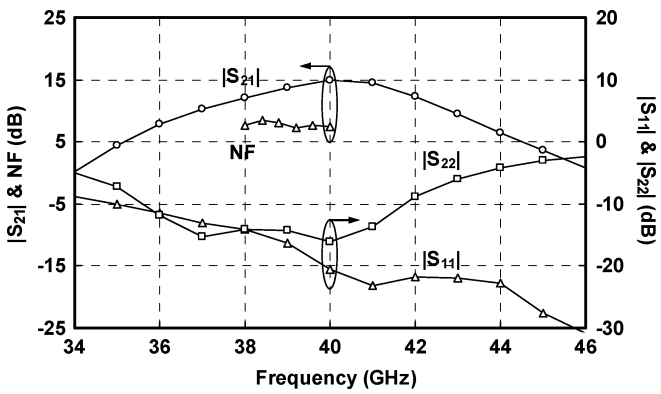

Fig. 14. Measured S-parameters and NF of the fabricated LNA.

The measured S-parameters and NF of the LNA are illustrated in Fig. 14. At the center frequency of 40 GHz, the LNA exhibits a peak gain of 15 dB. Within the 3-dB bandwidth from 38 to 42 GHz, the input and output return losses are generally better than 10 dB. Fig. 15 depicts the experimental setup for the NF measurement. The measured NF of the fabricated circuit is 7.5 dB at the center frequency. In addition, the linearity and large-signal behavior of the LNA were characterized by using an

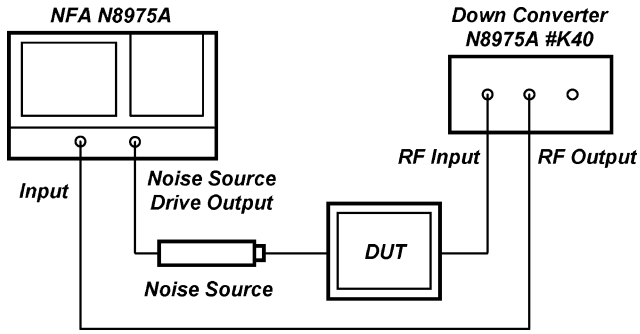

Fig. 15. Measurement setup to characterize the NF of the LNA.

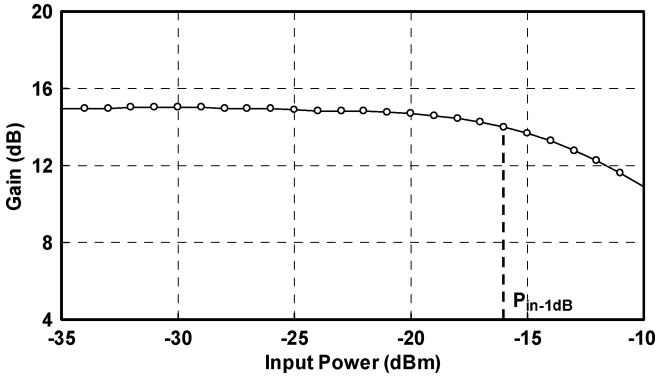

Fig. 16. Measured input 1-dB compression point of the fabricated LNA.

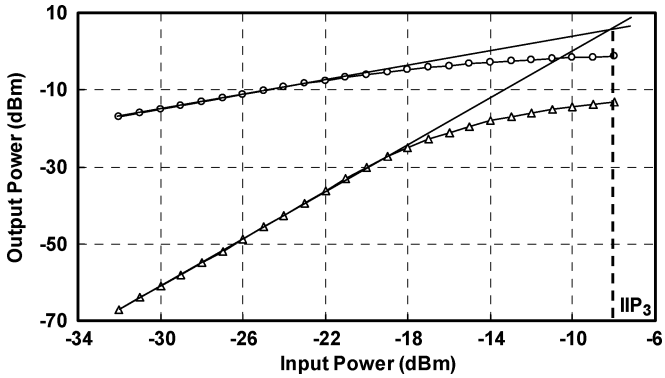

Fig. 17. Measured two-tone test of the fabricated LNA with 20-MHz input frequency spacing.

TABLE II
COMPARISON OF THE SIMULATED AND MEASURED CIRCUIT PERFORMANCE

Specifications	Unit	40-GHz LNA	
		Measured	Simulated
Frequency	GHz	40	
Supply Voltage	V	1.8	
$\|S_{21}\|$	dB	15.0	16.5
$\|S_{11}\|$	dB	-20.5	-15.9
$\|S_{22}\|$	dB	-16.2	-24.0
$\|S_{12}\|$	dB	-57	-59
NF	dB	7.5	7.4
$P_{in\text{-}1dB}$	dBm	-16	-17
IIP_3	dBm	-8	-9

Agilent E4448A spectrum analyzer. As the input level increases, the measured gain is demonstrated in Fig. 16, while the results

TABLE III
PERFORMANCE COMPARISON OF STATE-OF-THE-ART RF AMPLIFIERS

	Unit	This Work	[14]	[15]	[16]	[17]	[18]
Technology	—	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.13-µm CMOS
Frequency	GHz	40	26	32	40	40	40
Supply Voltage	V	1.8	1.8	1.8	3.0	1.5	1.5
DC Power	mW	36	54	27	300	36	36
$\|S_{21}\|$	dB	15.0	8.9	10.2	7.0	19.0	17.5
$\|S_{11}\|$	dB	-20.5	-14	-13.3	< -15	< -15	< -11
$\|S_{22}\|$	dB	-16.2	-12	-13.4	< -15	< -15	< -11
$\|S_{12}\|$	dB	-57	-32.5	-19.1	—	< -50	—
3-dB BW	GHz	38-42	23-27.5	—	—	34-44	34-44
NF	dB	7.5	6.9	—	—	—	6.3 @ 41 GHz
$P_{\text{in-1dB}}$	dBm	-16	-10.2	—	—	-18.9	-12.5
IIP_3	dBm	-8	2.8	—	—	-7.4	-3

from the two-tone intermodulation distortion test are shown in Fig. 17. Operating at the 40-GHz frequency band, the fabricated circuit exhibits a $P_{\text{in}-1\text{ dB}}$ of -16 dBm and an IIP_3 of -8 dBm.

The small- and large-signal specifications of the proposed LNA are tabulated in Table II. Due to the accuracy in the device modeling and full-wave electromagnetic (EM) simulations, good agreements are demonstrated between circuit simulation and experimental results. Table III summarizes the performance of the fabricated LNA along with results from previously published works [14]–[18] for comparison.

VI. CONCLUSION

Using a standard 0.18-μm CMOS process, a 40-GHz LNA has been demonstrated in this study. To facilitate high-frequency circuit implementations, a positive-feedback technique has been introduced such that the stringent performance limitations in terms of gain and NF can be effectively alleviated. In addition, LC ladders are utilized as the matching networks to provide broadband circuit operations at millimeter-wave frequencies. With the proposed circuit topology, it becomes feasible to realize a CMOS LNA operating at an RF band near the cutoff frequency of the transistors while maintaining desirable small- and large-signal circuit characteristics.

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