Single and Four-Element Ka-Band Transmit/Receive Phased-Array Silicon RFICs With 5-bit Amplitude and Phase Control

Dong-Woo Kang, *Associate Member, IEEE*, Jeong-Geun Kim, *Member, IEEE*, Byung-Wook Min, *Member, IEEE*, and Gabriel M. Rebeiz, *Fellow, IEEE*

***Abstract*—Ka-band SiGe BiCMOS single- and four-element phased arrays capable of both transmit and receive operation with 5-bit phase and amplitude control are presented. The design is based on the *All-RF* architecture with RF phase shifters and attenuators, and a 4:1 passive power combining/dividing network. The four-element array results in an average gain of $\sim$0 dB per channel and a noise figure of 9.0 dB, and is designed to be placed behind III–V T/R modules. The rms phase error is $< 5.6^\circ$ (5-bit operation) and $< 12.5^\circ$ (4-bit operation) over a 2 or 5 GHz instantaneous bandwidth, respectively, centered at around 36.5 GHz. In the receive mode, the input P1dB is -16 dBm per channel (IIP3 of -5.9 dBm), and in the transmit mode, the output P1dB is $+4$–5 dBm, all at 35–36 GHz. The measured isolation between the channels is better than 30 dB. The array maintained excellent phase characteristics up to 100 °C with no change in the rms phase error. Also, ten different four-element phased arrays were tested (40 channels) and result in an rms gain variation of $<$0.5 dB at 34–39 GHz. The four-element array consumes 171 and 142 mW in the Tx and Rx modes from 1.8 V, and occupies an area of 2.0 $\times$ 2.02 mm^2. To our knowledge, this is the smallest and lowest power consumption on-chip Ka-band phased-array to-date.**

***Index Terms*—Phase shifter, phased array, SiGe BiCMOS, T/R module, variable gain amplifier.**

I. Introduction

PHASED arrays allow the electronic scanning of the antenna beam and have been in extensive use since the 1970s for defense applications such as radars and communication systems [1]–[3]. However, phased arrays are only used in defense systems due to their high implementation cost which is partly due to the discrete implementation of the III–V transmit/receive chips together with silicon-based chips used for address decoders, power management, and digital control [4].

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D.-W. Kang and G. M. Rebeiz are with the Department of Electrical Engineering and Computer Science, University of California at San Diego, La Jolla, CA 92093 USA (e-mail: dwkang@ucsd.edu; rebeiz@ece.ucsd.edu).

J.-G. Kim was with the Department of Electrical Engineering and Computer Science, University of California at San Diego, La Jolla, CA 92093 USA. He is now with the Department of Electronic Engineering, Kwangwoon University, Seoul 139-701, Korea (e-mail: junggun@kw.ac.kr).

B.-W. Min was with the Department of Electrical Engineering and Computer Science, the University of Michigan at Ann Arbor, Ann Arbor, MI 48109 USA. He is now with Qualcomm Inc., Santa Clara, CA 95051 USA (e-mail: byungmin@qualcomn.com).

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Recently, silicon RFICs have been emerged as a practical solution for phased array back-ends due to their high integration density, yield, and functionality on a single chip. An optimal phased array for high performance applications will therefore use III–V components for low-noise amplification and RF power generation together with silicon RFICs for the back-end functions (phase and gain control, power combining, digital control and processing, etc.). Also, with silicon RFICs, one can integrate multiple elements (8–16) on a single silicon chip with excellent uniformity. This not only reduces the number of chips to be assembled in the phased array but also greatly simplifies the control routing in large arrays.

Silicon-based phased-arrays have been recently demonstrated at 6 to 77 GHz using a variety of architectures: All-RF phase shifting [5]–[12], IF-path [13], or LO-path [14]–[17], phase shifting, and digital beam-forming techniques [18]–[20]. The transmit/receive implementation in [14] employs separate phase shifters for the transmit and receive paths and results in potential phase errors between the transmit and receive paths across temperature and process variations. The classical design presented in [4], [5], [11], and in this work uses a single passive (bidirectional) RF phase shifter and results in excellent tracking between the transmit and receive beams, reduced chip area and power consumption (see Fig. 1).

In addition to the results presented in [5], this paper discusses the T/R module system level design, presents single element results and their comparison with simulations, presents new results on the VGA control, P1dB, IP3, and NF, characterizes the channel to channel coupling both at the S-parameter level and in the rms gain and phase error introduced from one channel to the other, shows chip-to-chip variations over 10 chips and 40 channels, and analyzes and shows the T/R module performance versus temperature.

II. System Level and Circuit Design

Fig. 1 presents the system-level diagram of the four-element transmit/receive Ka-band phased array built using the IBM 8HP process. The silicon chip is designed to be "transparent", that is, with a gain of $\sim$ 0 dB per channel, relatively high linearity, and a noise figure of $\sim$ 9 dB at 35 GHz. The additional increase in the system-level noise figure due to this chip is only 0.3 dB when coupled to a GaAs LNA with a gain of 16 dB. The chip is built in 50 Ω blocks for ease of design and analysis. The transmit and receive gain stages are designed with 21–22 dB gain so as to offset

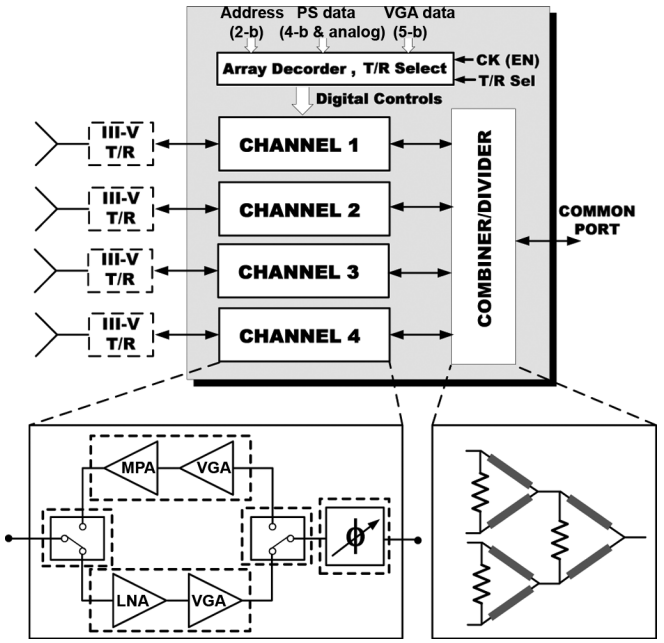

Fig. 1. Block diagram of the four-element Ka-band phased array silicon chip. The 50 Ω blocks are shown in dashed lines. (After [5].)

the loss of the two SPDT switches, the passive 5-bit phase shifter and the 4:1 Wilkinson power combiner. Gain control is implemented using variable-gain amplifiers (VGAs) in the transmit and receive paths. The chip contains all the necessary digital circuits for phased array control (address decoders, phase shift buffers, T/R select, etc.) which are implemented using 0.13-μm CMOS transistors.

The phased array chip has four antenna ports and one common RF port, and is built using a single-ended implementation throughout the entire chip for reduced power consumption and chip area. It is well known that a differential implementation results in a lower channel-to-channel coupling [7], [8], but the single-ended design, when well designed, still results in excellent performance (see Section III).

Figs. 2 and 3 present circuit-level implementations of a single channel. Starting from the antenna port, the series-shunt single-pole double-throw (SPDT) switch is based on triple-well 0.13-μm CMOS transistors with a loss of $\sim$2.5 dB, an isolation of $>$ 27 dB [21], an input P1dB of $\sim$ 13 dB, and an IIP3$>$ 24 dBm at 35 GHz. The switch is matched to 50 Ω at its input and output ports. The SiGe receive LNA is a cascode design with an inductive load and de-Q resistors for wideband operation ($V_{\rm dd} = 1.8$ V, $I = 4$ mA) and a simulated gain of 14.3 dB at 35 GHz. This is followed by a current-steering SiGe VGA with $+7.7$ to -2.3 dB gain control using 5-bit current steering (14 mA) [22], and by another SPDT CMOS switch. The VGA role is to equalize the amplitude variation in the phase shifter and to set a specific taper on the phased array aperture for reduced sidelobes. The simulated gain, NF, input P1dB, and IIP3 of the LNA/VGA is 22 dB, 5.2 dB, -22.5 dBm, and -12 dBm at 35 GHz, respectively, and for maximum VGA gain setting. The linearity is limited by the LNA stage and not by the VGA or SPDT switches.

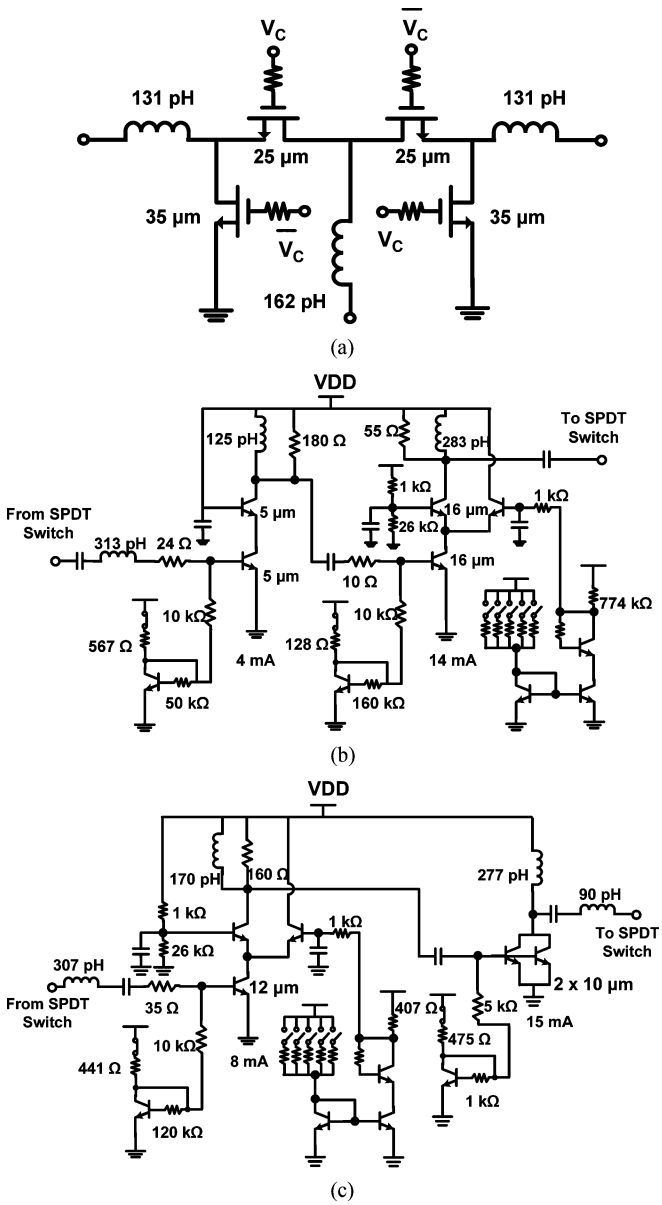

Fig. 2. Circuit diagrams of (a) series-shunt SPDT, (b) LNA/VGA, and (c) medium power amplifier/VGA. (After [5].)

In the transmit path, the SPDT switch feeds a similar VGA circuit with a gain control of $+16$ to 6 dB, which is then followed by a SiGe medium-power amplifier (MPA) with a gain of 6 dB at 35 GHz. The output stage consumes 15 mA $(\mathrm{PAE} = 17.7\%)$. The simulated gain and output P1dB of the VGA/MPA is 22 dB and $+6.8$ dBm, respectively, at 35 GHz.

The transmit-receive cell composed of the SPDT/LNA/VGA/SPDT/VGA/MPA is stable at all frequencies. This is due to the high isolation of the SPDT switches $(>$ 25 dB$)$ and the low electromagnetic coupling between the transmit and receive amplifiers.

The 5-bit phase shifter is a switched LC network design for the 4-bit stages $(22.5^\circ,\ 45^\circ,\ 90^\circ,\ 180^\circ)$ and an LC-π network for the 11° state using hyperabrupt varactor (HAVAR) diodes used in a digital mode (see Fig. 3) [23]. The fifth-bit can also be used in the analog mode for continuous phase coverage. The

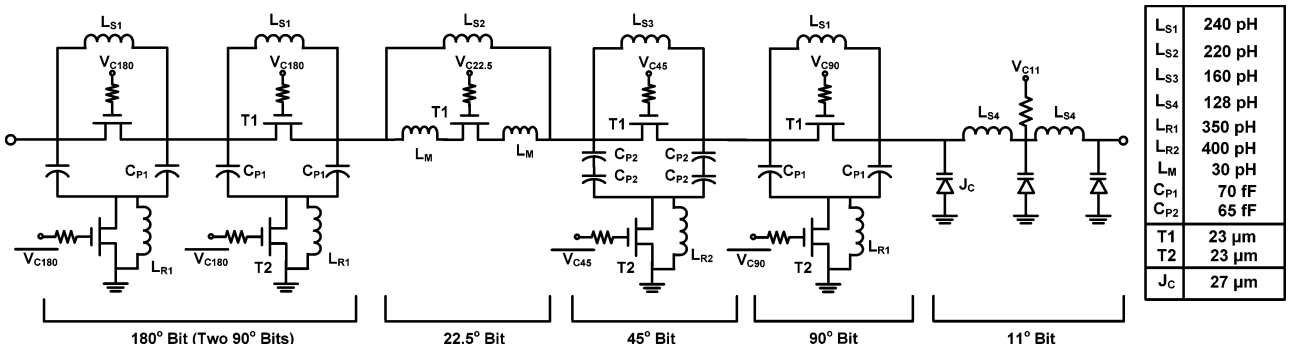

Fig. 3. CMOS phase shifter with 4-bit digital tuning and analog/digital for the fifth bit.

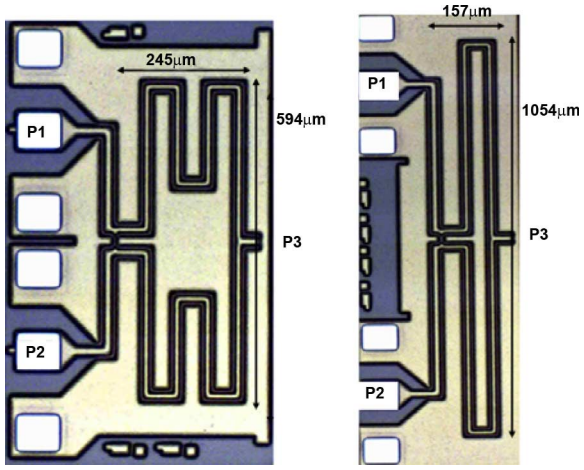

Fig. 4. Ka-band Wilkinson dividers/combiners using folded CPW transmission-lines. (From [5].)

phase shifter switches between a bypass state (T1 on, T2 off, $\sim 0°$) and various CLC low-pass networks (T1 off, T2 on, 22.5°, 45°, 90°, 180°) using 0.13-μm CMOS transistors. The design is based on true-time delay networks with a linear phase versus frequency. The simulated loss of the passive phase shifter is of 13.6 ± 1.9 dB at 35 GHz depending on the phase shift, and is matched to 50 Ω at both ports (S11, S22 < -13 dB). A VGA is therefore imperative to result in low rms gain error. The simulated input P1dB depends on the phase state and is 8.7–11.2 dBm and 9.5–11.7 dBm, from Port 1 (180° bit) and Port 2 (11° bit), respectively. The phase shifter can therefore be used behind the high-gain receiver or in a medium-power transmit path without any system-level degradation.

A two-stage 50 Ω Wilkinson network is used at the common port of the phased array chip and is based on meandered 70-Ω quarter-wave transmission lines (see Fig. 4) [24]. This bidirectional network provides high isolation between the channels, and acts as a power divider or a power combiner in the transmit and receive modes, respectively. It also has high power handling capability with zero current consumption. This is important since the input power must be $\sim +9$ dBm for a channel gain of ~ 2 dB and an output power of $\sim +4$ dBm per channel, and an active combiner network, other than being unidirectional, will require a high bias current. The Wilkinson networks were tested at 34–39 GHz and show an insertion loss of 0.6–0.7 dB, an isolation of >23 dB, a return loss < -20 dB and < -15 dB at the input and common ports, respectively [5].

The system-level simulations done on the four-channel transmit/receive chip show a receive channel gain and NF of 1.9 and 8.0 dB, respectively, at 35 GHz, with an input P1dB of -21 dBm. On the transmit side, the channel gain is also 1.9 dB with an output P1dB of $+4.3$ dBm at 35 GHz. The inherent 6 dB power divider loss (or combiner gain) is not taken into the gain values. Note that the input power must be quite high ($> +10$ dBm) in order to drive all channels to their output P1dB or Psat levels and thus the use of a Wilkinson power divider/combiner. All simulations are done at maximum gain settings.

The phased array chips are implemented in the IBM 8HP process with 8 metal layers. This process has 0.13 μm SiGe transistors (f_T of 180–200 GHz) and 0.13 μm CMOS transistors (f_T of 90–100 GHz). Grounded CPW transmission lines are used with dimensions of $11/12/11$ μm and $11/6/11$ μm for 50 and 70 Ω, respectively, and with a measured loss of 0.4 dB/mm for the 50 Ω line at 35 GHz. Standard IBM transistor cells and models are used, and deep trench isolation is employed to reduce substrate coupling between the channels. Full electromagnetic modeling is done on all passives (especially inductors) using Sonnet,[1] and to estimate the channel-to-channel coupling (< -40 dB at 30–40 GHz).

Two phased array chips were produced: a single channel chip and a four-element chip using identical circuits except for the Wilkinson couplers. The single channel chip is a low risk approach and results in shorter transmission lines between a single III–V module and the silicon chip, but requires off-chip power combiners and control lines to every antenna element. The four-channel design requires longer transmission lines between the III–V modules (placed at the antennas) and the silicon chip, but results in easier phased array control (one control line for every four antenna elements). The chip dimensions are 1.7×0.75 mm^2 (single channel) and 2.00×2.02 mm^2 (four-channels). The power consumption is 43/35.5 and 172/142 mW in the transmit and receive modes, for the single channel and four-channel phased-array chips, respectively, from a 1.8 V RF supply. The digital supply is 1.5 V with nearly zero current consumption.

[1]Sonnet, ver. 11.52, Sonnet Software Inc., Syracuse, NY, 1986–2007

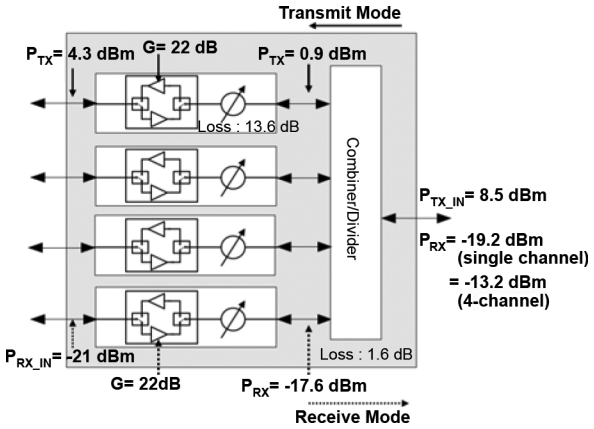

Fig. 5. System level simulations in the transmit and receive modes using the simulated S-parameters of the 50 Ω blocks.

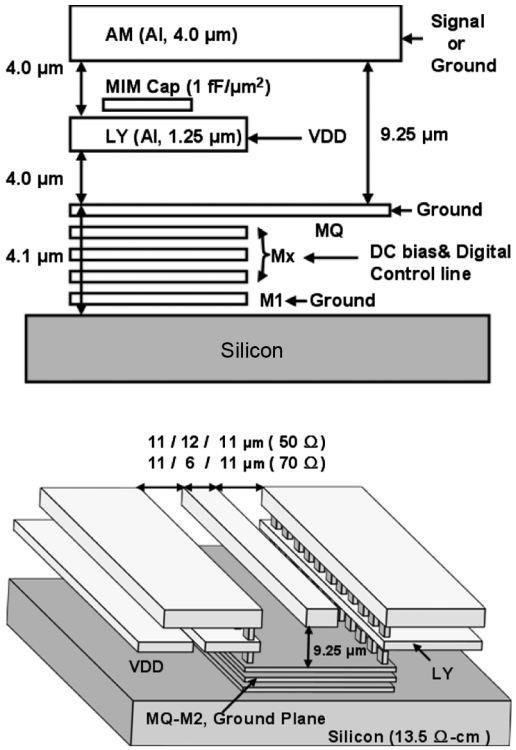

Fig. 6. Metal-stack layers of the IBM 8HP process and the CPW transmission lines.

III. Measurements

The single-element and four-element phased array chips were measured on-chip after a standard probe-tip TRL calibration. The CPW input and output pad loss is included in the measurements and is < 0.2 dB per pad at 35 GHz [23]. The only control inputs applied to the chips are supply voltages (analog and digital), address bits (2 bits for the four-element array), data bits (5 bit) and enabling clock signals to load the phase shifter data into the registers (four-element chip). The single element and four-element chips consumed a total current of 24/19.5 and 95/78 mA for the transmit and receive modes, respectively, from a 1.8 V supply, and agree quite well with simulations.

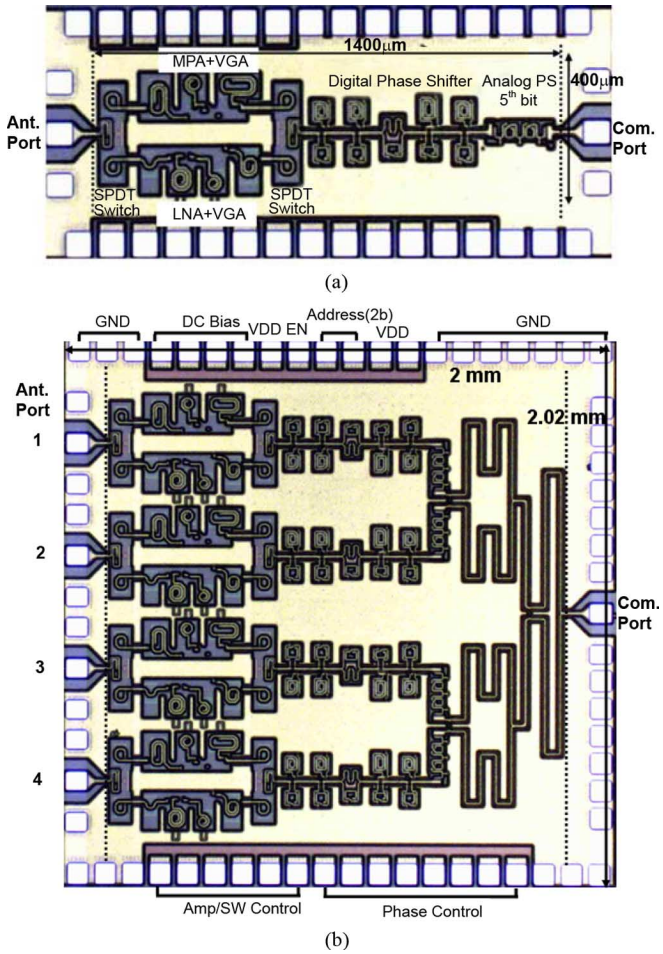

Fig. 7. Microphotographs of (a) single-element phased-array and (b) four-element phased array chip. (After [5].)

A. Single-Element Phased Array

Fig. 8 presents the measured S-parameters in the transmit and receive modes over the 32 different phase states. At the antenna port, the measured S_{11} is > 8 dB (transmit) and > 16 dB (receive) at 34–39 GHz. The measured receive gain is ~ 4 dB lower than the simulated value, and the measured transmit gain agrees decently well with simulations. The difference is due to an additional 1.2 dB loss in the measured 5-bit phase shifter (see below) and to a ~ 3.5 dB reduction in gain in the LNA, obtained from standalone test cells. The measured transmit gain is ~ 2 dB lower than the simulated value at 35 GHz and is mostly due to the phase shifter. The measured reverse isolation (not shown) is > 50 dB at 30–40 GHz in both the transmit and receive modes.

The measured VGA shows 7.5 dB of gain control over the 5-bit control states at 35 GHz (simulations show 10 dB of gain control) (see Fig. 9). The VGA insertion phase changes by 15°–20° with gain control, but this can be taken into account when controlling the phased array. The phase change within 1–2 dB of gain control is $\ll 5^\circ$ and the VGA can be used to adjust the rms gain error in the phase shifter without changing the rms phase error.

The measured phase for the transmit and receive modes are nearly identical, as expected from the design (see Fig. 10). The

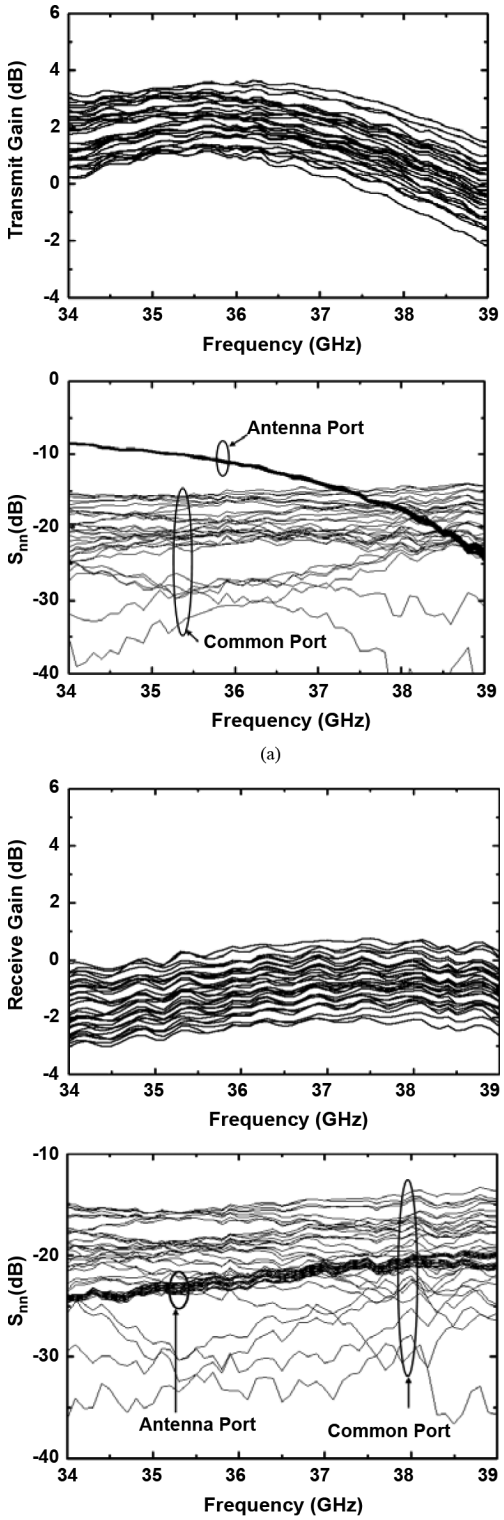

Fig. 8. Measured S-parameters of the single-element phased array over 32 phase states: (a) transmit and (b) receive mode.

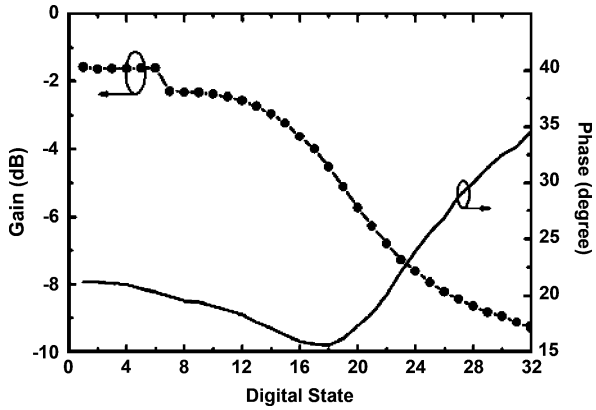

Fig. 9. Measured VGA gain control and associated change in phase shift at 35 GHz.

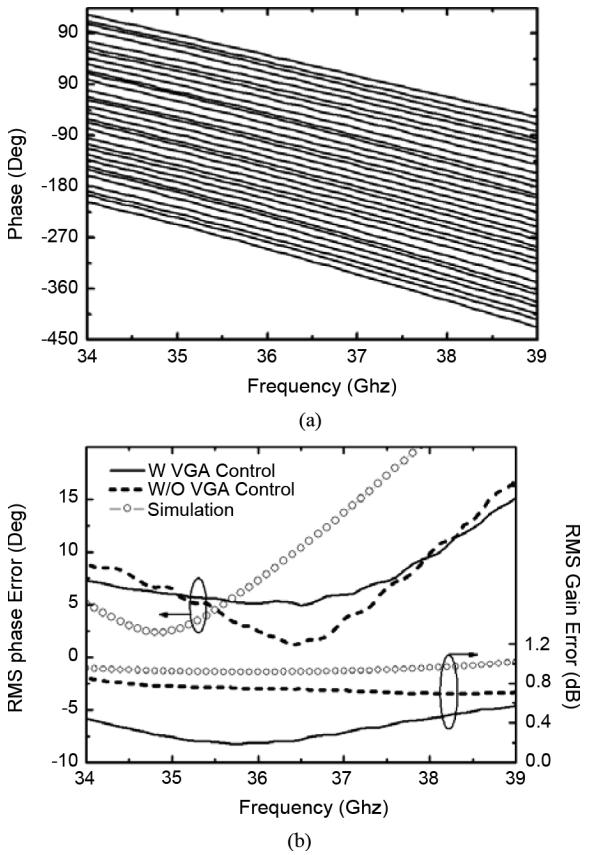

Fig. 10. (a) Measured 5-bit phase shifter using the fifth bit in an 11° digital mode and (b) associated rms gain and phase error with and without VGA control. (After [5].)

phase shifter gain, measured on a standalone unit with 50 Ω ports, is 14.8 ± 1.7 dB at 35 GHz and is about 1.2 dB higher than simulations. The measured rms phase error is $< 12^\circ$ and $< 5.6^\circ$ showing 4- and 5-bit performance over an instantaneous bandwidth of 5 GHz (34–39 GHz) and 2 GHz (36–38 GHz), respectively (see Fig. 10). The best performance shifted slightly from the design frequency of 35 to 36–37 GHz and is most probably due to passive element modeling. The corresponding rms gain variation for the transmit and receive modes is 0.7–0.9 dB with no VGA control and < 0.50 dB with VGA control at 34–39 GHz. Note that when the VGA is used to improve the rms gain error, it naturally introduces a small phase error when toggling between different gain states, and therefore slightly degrades the rms phase error. Still, the rms phase error remains $< 6^\circ$ with VGA control over a 2 GHz bandwidth (see Fig. 10). Finally, the phase shifter can also operate in the analog mode for the lowest bit, and a 0–1.5 V control results in a 0°–22°

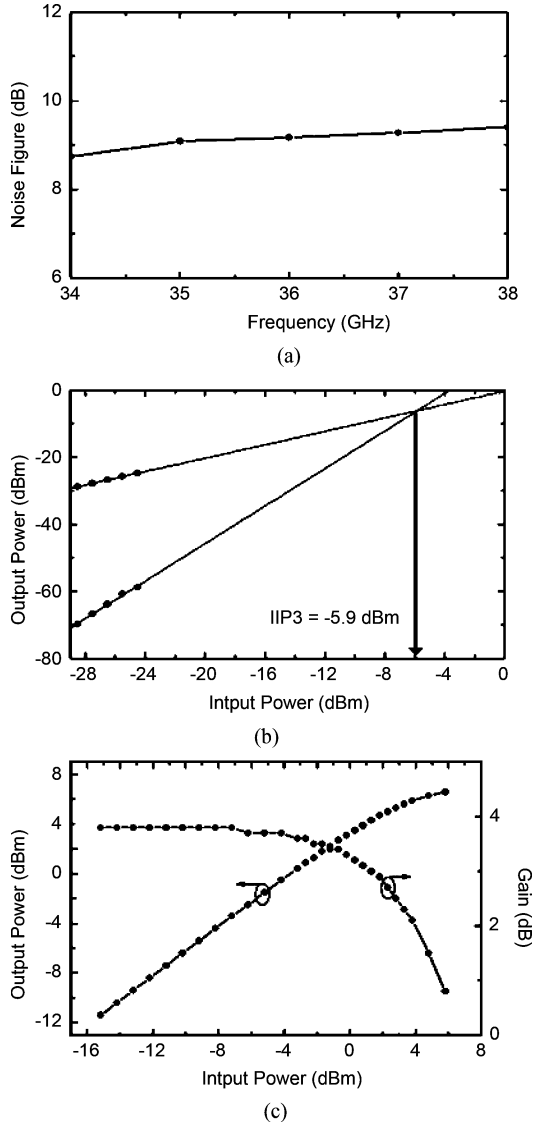

Fig. 11. Measured single element: (a) noise figure; (b) IIP3 at 36 GHz; (c) P1dB at 36 GHz. Measurements done at the 00000 phase state.

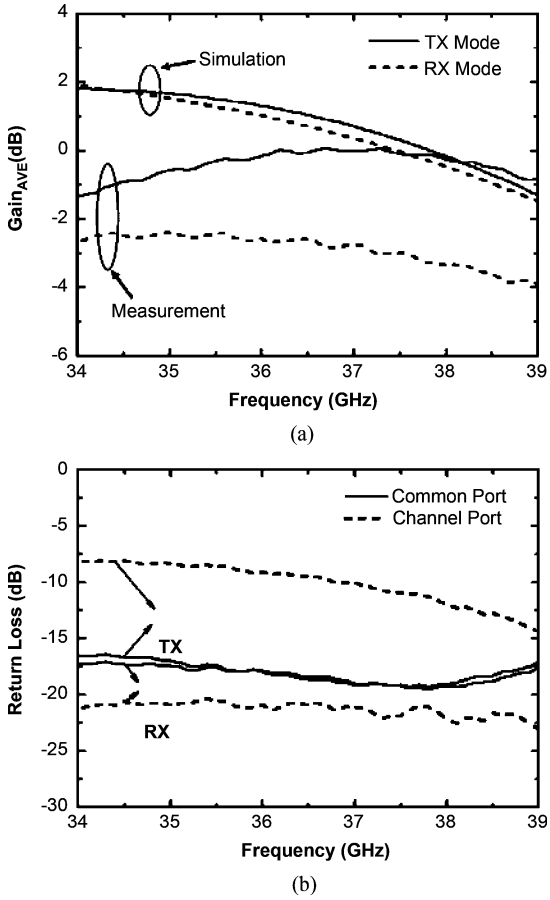

Fig. 12. Four-element phased array: (a) measured average gain in the transmit and receive modes and the (b) measured average antenna port and common port return loss in the transmit and receive modes.

TABLE I
PERFORMANCE SUMMARY AT 34–39 GHZ

	RX	TX
Gain @36 GHz (single)	-1 dB	2.0 dB
Gain* @36 GHz (array)	-2.5 dB	0 dB
Phase Error (RMS)	< 5.6° @ 36-38 GHz < 12° @ 34-39 GHz	< 4.9° @ 36-38 GHz < 12° @ 34-39 GHz
Gain Error (RMS)	< 0.9 dB (w/o VGA) < 0.5 dB (w VGA)	< 0.7 dB (w/o VGA) < 0.5 dB (w VGA)
Common Port Return Loss	> 16 dB > 14 dB (single)	> 16 dB > 14 dB (single)
Antenna Port Return Loss	> 20 dB > 20 dB (single)	> 8 dB > 8.6 dB (single)
Power Consumption	142 mW /35.5 mW (single)	171 mW /43 mW (single)
OP1dB @ 36 GHz	-18 dBm (single)	4.7 dBm (single)
IP1dB @ 36 GHz	-16 dBm (single)	3.7 dBm (single)
IIP3 @ 36 GHz	-5.9 dBm (single)	13 dBm (single)
Common port P1dB	-13.5 dBm (array)	11.3 dBm (array)
Gain Control	7 dB (5-bit)	
Phase Control	5-bit	
Noise Figure	9 dB (single)	
Supply Voltage	1.8 V (analog), 1.5 V (digital)	
Area	2.00 x 2.02 mm^2 / 1.7 x 0.75 mm^2(single)	
Technology	0.13-μm SiGe BiCMOS	

phase change. This is recommended if a $>$ 5-bit phase resolution is required but with a narrower bandwidth.

In the receive mode, the measured noise figure is 9 ± 0.2 dB at 34–37 GHz and is 1 dB higher than simulations (see Fig. 11). The measured input P1dB is -16 dBm at 35 and at 36 GHz, and is 5 dB better than simulations. Both results are expected due to the decrease in the measured versus simulated LNA gain. The IIP3 is -5.9 dBm which is acceptable for satellite communication systems. In the transmit mode, the measured output P1dB is $+3.9$–5.0 dBm at 35 and 36 GHz, and agrees well with simulations. The simulated output IP3 is 14.8 dBm at 36 GHz.

B. Four-Element Phased Array

The measured gain in the transmit and receive mode is very similar to single channel chip except for an additional 1.2–1.4 dB loss due to the two-stage Wilkinson coupler. Fig. 12 presents the measured *average* gains in the transmit and receive modes, together with the antenna port and common reflection coefficients. The measured gain for all 32 states (not shown) is the same as the single element. The measured common-port reflection coefficient is $>$ 17 dB at 30–40 GHz in the transmit and receive modes since it is connected to the Wilkinson network. The measured phase response and corresponding rms phase and gain errors are identical to Fig. 10. The reverse isolation is $>$ 50 dB at 30–40 GHz. Other values are listed in Table I.

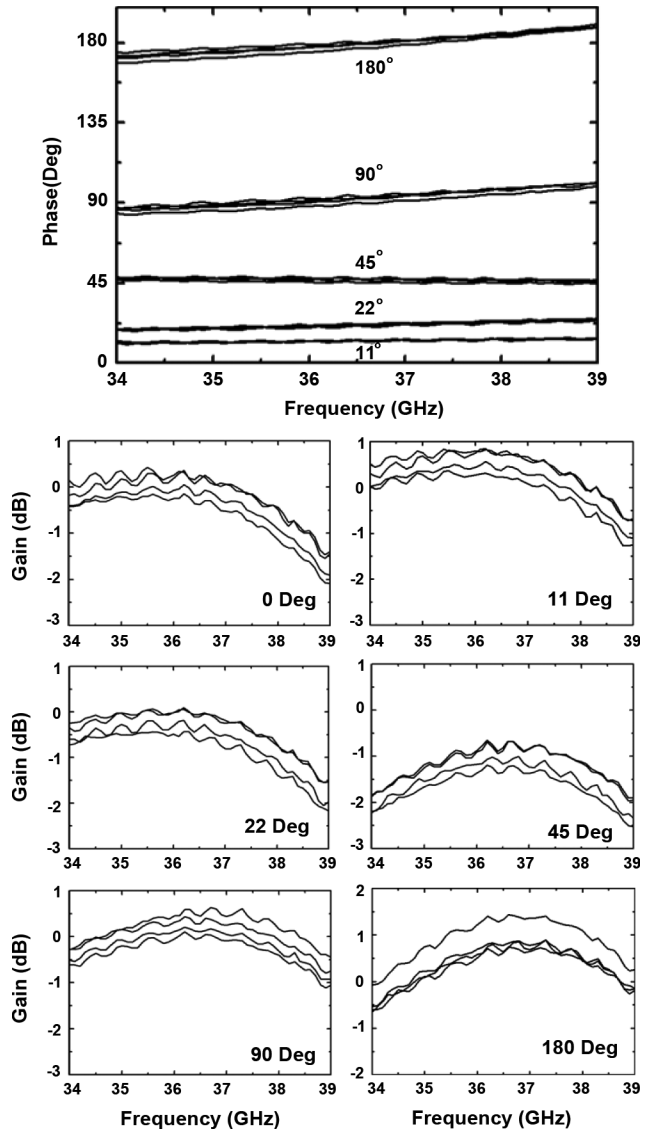

Fig. 13. Measured gain and phase response for four channels (transmit mode shown). (After [5].)

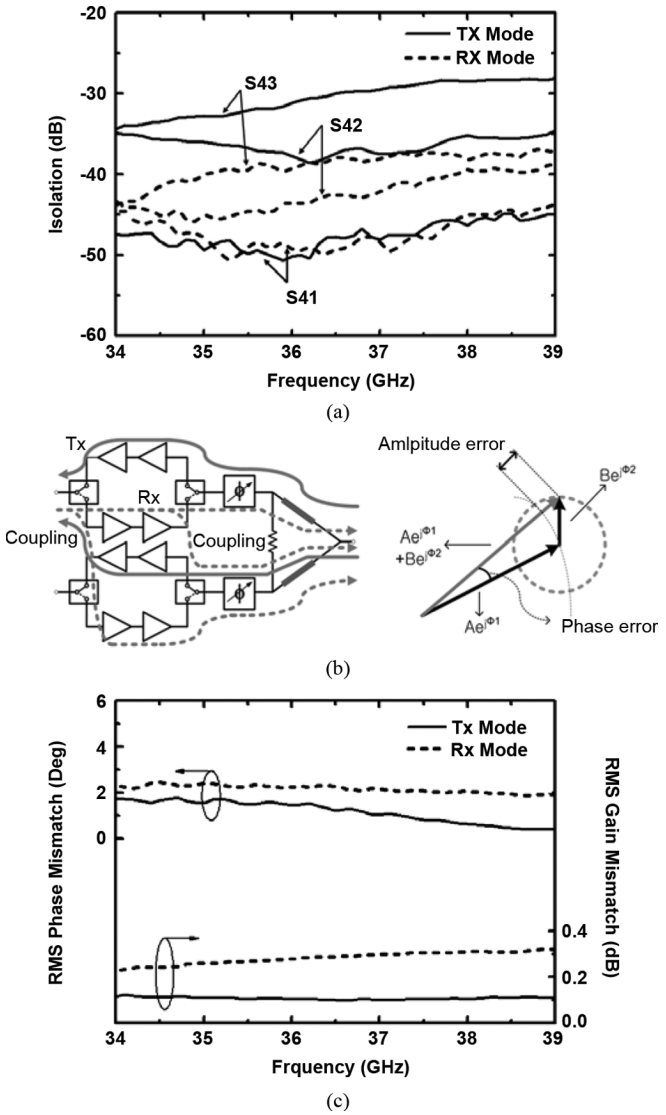

Fig. 14. Measured coupling between the different channels: (a) *Smn* measurements; (b) simplified coupling mechanism between adjacent two channels; and (c) rms error in Channel 1 due to the phase change in Channel 2 in the transmit and receive modes.

Fig. 13 presents the measured four channels phase and amplitude response with virtually identical response between all channels over all phase states. In these measurements, the other channels were left open-circuited which presents a worst-case condition in terms of coupling [6], [7]. No calibration was done on the array, and the measurements include probe placement errors, cable movement effects, etc.

The measured isolation S_{nm} between the channels is >36 dB in the receive mode and >28 dB in the transmit mode. Again, all other channels not connected to ports (n, m) are left open-circuited. Also, in this measurement, two independent ground-signal ground (GSG) CPW probes are used and are placed very close to each other. The channel-to-channel isolation is also measured by setting Channel 1 to 0°, changing the phase in Channel 2 from 0° to 360°, and seeing its effect at the common port (in the receive mode) or at the antenna port (in the transmit mode). As discussed in [6] and [7], this represents a stringent coupling test since any leakage from Channels 1 to 2 will undergo a different phase delay and add to Channel 1. The leakage signal therefore causes amplitude and phase errors in the true signal from Channel 1. During this measurement, the antenna port of Channel 2 is left open-circuited which results in the worst coupling case. Fig. 14 proves that the array has minimal coupling between the elements and that a phase change in Channel 2 does not affect the operation of Channel 1. A similar experiment was done between Channels 1 and 3 and resulted in insignificant coupling.

C. Performance Versus Temperature

Fig. 15 presents the measured rms phase and gain error versus temperature of Channel 1 in the transmit mode for the four-element phased array chip. The phase shifter results in excellent rms phase error performance versus temperature since it is based on switched *LC* circuits. The only penalty is a slight increase in the rms gain error due to the additional loss of the CMOS

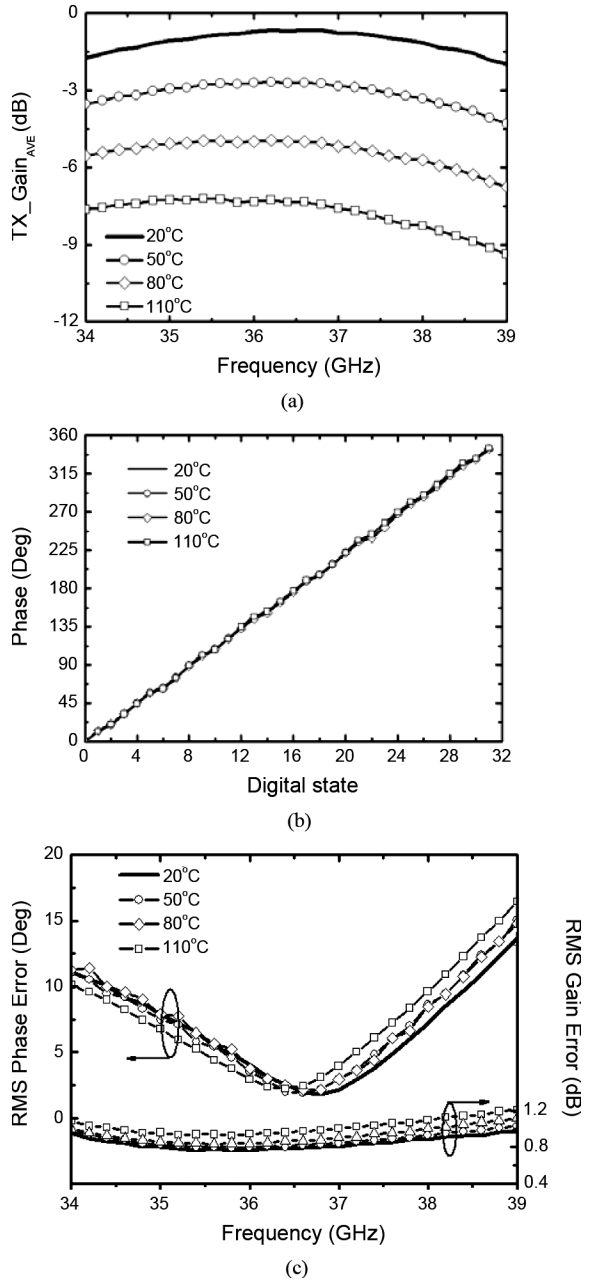

Fig. 15. (a) Measured average channel gain, (b) measured phase shift at 36 GHz versus temperature, and (c) rms phase error and gain error versus temperature. The chip does not contain a PTAT current source and draws the same current per channel (27 mAx4) from 20 °C to 110 °C. The simulated phase and phase error at 0 °C is the same as 20 °C and is not shown.

switches in the phase shifter. This can be explained by looking at the CMOS in the triode mode with [25]

$$R_{\rm on} = \left[\mu_n C_{\rm ox}\frac{W}{L}(V_{\rm GS} - V_{\rm TH})\right]^{-1}. \tag{1}$$

The reduction mobility with increasing temperature is modeled using

$$\mu(T) = \mu(T_o)\left(\frac{T_0}{T}\right)^{1.5} \tag{2}$$

and the threshold voltage decreases with temperature as

$$\frac{\partial V_{\rm th}}{\partial T} \cong -0.6\,\frac{mV}{C^0}. \tag{3}$$

Using (1) to (3), the $R_{\rm on}$ change with temperature is

$$\frac{R_{\rm on}(110°{\rm C})}{R_{\rm on}(20°{\rm C})} = \frac{\mu_n(20°{\rm C})}{\mu_n(110°{\rm C})}\,\frac{V_{\rm GS} - V_{\rm TH}(20°{\rm C})}{V_{\rm GS} - V_{\rm TH}(110°{\rm C})}. \tag{4}$$

For $V_{\rm GS} = 1.5$ V, $V_{\rm TH}(20°{\rm C}) = 0.4$ V, we find

$$\frac{R_{\rm on}(110°{\rm C})}{R_{\rm on}(20°{\rm C})} = 1.41 \tag{5}$$

and $R_{\rm on}$ increases from 20 Ω (20 °C) to 28 Ω (110 °C). This results in an increase in the loss of the 90° phase shifter cell by 0.1 dB from 20 °C to 110 °C. The simulated average phase shifter gain therefore decreases from −13.6 dB at 20 °C to −15.1 dB at 110 °C due to the increase in the CMOS switch loss. The corresponding rms gain error increases from 0.7 dB to 1.1 dB at 36 GHz. The simulated values at 35–36 GHz agree well with measurements. The rms phase error shift from −55 °C to 20 °C is verified by simulations only due to the absence of a low-temperature measurement setup, and shifts 2.5°.

Fig. 15 shows that the measured channel gain drops by 4.0–6.5 dB at 80–110 °C, but it should be noted that the design does not use a PTAT bias circuit and therefore, the chip is operating at the same current up to 110 °C. Simulations indicate that at 110 °C, the MPA and VGA result in 2.5 and 1.5 dB gain reduction, respectively, the SPDT switch in 0.2 dB additional loss, the phase shifter in 1.5 dB additional loss (as shown above), and yields a total simulated additional loss of 6.0 dB. This agrees well with measurements. In the future, a PTAT biasing should be used to reduce the gain variation versus temperature. Similar results were obtained in the receive mode versus temperature and are not shown.

D. Chip-to-Chip Measurements

In order to characterize the IBM 8HP silicon process, ten random single element and ten four-element phased-array chips were measured at room temperature. The chips are selected from the same fabrication lot (December 2007 IBM 8HP), and all measurements were done on-wafer with a probe tip calibration. Every channel was measured in the four-element phased array resulting in 40 different S-parameter measurements (see Fig. 16). All ten chips consumed the same current in the transmit and receive modes (to within ± 3 mA) from a 1.8 V supply. The measured gains, all taken at the 0000 phase shift state, show a peak-to-peak variation of $\sim$ 2 dB and an rms gain variation of $<$ 0.5 dB at 34–39 GHz, and demonstrate the yield and repeatability of the silicon chips. The measurements were done manually and include probe placement errors and drift in calibration over the six-hour measurement period. The single-element measurements are even better (10 channels instead of 40 channels) and are not shown.

IV. Discussion

The individual circuit blocks in millimeter-wave circuit design are generally quite straightforward in phased-array designs (LNA, VGA, SPDT switch, phase shifter) or even in transceivers

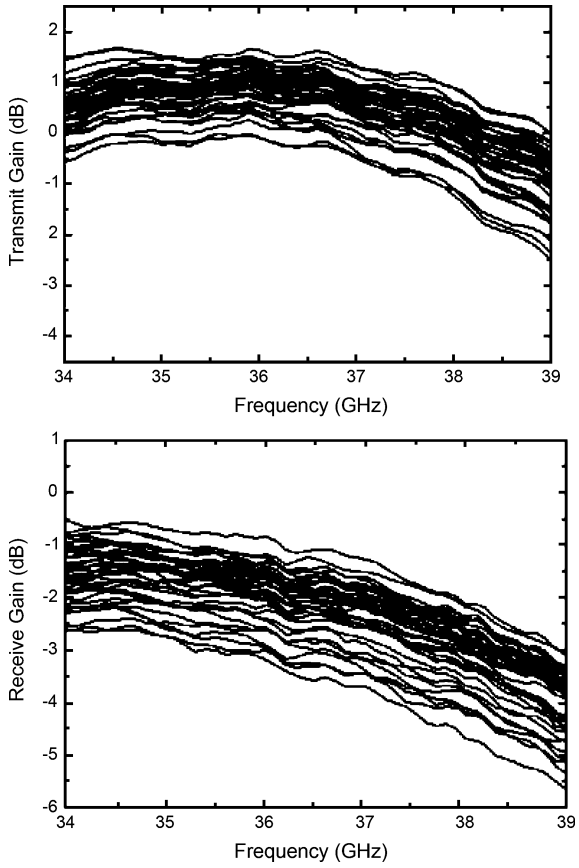

Fig. 16. Measured channel gain of ten four-element phased array chips (40 channel measurements shown). Measurements done at the 00000 state.

(LNA, mixer, SPDT switch, IF amplifier, etc.) [26], [27]. The key design points are the layout techniques for low parasitic capacitance and inductance, passive component modeling using full-wave electromagnetic techniques, and on-chip coupling reduction and simulation.

In this work, a large set of decoupling capacitors ($>$ 20 pF in total) were used all over the chip between the $V_{\rm dd}$ layer and ground in order to reduce the power-supply coupling between the different channels. Also, via-hole "walls" were used around every channel to tie the top-metal ground to the deep trench isolation layer in the silicon substrate, again to reduce the channel-to-channel coupling. Furthermore, the receive and transmit circuits for each channel are placed $>$ 400 μm from each other, and this greatly reduces the on-wafer coupling. Finally, separate bias lines and planes were used for the digital control so as to further reduce the coupling between the power supplies.

The measurements shown in this paper are all done on-chip, and careful design is needed in the future to package such a complex chip and maintain the high isolation between the channels. This can be done using flip-chip techniques with low ground-inductance connections [28].

V. Conclusion

This paper shows that complex silicon RFICs can be used as the back-end chips for high performance Ka-band phased arrays. The All-RF architecture results in a small-chip area and low power consumption while still maintaining excellent phase and amplitude control over an instantaneous bandwidth of 2–5 GHz. The design can be extended to 8–16 element arrays using an identical design and with the addition of one or two Wilkinson combining stages. This shows an important aspect of the All-RF architecture: its ease of scalability even at millimeter-wave frequencies.

Acknowledgment

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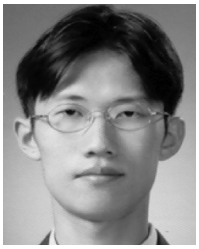
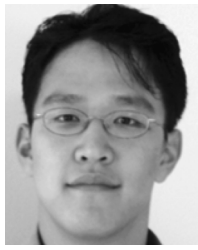


Dong-Woo Kang (A'07) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2001, 2003, and 2007, respectively.

He is currently a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla. His research interests include CMOS/SiGe ICs for microwave and millimeter wave phased arrays systems.

Jeong-Geun Kim (M'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1999, 2001, and 2005, respectively.

From October 2005 to February 2008, he was a Postdoctoral Research Fellow with the Department of Electrical and Computer Engineering, University of California at San Diego (UCSD), La Jolla. He is currently with the Department of Electronic Engineering, Kwongwoon University, Seoul, Korea. His research interests include millimeter-wave ICs and systems for short-range radar and phased-array antenna applications.



Byung-Wook Min (M'08) was born in Seoul, Korea. He received the B.S. degree from Seoul National University, Seoul, Korea, in 2002, and the M.S. and Ph.D. degrees in electrical engineering and computer science from The University of Michigan at Ann Arbor, in 2004 and 2007, respectively.

In 2006–2007, he was a Visiting Scholar with the University of California at San Diego, La Jolla. In 2008, he joined Qualcomm Inc., Santa Clara, CA. His research interests include Si/SiGe RFIC and RF MEMS for microwave and millimeter-wave applications.

Dr. Min was a recipient of the Samsung Scholarship in 2002–2007.

Gabriel M. Rebeiz (F'97) received the Ph.D. degree from the California Institute of Technology, Pasadena.

He is a Professor with the Department of Electrical and Computer Engineering, University of California at San Diego, La Jolla. Prior to this appointment, he was with The University of Michigan at Ann Arbor, from 1988 to 2004. He has contributed to planar millimeter-wave and tetrahertz antennas and imaging arrays from 1988–1996, and his group has optimized the dielectric-lens antennas, which is the most widely used antenna at millimeter-wave and tetrahertz frequencies. His group recently developed 6–18 and 30–50 GHz 8- and 16-element phased arrays on a single chip, making them one of the most complex RFICs at this frequency range. As a consultant, he developed the 24 GHz single-chip radar with USM/ViaSat, X, Ku-band, and W-band phased arrays for defense applications, the RFMD RF MEMS switch and the Agilent RF MEMS switch. He is the Director of the UCSD/DARPA Center on RF MEMS Reliability and Design Fundamentals. He is the author of the book *RF MEMS: Theory, Design and Technology* (Wiley, 2003).

Prof. Rebeiz has been an Associate Editor of IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES, and a Distinguished Lecturer for the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) and IEEE TRANSACTIONS ON ANTENNAS AND PROPAGATION. He leads a group of 21 Ph.D. students and 3 post-doctoral fellows in the area of millimeter-wave RFIC, microwaves circuits, RF MEMS, planar millimeter-wave antennas and terahertz systems. He was a recipient of an URSI Koga Gold Medal, NSF Presidential Young Investigator, Recipient, an IEEE MTT-S Distinguished Young Engineer (2003), the IEEE MTT-S 2000 Microwave Prize, the 1998 Eta-Kappa-Nu Professor of the Year Award, the 1998 Amoco Teaching Award given to the best undergraduate teacher at The University of Michigan at Ann Arbor, and the 2008 Teacher of the Year Award at the Jacobs School of Engineering, UCSD.