A 108–114 GHz 4 × 4 Wafer-Scale Phased Array Transmitter With High-Efficiency On-Chip Antennas

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***Abstract*—This paper presents a W-band wafer-scale phased-array transmitter with high-efficiency on-chip antennas. The 4×4 array is based on an RF beamforming architecture with an equiphase distribution network and phased shifters placed on every element. The differential on-chip antennas are implemented using a 100 μm thick quartz superstrate and with a simulated efficiency of $\sim$ 45% at 110 GHz. The phased array is designed with low mutual coupling between the elements and results in a stable active antenna impedance versus scan angle. The phased array is built in the Jazz SBC18H3 SiGe BiCMOS process, and is 6.5×6.0 mm^2. Measurements show two-dimensional pattern scanning capabilities with a directivity of 17.0 dB, an array gain of $\sim$ 26.5 dB at 110 GHz, and an EIRP of 23–25 dBm at 108–114 GHz. The power consumption is 3.4 W from a 1.9 V supply. To our knowledge, this work represents the first W-band wafer-scale phased array to-date. The application areas are in point-to-point communication systems in the 100–120 GHz range.**

***Index Terms*—Antenna array, millimeter-wave integrated circuits, on-chip antennas, phased arrays, silicon germanium.**

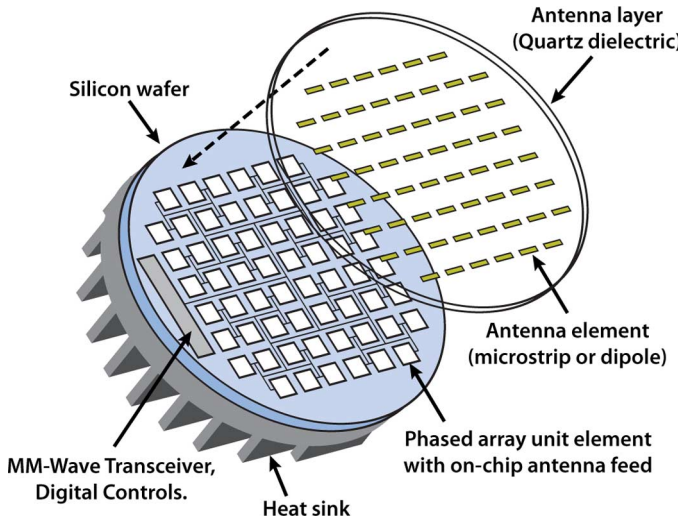

Fig. 1. Conceptual diagram of a millimeter-wave wafer-scale phased array with on-chip antennas.

I. Introduction

MILLIMETER-WAVE phased-arrays on silicon RFICs have been an important topic of research in the past 5 years with application areas in Gbps communications and automotive radars. After the early demonstrations of single, four and 8-elements arrays on a single-chip [1]–[9], the phased-arrays quickly jumped to 16 and 32-elements on a single-chip [10]–[15]. For a phased array with N-elements and in the transmit mode, the EIRP (effective isotropic radiated power) is defined as $P_T G_T$ where P_T is the total transmit power and G_T is the transmit antenna gain [16]. P_T is N times the power radiated per element and G_T is proportional to N and the EIRP is proportional to N^2. In the receive mode, the phased array antenna gain is also proportional to N. Therefore, the link budget, which is proportional to $P_T G_T G_R$ has an N^3 dependence, and phased arrays with $N = 16 - 32$ or even $N = 64 - 256$ are therefore required for medium to long-range Gbps communication links, automotive radars or active imaging arrays.

The 8, 16, and 32-element phased-array chips did not include any antennas, and therefore, a transmission-line distribution network was used between the N-element silicon chip and the planar antenna array. This required mm-wave transitions between the silicon chip and the distribution network, and was successfully done using flip-chip techniques and multilayer organic, Teflon or LTCC substrates [11], [12], [17]–[26], or using polyimide re-distribution layers on-top of the silicon chip to result in a wafer-level package (WLP) or chip-scale package (CSP) [27]–[29]. However, the transitions and distribution network adds a substantial amount of loss (2–4 dB at 60–80 GHz for 16 elements) between the silicon chip and the antennas, and requires careful design so as not to introduce electromagnetic coupling between the different antenna elements which can degrade the patterns. Also, it is not scalable beyond 16 (or 32) elements due to the additional loss and distribution complexity. Finally, multi-layer Teflon and LTCC substrates for mm-wave systems are generally as expensive as the silicon chip, which can double the cost of the front-end system.

Wafer-scale phased arrays offer a simple solution to the complex distribution problem (Fig. 1). In this case, a wafer-scale antenna layer is placed directly above the silicon substrate and each antenna is fed by a corresponding phased-array cell (phase shifters, VGA, etc.). This approach eliminates the distribution network loss, can be applied to a 4-element and even a 64-element phased array, and has been proven before at 77 GHz [30], at 90–100 GHz for a 3×3 power amplifier array [31], and at

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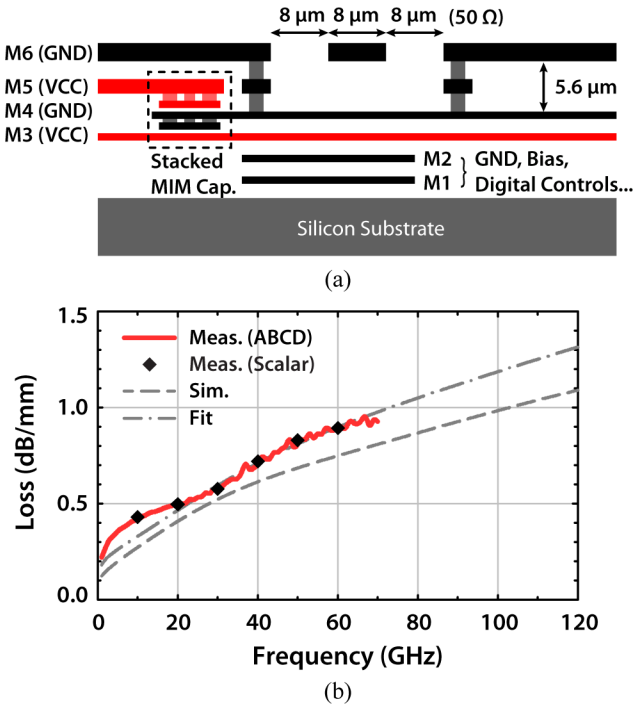


Fig. 2. (a) Cross section view of metal layers of the Jazz SBC18H3 technology. An on-chip 50 Ω G-CPW transmission line is shown. (b) Measured and simulated loss of the transmission line.

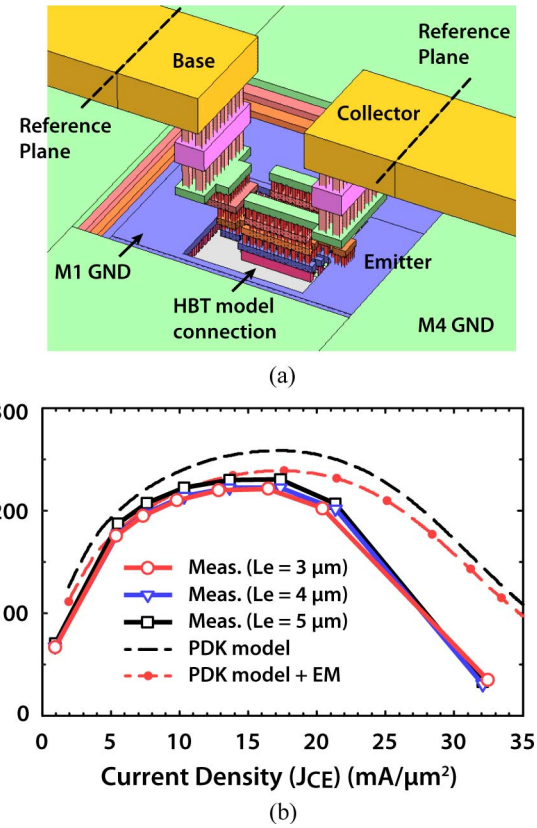


Fig. 3. (a) 3-D EM modeling of the transistor contact. (b) Simulated and measured f_t of HBT transistors.

110 GHz in a 16-element wafer-scale phased array [32]. The concept is also scalable to a very large number of elements (true wafer-scale) but in this case, care should be placed on the power and RF distribution loss for such systems. The antennas must be efficient ($\sim 50\%$) so as to be competitive with the standard technique, and such antennas are currently being demonstrated in many self-contained sensors, radars and short-range communication systems [33]–[38]. The wafer-scale approach is also popular at THz frequencies and several groups have demonstrated imaging arrays [39]–[41] and transmitters [42] based on high-efficiency on-chip antennas.

It is important to note that the wafer-scale approach does require that the silicon chip be as large as the antenna aperture, which may not be feasible below 60 GHz. For these applications, it is best to build a smaller silicon chip and fan out to the antennas using a multi-layer substrate [12], [18], [22]. However, above 60 GHz, and especially for large systems, the wafer-scale approach may be an excellent solution for phased arrays knowing that the silicon cost continues to drop even for advanced CMOS and SiGe nodes.

II. Design

A. Technology

The 16-element wafer-scale phased array is built using Jazz SBC18H3 process. It is 0.18 μm SiGe BiCMOS process which provides high-speed HBT (0.13 μm emitter width), 6 aluminum metal layers (2.8 μm top metal thickness), and high-density MIM capacitors (5.6 fF/μm^2). The cross section view of the technology backend is shown in Fig. 2. The high-speed HBT has a peak $f_t/f_{\max}$ of 240/280 GHz [43].

Grounded co-planar waveguide (G-CPW) transmission lines are heavily used in this phased array for the distribution network and as inductor loads, in order to have high isolation between two adjacent lines or components. The 50 Ω transmission line is implemented using M6 for the signal line and M4 for the ground plane (Fig. 2(a)). The electromagnetic (EM) simulations using Sonnet [44] show an attenuation (α) of 1.0 dB/mm and propagation constant (β) of 4.4 rad/mm at 110 GHz, resulting in transmission line Q ($\beta/2\alpha$) of 18.8. The effective dielectric constant ($\epsilon_{r,eff}$) is 3.64, resulting in a wavelength of 1.43 mm at 110 GHz.

A 1 mm-long line is measured at DC–67 GHz, and the GSG pad parasitics are de-embedded using an on-chip through standard. Fig. 2(b) presents the measured line loss along with simulations. The line loss is calculated in two ways, one using ABCD-parameters [45] and the other using scalar loss subtraction. Both calculations show consistency, and the measured line loss is 0.9 dB/mm at 60 GHz while the simulation predicts 0.75 dB/mm. A modified simulation fitted to the measurement predicts 1.25 dB/mm line loss at 110 GHz, with a t-line Q of 15.0.

Several transistor test structures are also measured in order to examine the effect of metal interconnect parasitics on the transistor performance. A two-step open-short de-embedding in M6 is performed for the test structures, and resulting data include the effect of base/collector contacts and the ground plane (Fig. 3(a)). The measured f_t of the transistor along with simulations are presented in Fig. 3(b). f_t is extrapolated from H_{21} at 20 GHz assuming -20 dB/dec slope, and the measured peak f_t is 220–230 GHz at a current density of 10–17 mA/μm^2.

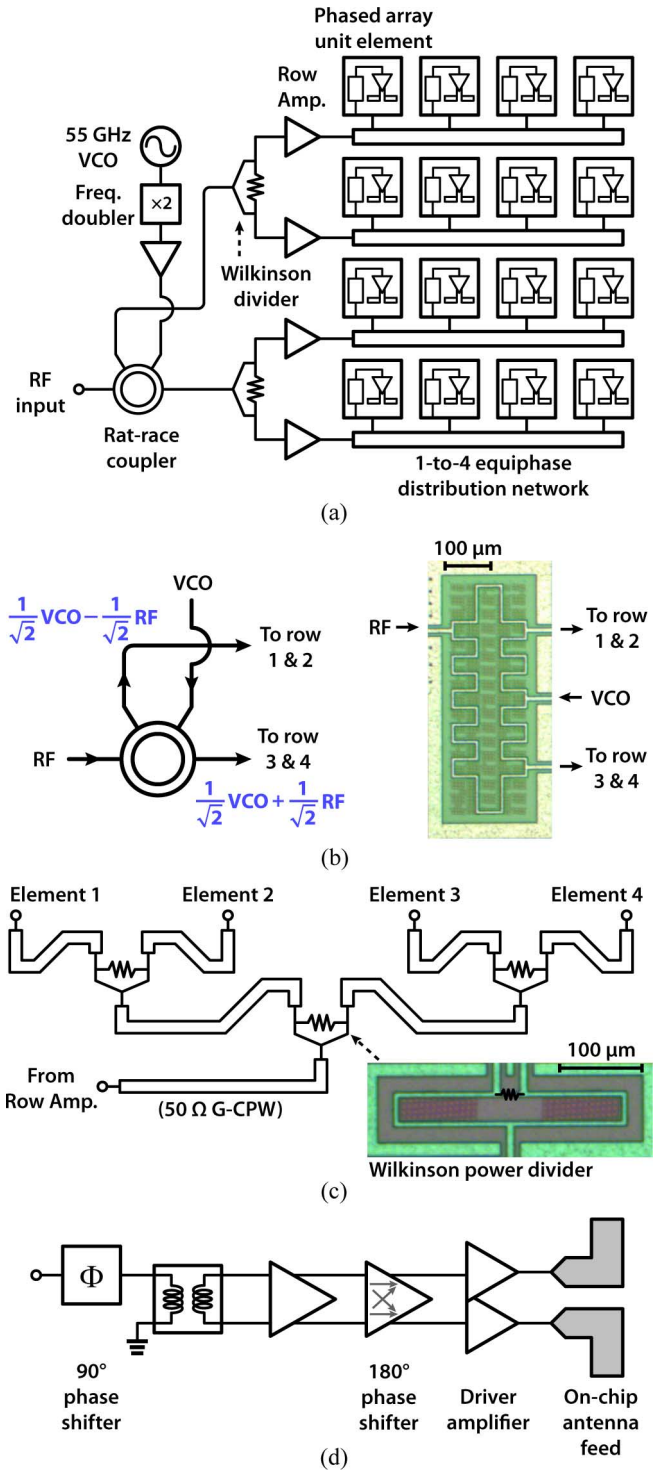


Fig. 4. Block diagrams of (a) the 4 × 4 wafer-scale phased array, (b) the rat-race coupler, (c) the 1-to-4 equiphase distribution network, and (d) the phased-array unit-element.

B. Architecture

The block diagram of 4 × 4 wafer-scale phased array is shown in Fig. 4(a). A 54–56 GHz oscillator is used together with a frequency doubler and an amplifier as a 108–112 GHz on-chip source. A rat-race coupler (0°/180° hybrid) is employed and is connected to the VCO and an external RF input. The rat-race coupler provides > 20 dB isolation at 95–130 GHz between the two different inputs and allows the use of either the on-chip VCO or the external input as the transmission source (Fig. 4(b)). It also provides a 3-dB power division between the top-half and bottom-half of the chip, which is necessary for power distribution. The VCO signal results in a 0°/0° phase difference at the outputs of the rat-race coupler and no phase correction is needed. The signal from the RF input results in a 0°/180° phase difference at the outputs of the rat-race coupler, but this is corrected using the 180° phase shifter in each unit element. The rat-race coupler therefore allows an efficient selection of two different input signals together with power division in a 4-port network with minimal loss.

The RF signals are then split using two Wilkinson dividers into 4 row amplifiers, and then split again in an equiphase network consisting of additional Wilkinson dividers and transmission-lines (Fig. 4(c)). This ensures that all the 16 signals arriving to each unit element are in phase and no phase correction is needed for the distribution network (other than the 0°/180° from the external RF input due to the rat-race coupler). The unit element consists of a single-ended 90° phase shifter, a passive balun with a buffer amplifier, a differential 180° phase shifter, a pseudodifferential driver amplifier, and a differential high-efficiency wafer-scale dipole antenna. (Fig. 4(d)). The design therefore has a 2-bit phase shifter in each unit element capable of generating phase shifts of 0°, −90°, −180°, and −270°.

C. On-Chip VCO and Distribution Network

An 112–114 GHz source is integrated on-chip so as to test the wafer-scale phased array without an external W-band proble. A differential cross-coupled oscillator with a common-collector buffer is used for the VCO (Fig. 5(a)). A DC decoupling capacitor (C1) is used for bias control and a common-mode tail resistor (R1) is used for bias stabilization. The shunt capacitor C2 is used to suppress noise from R1 [46]. An accumulation-mode MOS (AMOS) varactor (M1) in series with an MIM capacitor (C3) is used for capacitive tuning. C3 allows a full range (0–V_{CC}) on the control voltage and increases the tuning range. The bias current density is 5.8 mA/μm^2 in order to achieve a balance between output amplitude, power consumption, and phase noise. The VCO and buffer consume 30 mA from 1.5 V supply and result in a simulated 1.0 dBm output power with a phase noise of −85 dBc/Hz at 1 MHz offset. Its tuning range is 56–57.5 GHz with 0–1.5 V control voltage.

The 55–110 GHz balanced doubler is designed using a differential pair (Q1) followed by a cascode stage (Q2) (Fig. 5(b)). The Q1 transistors are biased at a low current level (1.6 mA/μm^2) in order to efficiently generate harmonics of the input signal [47], [48]. Due to its balanced operation, only even harmonics are combined constructively at the collector node. Input and output matching provide maximal power transfer at 1st and 2nd harmonics, respectively. The simulated conversion gain is −5.0 dB at 110 GHz with 1.0 dBm input.

A 4-stage common source (CS) amplifier is used after the doubler (Fig. 6), and it is also used in the 1-to-4 distribution network (referred as "row amplifier"). An emitter length of 3–5 μm is found to be optimal as it has a low base resistance and provides a maximum available gain (MAG) of 4.4 dB at 110 GHz. Each transistor is biased at 10–15 mA/μm^2 collector current density for high f_t and $f_{\max}$. G-CPW 50 Ω transmission lines are used as inductive loads and single-stack MIM capacitors are

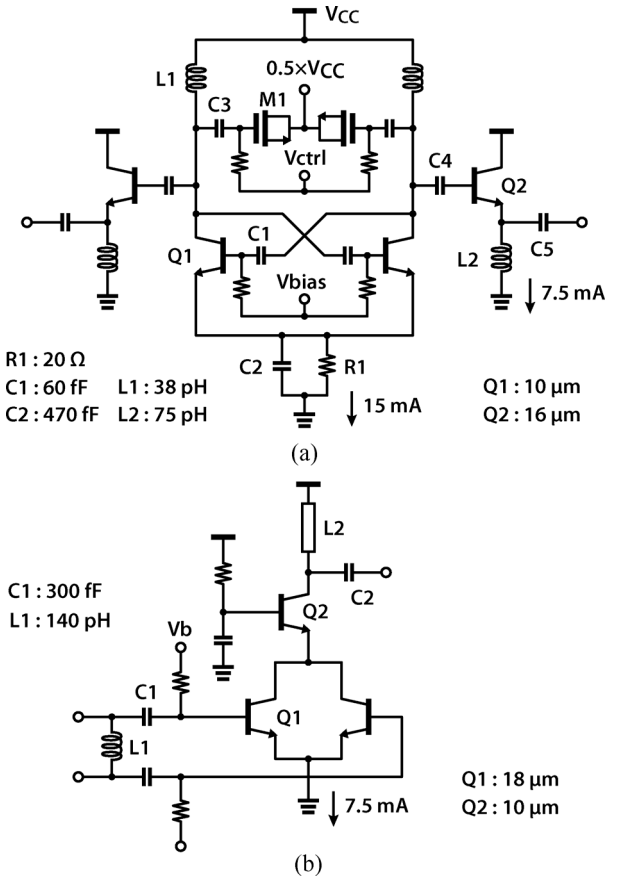


Fig. 5. Schematic of (a) the 55 GHz VCO and (b) the 110 GHz frequency doubler.

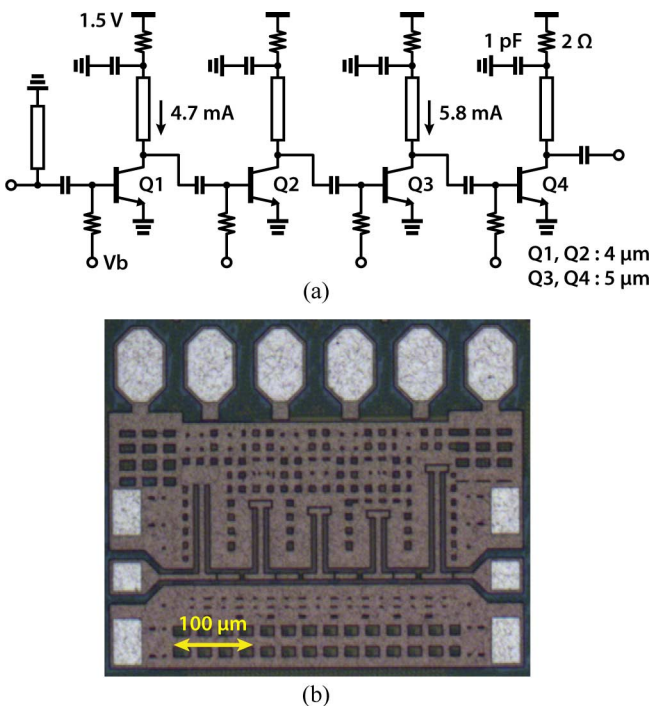


Fig. 6. (a) Schematic of the 4-stage common source amplifier (row amplifier). (b) Layout of the row amplifier breakout.

used as matching capacitors. Small resistors (2 Ω) are placed between the power supply and AC ground in order to prevent low frequency oscillation. On-chip bypass networks composed of 3 Ω polysilicon resistors and stacked MIM capacitors are placed around the amplifier in order to prevent coupling through the supply line. Also, the input matching is achieved using a high-pass LC network in order to achieve a wide bandwidth. The simulated gain is 12.5 dB at 110 GHz with a 3-dB bandwidth of 94–121 GHz. The simulated 1-dB output compression point ($OP_{1\,\mathrm{dB}}$) and saturated output power (P_{sat}) are -1.5 dBm and 2.5 dBm, respectively, at 110 GHz. The current consumption is 21 mA ($P_{DC} = 31.5$ mW).

The single-ended rat-race coupler is implemented using 70 Ω $\lambda/4$- and $3\lambda/4$-long microstrip transmission lines [49]. The meandered microstrip line occupies a smaller area compared to a G-CPW line since it eliminates the side ground walls. A 5 μm width signal line in M6 and ground plane in M4 results in 70 Ω line. The rat-race coupler occupies 510×180 μm^2 area with simulated insertion loss of 4.0 ± 0.2 dB (including the 3 dB power division) at 96–125 GHz and < 0.5 dB difference between the two output ports. The Wilkinson coupler is also designed using the 70 Ω $\lambda/4$ microstrip lines, and is employed as a matched power divider in the signal distribution network [49]. It has simulated insertion loss of 3.8 dB (including the 3 dB power division) and an isolation of > 18 dB between the two output ports at 110 GHz. Its physical size is 330×90 μm^2.

The 1-to-4 distribution network is based on G-CPW transmission line and two-stage Wilkinson power dividers. The G-CPW meanders between the phased array unit elements so as to provide an equiphase feed to the 4 unit cells. Its simulated insertion loss is 12.7 dB at 110 GHz (including the 6 dB power division), and all unit elements are fed within $\pm 5°$ phase difference.

D. Phased Array Unit Element

The 90° phase shifter is connected to the 1:4 distribution network and has single-ended input and output ports (Fig. 7(a)). An RC-CR network is used to generate the $-90°$ phase difference, and the bottom ground plane underneath the RC-CR network is removed in order to reduce the shunt parasitic capacitance to ground. Each of the two outputs from the RC-CR network is followed by a CS buffer (Q1, Q2), which provides gain and isolation from the active-switching stage (Q3–Q6). The switching stage selects one of two signals depending on the phase state. For a phase state of 0° phase shift, Q5 (and Q4) is on and $+45°$ signal is selected to the output. For the $-90°$ phase state, Q6 (and Q3) is on and $-45°$ signal is selected to the output port. The unselected signal in each case is bypassed by Q3 (or Q4) to AC ground (V_{CC}), and prevents leakage of the unselected signal to the output. This improves the gain and phase response of the 90° phase shifter.

Fig. 8 presents a comparison of the gain difference and phase error for the 90° phase shifter as different configurations are used. The gain and phase error are substantially better with the use of bypass switches. The buffer stage has no effect on the gain and phase error when the bypass stages are used, but it provides an additional $\sim$ 3 dB gain at 110 GHz. After full EM simulation (Fig. 7(b)), the 90° phase shifter has a simulated phase error of $10 \pm 3°$ from 90–118 GHz, an insertion gain of -4.7 dB with < 1 dB gain difference from 102–120 GHz, and an $OP_{1\,\mathrm{dB}}$

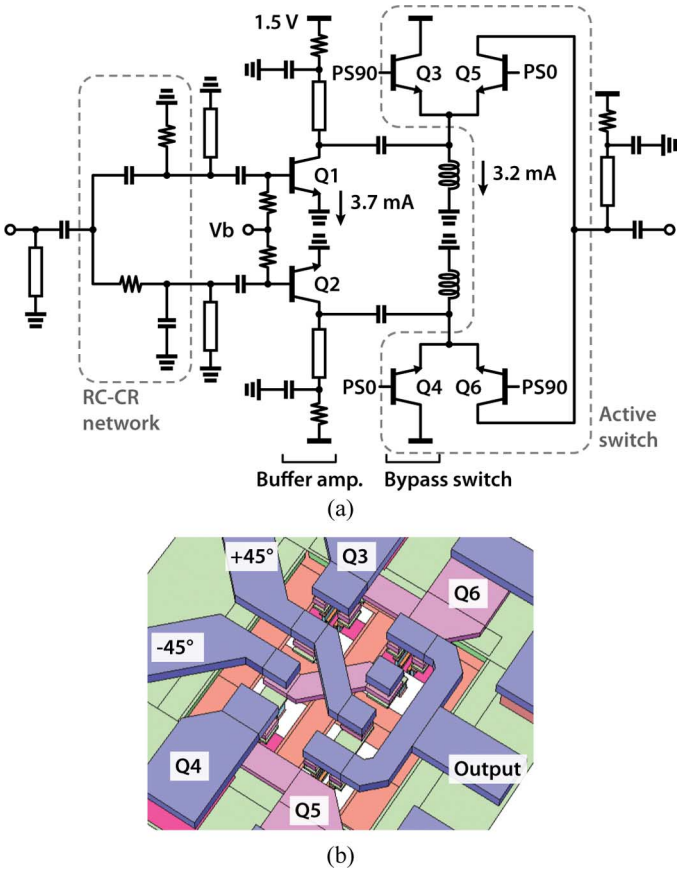


Fig. 7. (a) Schematic of the 90° active phase shifter and (b) EM modeling of the active switch layout.

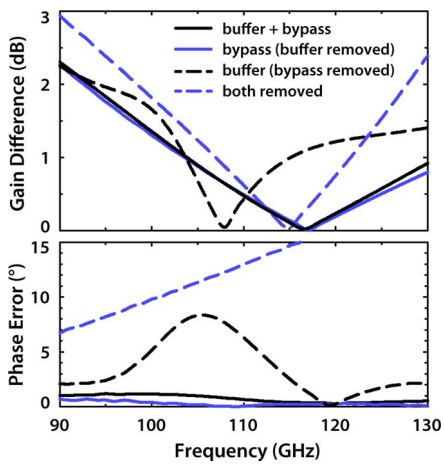


Fig. 8. Simulated gain difference and phase error for different configurations of 90° active phase shifter.

of -5.5 dBm. The current consumption is 13.8 mA (P_{DC} = 20.7 mW).

A passive balun is inserted between the 90° phase shifter and the 180° phase shifter (Fig. 9(a)). The primary inductor is done in M6 and the secondary inductor in M5, and they are stacked for vertical magnetic coupling. A custom metal-oxide-metal (in M4–M6) capacitors are used at the input and the output for impedance matching. The simulated insertion loss is 1.6 dB, and the return loss is < -10 dB at 90–140 GHz. The gain and phase imbalance is < 0.9 dB and $< 4°$, respectively, at 90–120 GHz.

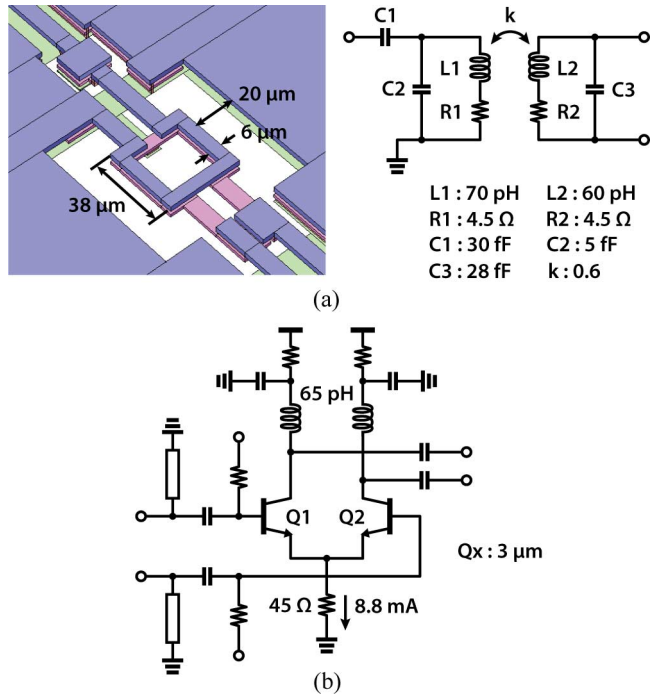


Fig. 9. (a) EM-modeling of the passive balun and its simple circuit model. (b) Schematic of the differential buffer amplifier following the balun.

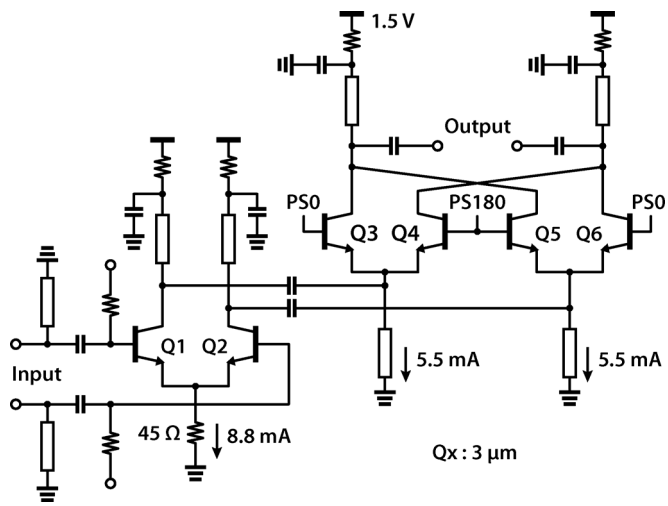


Fig. 10. Schematic of the 180° active phase shifter.

A differential buffer amplifier is then placed after the passive balun to improve the gain and phase balance. A 45 Ω resistor is used as common-mode source degeneration and resulting in common-mode gain of -5 dB at 110 GHz. The differential buffer amplifier has a simulated gain of 2.4 dB at 110 GHz with an $OP_{1\,\mathrm{dB}}$ of -2.8 dBm. The gain and phase imbalance after the buffer amplifier is < 0.25 dB and $< 5°$ at 90–120 GHz.

Fig. 10 shows the differential 180° phase shifter based on a separated Gilbert-cell approach. This approach allows a low supply voltage of 1.5 V which is common for all circuit blocks. The first stage (Q1–Q2) uses resistive degeneration in order to further improve the common-mode rejection. The active switching stage (Q3–Q6) crosses the signal at the output, resulting in the 180° phase shift. All interconnections in the circuit are modeled with EM simulations and are accounted in the top level circuit simulation. The 180° phase shifter has a

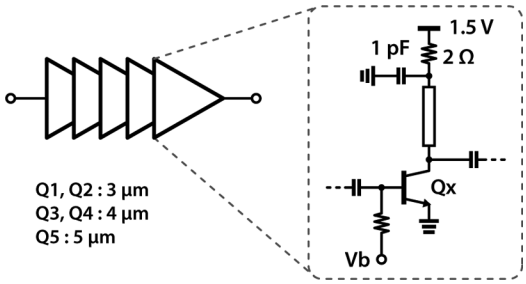


Fig. 11. Schematic of the 5-stage common source amplifier which drives the on-chip antenna (2 units are used for a differential feed).

simulated gain of 2.5 dB with 3-dB bandwidth of 96–135 GHz. The gain and phase error between the two states are < 0.7 dB and $< 5^\circ$ up to 120 GHz, respectively. It consumes 20 mA from 1.5 V and occupies an area of $310 \times 380\ \mu\text{m}^2$.

In order to drive the differential on-chip antenna feed, the output amplifier is designed as a pseudo-differential amplifier. Fig. 11 shows the schematic diagram of its single-ended half circuit which is a 5-stage common-source amplifier. The design approach is similar to the row amplifier, and the simulated gain is 15 dB with a -3 dB bandwidth of 100–123 GHz. The half-circuit $OP_{1\text{ dB}}$ and P_{sat} are $-2\ \text{dBm}$ and $+2\ \text{dBm}$, respectively, while consuming 22 mA from a 1.5 V supply. The layout is staggered in order to adapt to the wide spacing of the differential antenna feed, and the differential amplifier occupies an area of $760 \times 380\ \mu\text{m}^2$. Its differential output impedance is $94 + j3\ \Omega$ which matches well with the antenna input impedance.

E. High-Efficiency Differential Dipole Antenna

A dipole antenna with a differential feed is chosen for the following reasons: 1) it occupies less area than a microstrip antenna, and 2) differential signaling allows for a simple implementation of the 180° phase shifter. The smaller area of the differential dipole antenna as compared to a microstrip antenna is critical for this work since it determines the available area for the active circuits in a unit cell ($0.5\lambda_0 \times 0.5\lambda_0$). The electromagnetically (EM)-coupled dipole antenna is patterned using 7000 Å of sputtered gold on an additional quartz wafer on top of the silicon chip (Fig. 12). This novel antenna with a quartz superstrate allows for high efficiency designs at 60–200 GHz and has been presented before for single-ended and differential structures [31], [33], [50]–[52]. The dipole feed is placed on the top metal layer (M6), and the ground plane is implemented with combined M3 and M4 layers. The EM-coupling eliminates the use of a direct metal-via feed (and its associated parasitic inductance) from the silicon chip to the radiating structure, and lowers the cost of the entire package.

The thickness of the quartz layer ($\epsilon_r = 3.8$) is 100 μm, which is found to be optimal at 110 GHz based on HFSS simulations (see [50] and [52] for details on the quartz thickness optimization of such antennas). The M3 and M4 layers also act as a ground plane for the radiating dipole antenna (107.4 μm away), and cover all the area dedicated to the antenna structure in a complementary fashion in order to observe the required density rules for fabrication. This on-chip ground plane isolates the radiated signal from the lossy (8 Ω-cm) silicon substrate, thus

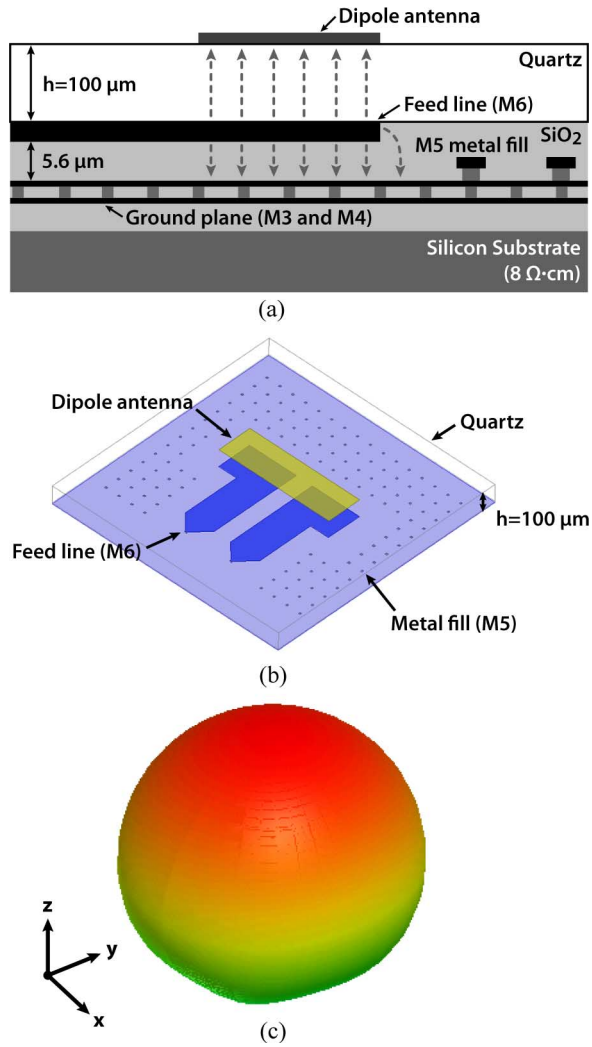


Fig. 12. Structure of EM-coupled dipole antenna (680 μm× 200 μm): (a) cross section view and (b) 3-D view. An exclusion area of $880 \times 740\ \mu\text{m}^2$ is placed around the antenna. (c) The simulated 3-D pattern of the dipole antenna on a finite ground plane.

resulting in a unidirectional pattern above the silicon and improved antenna efficiency.

In the 4×4 array, the entire M3/M4 on-chip metalization acts as a ground plane for the antenna array, but the results of the single dipole sets a guideline for the dedicated exclusion area around the antenna structure. Also, the metal-fill structures under the feedline degrade the antenna performance, and therefore the M5 metal-fill is placed 50 μm from the M6 feedline. Also, transistors and RF signal lines are not used underneath the antenna in order to avoid any potential coupling. Using HFSS, the antenna area is determined to be $880 \times 740\ \mu\text{m}^2$ ($0.32\lambda_0 \times 0.27\lambda_0$), which is $\sim 35\%$ of the unit element area. The dipole antenna dimensions are $680 \times 200\ \mu\text{m}^2$, which is the size of the feed line on M6 (Figs. 12(b) and 13).

The simulated differential dipole antenna impedance at the apex feed is $1 - j2.5\ \Omega$ due to the proximity of the M3/M4 ground plane to M6 feed (5.6 μm). Therefore, an impedance transformer consisting of a 180 μm wide and 330 μm long microstrip line ($Z_{odd} = 4.6\ \Omega$, $\theta_{line} = 103^\circ$ at 110 GHz) is connected to each side of the dipole, and transforms the dipole impedance to a differential $81 - j11\ \Omega$ at the amplifier output

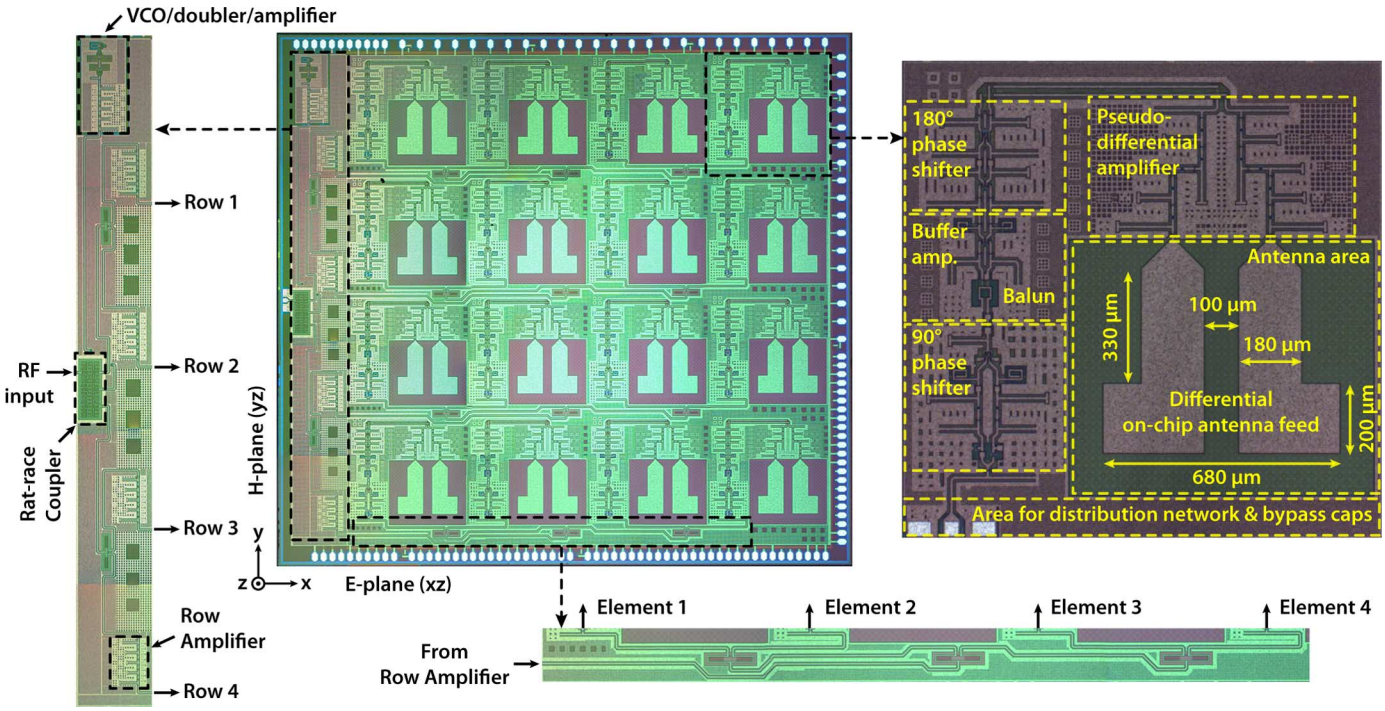


Fig. 13. Photograph of the 4 × 4 phased array transmitter (6.5 × 6.0 mm^2) and its distribution network. A unit element (1.365 × 1.365 mm^2) is also shown.

port. The efficiency is $45 \pm 2\%$ with a directivity of 6.0 dBi and gain of 2.7 dBi at 110 GHz. The differential S_{11} is < -10 dB at 106–114 GHz (referenced to 100 Ω), with a -3 dB gain bandwidth of 108–114 GHz (Fig. 14). The half-power beamwidth is 86°. This antenna results in high efficiency and wide bandwidth when compared to antennas built on a standard RFIC backends (typical efficiency of 5–10%) [53]–[55].

The EM-coupled dipole antennas on the quartz superstrate are aligned and attached to the silicon RFIC using a small dot of epoxy at the edge of the 4 × 4 array chip. Due to the fringing fields, the structure results in additional 0.3 dB additional gain loss (efficiency of 42%) for a $+/-20$ μm misalignment in the X or Y directions. Also, the structure is insensitive to air gaps and an air-gap of 2 μm results in a frequency shift of $\sim$ 2.0 GHz. Therefore, EM-coupled antennas are suitable for large wafer-scale phased arrays and are tolerant to misalignment errors.

F. Digital Control and Chip Integration

Each unit-element has a 2-bit register which stores the phase state. The register is composed of level-triggered D-flip-flops, and the enable clock for the register is controlled by 4-to-16 address decoder. Thus, 7-bit digital interface (4-bit address, 2-bit phase, and 1-bit for control enable) is required to control the entire phased array. The control logic is designed with 0.18-μm CMOS technology, and the delay of a D-flip-flop is $\sim$ 3 ns. The digital control signal is distributed using M1 and M2 metal layers, and the longest distribution line is about 10 mm which has estimated *RC* delay of 145 ps. Thus, the delay of the control signal is dominated by the logic gates, and based on the number of logic stages it can support up to 50 MHz of control signals.

A high density MIM capacitor in series with a 3 Ω resistor results in a low-Q DC bypass network and is used in all available area on the chip for improved stability. The total DC decoupling capacitance is $\sim$ 95 pF in a unit element and $\sim$ 1.6 nF for the entire chip. Current-mirror biasing is used for most of the circuit blocks, and they are tied in groups and connected to the bias control pin. The M3 and M5 layers are used for V_{CC} as much as possible in order to minimize the DC voltage drop in V_{CC} (IR drop).

Fig. 13 presents a detailed microphotograph of the fabricated 4 × 4 array. Layout arrangement of the circuit components is chosen to achieve efficient use of area with the equi-phase distribution network. An RF GSG pad is located at the west side for the external input, and DC pads including V_{CC} and GND are distributed as evenly as possible at the other three sides. The DC pad pitch is either 100 μm or 200 μm, and pads are allocated to be compatible with available DC probes. A dual-diode ESD protection cells are used for all DC pads, and foundry-provided power clamp circuit is also used between V_{CC} and GND. The fabricated 4 × 4 array occupies 6.5 × 6.0 mm^2 area, and simulated power consumption is 1425 mA from 1.5 V supply.

G. 4 × 4 Phased-Array Design

The 4 × 4 array is fabricated with $0.5\lambda_0$ spacing at 110 GHz (1365 μm) in both E-plane and H-plane directions (Figs. 13 and 24). The entire antenna array and feedlines are simulated using HFSS (without the front-end electronics), and show a directivity of 17.0 dBi and antenna gain of 13.5 dBi at 110 GHz and 0° scan angle, respectively, demonstrating an antenna efficiency of 45% (Fig. 14). The simulated mutual coupling between the antenna elements is < -20 dB in the E- and H-plane planes even for the nearest elements (Fig. 15(a)) due to the ground plane (M3/M4) proximity. The effect of the mutual coupling on the input impedance of all 16 elements is negligible as seen in Fig. 15(b).

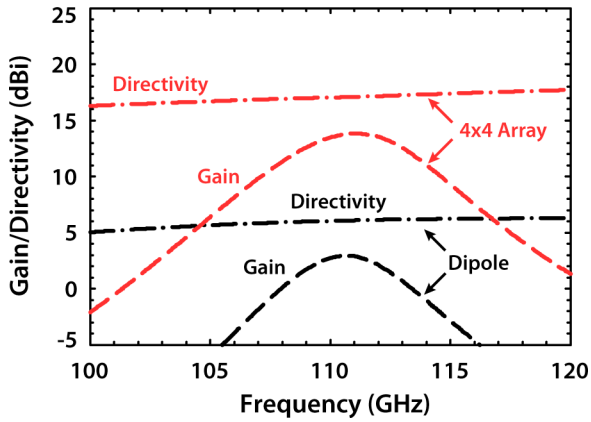


Fig. 14. Simulated directivity and gain of a single antenna and the 4×4 array antenna.

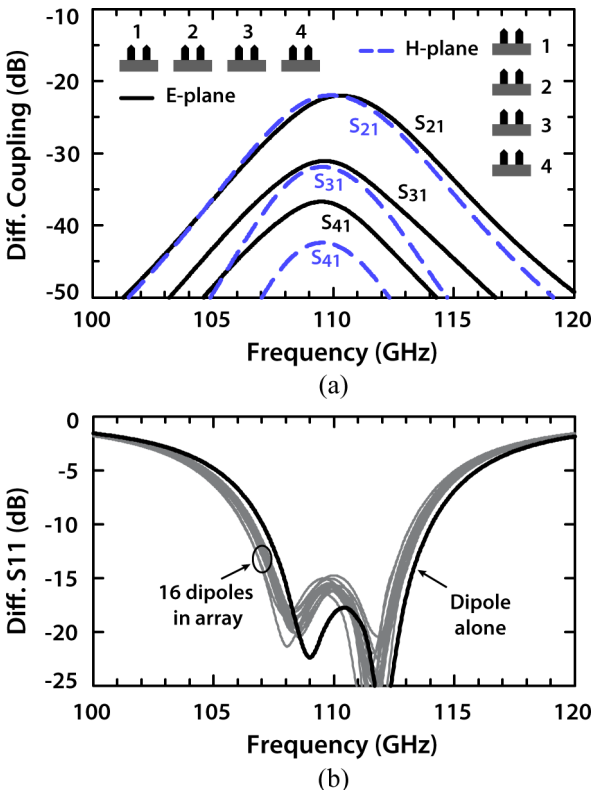


Fig. 15. (a) Simulated mutual coupling in E-plane direction and H-plane direction in the 4×4 antenna array. (b) Input return loss of each element in the array and an isolated dipole antenna.

Phased arrays can suffer from grating lobes or scan blindness if placed on a relatively high-ϵ_r substrate such as quartz dielectric ($\epsilon_r = 4.0$). Based on a method proposed in [56], the scan blindness angle θ_{sb} can be calculated using:

$$\theta_{sb} = \arcsin\left(\left|\frac{\beta_{sw}}{k_0} - \frac{1}{\frac{dx}{\lambda_0}}\right|\right) \quad (1)$$

where β_{sw} is the surface-wave propagation constant for the TM_0 mode in the grounded quartz substrate ($h = 107.4\ \mu$m), $k_0 = 2\pi/\lambda_0$ is the free-space wavenumber, and dx is element spacing in the x-direction. It is seen that the 4×4 array can

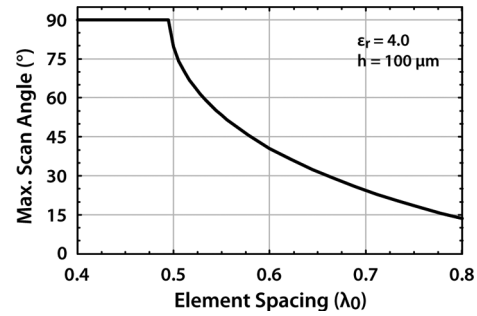


Fig. 16. Maximum scan angle of a phased array in a dielectric substrate with $\epsilon_r = 4.0$ and the thickness of 100 μm.

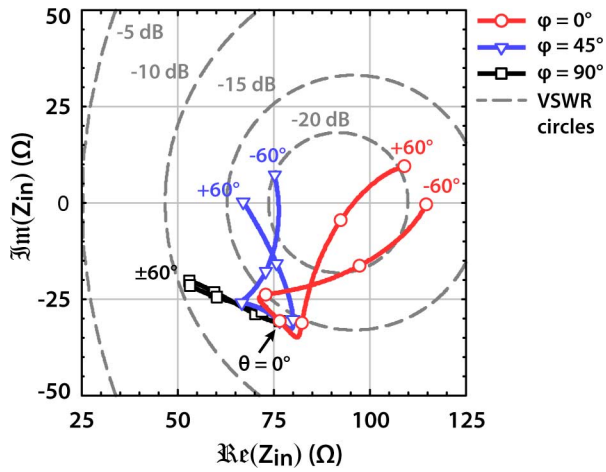


Fig. 17. Simulated active input impedance of an inner element ($m = n = 2$) for three different principal axes: $\phi = 0°$ (E-plane), $\phi = 45°$, and $\phi = 90°$ (H-plane). Scan angle (θ) varies from $-60°$ to $+60°$, and markers are placed every $20°$.

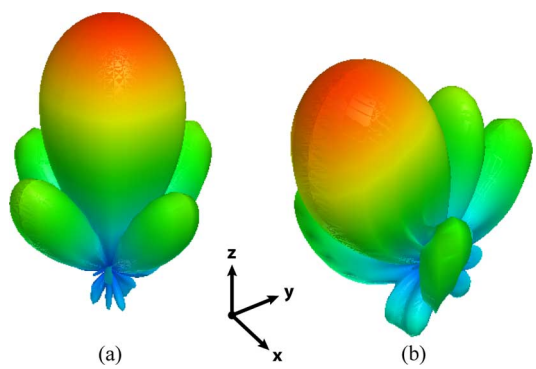


Fig. 18. Simulated 3-D patterns of the 4×4 antenna array for different H-plane beam-steering positions: (a) $\theta = 0°$ with $(0°, 0°, 0°, 0°)$, (b) $\theta = 30°$ $(0°, -90°, -180°, -270°)$.

scan to $\pm 80°$ before triggering a dominant substrate mode in the quartz dielectric. Fig. 16 presents the maximum achievable scan angles for $\epsilon_r = 4$ and different spacing. The scan angle reduces to $\pm 54°$ for $dx = 0.55\lambda_0$.

Another important aspect of phased arrays is the input impedance of an antenna element versus scan angle (typically called active impedance or driving point impedance) [16]. For a 4×4 array in an (m, n) grid with $m = 1 - 4$ and $n = 1 - 4$, the input impedance of an antenna at $(m = 1, n = 1)$ and a

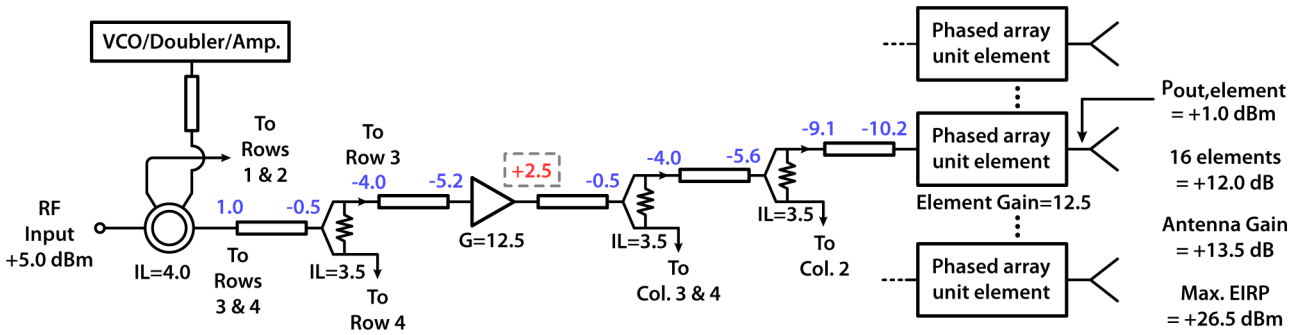


Fig. 19. Maximum EIRP estimation based on the simulation results. Power level at each point in dBm is denoted with blue number. Maximum EIRP is limited by the row amplifiers ($P_{sat} = 2.5$ dBm shown in dash). Antenna driver amplifier is also in weak compression.

scan angle of (θ, ϕ) can be obtained using the Z-parameter matrix as:

$$Z_{in,11} = \frac{V_{11}}{I_{11}} = Z_{11} + Z_{21,11}\frac{I_{21}}{I_{11}} + Z_{31,11}\frac{I_{31}}{I_{11}} + \cdots$$
$$I_{mn} = |I_{mn}|e^{-jk_0(mdx\sin\theta\cos\phi + ndy\sin\theta\sin\phi)}$$

where $Z_{in,11}$ is the active impedance of the driven element, Z_{11} is the self-impedance of the driven element, $Z_{mn,11}$ are the mutual impedance between the driven element and one of the other elements, and I_{mn} is an excitation current at the (m, n) position. In this work, $dx = dy = 0.5\lambda_0$, and $|I_{mn}/I_{11}| = 1$ for a uniformly driven array. Since $Z_{mn,pq}$ varies with antenna spacing, and the excitation current phase varies with scan angle, the active impedance is different for every scan angle. Fig. 17 presents the calculated antenna impedance for element $(2, 2)$ in the 4×4 array as the array is scanned from $-60°$ to $+60°$ in the E-, H-, and 45° planes. The active impedance does not vary much versus scan angle because the mutual coupling components, $Z_{mn,pq}$, are quite low. The active impedance reflection coefficient is < -15 dB (referenced to 90 Ω) over all scan angles.

Fig. 18 presents the simulated 3-D pattern of the array under two different scan conditions showing beam-forming and beam-steering capability of the wafer-scale phased array. The first sidelobe level is < -13 dB in the H-plane and < -12 dB in the E-plane, and the far sidelobes are < -25 dB at 0° scanning. Some backside radation is present due to the finite size of the ground plane in the simulation setup.

H. Electronic System Gain, EIRP, and Array Gain

The 4×4 phased array functional blocks are shown in Fig. 19 together with the small-signal gain (or insertion loss) of each block. The simulated system electronic gain, G_s, is defined as the available power at a *single* dipole feed divided by the input power and is 2.3 dB at 110 GHz. This definition of G_s is compatible with a 2-port probe measurement when port 2 is located at the antenna feed. The array gain, G_{array} is defined as the effective isotropic radiated power (EIRP $= P_T G_T$) divided by the input power in the small-signal regime, and is:

$$G_{array} = \frac{\text{EIRP}}{P_{\text{in}}} = G_s + 10\log N + G_T \text{ (dB)} \qquad (2)$$

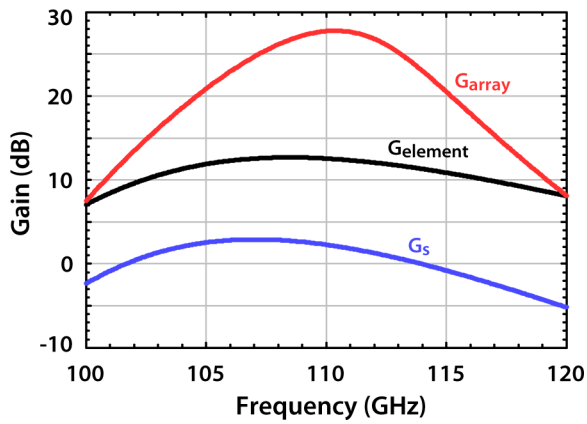


Fig. 20. Simulated gain of the 4×4 phased array: G_s, $G_{element}$, and G_{array}.

where N is the number of elements ($N = 16$) and G_T is the 4×4 antenna array gain ($G_T = 13.5$ dB at $\theta = 0°$). Fig. 20 presents the system gain (G_s), the array gain (G_{array}), and the unit element gain ($G_{element}$, see Fig. 4(d) to the dipole feed). G_s has almost same frequency response as $G_{element}$ due to the wideband distribution network, but G_{array} has a narrower frequency response due to the dipole antenna bandwidth. The simulated G_{array} is 27.7 dB at 110 GHz with a 3-dB bandwidth of 107–113 GHz.

The absolute EIRP of the 4×4 array can also be calculated using a similar formula:

$$\text{EIRP} = P_{avs} + 10\log N + G_T \text{ (dBm)} \qquad (3)$$

where P_{avs} is the available output power from the unit-element differential amplifier. For an input power of $+5$ dBm, $P_{avs} = +1$ dBm per channel, and the simulated EIRP is 26.5 dBm at 110 GHz. This is equivalent to a transmitted power of 13.0 dBm (at the dipole feeds) and a radiated power of 9.5 dBm (in the air).

The EIRP is limited by saturation in the row amplifiers, which results in $+1$ dBm power at the input of the dipole antenna (and not $+4.5$ dBm, which is the simulated P_{sat} of the differential antenna amplifiers). Therefore, an EIRP of ~ 30 dBm at 110 GHz can be expected with a design iteration with improved row amplifiers.

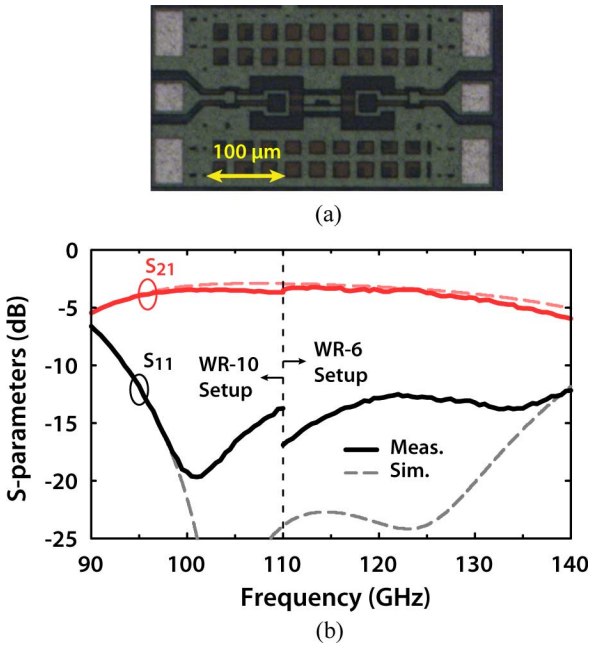


Fig. 21. (a) Photograph of back-to-back passive baluns and (b) measured S-parameters.

III. Measurements

A. Circuits

The W-band circuit breakouts were tested using two different S-parameter measurement setups: one is at 75–110 GHz (WR-10 waveguide band) and the other is at 110–170 GHz (WR-8 waveguide band). The measurement at both frequency bands are taken with an SOLT calibration with a CS-5 calibration substrate [57]. Fig. 21 presents the measured S-parameters of back-to-back passive baluns. The back-to-back passive baluns show good agreement with the simulation and have wide input and output matching bandwidth (S_{22} is not shown due to symmetry), and a measured insertion gain of -3.6 dB.

Fig. 22(a) presents the measured S-parameters of the row amplifier breakout. The row amplifier has a frequency upshift, but still maintains 13.5 dB gain at 110 GHz with -3 dB bandwidth of 100–133 GHz. The large signal behavior is also characterized at 110 GHz (Fig. (b)), and its input and output 1-dB compression points are -12.5 dBm and -0.5 dBm, respectively. It has a saturated power (P_{sat}) of 1.5 dBm with -1.5 dBm input. It consumes 28.5 mA from 1.5 V supply.

The measured gain response over frequency of the 90° phase shifter for two different phase states are shown in Fig. 23. The insertion gain is -5.2 to -4.5 dB, with a gain difference of < 0.5 dB and a phase error of $\sim 5°$ at 110 GHz. It consumes 18 mA from 1.5 V supply. Although a frequency upshift is also observed, measured gain and phase at 110 GHz agree well with the simulation.

The breakouts of VCO and frequency doubler are also measured. The VCO output frequency is 58.4–59.9 GHz with 0–1.5 V control voltage, with an output power of -3 dBm. The measured conversion loss of the frequency doubler is $\sim$ 8 dB at 110 GHz, and $>$ 13 at 120 GHz. The frequency upshift of the VCO turned out to be sub-optimal for the 4×4 array, and the array measurements are therefore obtained using an external signal.

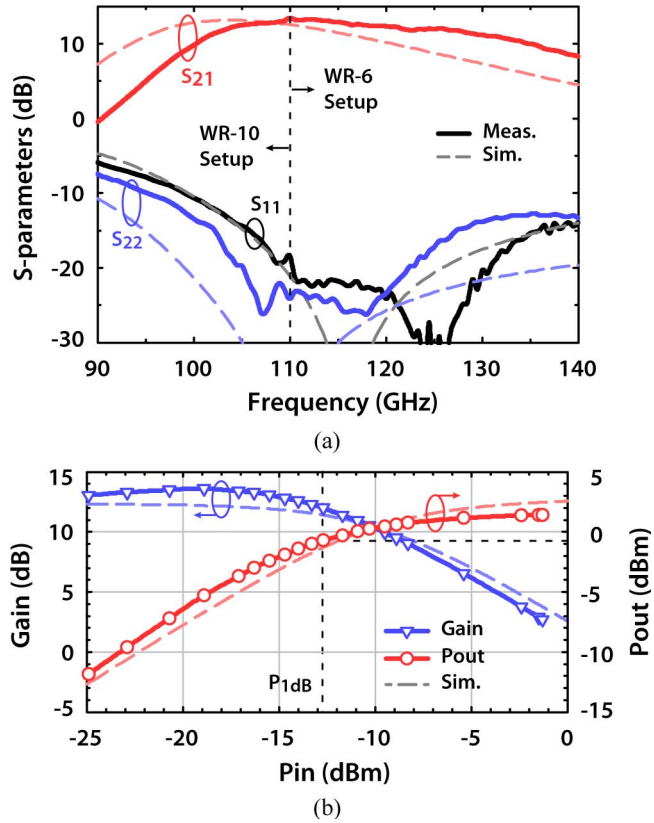


Fig. 22. Measured and simulated S-parameters of the row amplifier test cell.

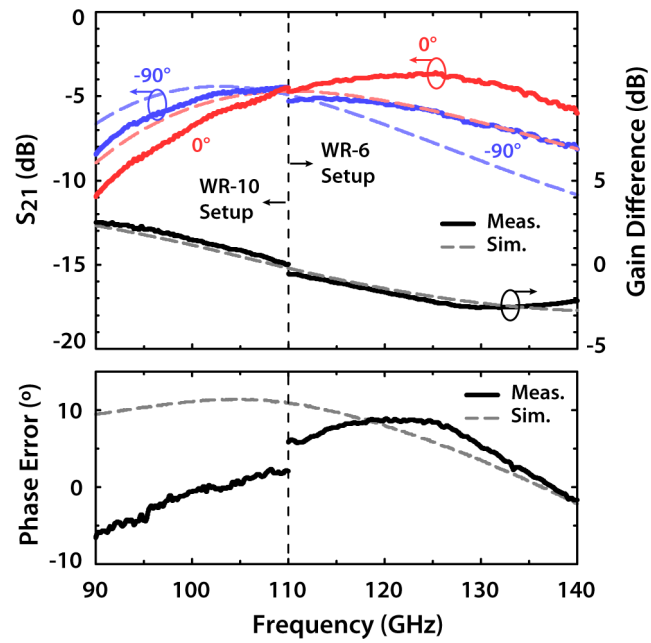


Fig. 23. Measured and simulated of the 90° phase shifter test cell: (a) S_{21} for both phase states and the associated gain difference and (b) phase error from ideal 90° phase shift.

B. Phased Array

The 4×4 dipole array is fabricated on a 100 μm-thick quartz wafer and is placed on top of the 4×4 phased array IC using small dots of glue at the corners. (Fig.) The wafer-scale phased

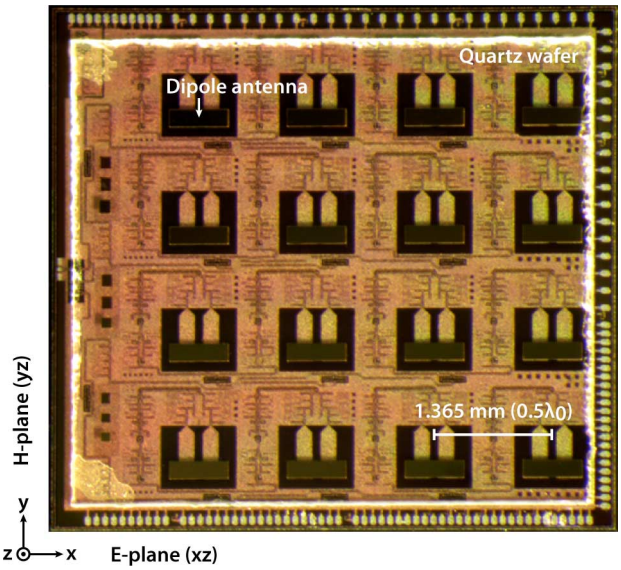


Fig. 24. Chip photograph of the wafer-scale 4 × 4 phased array. (6.5 × 6.0 mm^2).

array is then placed on a probe station metal chuck and is fed with an external RF signal source using a W-band waveguide GSG probe. The output of the wafer-scale phased array is a plane wave and is received by a rectangular horn antenna which is placed at a far-field distance of $R = 25$ cm ($R_{far-field} > 2D^2/\lambda_0 = 22$ cm when $D =$ antenna aperture size). RF absorbers are placed around the chip and probe station in order to reduce unwanted reflection and standing waves. The phased array chip is biased with a 31-pin 200 μm-pitch DC probe on the south side and an 11-pin 100 μm-pitch DC probe on the north side. In order to overcome uneven distribution of the DC supply and IR drop across over the chip, the V_{CC} is increased for the pattern and EIRP measurements. The measured power consumption of the 4 × 4 array is 1.78 A from 1.9 V supply.

Fig. 25 presents the measurement setup. The external RF input is composed of a signal generator, a frequency tripler, and a W-band amplifier so as to maximize available power from the source. The RF GSG probe loss (1.5 dB) is taken into account and the input power is referenced to the probe tip. The receiving antenna and power detector are placed on a rotational positioner which scans 0–±60° in the E- and H-planes. The input signal is AM modulated at 1 kHz square-wave with 50% duty cycle, and the power detector detects the envelope of the modulated received signal. The received voltage from the Schottky diode power detector is fed to the SR830 lock-in amplifier [58] and its relative strength is recorded in a desktop computer.

Fig. 26 presents the measured patterns in both E- and H-plane at 110 GHz with 0° scan angle. The 3-dB beamwidths of E- and H-plane patterns are 28° and 27°, respectively. The measured pattern and directivity agree well with simulations, and the phased array shows a symmetrical pattern, as designed. The cross polarization for each plane is < -20 dB and is not shown.

The change of row or column phase settings from (0°, 0°, 0°, 0°) to (0°, −90°, −180°, −270°) or (−270°, −180°, −90°, 0°) results in ±30° scan angles in the E- and H-plane, respectively (Fig. 27). The measured patterns show clear main beams and deep nulls between sidelobes, and beam-steering capability is

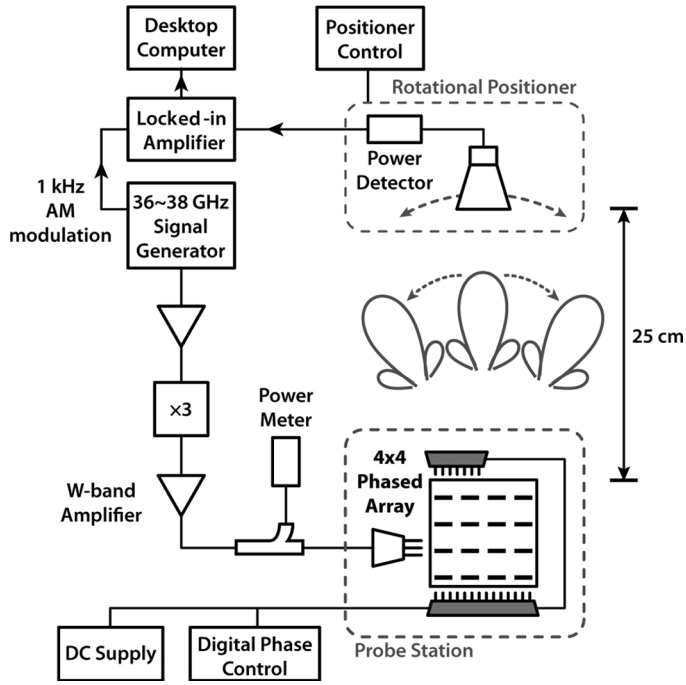


Fig. 25. Measurement setup of the 4 × 4 arrays for radiation pattern and EIRP. The power detector is replaced by an absolute power meter for EIRP measurements.

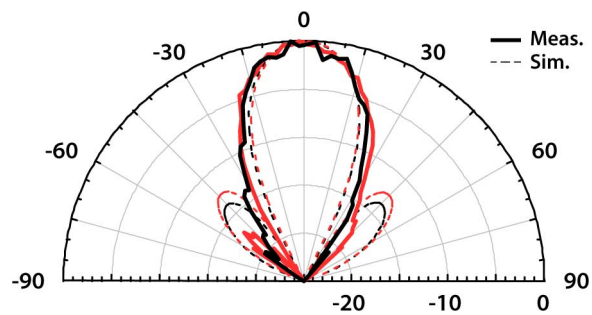


Fig. 26. Measured and simulated E-plane (black) and H-plane (red) patterns of the 4 × 4 array.

demonstrated in both E- and H-planes. The observed distortion in the E-plane patterns is introduced by scattering with the RF GSG probe, and slight a tilt in main beams are also believed to be due to scattering and measurement system misalignment. The patterns are normalized to the maximum level of 0° scan angle, and a gain drop of 2–2.5 dB is seen at ±30° scan angle (0.65 dB due to $\cos(\theta)$, 1.4 dB due to element pattern). No scanning was done in the diagonal plane ($\phi = 45°$) due to the limitation of the available setup.

The phased array can also be scanned to intermediate angles by setting the row or column phases to (0°, −90°, −90°, −180°; $\theta \simeq 20°$) or (0°, 0°, −90°, −90°; $\theta \simeq 10°$). Fig. 28 presents resulting 5 patterns with different scan angles in the H-plane at 110 GHz.

The EIRP is obtained by first measuring the absolute received power from the 4 × 4 array, and then using the Friis communication link equation:

$$P_R = \left(\frac{\lambda_0}{4\pi R}\right)^2 (P_T G_T G_R) \tag{4}$$

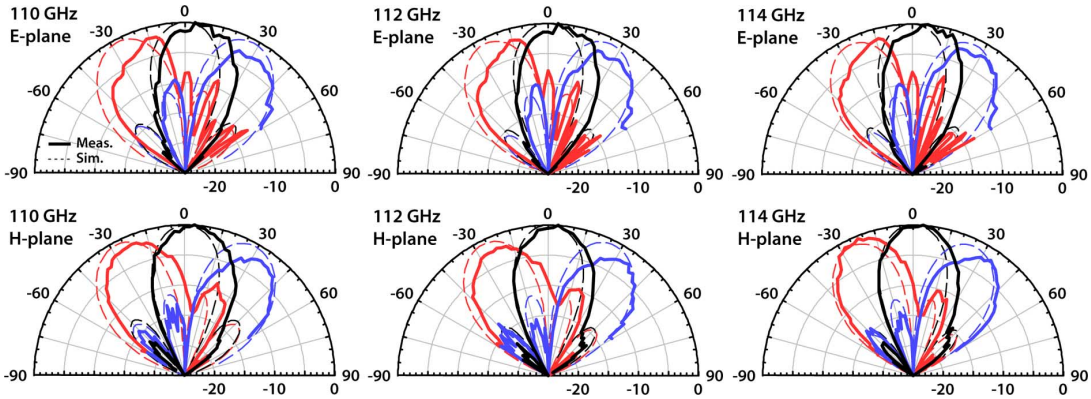


Fig. 27. Measured (bold) and simulated (dashed) phased array patterns with ±30° beam steering in both E-/H-planes at 110, 112, and 114 GHz. E-plane pattern is distorted due to metal structrue of RF GSG probe.

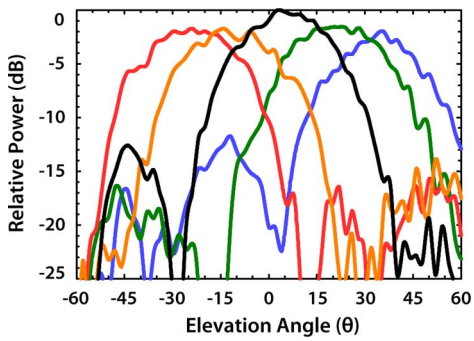


Fig. 28. Measured radiation patterns with intermediate beam steering for H-plane scanning at 110 GHz.

and

$$\text{EIRP} = P_T G_T = \frac{P_R}{G_R}\left(\frac{4\pi R}{\lambda_0}\right)^2. \tag{5}$$

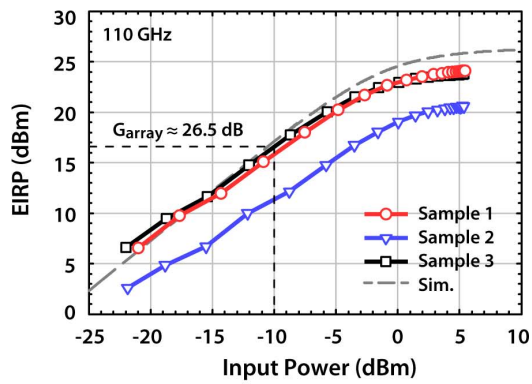
Therefore, due care is taken to independently measure the gain of the receiving horn antenna ($G_R = 21 \pm 0.5$ dB at 110 GHz) and calibrated Agilent power sensors (W8486A) are used to measure both input and output power.

Fig. 29(a) presents the measured EIRP versus input power for three different samples at 0° scan angle. The maximum EIRP is 24.0–24.5 dBm at 110–112 GHz for an input power of 5 dBm. The array gain ($G_{array} = \text{EIRP}/P_{\text{in}}$) can also be obtained in the small signal regime, which is 26.5 ± 0.5 dB. The maximum EIRP is also measured over frequency at 106–118 GHz (Fig. 29(b)), and it shows the repeatability of the measurement. The EIRP at different scan angles can be obtained from the measured patterns, and is 2–2.5 dB lower than the 0° values.

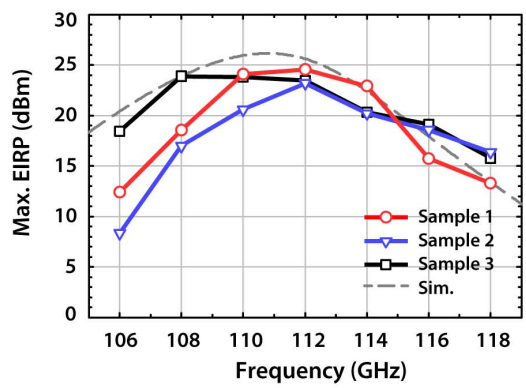
The EIRP can also be expressed as:

$$\text{EIRP} = P_T G_T = \epsilon P_T D_T = P_{rad} D_T \tag{6}$$

where ϵ is the antenna efficiency and D_T is antenna dirctivity ($G_T = \epsilon D_T$). The EIRP can therefore be referenced to the radiated power (P_{rad}), with $D_T \simeq 17$ dB. P_T and P_{rad} are calculated from the measured EIRP and are 10.5–11 dBm and 7.0–7.5 dBm, respectively, at 110–112 GHz.



(a)



(b)

Fig. 29. Measured (a) EIRP at 110 GHz for 3 different samples and (b) maximum EIRP at different frequencies.

TABLE I
PERFORMANCE SUMMARY

Metric	Meas.	Sim.
Array Gain (G_{array})	26.5±0.5 dB	27.7 dB
Max. EIRP	24±0.5 dBm	26.5 dBm
Scan Angle	±30° in both E-/H- direction	
3-dB Beamwidth	28±2°	25±1°
Power Consumption	1.78 A @ 1.9 V	1.43 A @ 1.5 V

The salient features of the wafer-scale phased array chip are summarized in Table I.

IV. Conclusion

This paper presented a 16-element wafer-scale phased array with high efficiency on-chip antennas and $\pm 30^\circ$ scanning capabilities in the E- and H-planes. The wafer-scale array eliminates lossy transitions to external antennas, and can be scaled to 32–64 elements on a single chip with additional row amplifiers. Measurements done on several chips at 108–114 GHz agree well with simulations showing the possibility of this technology for high gain systems. The wafer-scale approach is particularly useful at frequencies above 60 GHz where the chip size is the same as the antenna aperture and high antenna gain can be achieved with 5×5 to 10×10 mm^2 chips, and has the potential to drastically reduce the cost of mm-wave phased arrays. Future work include integrating a complete transceiver instead of the VCO, improving the row amplifiers and increasing the transmit power per element for a higher EIRP. Also, the design can be scaled to 94 GHz for aircraft landing systems, 120 GHz for sensors and communication systems, or 140 GHz for future automotive radars.

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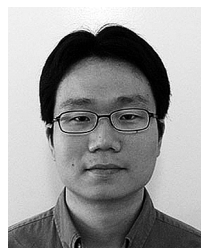

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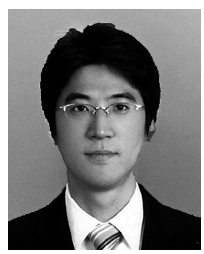

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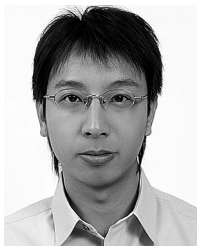

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