Ka-Band BiCMOS 4-Bit Phase Shifter with Integrated LNA for Phased Array T/R Modules

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***Abstract*— This paper presents a 30−38 GHz 4-bit phase shifter with an integrated LNA using a 0.12 μm SiGe BiCMOS process. The two-stage LNA is implemented using SiGe HBT, and the phase shifter is based on MOSFET switches and miniature low-pass networks. The LNA/phase shifter achieves 1±1.5 dB of gain and 5 dB noise figure at 34 GHz. The RMS phase error is less than 7° at 30−38 GHz. The total chip size is 900×400 μm^2 (0.36 mm^2) excluding pads, and the chip consumes only 3 mA from a 1.8 V bias supply (5.4 mW). To our best knowledge, this is the first implementation of a Ka-band silicon-based phase shifter.**

***Index Terms*— phase shifter, LNA, CMOS switch, SiGe, Ka-band, T/R module, phased array**

I. Introduction

Phased array systems have been used for defense and commercial applications to achieve electronic beam control and fast beam scanning and require a phase shifter per antenna element. At Ka-band frequencies, the phase shifters have been implemented using GaAs technologies, resulting in relatively high cost and low integration density [1]–[5]. However, with recent developments in silicon technologies, Ka-band phase shifters can be now implemented using silicon RFICs resulting in excellent performance over a wide frequency range.

A 4-bit digital phase shifter with a 22.5° minimum phase step is the most specified design in phased array systems. The reason is that a 4-bit design results in low sidelode levels as long as the amplitude variation is below ±2 dB. The phase shift can be achieved by a delay line, loaded line, delayed reflection and low-pass/high-pass networks [6]. In our phase shifter design, low-pass networks are used to reduce the chip size and insertion loss and MOSFETs are used for switching between bypass and low-pass networks at Ka-band. A low noise amplifier (LNA) using SiGe HBTs is implemented in front of the phase shifter to compensate for the loss of phase shifter and reduce the system noise figure (NF).

II. Design

The LNA and phase shifter are designed in the IBM 8HP 0.12 μm SiGe BiCMOS process. The LNA and each bit of phase shifter are designed with the input and output impedance of 50 Ω and cascaded together using short 50 Ω transmission lines. Because only the top two metal layers out of 7 metal layers are not affected by the metal density rules of IBM 8HP process, the transmission line is designed using the three top metal layers and results in a microstip line with side ground shields (Fig. 1). The side ground shields allow a compact layout with virtually no coupling between nearby inductors or transmission lines. The bottom microstrip ground plane shields the signal line from the lossy silicon substrate. The transmission line of Fig. 1 was measured with TRL calibration and results in a impedance of 48.5 Ω, a loss of 3.8 dB/cm, and an effective permittivity of 3.9 at 34 GHz.

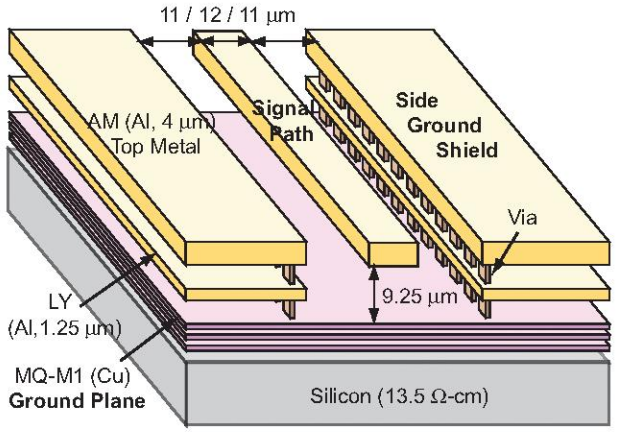

Fig. 1. Shielded 50 Ω microstrip line structure using 7 metal-layer profile of the IBM 8HP process.

A. Low Noise Amplifier

The LNA is designed using SiGe HBT amplifier as shown in Fig. 2. The first stage is an inductively degenerated cascode amplifier. The input impedance is matched with $L1$ and $L2$ for a minimum noise figure and maximum power transfer, by sizing the HBT and changing the bias current [7]. The HBT has a emitter size of 0.12×8 μm^2

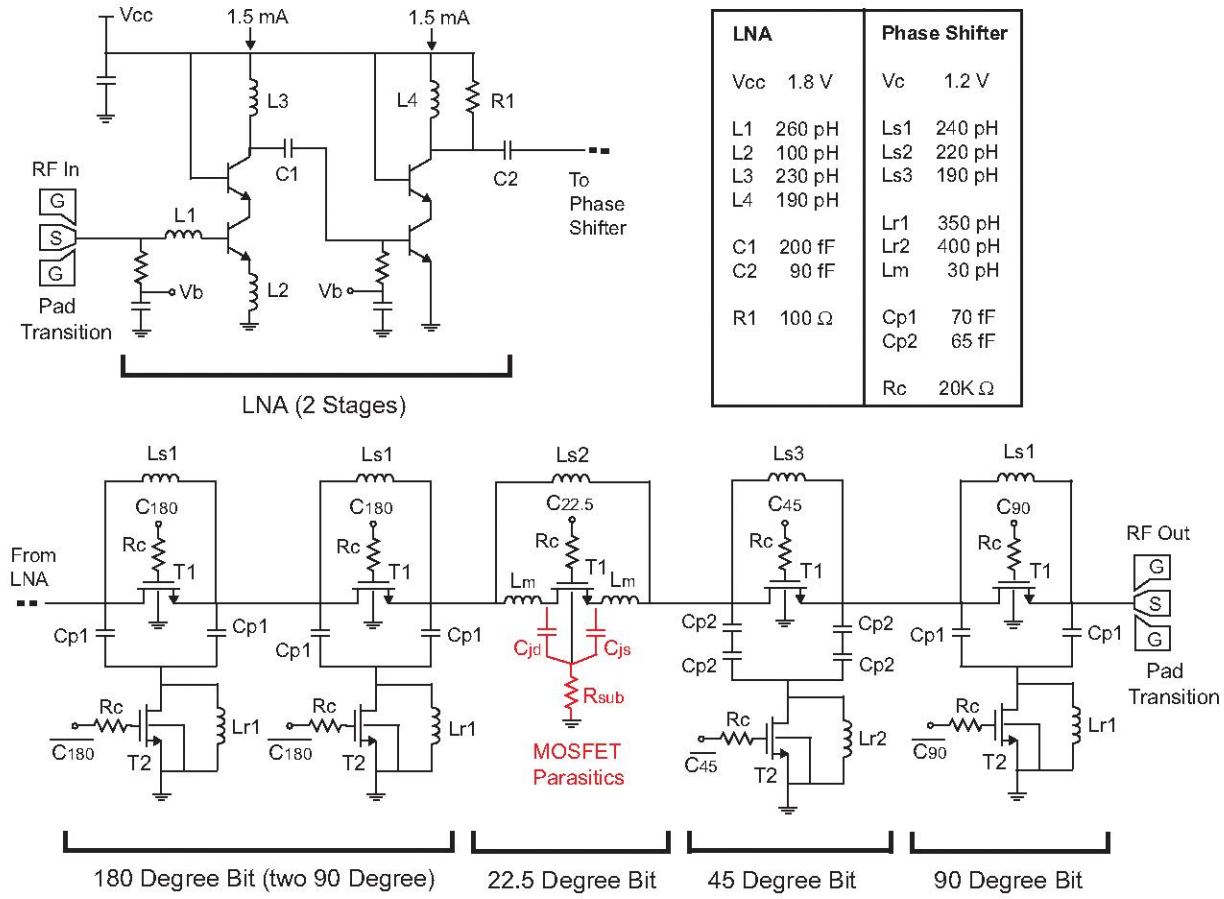

Fig. 2. Schematic of LNA/phase shifter: LNA bias circuitry is not shown.

and is biased at 1.5 mA, resulting in f_T of 120 GHz. $L3$ and $C1$ are for inter-stage matching between the first and second stages. The second stage is also a cascode amplifier with a load resistor, $R1$ (100 Ω), which allows wide band output matching together with $L4$ and $C2$. Output matching of the LNA is important because the phase shifter requires a well matched input impedance for wide band operation. The bias current is 1.5 mA with a supply voltage of 1.8 V for each stage (3 mA total current), resulting in a power consumption of 5.4 mW. The measured LNA gain is 15 dB with a corresponding NF of 4.5 dB at 34 GHz. The measured output 1 dB power compression point (P1dB) is -2 dBm.

B. Phase Shifter

The 4-bit phase shifter consists of 5 stages of phase shifting elements (Fig. 2). The first two 90° phase shifters are tied together to become the 180° bit, and the 22.5°, 45° and 90° bits are placed in series afterwards. Each bit is designed using a low-pass network which consists of a series inductor ($Ls1$) and two shunt capacitors ($Cp1$, $Cp2$). Low-pass Π-networks are used because they require a single inductor. Arranging the MOSFET switches as shown in Fig. 2 permits the switching between a phase delay state and a bypass state. When $T1$ is open and $T2$ is closed, Ls and Cp form a low-pass Π-network. With $T1$ open and $T2$ closed, Lr resonates with the parasitic capacitance of $T2$, and Ls and Cp have a minimal impact on the insertion phase. The values of Ls, Lr and Cp are optimized using full electromagnetic simulations for the desired phase shift and take into account the parasitics of $T1$ and $T2$. The 45° phase shifter is designed with two shunt capacitors ($Cp2$) in series due to the minimum available MIM capacitor value. For the 22.5° phase shifter, the parasitic junction capacitances (Cjd, Cjs) are used as the shunt capacitor of the low-pass network.

A large MOSFET device results in a small series resistance, but the shunt capacitances of source and drain junctions limit the frequency bandwidth. Therefore, the MOSFET sizes are optimized for the lowest loss over the Ka-band range, and $T1$ and $T2$ have a width of 23 μm and 34 μm, respectively. Also, the uncertainty of the substrate resistance ($Rsub$) between the source/drain junctions and the RF ground (substrate contacts) is a design issue. The

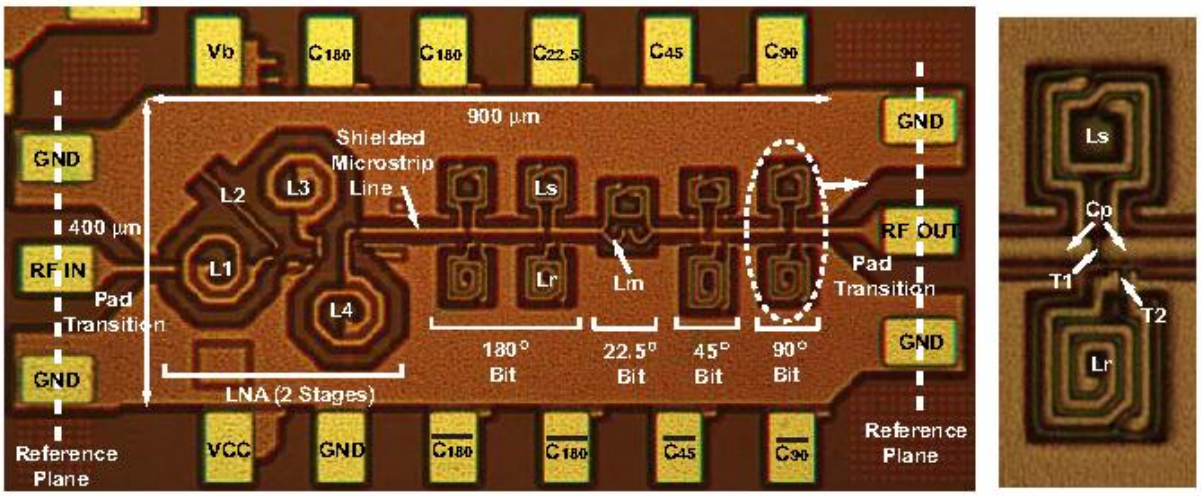

Fig. 3. Ka-band LNA/phase shifter chip photograph.

MOSFET device model roughly estimates this resistance value at 50 Ω, but the actual resistance highly depends on the number and distance of substrate contacts as well as the MOSFET size. Therefore, large substrate contacts ($35\times50\ \mu m^2$) are placed closely all around each MOSFET switch to achieve the modeled 50 Ω value and minimize signal coupling through the substrate.

The source and drain junctions limit the power handling of MOSFET switches since the junctions are forward biased when the peak voltage of signal is high in negative. Therefore, the resulting input P1dB of phase shifter is around 10 dBm. The MOSFET devices also have an oxide breakdown voltage, but the voltage between the gate and source/drain does not exceed the breakdown voltage because the gate voltage is bootstrapped by the source and drain voltage due to a large resistor ($Rc = 10\ K\Omega$). Rc also prevents the RF signal from leaking through the gate bias line. The simulated insertion loss for every phase shifting element is 2.0–2.5 dB and the insertion loss of the phase shifter is about 13 dB at 30–38 GHz.

A picture of the complete LNA/phase shifter is shown in Fig. 3. A tapered transition from G-S-G pads to the microstrip line are designed to provide a 50 Ω input and output impedance. Inductors are surrounded closely by ground planes to reduce their size and coupling, and the parasitics are taken into account. The quality factor of inductors at 34 GHz is 12–15 for 200–400 pH. The chip measures $900\times400\ \mu m^2$ (0.36 mm^2) excluding RF and bias pads.

III. Measurements

The LNA/phase shifter was measured on-chip with Agilent E8364B network analyzer using SOLT calibration

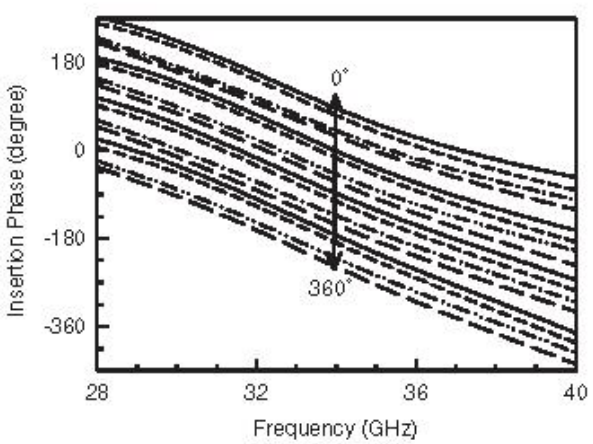

Fig. 4. Measured insertion phase of 16 different phase states.

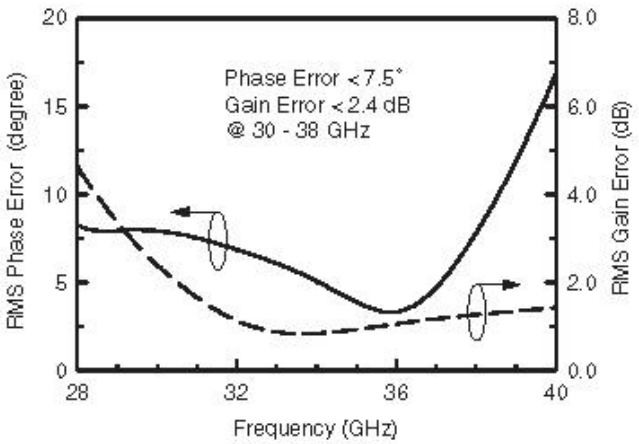

Fig. 5. RMS phase and gain error of LNA/phase shifter.

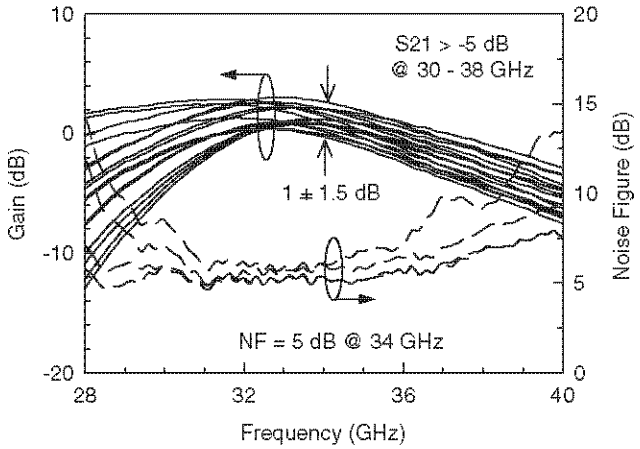

Fig. 6. Measured gain of 16 different phase states and noise figure of 4 different phase states.

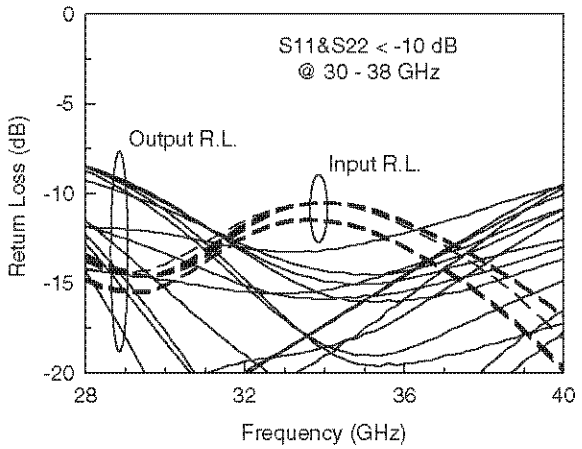

Fig. 7. Measured input and output return loss of 16 different phase states.

to the probe tips. Fig. 4 presents the measured absolute phase performance of the LNA/phase shifter. The RMS phase error is shown in Fig. 5. The phase error is less than 7.5° at 30–38 GHz which is much less than the 5th significant bit (11.25°).

The measured gain of all 16 different phase states and the RMS gain error are shown in Fig. 6 and Fig. 5, respectively. The combined input and output losses for pad transitions, measured to be 0.35–0.45 dB from 28 to 40 GHz, are not taken out of the measurements. The LNA/phase shifter results in 1±1.5 dB of gain at 34 GHz. The noise figure was measured at 4 different phase states (0°, 180°, 270°, 337.5°) and results in an average of 5 dB at 34 GHz. The input and output return loss is less than −10 dB over 30–38 GHz and shown in Fig. 7. The simulations agree very well with the measurements and are not included due to space limitations. The P1dB of the LNA/phase shifter is limited by the LNA stage since the measured P1dB of each phase shifter bit is higher than 10 dBm. The measured input P1dB of LNA/phase shifter chip is −16 dBm.

IV. Conclusion

A Ka-band 4-bit phase shifter with an integrated LNA are presented. The LNA/phase shifter achieves 1±1.5 dB of gain and 5 dB noise figure at 34 GHz. The RMS phase error and gain error are less than 7.5° and 2.4 dB at 30–38 GHz. This results are better in terms of bandwidth, phase accuracy and gain variation than most GaAs phase shifters in the Ka-band frequency range [1]–[5]. The only difference is the silicon chip NF, which as is well known, cannot compete with GaAs or InP devices at 30–40 GHz. Therefore, in systems requiring a NF of 1–2 dB, the silicon chip should be preceded by a III-V LNA. This paper shows, for the first time, that one can build Ka-band T/R modules using silicon RFICs providing accurate phase shifts over a wide-frequency range, and with very low power consumption (5.4 mW).

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