A 22–24 GHz 4-Element CMOS Phased Array With On-Chip Coupling Characterization

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***Abstract*—This paper presents a 22–24 GHz CMOS 4-element phased array based on the *All-RF* architecture with very low power consumption and chip area. The measured array performance, done at the system level at 22–24 GHz, shows an input and output match of <-13 dB, 9–12 dB gain, 7.5–8.0 dB NF, an IIP3 of -9.5 to -12.5 dBm, and a 4-bit phase control with an *rms* gain and phase error of <1.2 dB and $<6^\circ$, respectively (<0.5 dB and $<3^\circ$ at 23.5–24.5 GHz). The chip consumes 76.5 mA from a 1.5 V supply and is 3 mm^2 in area. Extensive coupling measurements show that the dominant on-chip coupling components result in system-level gain and phase errors which are proportional to the LNA gain. To our knowledge, this is the first analysis of on-chip coupling effects on phased array performance, and the first demonstration of an *All-RF* mm-wave CMOS phased array with full amplitude and phase control on each element. The application areas are in high data-rate communications and automotive radars.**

***Index Terms*—Active phase generator, CMOS integrated circuits, MIMO systems, phased arrays, phase shifters, radar, RF phase shifting, wireless communications.**

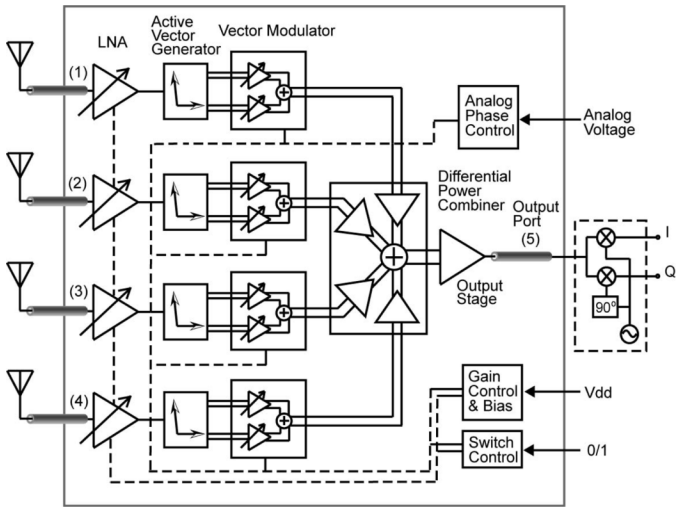

Fig. 1. Block diagram architecture of the 4-element All-RF phased array chip.

I. Introduction

RFIC-BASED phased arrays have been an active topic of research in the past five years, and several implementations have been proven in silicon technologies for microwave and millimeter-wave applications [1]–[6]. In terms of architecture, the *All-RF* architecture employs phase shifters and amplitude controllers in the RF path and requires an RF combiner, which can be challenging at millimeter-wave frequencies (Fig. 1). The mixer-based architectures, with either LO or IF phase shifting, require a mixer and LO routing to every element, which can be challenging for large arrays, but the IF combining stage is easy to build. The advantage of the *All-RF* architecture, especially with active phase shifters, is a reduction of chip size compared to the mixer-based architecture since the local oscillator routing and the multitude of mixers consume a lot of area on the silicon chip. Another advantage of the *All-RF* architecture is that one receiver is used after the array pattern is synthesized, which results in an improvement of signal-to-noise (S/N) ratio and high signal-over-interferer-ratio at the receiver.

This paper demonstrates a 24 GHz 4-element phased array in 0.13 μm CMOS based on the *All-RF* architecture, and with independent control of the phase and amplitude of each antenna path. Previously, H. Krishnaswamy, *et al.* have demonstrated a CMOS 24 GHz phased array based on a novel VCO technique, but this work did not provide independent phase and amplitude control for each element which is essential for synthesizing low sidelobe arrays or monopulse-type (difference) beams [7]. The 24 GHz band can be used for automotive radars (22–29 GHz) and industrial, scientific, medical and communication applications (ISM band, 24–24.25 GHz).

The work also presents the first comprehensive study of on-chip coupling between the different array elements, and how this coupling can introduce unwanted phase and amplitude errors at the output of the phased array chip. As is well known, these errors can significantly deteriorate the scanned antenna pattern and should be avoided at all costs. The coupling study is made possible due to the individual control of the amplifier and phase shifter in each phased array element on the CMOS chip. Also, the effect of the load terminations on the different ports of the phased array is investigated. The final array settings are then selected so as to result in state-of-the-art phased array performance even with the presence of on-chip coupling effects.

II. Phased Array Building Blocks

Fig. 1 presents the 24 GHz 4-element phased array based on the *All-RF* architecture. This is a beamformer chip and the receiver chip (mixer/LO/IF-amplifiers) is connected to the output port (port 5). The phased array has four single-ended RF inputs and one single-ended RF output, and uses internal differential-line phase shifting and combining. The single-ended input makes it easier to connect to the off-chip antennas using microstrip lines on a Teflon substrate. The single-ended output is

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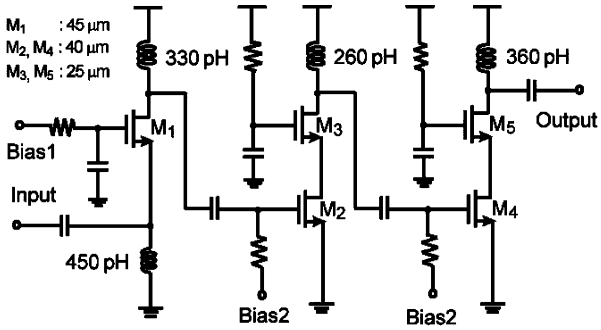

Fig. 2. Three-stage LNA with a common-gate input.

used for RF probe testing, and a differential output is the preferred implementation for differential receivers. The low-noise amplifier (LNA) is a single-ended three-stage amplifier with an analog controllable voltage gain of 8–28 dB. This is followed by an RF phase shifter which is composed of an active vector generator and a differential vector modulator. The active vector generator also acts as a single-ended-to-differential converter. The four different phase shifted signals are then summed together in an active differential power combiner, and the final output stage is a differential-to-single-ended converter and drives a 50 Ω load. Each array element (amplifier-phase shifter) can be turned on or off using external controls and this will be used for on-chip coupling studies.

A. Common-Gate Low-Noise Amplifier

The common-gate (CG) topology was adopted for the LNA input stage (Fig. 2) mainly in consideration for chip area and input match bandwidth. The CG topology uses one inductor at the source for the input match but a common-source (CS) LNA requires a source degeneration inductor at the source and a matching inductor at the gate, and therefore occupies less chip area than the CS LNA [8]–[10]. The CG topology can also achieve a wideband input match at mm-wave frequencies if $1/\mathrm{gm}$ of the CG transistor is chosen to be 50 Ω. The design of the CG LNA is done using a 450 pH inductor with a $Q = 17$ at 24 GHz at the M_1 source and a 330 pH $(Q = 18)$ at the load. M_1 is sized to have a gm of 20 mA/V for a bias current of 2 mA. The LNA input stage is then followed by two cascode stages for a total bias current of 8.5 mA and achieves a maximum voltage gain of 28 dB (V_o/V_i) and a resonant output impedance of 500 Ω at 24 GHz. The output impedance is quite high because the 360 pH load inductor $(Q = 18)$ resonates the total node capacitance at the M_5 drain. The simulated noise figure (NF) of the three-stage LNA is 5.6–6.0 dB at 22–24 GHz for the maximum gain setting and is about 1 dB higher than the best 24 GHz common-source LNA [10], [11]. For the NF simulations, the output impedance is taken to be a 50 Ω load (at the M_5 drain). The LNA voltage gain can be changed from 0–28 dB by controlling the bias voltages on $\mathrm{M}_1/\mathrm{M}_2/\mathrm{M}_4$ at the expense of slightly increased NF (Fig. 2). The NF increases from 6 dB to 10 dB for a gain control from 28 dB to 13 dB, respectively.

B. Active Vector Generator and Vector Modulator

The input of the active vector generator is divided into path1 and path2 through a T-junction (Fig. 3) [12]. Each path has a single-ended-to-differential stage (A1 and A2) and path2 also

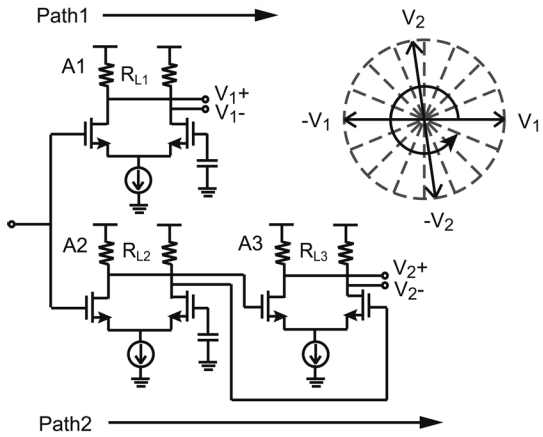

Fig. 3. Active vector generator with resistive loads.

includes a phase-shift amplifier (A3). The transfer functions of path1 and path2, $T_1(s)$ and $T_2(s)$, can be expressed as

$$\begin{aligned} T_1(s) &= \frac{V_1}{V_{\text{in}}} = -\left(G_{m1}R_{L1}\right) \\ &\quad \times \left(\frac{1-\frac{sC_{gd1}}{G_{m1}}}{1+s\left(C_{gd1}+C_{L1}\right)R_{L1}}\right) \\ T_2(s) &= \frac{V_2}{V_{\text{in}}} = \left(G_{m2}R_{L2}\right)\left(G_{m3}R_{L3}\right) \\ &\quad \times \left(\frac{1-\frac{sC_{gd2}}{G_{m2}}}{1+s\left(C_{gd2}+C_{L2}\right)R_{L2}}\right) \\ &\quad \times \left(\frac{1-\frac{sC_{gd3}}{G_{m3}}}{1+s\left(C_{gd3}+C_{L3}\right)R_{L3}}\right) \end{aligned} \tag{1}$$

where G_{m1}, G_{m2}, and G_{m3} are the transconductances, C_{gd1}, C_{gd2}, and C_{gd3} are the gate-drain capacitances, R_{L1}, R_{L2}, and R_{L3} are the load resistances, and C_{L1}, C_{L2}, and C_{L3} are the load capacitances of A1, A2, and A3, respectively. The phase difference $\angle T_2(s) - \angle T_1(s)$ is

$$\begin{aligned} \angle T_2 - \angle T_1 = &-180^\circ - \tan^{-1}\left(\frac{\omega C_{gd1}}{G_{m1}}\right) \\ &+ \tan^{-1}\left(\frac{\omega C_{gd2}}{G_{m2}}\right) \\ &- \tan^{-1}\left(\omega\left(C_{gd1}+C_{L1}\right)R_{L1}\right) \\ &+ \tan^{-1}\left(\omega\left(C_{gd2}+C_{L2}\right)R_{L2}\right) \\ &+ \tan^{-1}\left(\frac{\omega C_{gd3}}{G_{m3}}\right) \\ &+ \tan^{-1}\left(\omega\left(C_{gd3}+C_{L3}\right)R_{L3}\right) \end{aligned} \tag{2}$$

where the model parameters are given as follows: $G_{m1} = G_{m2} = G_{m3} = 11$ mA/V ($I_1 = I_1 = 2$ mA), $C_{gd1} = C_{gd2} = C_{gd3} = 16$ fF ($W/L = 25\ \mu$m/0.12 μm), $R_{L1} = 280\ \Omega$, $R_{L2} = 260\ \Omega$, $R_{L3} = 270\ \Omega$, $C_{L1} = 75$ fF, $C_{L2} = 112$ fF, and $C_{L3} = 75$ fF. $T_1(s)$ and $T_2(s)$ have about 0 dB gain at 24 GHz and show slight gain difference at other frequencies. The calculated phase difference using the

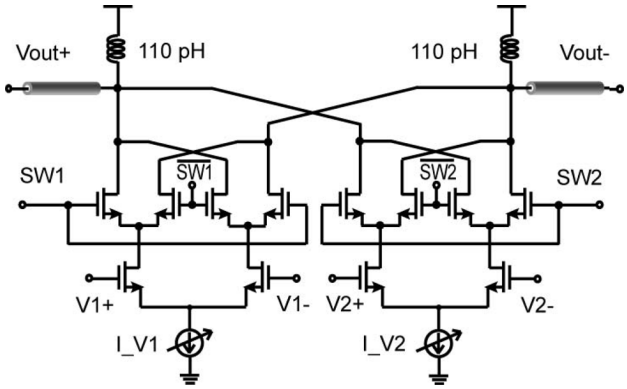

Fig. 4. Active vector modulator. The output nodes are connected to the RF power combiner using a 270 μm GSSG transmission line.

simplified model $\angle T_2 - \angle T_1 = 95^\circ$ at 24 GHz. The transistor sizes and the resistor values of the active vector generator are chosen so that the two paths have equal gain at 24 GHz. However, the frequency response slope of A2–A3 is steeper than that of A1 due to the additional pole in Path 2 and this causes a slight magnitude difference between V_1 and V_2 at different frequencies. Simulations with Spectre RF show that the active vector generator results in a phase and magnitude difference of $103^\circ \pm 2.5^\circ$ and 0 ± 0.5 dB at 21–26 GHz, respectively. An angle of 103° between two vectors V_1 and V_2 is acceptable since one can still synthesize any phase using the vector summing method [2]. The vector generator occupies an area of 50×150 μm^2 with a current consumption of 6 mA and a gain of 0 dB at 24 GHz.

A Gilbert-cell topology is used for the vector modulator (Fig. 4) [13]–[15]. The gain of each path is controlled by adjusting the bias current and the polarity of each vector is controlled using a digital signal on SW1 and SW2. The two vectors are added together at the output port in the current domain to synthesize the required phase shift. Since the bias current for each path is controlled using an external analog voltage, this design can easily result in a 4-bit phase shifter when an external 12-bit A/D controller is used. The vector modulator has two single-ended inductors ($L = 110$ pH, $Q = 23.5$) each built using an 90 Ω CPW transmission line of length 140 μm, and results in a voltage gain of 0 dB at 24 GHz with a current consumption of 4.3 mA.

The active generator/vector modulator together result in a gain of 0 dB and a simulated input $P_{1\mathrm{dB}}$ and IIP3 of 0 dBm and 9.5 dBm, respectively, for a current consumption of 10.3 mA. The phase shifter linearity is better than active mixers, but not as high as passive mixers (with a penalty of 8–10 dB loss at mm-wave frequencies).

C. RF Power Combiner and Output Stage

The 4-channel RF differential power combiner is based on a current-summer cascode amplifier with a differential load inductor. The layout of the differential combiner is challenging knowing that the phased array channels are separated 0.45 mm and 0.6 mm apart in the x and y directions, respectively [Fig. 5(a) and (b)]. The output of the vector modulator for each channel is connected to the cascode amplifier using a GSSG

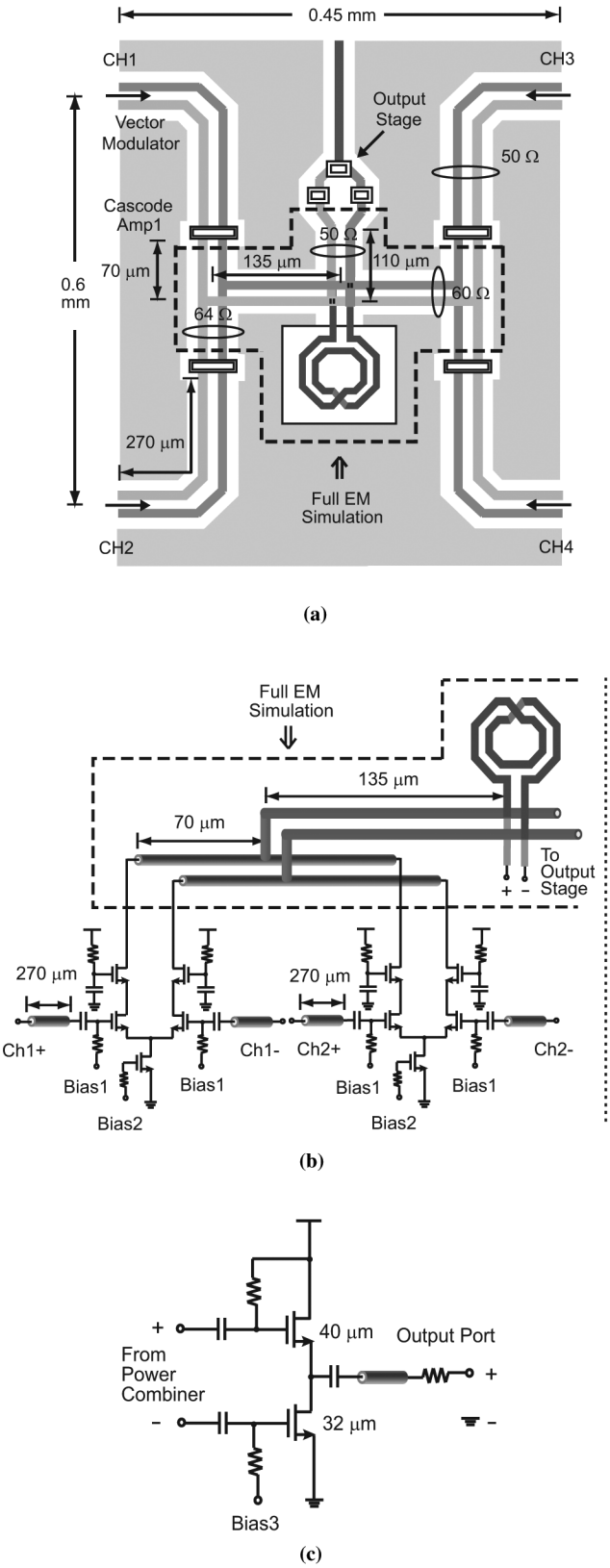

Fig. 5. (a) Layout and (b), (c) circuit model of the 4-channel RF combiner with the output stage. A half-circuit is shown for the 4-channel RF combiner. The x-y spacings are given by layouts of the LNA/active phase shifter.

differential line with an impedance of 50 Ω and a length of 270 μm (15° at 24 GHz). The transmission-line translates the input impedance of the cascode stage to $17.5 - j39$ Ω at the

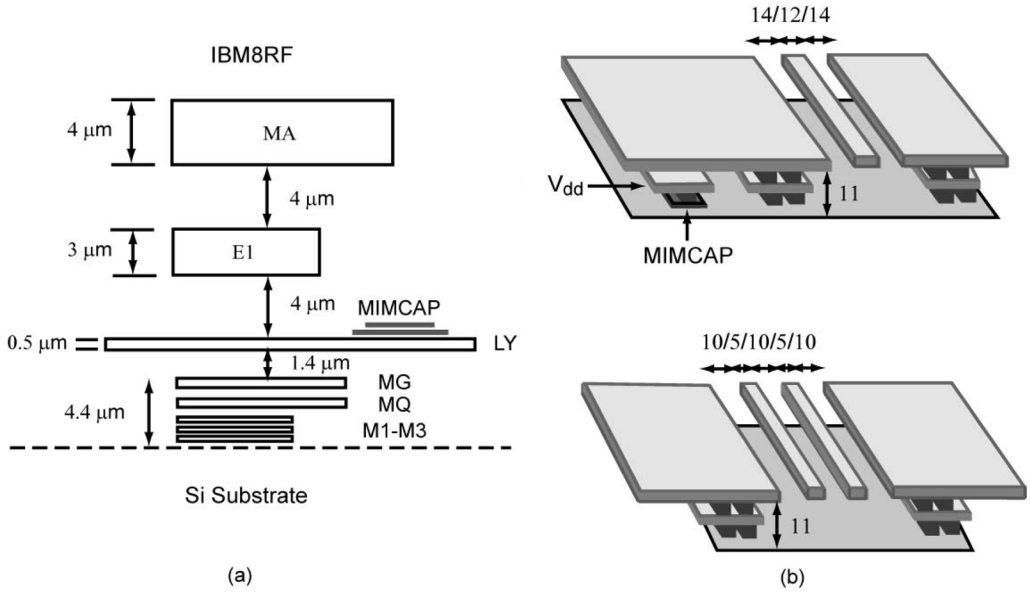

Fig. 6. (a) The IBM 8RF metal stack and (b) the GSG and GSSG transmission line implementation (the unit is μm).

vector modulator output, and is matched using the 110 pH load inductor at the vector modulator. Channels 1 and 2 are first current summed, and then summed again to channels 3 and 4 using a cross-junction which is also connected to the differential load inductor and the output stage. The transmission-line length from the output of the cascode stage to the differential inductor is 205 μm (11° at 24 GHz) with slightly varying impedance (64 Ω, 60 Ω, and 50 Ω). The GSSG impedance of 64 Ω to 50 Ω has minimal effect on the performance, and the dimensions were chosen primarily for layout simplicity. The entire current-summing section, including the transmission-line crossovers, differential inductor and finite ground plane, is simulated using Sonnet with five differential ports, and the resulting S-matrix is connected to the cascode stages and the output stage using Cadence Spectre RF [16]. The differential load inductor was then tuned for maximum gain at 24 GHz, and has a value of 300 pH ($Q = 18.5$ at 24 GHz).

Each branch of the power combiner consumes 2.5 mA and has a voltage gain of 1 dB at 24 GHz. The simulated isolation between Ch1 and Ch2 (or Ch3 and Ch4 is -44 dB at 24 GHz. Also, the isolation is <-50 dB between Ch1 and Ch3). The RF power combiner results in a near-ideal summing performance, and the gain and phase errors between the output nodes of the four vector modulators and the RF power combiner sum port are <0.1 dB and $<2^\circ$ at 20–30 GHz due to the perfect symmetry in the layout. The simulated input $P_{1\mathrm{dB}}$ and IIP3 are -1 dBm and 8.5 dBm, respectively.

The output stage is based on a differential-to-single-ended amplifier in a push-pull design [Fig. 5(c)] with a bias current of 3.5 mA, and its output port is connected to a 0.3 mm long (17° at 24 GHz) 50 Ω GSG transmission line. An additional 16 Ω series resistor is used at the output port, resulting in a wideband match at the expense of 2 dB loss. The simulated output stage gain is 3 dB with an output $P_{1\mathrm{dB}}$ of 1.8 dBm. In fully integrated designs, the output node should remain differential to feed a differential receiver.

D. Transmission Lines, Bias Planes, Decoupling Capacitors

Fig. 6(a) shows a simplified cross-section of the IBM 8RF backend with eight metal layers. This 0.13 μm CMOS process results in an f_t of 85 GHz ($W/L = 40$ μm/0.12 μm, $I = 6$ mA). The GSG and GSSG transmission lines were built in the top metal layer (MA). Metal LY is chosen as the RF bottom ground to shield from the unexpected effects of metal filling below the LY layer. The top ground of the MA layer is connected to the LY layer to form a shielded coplanar waveguide with a height of 11 μm. The 50 Ω GSG and GSSG transmission lines have a simulated attenuation of 4 dB/cm and 3.3 dB/cm, respectively, and a guided wavelength of 6.4 mm at 24 GHz [Fig. 6(b)]. The top thick metal covers more than 50% of the chip area and provides a robust ground to prevent EM coupling between the adjacent stages. Several holes are placed in the MA ground plane to satisfy the metal filling rule and are placed far away from the GSG and GSSG transmission lines.

The analog power supply line (V_{dd}) is built in the second thick metal E1 and is 50 μm wide to reduce the inductance of the long supply lines. A large number of 1 pF MIM-capacitors are used as the decoupling capacitors and placed all along the V_{dd} lines. The digital power supply is built also using metal E1, but not connected on-chip to the analog supply voltage. Again, 1 pF capacitors to ground are used along the digital power supply for RF decoupling. The digital signal routing is built using metal layers M1 and M2 and is shielded by metal LY. A die microphotograph is shown in Fig. 7 with dimensions of 2.11×1.43 mm^2 (3 mm^2) including all pads.

E. Phased Array Channel Simulations

The performance of a single channel was simulated in Cadence Spectre RF using the 0.13 μm CMOS models provided by IBM (BSIM4). The simulated *channel gain* (LNA, phase shifter, RF power combiner, and output stage) is 0–20 dB at 24 GHz depending on the LNA bias current (5–8.5 mA), and the

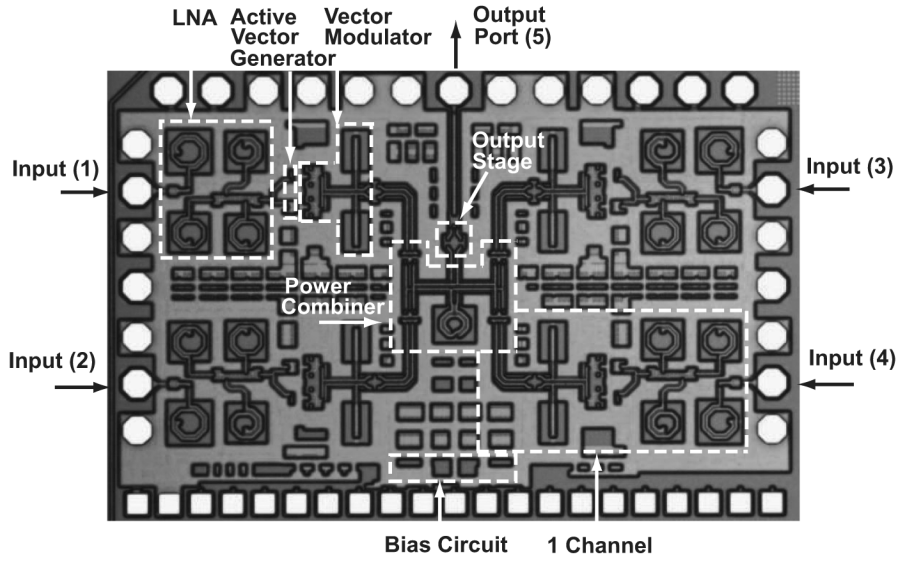

Fig. 7. Microphotograph of the 0.13 μm CMOS 4-element phased array chip (2.11 × 1.43 mm^2).

NF is 7.5–6.0 dB for a channel gain of 10–20 dB. Most of the gain is set by the three-stage LNA since the phase shifter, power combiner, and output stage result together in a gain of 2–3 dB at 22–24 GHz. The simulated input $P_{1\mathrm{dB}}$ and IIP3 are -22 to -32 dBm and -13 to -23 dBm, respectively, for a channel gain of 10–20 dB, and are entirely limited by the LNA.

III. Phased Array Coupling Studies

The coupling between individual channels in a phased array may result in significant gain and phase errors at the output port. The reason is that power coupled from channel 1 to channel 2 will undergo an independent phase shift, ϕ_2, and then add again to channel 1 in the RF combiner. The resulting output vector is $V_o = e^{j\Phi_1} + ce^{j\Phi_2}$, where c is the normalized channel-to-channel coupling value [Fig. 8(a)]. The maximum amplitude error is $1 \pm c$ and occurs when $\phi_2 = \phi_1 \pm n\pi (n = 0, 1, 2 \ldots)$. The maximum phase error is $\sin^{-1}(c)$ and occurs when ϕ_2 results in a 90° triangle as shown in Fig. 8(a). For a 4-bit phased array, the vector can be at 16 different positions on the small circle and the resulting amplitude and phase errors are plotted in Fig. 8(b). It is seen that a coupling of -20 dB $(c = 0.1)$ results in an *rms* amplitude and phase error of 0.5 dB and 3°, respectively.

The coupling paths between two neighboring channels in the CMOS phased array are shown in Fig. 9. The α, β, γ paths represent coupling from channel 1 to the input port of channel 2, while $\delta_1', \delta_2', \delta_1'', \delta_2''$ represent inter-chip coupling paths between channels 1 and 2. The coupling between ports 1 and 3 (or 4) was measured and found to be <-50 dB, and is therefore not included in this analysis. Fig. 10(a) shows the measured isolation, S_{21}, when LNA1/PS1 and LNA2/PS2 are both turned "off" or "on", and PS1 and PS2 are set to the same phase state. In this case, α can be estimated to be -40 to -45 dB at 20–27 GHz due to the single-ended inputs, while β and γ are significantly higher and are linearly dependent on the LNA gain. It is seen

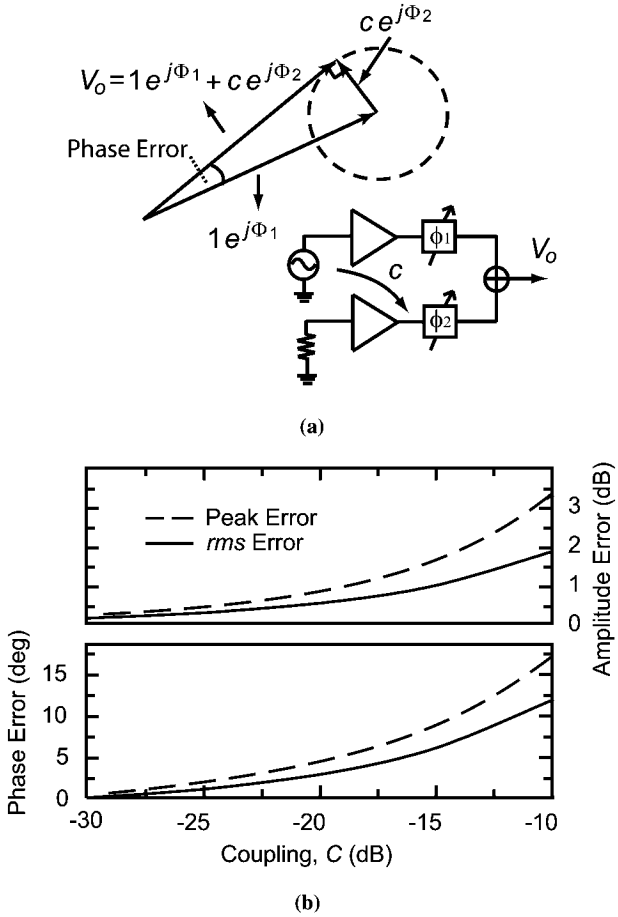

Fig. 8. (a) Vectorial representation of the output voltage and (b) the associated amplitude and phase error with the presence of channel-to-channel coupling.

that the coupling is highest at 20–22 GHz due to the LNA response which peaks at 20–22 GHz with a voltage gain of 28 dB. The voltage gain is much higher than the channel gain due to the large output impedance of the LNA at the drain of M_5 (500 Ω).

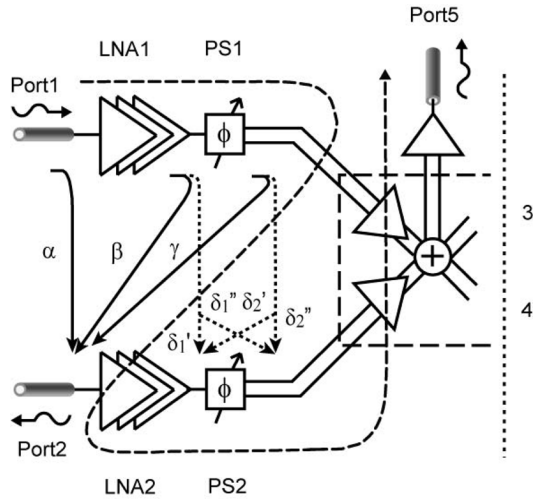

Fig. 9. Coupling plots between channel 1 and 2 before the RF combiner.

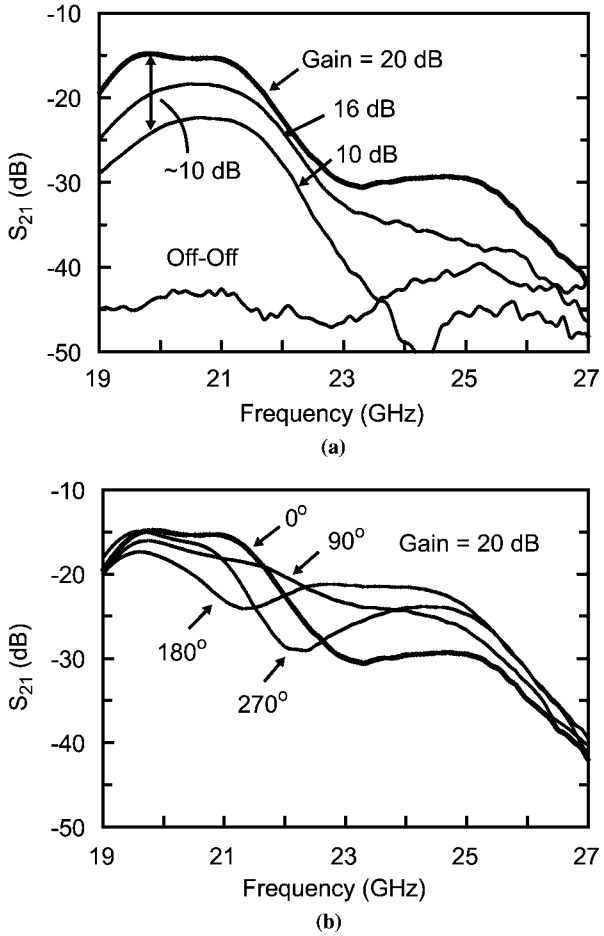

Fig. 10. Measured isolation S_{21}: (a) LNA1/PS1 and LNA2/PS2 are both "off" or "on" with different channel gains; (b) LNA1/PS1 and LNA2/PS2 are both on with a gain of 20 dB and different PS1 phase settings (PS2 is kept constant).

The measured isolation, S_{21}, can be significantly affected if the phase shifter in channel 1 (PS1) is changed over four states (0°, 90°, 180°, 270°) while PS2 is kept constant [Fig. 10(b)]. This shows that the β and γ coupling terms are of the same order of magnitude and can constructively or destructively interfere at

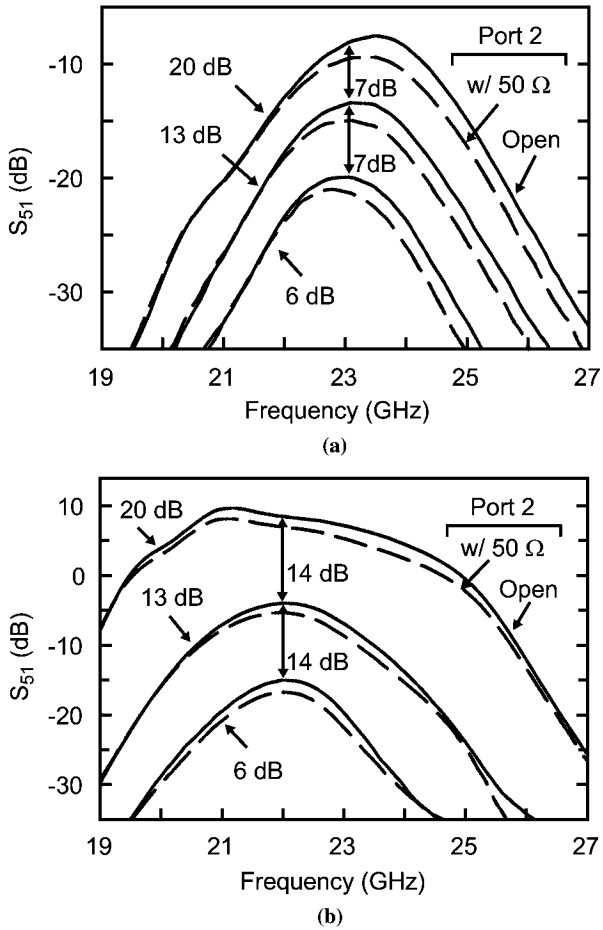

Fig. 11. Measured S_{51}: (a) LNA1/PS1 are "off" while LNA2/PS2 are "on" with different channel gains; (b) LNA1 and LNA2/PS2 are "on" with different channel gains.

port 2. This is important to know because, as will be seen later, the β and γ terms are the dominant coupling mechanisms in the phased array.

The on-chip coupling can also be characterized using a different experiment. In the first case, LNA1/PS1 are turned off, while LNA2/PS2 are biased for a channel gain of 20 dB, 13 dB and 6 dB, respectively, and S_{51} is measured with either an open circuit or a load at port 2. PS1 and PS2 are both set to 0°. Notice that there is no direct path between port 1 and port 5 (Fig. 9). It is seen that S_{21} for a 50 Ω load results in less coupling than an open circuit at port 2, as is expected from a voltage perspective at port 2 [Fig. 11(a)]. Also, the coupling is proportional to G as expected, where G is the LNA gain (phase shifter gain $\sim$ 0 dB). For the second case, LNA1 is turned on, but PS1 is turned off and this isolates channel 1 from the power combiner. LNA2/PS2 are also turned on, and both LNA1 and LNA2 are biased for a channel gain of 20 dB, 13 dB and 6 dB, respectively. PS1 and PS2 are both set to 0° as before. One can clearly see that S_{51} is high, even with the absence of a direct path between port 1 and port 5, and the coupling is proportional to G^2 [Fig. 11(b)]. Note that a 7 dB reduction in the channel gain results in a 14 dB reduction in S_{51}, and shows that β is the dominant coupling coefficient.

The output vector V_o can therefore be written as (normalized input of 1)

$$V_o = Ge^{j\Phi_1} + \Big\{\alpha Ge^{j\Phi_2} + G\beta Ge^{j\Phi_2} + Ge^{j\Phi_1}\gamma Ge^{j\Phi_2} + G\delta_{1'}e^{j\Phi_2} + G\delta_{1''} + Ge^{j\Phi_1}\delta_{2'}e^{j\Phi_2}\ldots\Big\}$$
$$\approx Ge^{j\Phi_1} + \Big\{\beta G^2 e^{j\Phi_2} + \gamma G^2 e^{j(\Phi_1+\Phi_2)}\Big\}$$

where ϕ_1 and ϕ_2 are the phase shifts for PS1 and PS2 and the gain of PS1 and PS2 are assumed to be 0 dB. It is evident that the β and γ terms are the dominant coupling mechanisms in a phased array since they undergo a G^2 gain. Knowing that the signal itself undergoes a G gain, it is seen that the β and γ terms increase as G *relative to the signal*, and therefore, one must operate the phased array chip with a relatively low LNA gain (10–15 dB) in order to avoid the deleterious effects of channel-to-channel coupling.

Finally, S_{51} is measured with both LNA1/PS1 and LNA2/PS2 biased for three different channel gains (20 dB, 10 dB, and 0 dB at 23 GHz), and PS2 is set to 0°, 90°, 180°, and 270° while PS1 is kept constant at 0° [Fig. 12(a)]. It is seen that the β and γ coupling terms result in a significant effect on S_{51} for a channel gain of 20 dB. However, when the channel gain is lowered to 10 dB, the *rms* amplitude and phase error at 22.5–25 GHz are <0.5 dB and $<3°$, respectively, which is acceptable for phased array applications [Fig. 12(b)].

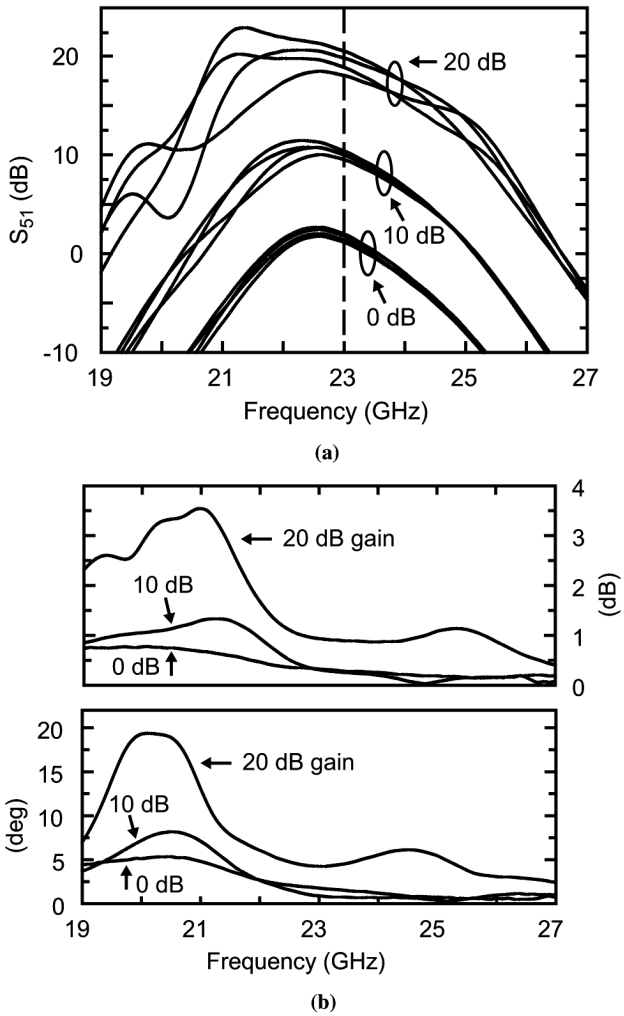

Fig. 12. (a) Measured S_{51} for a channel gain of 20 dB, 10 dB, 0 dB at 23 GHz, and PS2 set for 0°, 90°, 180°, 270°; (b) associated *rms* amplitude and phase error.

IV. Phased Array System-Level Measurements

The measured S-parameters of a single channel (channel 1) in the array are shown in Fig. 13 for 16 phase states which correspond to a 4-bit phase shifter setting in PS1. The phase states of PS2 are also randomly changed and contribute to the phased array system-level measurements. No attempt was done to control PS3 and PS4 due to their negligible coupling to channel 1 and they were randomly set to unknown phases. The analog phase states are controlled digitally using a computer and an external 16-bit D/A converter which sets the vector modulator gain for the quasi I and Q paths (V_1 and V_2). The D/A controller also sets the channel gain to be 9 dB at 24 GHz for all the PS1 phase states. The measurements are done on a single channel while all other channels are left open circuited (this results in more coupling as shown in Fig. 11). The chip consumes 76.5 mA from a 1.5 V supply (115 mW) for a measured gain of 9–12 dB per channel at 22–24 GHz.

The measured input and output reflection coefficients are <-10 dB and are virtually independent of the phase states. The measured average gain is 11.8 dB at 23 GHz with a 3-dB bandwidth of 2 GHz (22–24 GHz), and there is a slight shift in frequency between simulations and measurements. The measured output-to-input isolation (S_{15}) and channel 1 to channel 3 or channel 4 coupling (S_{31} and S_{41}) are all <-50 dB over all phase states. The measured channel 1 to channel 2 coupling has been extensively discussed in Section III. The measured system-level phase response (S_{51}) shows minimal effect from channel 2 at 23–25 GHz as expected from the coupling studies. The *rms* gain error for all phase states of PS1 and PS2 is <1.2 dB from 22–25 GHz, and <0.5 dB from 23.5–24.5 GHz. The *rms* phase error is $<6°$ at 22–25 GHz and increases slightly above 24 GHz due to the response of the active vector generator. The group delay, obtained from the measured phase response is 300 ± 50 ps at 22–24 GHz over all 16 phase states (± 25 ps over a single phase state), and shows that the *All-RF* architecture introduces minimal distortion in the RF signal path, and can support Gb/s data rates.

The measured NF is done for one channel while all the other channels are turned off so as to eliminate their noise contribution in the power combiner. A NF of 7.5–8.0 dB at 22–24 GHz is obtained and is independent of the phase state. The measured input $P_{1\mathrm{dB}}$ and IIP3 at 24 GHz are -20 dBm and -9.5 dBm, respectively, and are limited by the LNA.

Channels 2, 3, and 4 were also independently tested and result in the same performance (frequency response, *rms* gain, phase

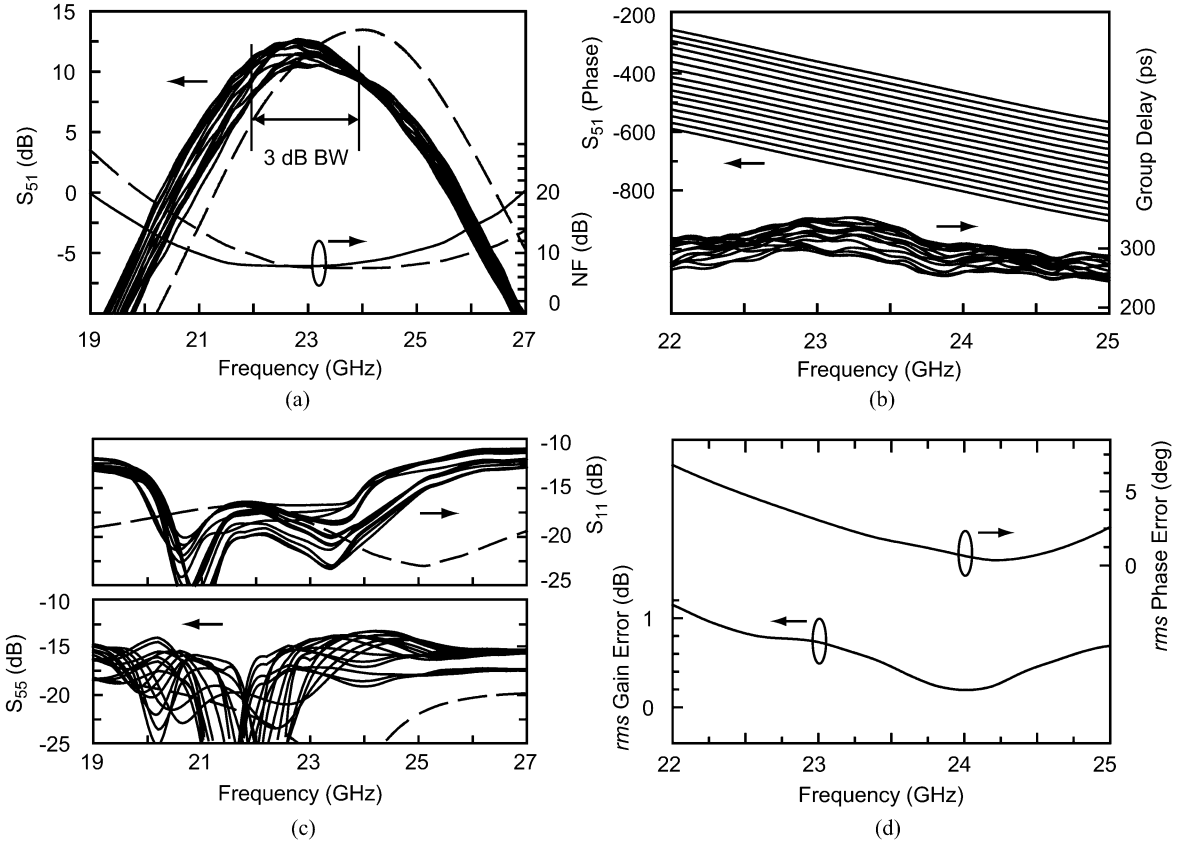

Fig. 13. Measured (solid lines) and simulated (dashed lines) S-parameters and NF of channel 1 with a gain setting of 9–12 dB at 22–24 GHz and a 4-bit phase setting.

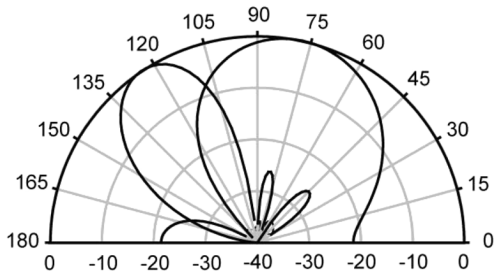

Fig. 14. Synthesized 2-element (scanned to $-15°$) and 4-element (scanned to $+35°$) antenna patterns based on the measured phased array chip.

errors, etc.) as channel 1 and are not shown. The maximum gain difference for the same LNA bias current and same phase state settings is ± 0.75 dB between all four channels. Fig. 14 shows the synthesized array patterns for a 2- or 4-element array based on the measured S-parameters with all coupling effects. It is seen that the patterns are very close to the ideal array patterns due to the excellent amplitude and phase balance between the channels, and the minimal channel-to-channel coupling for a channel gain of 9–12 dB at 22–24 GHz.

TABLE I
SUMMARY OF RESULTS

Phased Array Receiver Front-End	
Technology	0.13 μm CMOS (IBM 8RF)
Designed Frequency	22-24 GHz
Supply Voltage	1.5 V
Current Consumption	76.5 mA
Power Consumption	115 mW
Chip Area	2.11 x 1.43 mm^2
Performance of Each Array Element	
Input Return Loss	< -10 dB @ 15-35 GHz
Output Return Loss	< -13 dB @ 15-35 GHz
Channel Gain	9-12 dB @ 22-24 GHz
-3dB BW	2 GHz
NF	7.5-8 dB @ 22-24 GHz
IIP3	-9.5 to -12.5 dBm @ 22-24 GHz
P_{1dB}	-20 to -23 dBm @ 22-24 GHz
Phase Accuracy	< 6° *rms* @ 22-25 GHz
Gain Variation vs. phase states	< 1.2 dB *rms* @ 22-25 GHz
	< 0.5 dB *rms* @ 23.5-24.5 GHz
Performance of the Phased Array	
Magnitude Mismatch (channel to channel)	< ±0.75 dB @ 22-24 GHz
Isolation (channel-to-channel)	< -27 dB @ 22-24 GHz (for a channel gain of 10 dB)
Reverse Isolation (output-to-input)	< -50 dB

V. DISCUSSION

It is clear from the coupling measurements that, in our design, the maximum allowable channel gain for low *rms* gain and phase errors is 9–12 dB, and a 20 dB LNA gain is totally unacceptable. This is due to several reasons such as 1) high LNA output impedance which results in a large voltage swing and thus large voltage coupling to the input port; 2) single-ended

TABLE II
RFIC-BASED PHASED-ARRAY RECEIVERS

Frequency	24 GHz	24 GHz	6-18 GHz	24 GHz
Number of Elements	8	4	8	4
Topology	LO Phase Shift + Mixer + PLL	VPRO-PLL	RF Phase Shift	RF Phase Shift
Phase Control	4 bit (360°)	± 60° continuous	4 bit (360°)	360° continuous
Amplitude Control	No	No	No	0 to -20 dB continuous
Technology	0.18-μm BiCMOS	0.13-μm CMOS	0.18-μm BiCMOS	0.13-μm CMOS
Power (mW)	717	362	561	115
Area (mm^2)	3.5 x 3.3 (11.55)	2.35 x 2.15 (5.05)	2.2 x 2.45 (5.39)	2.11 x 1.43 (3.02)
Gain (dB)	43 [a]	30 [a]	20 (12 GHz)	12
NF (dB)	7.4	15 [b]	3.8 (12 GHz)	7.5
IIP3 (dBm)	-11.5	N.A.	-21	-12.5
P_{1dB} (dBm)	-27	-42 [b]	-31 [b]	-23
Reference	[1]	[8]	[5]	This work

a Include IF amplifier gain.
b A better value can be achieved with a new design.

design for the three-stage LNA which results in an coupling of −40 dB between the adjacent channels; 3) the coupling component increasing as G^2 while the signal component increases as G, and to a lesser extent; and 4) the absence of $n+$ deep wells in the CMOS substrate between the adjacent channels which may improve the channel-to-channel isolation. If a high gain is required from the beamformer chip, then it is recommended that the additional gain be placed after the RF combiner node and not at the input of each channel. Also a fully-differential LNA can be used and with less on-chip coupling between the channels. In terms of linearity, it is clear that the active vector generator/vector modulator and the 4-channel RF power combiner can result in high linearity (input $P_{1\mathrm{dB}} \sim -1$ to 0 dBm, IIP 3–9 to 10 dBm) under low current consumption. The phased array linearity is therefore limited by the LNA design. The results are summarized in Table I. A comparison of various RFIC-based phased array receivers is presented in Table II.

VI. CONCLUSION

This paper presents a 4-element mm-wave CMOS phased array including extensive on-chip coupling characterization. An active vector generator is used and results in quasi I and Q vectors at 22–24 GHz with a very small chip area ($50 \times 150\ \mu\mathrm{m}^2$). The symmetrical 4-channel mm-wave RF combiner results in excellent balance between the four channels and shows that it is possible to build very high performance on-chip mm-wave combiners. It is seen that, in this design, the channel-to-channel coupling due to the single-ended LNA and the high output LNA impedance limit the allowable gain per channel to 9–12 dB at 22–24 GHz. The *All-RF* architecture results in a very small chip area ($< 3\ \mathrm{mm}^2$), a power consumption of 115 mW, an IIP3 of −9.5 to −12.5 dBm, and is a suitable architecture for low-cost mm-wave phased arrays.

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