A 94 GHz mm-Wave-to-Baseband Pulsed-Radar Transceiver with Applications in Imaging and Gesture Recognition

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***Abstract*—High-resolution mm-wave array beamformers have applications in medical imaging, gesture recognition, and navigation. A scalable array architecture for 3D imaging is proposed in which single-element phase coherent transceiver (TRX) chips, with programmable TX pulse delay capability, are mounted on a common board to realize the array. This paper presents the design of the enabling TRX chip: a highly integrated 94 GHz phase-coherent pulsed-radar with on-chip antennas. The TRX achieves 10 GHz of frequency tuning range and 300 ps of contiguous pulse position control, enabling its usage in the large-array imager with time-domain TX beamforming. The TRX is capable of transmitting and receiving pulses down to 36 ps, translating to 30 GHz of bandwidth. Interferometric measurements show the TRX can obtain single-target range resolution better than 375 μm (limited by equipment). Based on delay measurements, the time of arrival rms error would be less than 1.3 ps which, if used in a 3D imaging array, leads to less than 0.36 mm of RMS error in voxel size and position.**

***Index Terms*—Gesture recognition, high-resolution imaging, loop antenna, medical imaging, millimeter-wave transceiver, on-chip antenna, pulsed transceiver, pulser, silicon-based imager, ultra-short pulse, wideband transceiver, 94 GHz transceiver.**

I. Introduction

MOORE'S LAW is pushing silicon towards yet another emerging application: bio-medical devices. Starting from 1970–1980s, silicon technology has successfully revitalized different areas from measurement instrumentation to personal computers, communication devices, and ubiquitous computing. The next big opportunity is in the field of bio-medical devices. Examples include large-array low-power ultrasonic imagers and lab-on-chip devices for rapid detection of pathogens or sequencing of DNA [1]–[3]. Diagnostic medical imaging is another application that can greatly benefit from cost-reduction and/or miniaturization offered by silicon technology. Today, imaging devices are largely confined to health-centers and large hospitals. The dynamics of patient-health provider interaction will radically change if these diagnostic tools are available by the patient's side rather than at long distances.

In this work we focus on a pulsed radar technology that can enable dielectric measurement of tissue for imaging. Despite its great potential, electrical properties and polarization characteristics in the microwave/mm-wave spectrum have not yet received much attention for diagnostic and screening applications. There are many specific cases where electrical properties of tissue can greatly enhance image quality or provide alternative contrast to conventional techniques. Electromagnetic signatures have been used for medical imaging applications [4]–[6]. Breast cancer screening technology is an example that has been pursued by various researchers in the past [5], [7]. One of the main limitations with this modality has been obtaining adequate signal to noise levels as well as sufficient cost/size reduction. By using techniques developed in consumer electronics and leveraging Moore's law, vast innovation can be brought to the realm of medical imaging.

The goal of a dielectric imager is to detect boundaries with different electrical properties. This could be achieved by various signaling schemes, such as frequency chirp methods or pulse based techniques [8]–[10]. The focus of this work is on Time-Domain Ultra-Wideband Synthetic Imaging (TUSI) where short pulses are transmitted and the reflections are recorded at multiple sites [6]. A first step towards the realization of this system is the generation of high frequency and high-energy short pulses from a silicon array. This has been demonstrated in [6], [11], [12] where fully integrated mm-wave pulsed-transmitters capable of sub-50 ps pulse generation are designed in silicon.

In this work we introduce a fully integrated 94 GHz pulsed radar transceiver (TRX) with on-chip antennas. The transceiver is fully synchronous and provides phase, amplitude, and time-of-flight information on echo pulses. Variable pulse-width programming allows for high-resolution multi-target detection (narrow pulses) as well as better signal-to-noise ratio and penetration (wider pulses). This TRX was designed with intended usage in a scalable timed-array that provides 3D imaging capability for application in medical diagnostics. Fig. 1(a) shows the implementation of such an array where TRX chips are mounted on a common flexible board/substrate allowing for bi-static and multi-static imaging. This technology also enables applications like real-time gesture detection for media interfaces in which a small array resides on a portable device and detects movements

Manuscript received August 31, 2012; revised November 21, 2012; accepted November 21, 2012. Date of current version March 22, 2013. This paper was approved by Guest Editor Vivek De. This work was supported by the Berkeley Wireless Research Center, the NSF Infrastructure Grant 0403427, STMicroelectronics, NSF Grant ECCS-0702037, Intel Foundation, and Qualcomm Inc.

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Digital Object Identifier 10.1109/JSSC.2013.2239004

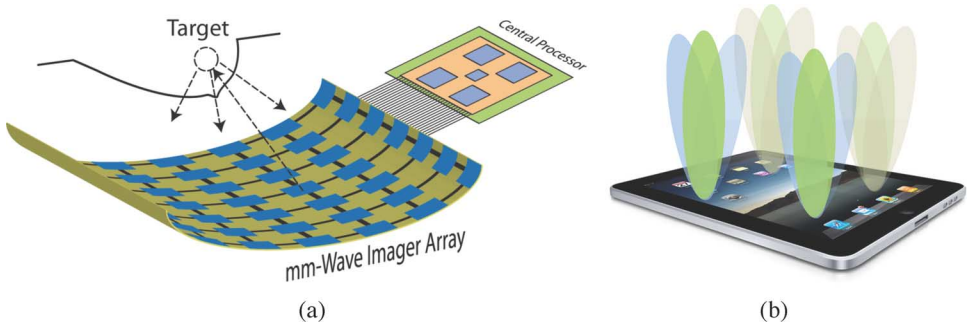


Fig. 1. Time-Domain Ultra-Wideband Synthetic Imager (TUSI). (a) TUSI array architecture for medical imaging applications. (b) Gesture detection application for TUSI array.

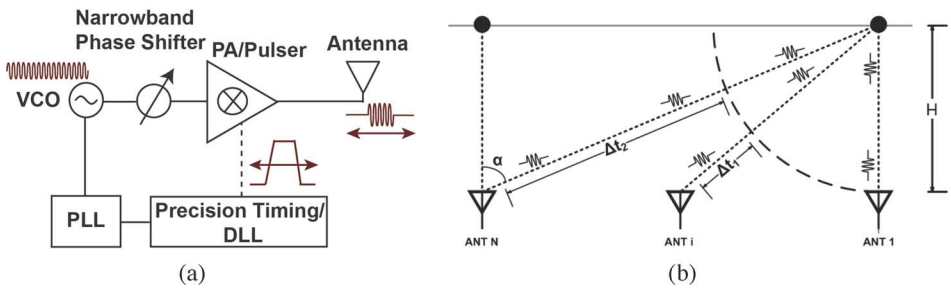


Fig. 2. (a) TX time-based beamforming architecture and (b) near-field time-array functionality with large span in time-of-transmission (TOT) programmability.

of the fingers (Fig. 1(b)). Other applications include remote detection of vital signs or other medically relevant signatures. This paper focuses on the design of the enabling technology for these applications, the single-element 94 GHz TRX.

II. Radar Imaging Array

In pulsed radar, short pulses are transmitted and reflections are measured to determine the object's location. The resolution of the system is determined by the pulse width (PW) (for depth resolution) as well as the center frequency and effective aperture (for cross resolution) [6], [8], [9]. The desired multi-target resolution in the proposed system is close to 1 mm in tissue and sub-cm for gesture detection applications. To realize timed-array functionality, it is critical to implement delay or phase-shift programmability. For large arrays with large bandwidth (BW), phase-shift approximation introduces unacceptable beam squint [13]. True-time delay elements become necessary but are not feasible for large field-of-views where maximum delay becomes too large for IC implementation [14]. Here, we introduce an alternate method for TX beamforming that covers large field-of-views by enabling time-shifts that far exceed the pulse width.

In the transmitter, we have the advantage of having prior knowledge of the intended waveform and use that information for accurate timing control. As shown in Fig. 2(a), for beamforming, we separate the carrier path from that of the envelope. Since the carrier signal is locked to the envelope control circuitry (using a co-locked PLL and DLL combination), this provides a stable delay control of the *modulated* pulse. The DLL moves the envelope of the pulse over a large span and a narrowband phase-shifter delays the carrier. Narrowband mm-wave phase shifting is relatively easy to implement and solutions are widely reported in the literature. Recently, compact versions have also been introduced using lumped-element baluns [15]. Alternatively, a vector interpolator can also be used as we have access to quadrature components of the carrier. In this chip, the narrowband phase shift is not included and the focus will be on envelope tracking.

Fig. 2(b) shows the basic concept of near-field time-domain beamforming for an N-element linear array. Due to the varying distances, each antenna must delay its time of transmission (TOT) w.r.t. the others in order to ensure coherent summation at the target. It follows that if larger antenna arrays are desired (for better SNR, and/or larger field of view), a wider range of TOT is needed. Furthermore, the resolution error of the selectable TOT must be minimized in order to reduce the error introduced by imperfect summation of pulses at the target. For a 10 cm^2 square array to image a 10 cm^2 cross-section (typical for imaging and gesture recognition applications) at a distance of 10 cm, a TOT range of 250 ps (close to 25 cycles of the carrier) is needed. This ensures that an antenna in one corner of the cubic volume can transmit to the target furthest away from it.

In the receiver, RF phase-shifting (or true-time delay) is eliminated and a coherent receiver provides quadrature baseband signals that could be directly digitized for maximum flexibility. Discussion of digitization methods will not be included in this paper.

System design constraints and specifications of the proposed array imager are given in previous publications [6], [16]. Table I summarizes the general specifications. Detailed discussions depend on application-specific assumptions and fall outside the scope of this paper. For example, in imaging applications, severe signal attenuation in tissue necessitates long averaging

TABLE I
GENERAL SYSTEM SPECIFICATIONS FOR IMAGING APPLICATIONS

Parameter	Value	Note
Center Frequency	94 GHz	Cross- resolution (10 cm aperture)
PW/ System BW	<50ps/ >20GHz (30GHz*)	Depth resolution
Peak RF Power	> +10dbm (+13dBm*)	Link Margin
Pulse Rep. Interval	>670ps	Max unambiguous range > 10cm
TOT program	Range: >250ps- Res.: < 2ps	Imaging 10cm^2 X-section at 10cm
Total TRX Jitter	< 1ps RMS **	Maintain res. with 10^7 avg.
PLL Cumulative Jitter	< 300fs (1KHz-1GHz)	Set as 1/3 of total RMS jitter budget Integ. range set by avg. window and PRF
RX Conv. Gain	>25dB	Baseband detection level

* Used for link calculations
**Does not include specifications for ADC but includes whole TRX chain

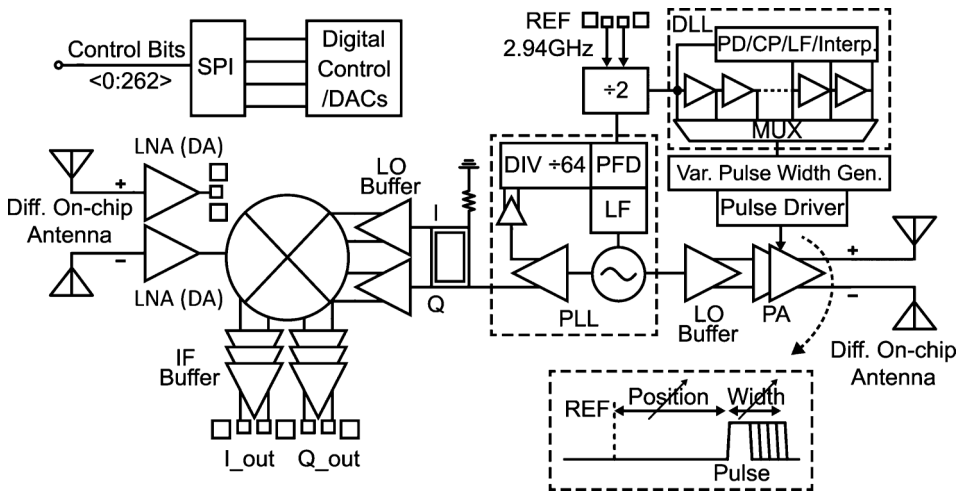


Fig. 3. TRX system block diagram.

windows for detection. Using numbers in Table I, to detect a cancer site with cross-section of 4 mm $\times$ 4 mm at effective depth of 3 cm in breast fat tissue using a 10 by 10 array, requires an averaging window of 10 ms to obtain 10 dB SNR (with 10 dB system margin, 1 GHz pulse repetition frequency (PRF), and 12 dB system noise figure). Tissue properties are obtained from [17]. On the other hand, for gesture detection, even without averaging, a 1 cm^2 target at 10 cm distance can be detected with a 3 $\times$ 3 element array (7 dB SNR and 10 dB system margin). Detailed system calculations need to take into account tissue interfaces, system stability for averaging, and various near-field beamforming effects [6], [16], [18].

In radar systems, cumulative phase noise—the phase error accumulated between transmission and reception of an echo signal—can cause system degradation [19]. In single-element radar, since noise is correlated due to the same synthesizer driving the TX and RX chains, phase noise is filtered and only short-term stability (pulse to pulse) is of concern [19]. In the proposed array architecture, part of the noise spectral density is uncorrelated (e.g., individual 94 GHz oscillators and loop), and hence a more complicated noise profile exists. Here, we assume worst-case condition of having total uncorrelated noise sources. The total accumulated jitter from two PLLs (i.e., $\sqrt{(\sigma_{TX}^2 + \sigma_{RX}^2)}$) is set to be 1/3 of the total RMS jitter budget (i.e., 300 fs).

III. SYSTEM OVERVIEW AND ARCHITECTURE

A single-chip, coherent, mm-wave radar has been designed in a 0.13 μm SiGe BiCMOS process (Fig. 3). The chip integrates RX/TX antennas, LNA, wideband active balun, quadrature mixers and IF gain stages, a 94 GHz PLL, programmable-width pulse generators, 1.47 GHz DLL, PA and quadrature LO distribution. An external 2.94 GHz reference is divided to provide the PRF for the pulser and a reference for the DLL and PLL thereby locking the carrier frequency to PRF and ensuring coherent pulse generation. This is a single element for intended use in a larger timed-array. As previously discussed, TX beamforming will be realized through a combination of DLL and PLL blocks. Array elements will later be synchronized using a common low-frequency (2.94 GHz) clock and local PLLs.

Starting from the RX chain in Fig. 3, the differential tapered-loop antenna output feeds two distributed amplifiers in the direct-conversion quadrature front-end. One is used purely for debug and testing purposes (at cost of losing signal power) and the other goes to the rest of the RX chain. The mixer is implemented as a micro-mixer [20] that incorporates single-ended to differential conversion and a large instantaneous BW of more than 40 GHz. The mixer is followed by a three-stage baseband gain element for each of the quadrature components.

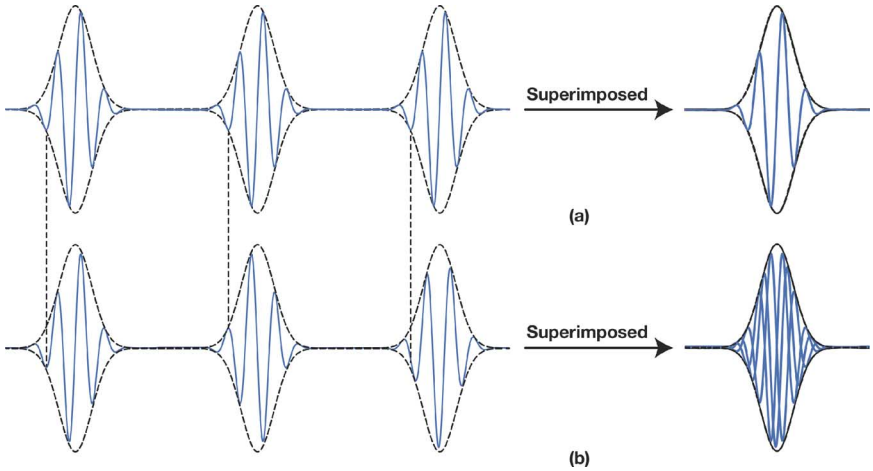


Fig. 4. Phase coherency between the carrier and envelope in train of pulses. Coherency leads to same initial phase for all pulses ((a) Top), while phase mismatch causes phase slip and leads to non-coherent pulses with averaging ((b) Bottom).

In the transmitter, the PLL is locked to a 1.47 GHz reference and its output drives the LO buffer and the two-stage transformer-coupled power amplifier (PA). A tapered-loop antenna, similar to that used in the RX, is integrated on the TX. The DLL is locked to the same common clock of 1.47 GHz and is used to provide timing to an edge-triggered programmable-width pulse generator. A final pulse driver modulates the output stage of the PA. With this design, both pulse position and pulse width are programmable. The pulse generation and control circuitry are similar to [6] and will not be discussed in this paper.

In this design, with co-locked PLL and DLL, the pulse repetition interval (PRI) is an integer multiple of the carrier cycle and all pulses will initiate with the same starting phase. Fig. 4 shows this effect with two cases of initiating pulses under coherent and non-coherent conditions. This unique feature of coherent pulse generation allows averaging prior to I/Q combination in which case carrier phase is preserved, thus enabling interferometric measurements. This is an enhancement to regular pulsed-radar techniques that only use envelope phase (or pulse position) information. The previous design of 90 GHz pulser in [6] did not incorporate this coherency, and therefore, with averaging phase (carrier) data inside the pulse was lost and only amplitude-based ranging was possible.

IV. Receiver

A. Distributed Amplifier Front-End

To provide sufficiently flat gain and group delay, the front-end amplifier needs to cover the frequency range between 60–130 GHz. For future integration with other (lower) frequency bands, a distributed amplifier with wideband characteristics is designed. In order to increase overall gain, a cascaded DA topology is selected [21], [22]. Three DA stages, each with 5 cascode gain elements, are cascaded to maximize gain while maintaining BW up to 130 GHz (Fig. 5).

The gain-bandwidth product of a distributed amplifier is limited by one of the three main factors: base (gate) line losses, collector (drain) line losses, and core device BW (due to internal poles) [22]–[26]. For a cascode device, as is implemented here, the output impedance of the gain element is relatively high

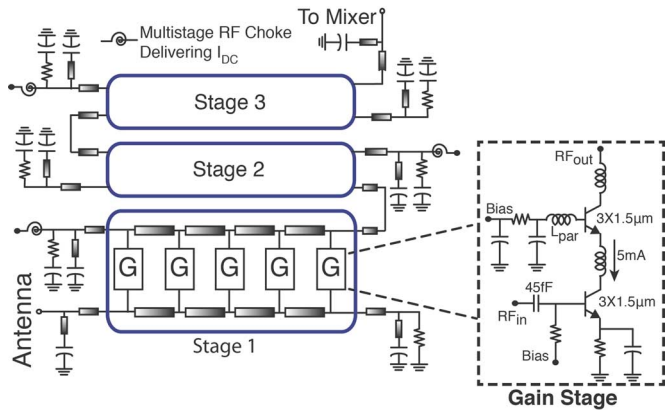


Fig. 5. Schematic of distributed amplifier.

and therefore the collector line losses are usually not the limiting factor. To increase the BW of the core element itself, an inter-stage inductor is placed in series in the cascode device [27], [28]. This inductor increases the impedance looking into the emitter of the cascode device and causes a BW extension similar to inductive peaking. To further increase BW, emitter capacitor-peaking is also employed [29].

The final bandwidth limitation arises from the base line of the DA, with the (equivalent) base resistance (r_b) playing a significant role. A single finger 1.5 μm bipolar device with 2 mA bias current has an input profile of $C_{ser} = 20$ fF and $R_{ser} = 43\ \Omega$ at 80 GHz leading to $\omega_{ser} = 185$ GHz. Sizing will scale C_{ser} and R_{ser} with the same ratio and will not help ω_{ser}. For BW close to 130 GHz, ω_{ser} has to be further out than what is achievable with sizing alone. In order to reduce the effect of r_b, a series input capacitor can be used [24], [25], [30].

Biasing the DA is another challenge that needs to be addressed for system integration. External bias-tees are not feasible due to lack of access to internal collector nodes of the first and second stage DAs. Providing the current through the collector termination resistances is problematic due to the large series RI^2 loss. Additionally, large current through the resistor causes problems for reliability (narrow resistor) or AC response due to parasitic capacitance (wide resistor). Instead, a multi-

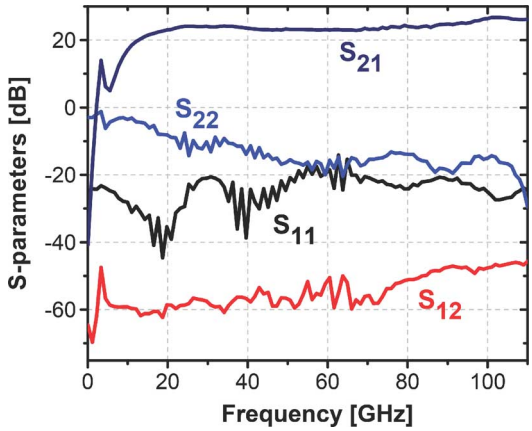


Fig. 6. S-parameter measurements of distributed amplifier (limited by VNA BW to 110 GHz).

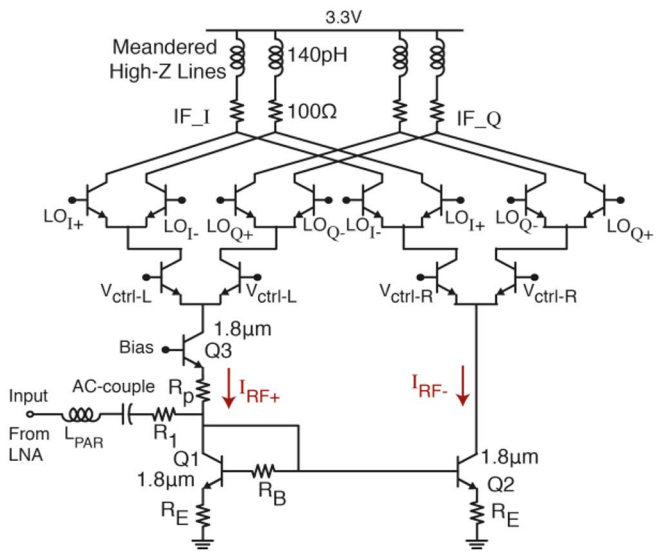


Fig. 7. Schematic of wideband active balun and mixer.

stage choke with a multi-turn spiral inductor at its core is used for biasing [30]. The spiral has a simulated self-resonance frequency of 190 GHz. The final design is similar to the standalone design in [30] but with extra programmable 4-bit biasing DACs and optimized interfaces for connection to the antenna and the mixer. S-parameter measurement of the DA is shown in Fig. 6 and includes all pads and parasitics. The amplifier provides an average gain of 24 dB (23–26.5 dB) and larger than 110 GHz of bandwidth (measurements limited by the VNA BW). Nominal simulated noise figure is between 7.4–9.5 dB.

B. Mixer

A fully-balanced active mixer with embedded single-ended to differential conversion is used in the direct-conversion receiver. The schematic of the mixer is shown in Fig. 7. Extremely wideband single-ended to differential conversion is performed through an active balun. The structure is similar to a "micromixer" proposed by Gilbert in [20].

To mitigate DC current error in the two differential branches, a resistor (R_B) is added in series with the base of the diode-connected device (Q1). In the AC response, adding the resistor will add a pole and zero to the impedance of this node. This could be used to equalize the response of the LNA-mixer interface section. The pole is located at

$$f_p = \frac{\beta g_m}{2\pi C_\pi(\beta+1)} \simeq f_t \tag{1}$$

and the zero frequency is located at

$$f_z = \frac{1}{2\pi C_\pi(R_B//r_\pi)} \tag{2}$$

This zero is common between the paths and will not affect the differential error of the active balun. In addition to R_B, R_1 and R_p are added for improved input match and phase/gain equalization, respectively.

The simulated differential phase error is less than 6° up to 130 GHz. The magnitude error before correction is below 10% for frequencies up to 110 GHz. This is partially corrected via the base control voltage of the current buffer that comes after the active-balun (and by that the collector-emitter voltage of Q2).

The mixer core has separate I/Q fully balanced cells that take the input from the current buffers (Fig. 7). The left and right current buffers mitigate capacitive loading (and hence BW reduction) by buffering lower devices (Q2 and Q3) and also reduce LO to RF feedthrough, which is a critical factor in pulsed radar arrays (e.g. to mitigate spurious re-transmit).

Various mismatch components in mixer can generate residual LO leakage to output. The LO varies between 87–97 GHz and the effective 3 dB bandwidth of output node is close to 40 GHz which does not sufficiently filter the LO component. This, together with the small allowable swing at that node (100 mV and programmable by mixer current DAC) may lead to receiver desensitization from LO feedthrough. To remedy this and other mismatch concerns, base bias voltage of the current buffers is made programmable by separate voltage DACs.

The mixer uses shunt-peaking in the form of high-Z meandered microstrip line. A peaking ratio of $m \simeq 2.2$ $(m = R^2C/L)$ is chosen as a tradeoff between bandwidth (BW) extension and group-delay flatness. The resulting BW extension ratio is 1.7 with a line inductance close to 140 pH in series with a 100 Ω load.

The simulated gain of the extracted mixer is shown in Fig. 8. The gain varies between -5 and -7 dB across the 65 GHz to 115 GHz band. Two single-ended to differential LO buffers are used to provide the required signal swing to the mixer LO port. The layout is completely balanced with dummy transmission lines placed to provide complete symmetry to the mixer and IF stages. The mixer nominal current is set to 2 mA for each of the branches and is programmable by a 4-bit DAC (0.4–3.4 mA per branch).

C. Baseband Gain Stages

The down-converted quadrature signals are fed to baseband amplifiers that buffer the output node of the mixer (which is critical in terms of BW limitations), provide modest gain, and finally drive 50 Ω lines. To support pulse widths down to 30 ps, a 3 dB bandwidth of at least 25 GHz is required on each of the quadrature signals. Group delay variations are kept below 20% of the pulse width to minimize distortion [19].

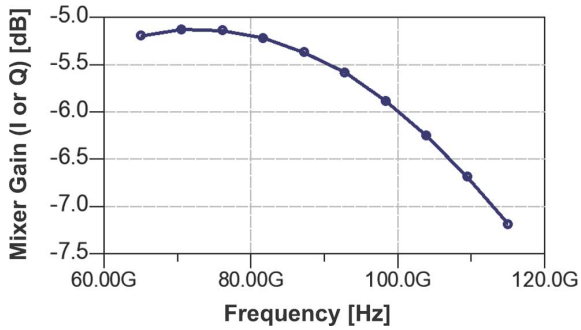


Fig. 8. Mixer gain referred to RF frequency (voltage gain with 200 Ω differential load).

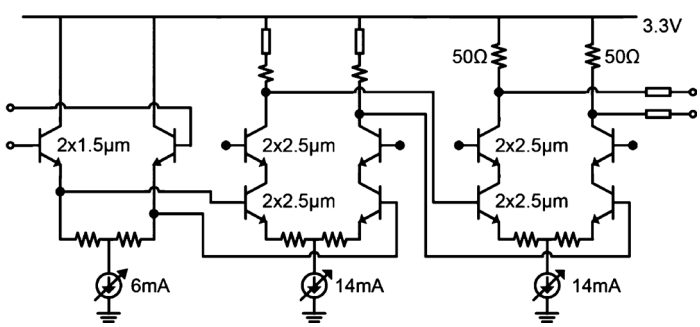


Fig. 9. Schematic of baseband buffer.

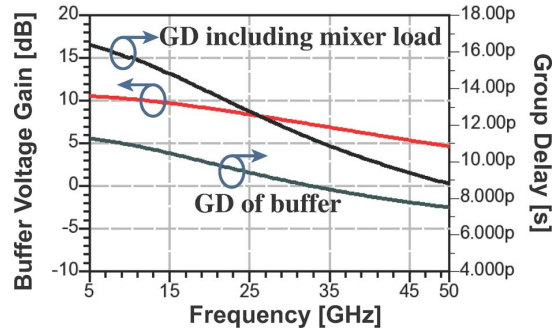


Fig. 10. Simulated baseband buffer voltage gain and group delay.

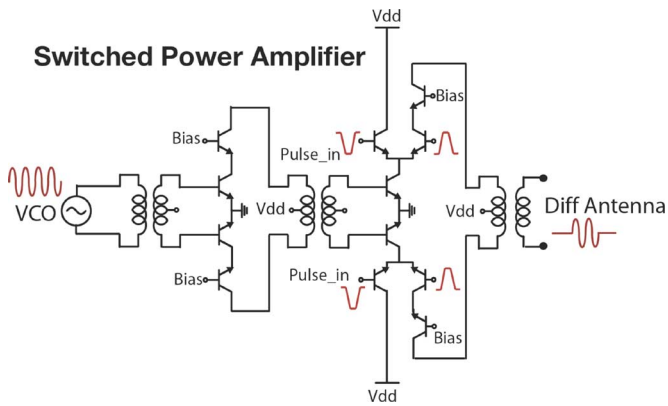


Fig. 11. Schematic of 2-stage power amplifier.

The input stage is designed as a differential follower to decrease input capacitive loading to the mixer. Here, stability concerns are balanced against bandwidth considerations. This stage is biased at 6 mA (device biased at 1 mA/μm) and the equivalent input shunt capacitance loading remains below 25 fF in the frequency band of interest.

The second stage is designed for gain. It uses larger devices (2×2.5 μm) in a differential cascode topology. Some emitter degeneration is used to reduce the input capacitive loading as well as for linearity improvements. Shunt-peaking is utilized and is implemented as meandered lines. This stage has a nominal bias current of 14 mA which places the transistor bias at 1.4 mA/μm. A third stage is used to drive the 50Ω line. Fig. 9 shows the schematic of the three-stage buffer.

Fig. 10 shows the simulation results of the baseband buffer including full EM simulations of connections and shunt-peaking load networks. The buffer provides 11 dB of gain across a 26 GHz BW while driving 50Ω loads of RF differential Ground-Signal-Signal-Ground (GSSG) pads. The current DACs provide a programmable range of 1.2–10.2 mA for the first stage and 2.8–23.8 mA for the second and third stages.

V. Transmitter

A. Power Amplifier

Millimeter-wave pulsed PAs were previously demonstrated in [6], [12]. Here, to decrease direct (capacitive) signal leakage in OFF mode, we have shifted to a three-stack topology (Fig. 11). Additionally, unlike our previous designs, we are using a differential baseband input pulse to the PA for better ON/OFF ratio. The core PA uses a two-stage transformer-coupled class AB power combining architecture. The first stage uses 5 (finger) $\times$ (2 μm) transistors and the second stage uses 5 (finger) $\times$ (4 μm) transistors. It achieves gain of 16 dB, $\mathrm{OP}_{-1\mathrm{dB}}$ of $+8$ dBm and $\mathrm{P}_{\mathrm{sat}}$ of $+13$ dBm at 94 GHz.

An ECL buffer is used to pass the pulse signal from the pulse generator (PG) to the pulse input port of second stage of the PA. The buffer has a 25 Ω resistive load with a nominal tail current of 25 mA. 10 Ω series resistors are placed between the buffer and PA to ensure stability. At the lowest bias setting, the driver obtains a differential rise-time of 28 ps over 1 V swing ($\pm$500 mV).

B. Delay-Locked Loop

In order to obtain fine phase control, a delay-locked loop (DLL) with embedded phase interpolation is used [31]. A block diagram of the DLL is shown in Fig. 12. The DLL is comprised of a 9-stage voltage controlled delay line (VCDL), phase blending phase detector (PD), V/I Converter, and loop filter (LF). In addition, an output MUX is used to increase the obtainable phase range. The DLL receives the divided down 1.47 GHz reference clock and drives the edge-triggered pulse generator, thus controlling the phase of the transmitted pulse.

Phase programmability is achieved via the embedded phase interpolation technique [31], [32] (Fig. 12). Two-phase detectors individually compare two taps of the VCDL to the reference clock and have their output currents summed. The output

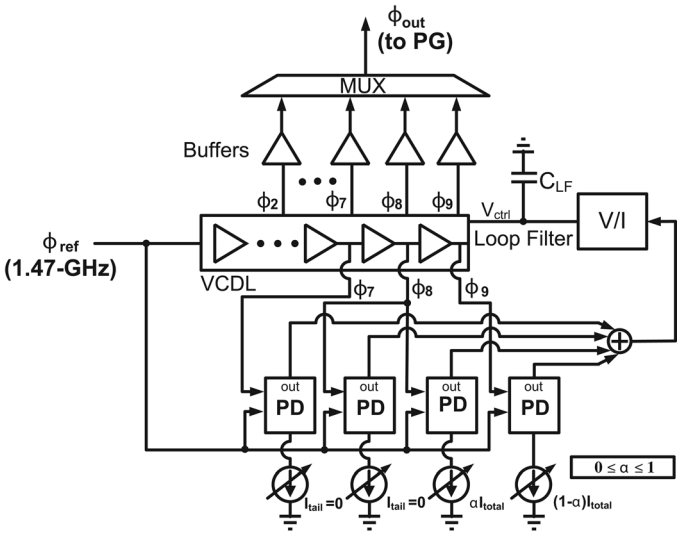


Fig. 12. Block Diagram of DLL w/ embedded phase interpolation (tail currents are set for first stage of interpolation).

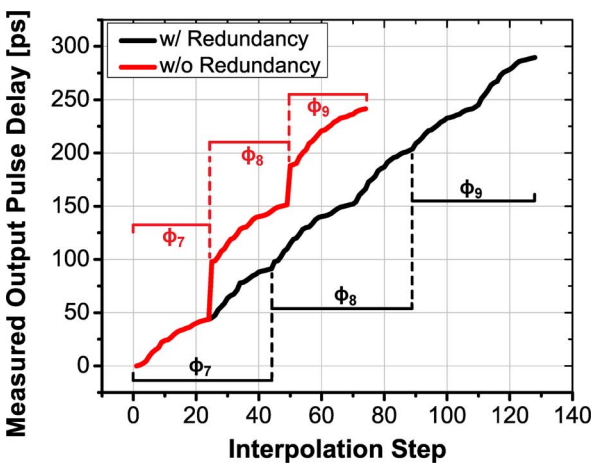


Fig. 13. Comparison of measured phase response of ϕ_7–ϕ_9 with and without redundancy.

of this programmable weighted summation is used to close the feedback loop and, in turn, controls the delay of each stage of the DLL. Thus, a change in phase is observed at *every* tap with each change in weight settings. Weighted summation is controlled via the tail currents. This enables control of the output phase by changing the current allocation of each PD.

Granularity in the current allocation is obtained by using current DACs for the tail current sources. The advantage here is that phase resolution is now dictated by the resolution of the current DACs and no longer by the number of interpolation stages, as is the case for conventional approaches, leading to a simpler design. In the figure, the tail currents are set such that the interpolation occurs between the last two taps of the DLL. Interpolating between $\Phi_8$and Φ_7 is also possible by simply performing the current sharing between the two leftmost PDs—the reason for wanting to do this is discussed later.

Letting α and $(1-\alpha)$ represent the percentage of current given to tap $N-1$ and tap N's PD, respectively, the change in the delay of the M^{th}stage of an N-stage DLL (w.r.t. the nominal delay of $M*(T_{\rm lock})/(N)$) is given by [31]:

$$\Delta t_M = (M * T_{\rm lock}) * \left[\frac{\alpha}{N*(N-\alpha)}\right] \tag{3}$$

where $T_{\rm lock}$ is the delay required to satisfy the locking condition. Due to accumulation of delay along the VCDL, Δt_M is proportional to M. As a result, care must be taken to make sure the worst-case phase step, which occurs at the last tap, is smaller than the required phase resolution. In this design, we use 5-bit thermometer-coded current DACs, leading to a theoretical worst-case phase step of less than 3 ps over a 425 ps range.

The phase range obtained from a single tap of the DLL is not sufficient for the imaging system. To solve this, a MUX is placed at the output of the DLL in order to combine the phase responses of multiple taps into a single output. With only one stage of interpolation (between Φ_9 and Φ_8's PDs), there will be abrupt phase jumps present in the phase response, making certain phase shifts unobtainable. This is undesirable since it would lead to "blind spots" where the imager cannot focus its beam. To solve this, redundancy [31] is introduced in the phase response by adding another stage of interpolation between Φ_8 and Φ_7. With this chip, the benefit of redundancy when switching across multiple taps is observable due to the integrated MUX (unlike [31]).

The extra stage of interpolation extends the phase response of each individual tap and, as a result, lessens the discontinuities between taps. This helps to increase the range of phase programmability over which minimum phase step specifications are met. Fig. 13 illustrates this point by comparing the measured phase response of Φ_7–Φ_9 for two cases: 1) with redundancy and 2) without redundancy. In the absence of redundancy, the phase range is 241 ps with a worst-case step of 54.2 ps. With redundancy, the range is increased to 290 ps while the worst-case step is reduced to 6.8 ps.

VI. Frequency Synthesis and Distribution

The 94 GHz PLL is shown in Fig. 14. This PLL uses similar loop elements and characteristics to that of the stand-alone PLL in [33], with some modifications for system integration. First, the varactors are divided into three groups, one for the loop filter and the other two groups for two-bit digital control. Hence the PLL has four frequency bands. Secondly, the VCO drives TX, RX, and the divider chain so more branching is required. For this, one more single-to-differential LO buffer is added in between VCO and a divider chain.

As described earlier, excessive PLL phase noise can play a detrimental role in pulsed-radar performance. For low phase noise and jitter, the PLL adopts several techniques. An on-chip input divider sharpens the clock transition by using a higher reference clock frequency. The VCO itself has a low phase noise (-124.5 dBc/Hz at 10 MHz offset), which relaxes the trade-off between VCO noise and reference noise. Also, the loop bandwidth can be adjusted by switching V-to-I currents, enabling optimal selection for in-band noise. Moreover, the PLL uses a

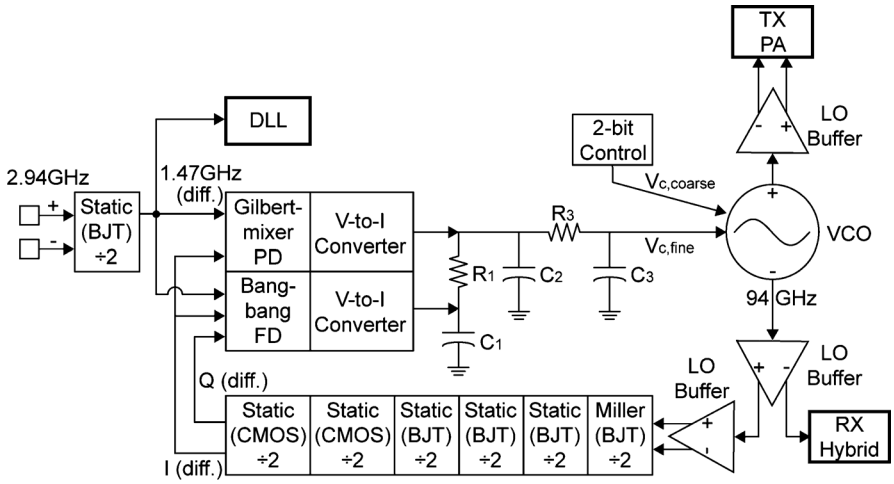


Fig. 14. Block diagram of PLL.

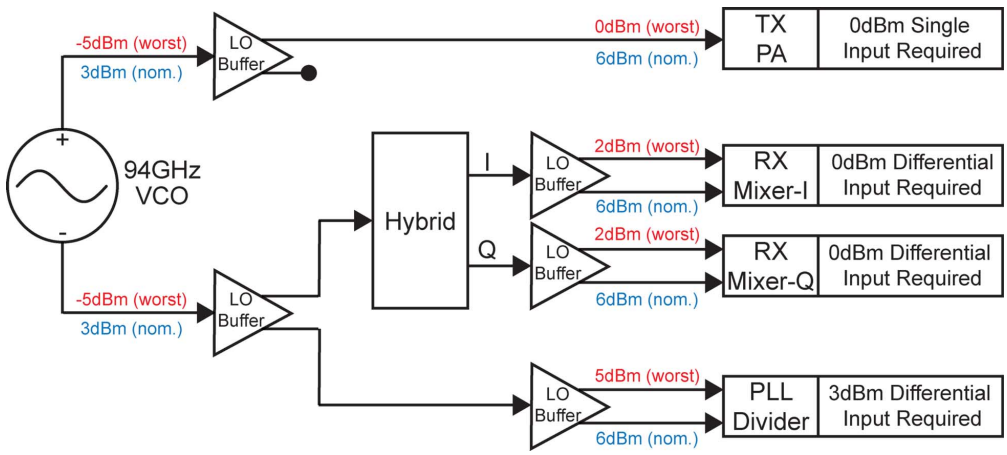


Fig. 15. Block diagram of LO distribution.

Gilbert-mixer phase-detector with much lower reference spur than a digital rail-to-rail XOR PD [34].

The LO signal is distributed to TX, RX, and PLL divider branches. The three different parts need different LO power as shown in Fig. 15. The TX PA requires at least 0dBm single-ended LO signal. The RX mixers take quadrature (I and Q) LO signals, both of which require 0dBm differential LO input to maintain the specified gain and noise figure for the mixer. Also, the PLL divider needs over +3 dBm differential input for proper operation. Thus, the LO distribution circuitry should appropriately deliver the LO signal to each part, while the VCO output power, buffer gain, and hybrid loss are taken into account.

Due to the PVT variations, each block suffers from performance variation and worst-case scenarios are considered in order to meet power-level requirements. Even in the worst case, the delivered output powers are higher than the required values for all the three branches. To provide flexibility in case of nominal conditions and excess power levels, the LO buffer gain is designed to be programmable (using 4-bit DACs) in the range 2–10 dB at 94 GHz.

The single-to-differential LO buffer is a differential cascode amplifier with a balun at the input and a transformer at the output. For stability and bandwidth, 16 Ω resistors are added in series with the collectors of the cascode devices. Also for convenient connections, the single-ended input is matched to 50 Ω and the differential output is matched to 100 Ω. The simulated buffer gain is 10 dB, $\mathrm{OP}_{-1\mathrm{dB}}$ is 2 dBm, and Psat is 5.4 dBm at 94 GHz. The hybrid is made of four microstrip lines and four MIM capacitors. The size of the hybrid is 162 μm × 237 μm. The simulated amplitude imbalance is less than 1dB and the phase imbalance is less than 8° over 94 GHz ± 10 GHz (Fig. 16).

VII. Antenna Design

A. On-Chip Antenna Design Challenges

Surface waves are a major cause for concern for on-chip antennas due to high silicon permittivity and can potentially degrade radiation patterns, introduce loss mechanisms, and reduce overall efficiency [35]. The energy coupled into surface waves can radiate out of the backside, diffract from the chip edges (causing sidelobes in the radiation pattern) or be resistively lost as heat within the conductive p-type doped Si substrate (15 ohm-cm substrate resistivity assumed here).

As seen in [35], [36], one elaborate method to mitigate backside radiation is to place a dielectric lens on the underside of the substrate, effectively removing the backside air-dielectric

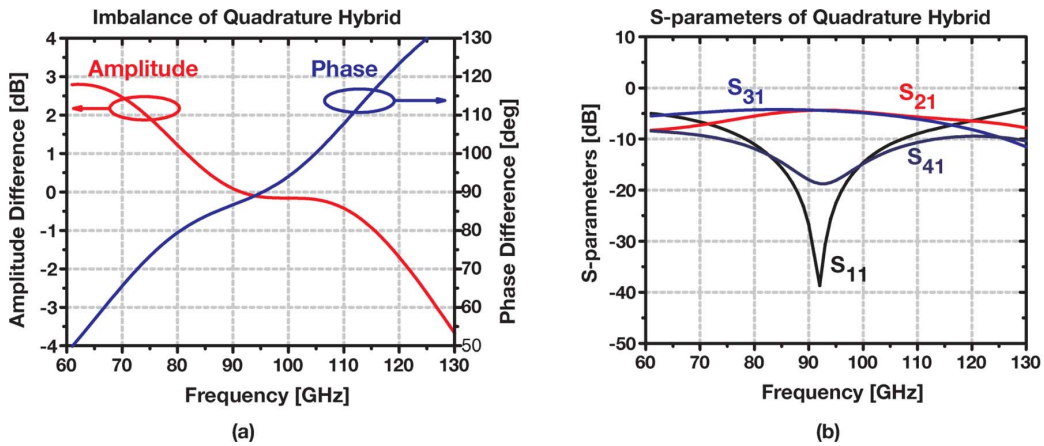


Fig. 16. Simulation results for (a) hybrid amplitude and phase error and (b) hybrid S-parameters.

boundary, approximating an infinite thickness dielectric and using backside as the main source of radiation. This works best in a lossless substrate [35]. However, for on-chip antennas, the Si substrate is conductive and this method would have reduced efficiency since the energy would be attenuated while travelling through the substrate. Substrate thinning [36] can be used in order to minimize this energy loss. In our case, we opted for a simpler and more cost effective process that does not require a dielectric lens nor substrate thinning. Backside radiation is mitigated in our design by placing an off-chip conductive reflector on the PCB backing the chip. This ensures that no backside radiation occurs but we still incur an efficiency reduction since majority of the radiated energy gets absorbed in the dielectric, makes a round trip around the bottom reflector and then radiates out the topside. In addition, this has implications on the input impedance of the antenna that need to be taken into account.

There are numerous works that discuss the excitation of different modes with respect to varying substrate height [35], [36]. Since our structure has radial symmetry, the surface wave modes propagate radially and we need to consider all modes of cylindrical nature as discussed in [37]. The cut-off frequency equations for the various TM and TE surface wave modes are provided in [35]. For our 375 μm Si substrate, TM_0 (zero-cutoff frequency) and TE_1 are the only modes present below 120 GHz and energy loss due to higher order modes is a non-issue.

B. Tapered Loop Antenna With Reflector

A large loop, suspended in air, has a symmetric and bi-directional radiation pattern. In our simulation model, we add the high permittivity and conductive silicon substrate on bottom side of the loop, which drastically reduces efficiency and transforms the radiation pattern such that the majority of the power is now radiated through the substrate, onto the backside. We also include the SiO_2 layer below the antenna metal in our simulations but due to the thinness, it does not have an impact on performance even at millimeter-wave frequencies.

Next, the conductive reflector below the substrate is added, changing the radiation pattern into a unidirectional one, with all the power radiated broadside to the structure. The input impedance is also affected—the real part (i.e., radiation resistance) decreases due to mutual coupling from the image elements while the imaginary part also decreases due to the capacitance formed with the high permittivity substrate and the conductive plate. The capacitive input is desirable since, as shown in [38], a thin loop near resonance is on the inductive side and this brings it closer to resonance. The lowered radiation resistance, although traditionally undesirable, can be mitigated by appropriately designing the drive circuit to maximize power transfer.

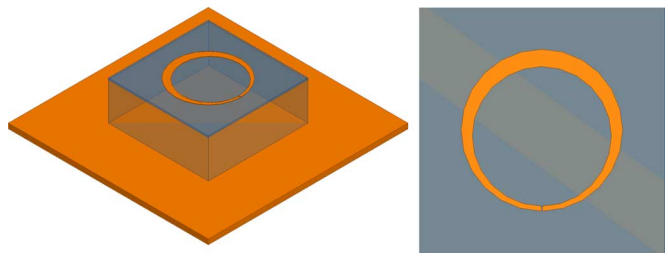


Fig. 17. Side and top view of circular tapered loop antenna with reflector on 1×1 mm^2 Si substrate.

Finally, the antenna thickness is tapered—20 μm thin at the feed point and 70 μm thick at the opposite end. This ensures that a CPW feed will not see a thick, abrupt transition at the feed point and the associated capacitance with it. It also provides a way to increase antenna metal thickness and mitigate finite metal conductivity losses. Tapers also naturally help extend the bandwidth of the structure. Tuned to the guided wavelength on the Si substrate, the final diameter of the antenna is 650 μm. Fig. 17 shows side and top views of the structure on a 1×1 mm^2 Si substrate backed by a 2×2 mm^2 gold reflector.

Fig. 18 shows radiation efficiency, peak gain, and input impedance versus frequency. Efficiency is rather high compared to similar on-chip designs, above 30% for our band of interest. Similarly, peak gain is above 1 dB (it should be noted that peak gain always occurs in the broadside direction in our band). Input impedance follows the trends in [38], lowered due to the mutual impedance from the image elements.

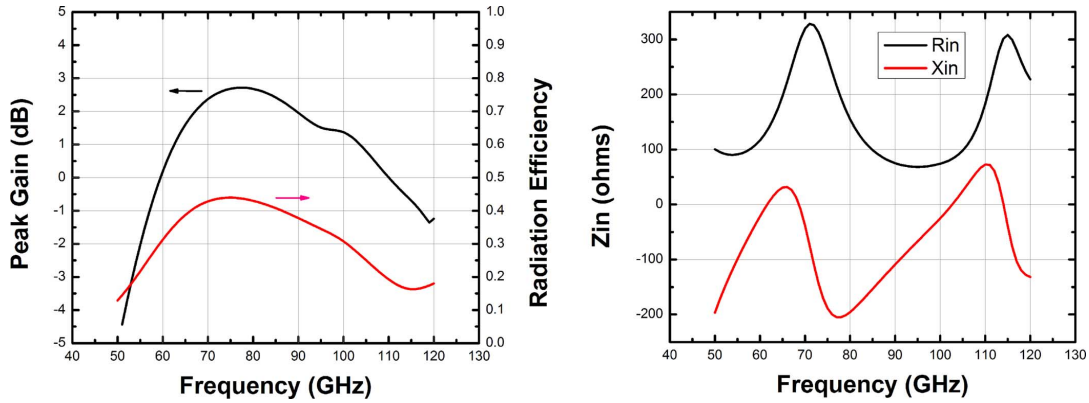


Fig. 18. Peak gain and radiation efficiency versus frequency of circular tapered loop antenna with reflector on 1×1 mm^2 Si substrate (left). Real and imaginary parts of the input impedance of circular tapered loop antenna with reflector on 1×1 mm^2 Si substrate (right).

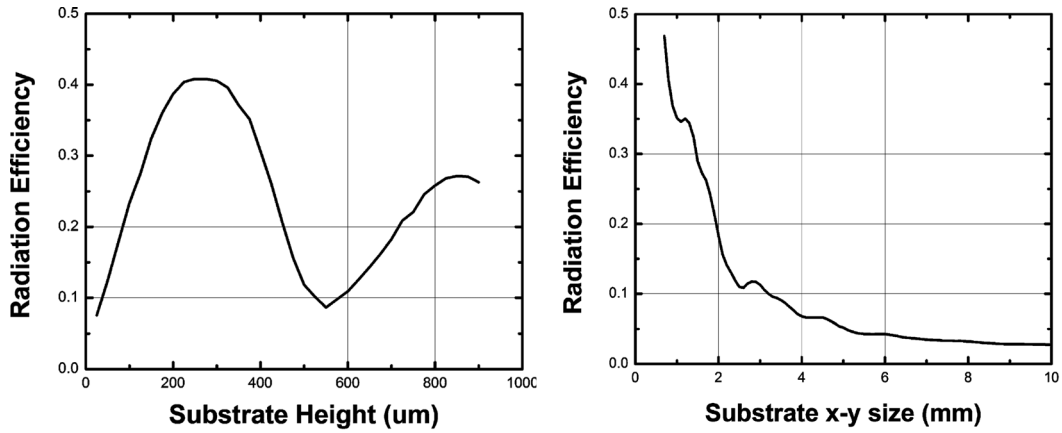


Fig. 19. Efficiency versus substrate thickness of circular tapered loop antenna with reflector on 1×1 mm^2 Si substrate (left). Efficiency versus substrate x-y size of circular tapered loop antenna with reflector (right).

C. Effect of Z and XY Sizing and Position on Antenna Performance

This design is backed by a conductive reflector. On one hand, reducing substrate thickness helps since it reduces the round-trip distance travelled by the wave in the conductive substrate before being radiated into free space. On the other hand, the image elements due to the reflector can constructively or destructively interfere with the real element, depending on the reflector distance in wavelengths. Plot of antenna radiation efficiency at 94 GHz versus thickness on a 1×1 mm^2 substrate is shown in Fig. 19, showing that peak in radiation efficiency occurs at a quarter wavelength separation of $\sim$280 μm. Thus for this antenna, a 375 μm thickness is close to optimal and a much thinner substrate would not have necessarily been better.

Using the transcendental equations provided in [39], the guided wavelength for the modes present in our substrate at 94 GHz can be calculate: $\lambda_{\mathrm{TM0}} = 1.15$ mm an $\lambda_{\mathrm{TE1}} = 3.04$ mm. For the 1×1 mm^2 substrate, the distance from the center to the vertex is 0.71 mm. Significant power is coupled into a certain mode only when the distance from the center of the antenna to the vertex of the substrate is on the order of the guided mode wavelength. Simulating with larger substrates, efficiency degradation and sidelobes in the radiation pattern is observed as the substrate starts supporting the two above mentioned modes. Fig. 19 shows radiation efficiency as a function of substrate x-y size.

As expected, larger substrates show a sharp drop in efficiency, as power is lost in surface wave modes. It is interesting to note that at the point where excitation in a particular mode begins, there is a brief positive slope in efficiency versus substrate size. It seems that power that was previously lost in the conductive substrate suddenly has an available mode to couple into, which then travels to the edge and diffracts. As the substrate gets larger, distance to the edge increases and efficiency decreases again since power in the mode is resistively lost as it travels outward. In addition, the radiation pattern shows the expected sidelobes from the power in the surface wave modes diffracting from the chip edges. From simulation, it is determined that substrates larger than 2×2 mm^2 show significant sidelobe patterns at 94 GHz. In the limit of large substrate size, the efficiency converges to $1/\varepsilon_{\mathrm{r}}^{3/2}$ (as expected from [35]) since almost all the power in the surface wave modes is resistively lost in the substrate before reaching the edge. This can also be seen in the surface current (plotted in Fig. 20 for 1×1, 2.5×2.5, and 5×5 mm^{2}cases) and electric field data from our simulator—for small substrates, a standing wave type pattern is observed while for larger substrates a radially directed travelling wave front within the substrate is observed that attenuates in magnitude as it propagates out.

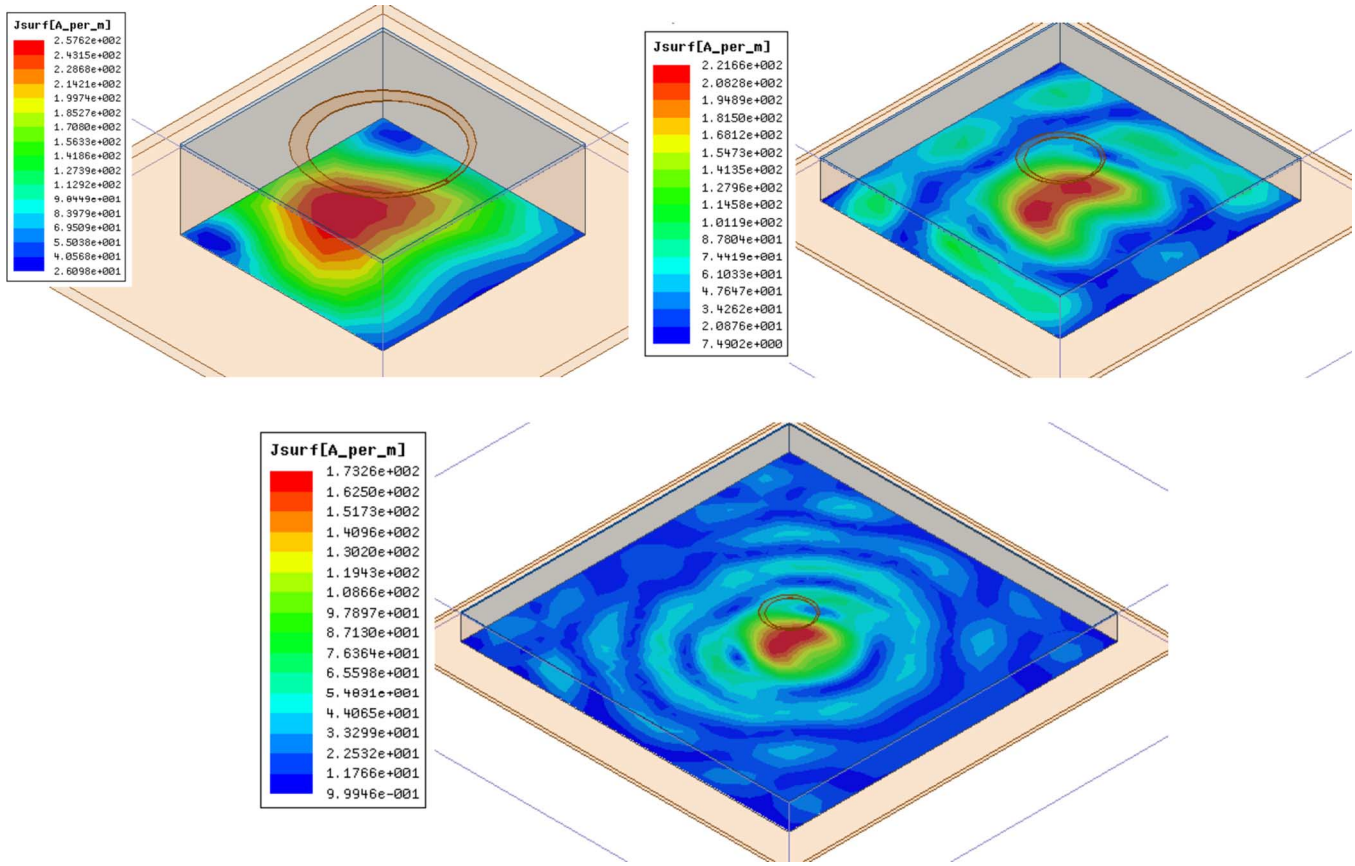


Fig. 20. Surface currents on the bottom of the Si substrate for circular tapered loop antenna with reflector on a 1×1 (left), 2.5×2.5 (right) and 5×5 (bottom) mm^2 substrate.

Fig. 21. Top view of hexagonal tapered loop antenna with reflector on 4.4×1.4 mm^2 Si substrate. The small metal pieces correspond to dummy fills required to satisfy min density design rules. These artifacts are included in the final simulation to ensure they do not disturb the antenna's performance.

D. Final Design

The final design is a hexagonal tapered loop antenna, with the same diameter (650 μm) and thicknesses at the two ends (20 μm and 70 μm). A hexagonal structure should have nearly identical performance as that of circular and the switch was made for ease of layout. Two antennas, one for each TX and RX, are placed on two edges of the 4.4×1.4 mm^2 chip. While the overall chip is much larger than the optimum found earlier, the antennas are strategically placed on the edges such that the higher order TE1 mode cannot be sufficiently excited. Fig. 21 shows the top view of the final design simulated. There is sufficient distance between the two antennas such that there would not be any substantial mutual coupling and only simulation from one antenna is shown.

Fig. 22 shows simulation results plotting radiation efficiency and peak gain versus frequency. Also shown are radiation patterns as polar plot and in feed and orthogonal planes at 94 GHz. The bottom end of usable frequency is around 60 GHz, below which the image elements due to the reflector are too close and start degrading broadside gain. The high end is around 110 GHz, above which surface modes excited start radiating from the chip edges and introduce sidelobes in the radiation pattern.

VIII. Measurement Results

The chip is fabricated in a 0.13 μm SiGe BiCMOS process with $f_T = 230$ GHz. The die micrograph is shown in Fig. 23. The die thickness is set to the standard 375 μm. The chip is bonded to a PCB board using a chip-on-board (COB) assembly.

The antenna ground reflector is implemented as a soft-gold ground plane underneath the chip. Here, a continuous ground plane is placed under the entire backside of the chip. To reduce direct coupling between the TX and RX, the grounds could be cut in the middle. The chip has two high-frequency interfaces: the input reference clock, which is at 2.94 GHz (nominal), and the IF output, which is probed. In total, the chip has 262 bits of control to set bias currents, select TX and RX settings, and to set the pulse width, delay and polarity.

To perform transceiver testing a sampling oscilloscope was used as the primary testing module. The input reference clock was provided by the Agilent 8267D. A different signal source triggers the oscilloscope. The two sources are locked together using the 10 MHz references. This is not an ideal

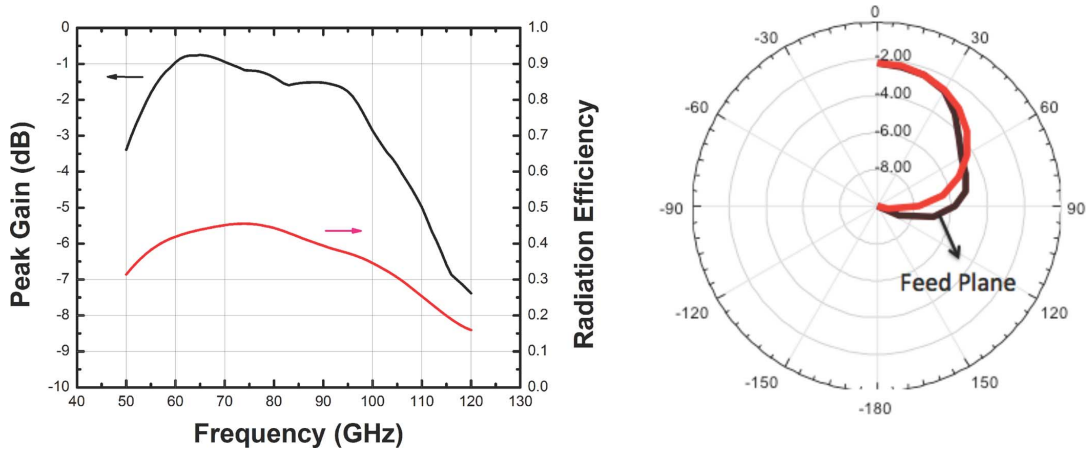


Fig. 22. Simulations of hexagonal tapered loop antenna with reflector on 4.4 × 1.4 mm^2 Si substrate: Peak gain and radiation efficiency versus frequency (left). Feed plane and orthogonal plane radiation patterns at 94 GHz (right).

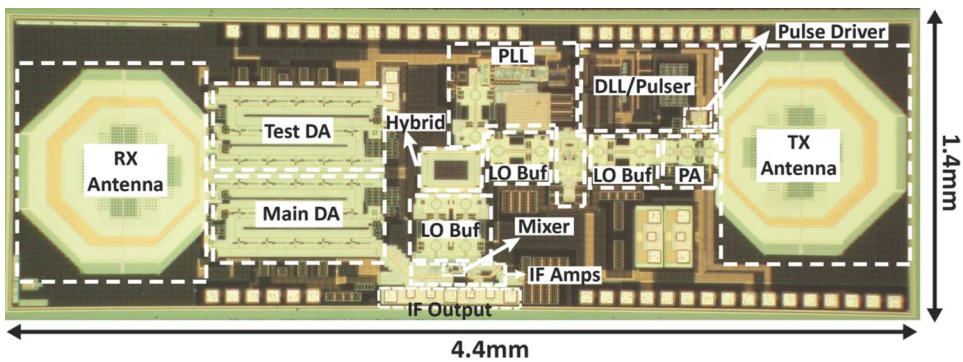


Fig. 23. Die photo of radar transceiver.

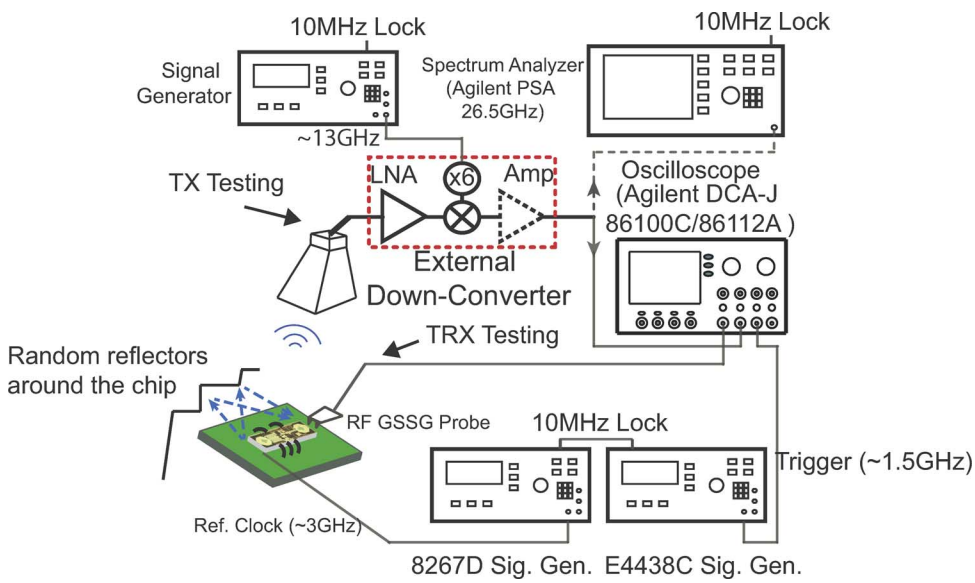


Fig. 24. Measurement setup for testing the radar transceiver. Both TRX and separate TX measurement setups are shown. The TX is measured by an external down-converter.

locking scheme and has some negative impact on the system measurements. The measurement setup is shown in Fig. 24.

The measured locking range of the PLL (measured when system is in actual pulse mode) is shown in Fig. 25. The VCO frequency band is selected by 2-bit digital control string that introduces extra fixed varactors to the tank. To adjust the frequency of the VCO and allow increase in locking, the VCO bias current can also be slightly modified from nominal. The PLL locks from 87.3 GHz to 97.2 GHz. The measured single-ended output power of standalone VCO is +3 dBm. The PLL phase

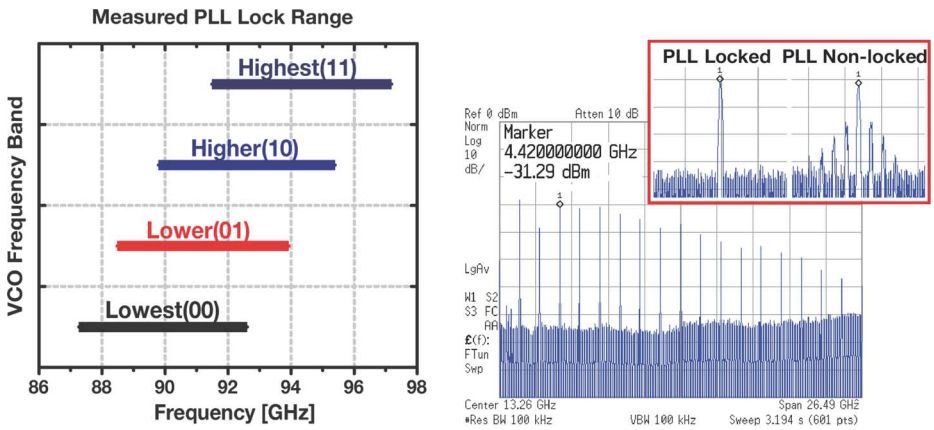


Fig. 25. Measured PLL locking range in pulsed mode (left). Frequency spectrum measurements of the transceiver together with zoomed in versions for locked and non-locked PLL conditions (right).

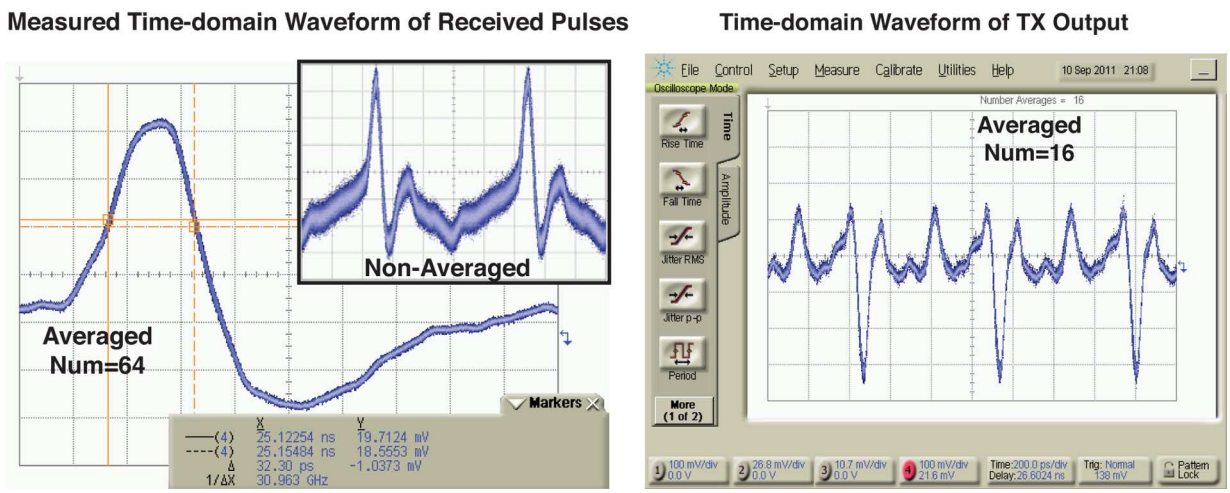


Fig. 26. Time-domain waveform reflected pulse received by RX (left). Time-domain waveform of pulse transmitted directly to an external horn antenna (right).

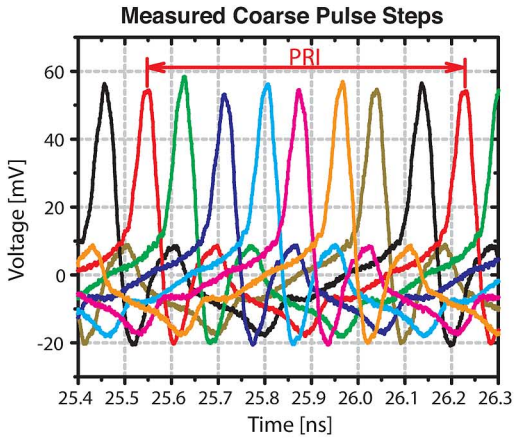
noise is -102 dBc/Hz at 1 MHz offset [33]. Measured RMS jitter of PLL (integrated from 1 KHz to 1 GHz) is below 167 fs. The total DC power consumption of the LO generation/distribution circuitry is 580 mW including biasing circuits.

When the frequency falls outside the PLL locking range, several changes are observable. In the frequency domain, the tones show a pulling behavior, as shown in Fig. 25. Here, the transceiver output (end-to-end measurements from the whole system including the TX and RX) is measured in the pulse mode. The zoomed figure shows the spectrum around 4.42 GHz (PRF is set to 1.47 GHz). This is shown for both locked and non-locked versions.

Once the PLL is locked and the carrier frequency is a multiple of the PRF, coherent integration of pulses, on each of I/Q channels independently, is made possible. To observe the output, infinite persistence mode is utilized in the sampling oscilloscope. In addition to persistence, oscilloscope averaging can be used to reduce amplitude noise. Fig. 26 shows measurements of the received pulses in TRX settings. Both averaged and non-averaged versions are shown with a PRF of 1.47 GHz. The measured pulse width can go down to $\sim$36 ps (50 % to 50 %) at which point some ringing starts to occur. Fig. 26 also shows the direct measurement of TX pulse using an external down-converter receiver.

Next, the DLL measurements are performed. As previously mentioned, these are end-to-end measurements that include the entire TRX system and the DLL control settings are adjusted to observe the timing position of the received waveform. The DLL provides both fine and coarse delay tuning. Coarse delay is achieved by observing different taps of the DLL via control of the DLL MUX. Fig. 27 shows measured time-domain waveforms for various coarse settings. As seen in the figure, the DLL provides sufficient delay range to cover the entire PRI. Furthermore, the phase can be finely tuned around each of these coarse phase settings. A list of various delay ranges that are obtainable across the PRI is included in Fig. 27.

A contiguous 290 ps tuning range is achieved by observing ϕ_7–ϕ_9 of the DLL. Two-stage interpolation is performed while each tap is sequentially observed. The last three taps are observed since redundancy is most effective for the latter stages, leading to the smallest worst-case delay jump across all taps. The measured fine-delay response was depicted in Section V-B. The delay response provides a full tuning range of 290 ps with an average step of 2.28 ps. The worst-case step is 6.8 ps and cor-



Coarse Tuning w/ Ranges

DLL Tap	Phase Range* [ps]
ϕ_2	0 - 19.2
ϕ_3	104 - 130
ϕ_4	199 - 237
ϕ_5	289 - 340
ϕ_6	386 - 455

* Referenced to ϕ_2's phase response

Fig. 27. Measured coarse delay settings (left). Coarse phase settings across various taps w/ respective tuning ranges (right). All measurements are end-to-end and include the entire TRX.

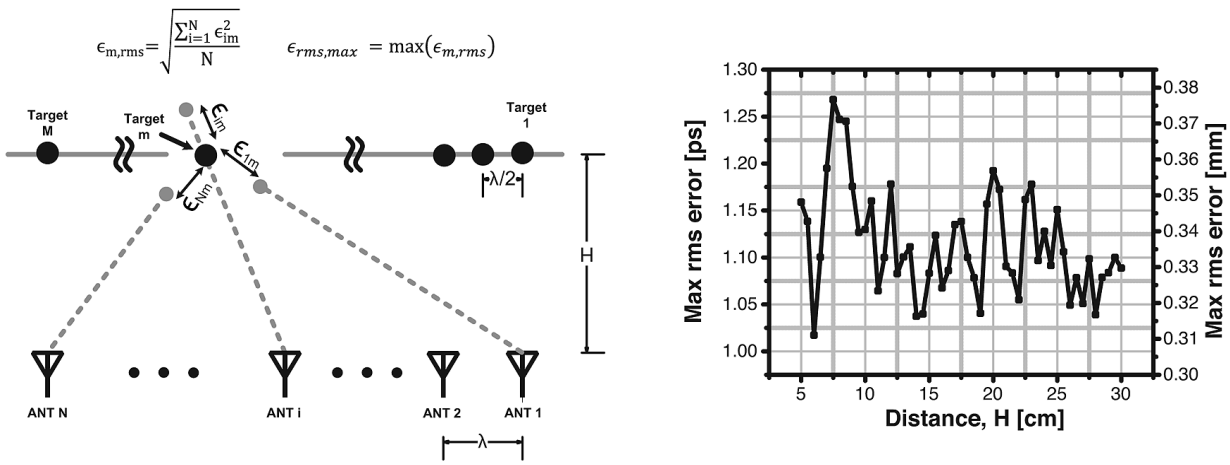


Fig. 28. Depiction of timing error due to quantized delay values (left). Plot of maximum RMS error (calculated as shown in depiction on left) versus distance to array (H). Given the 290 ps span, at each height, the maximum broadside coverage is calculated. N is selected such that size of the array is equal to the broadside coverage. N varies between 40 ($H = 5$ cm) and 77 ($H = 30$ cm) elements.

responds to the transition between taps. Redundant delay points are removed from these measurements.

Given this measured delay response, the maximum RMS error in time of arrival (TOA) of transmitted pulses was computed for a hypothetical arrayed system. Here, we assume a linear array of N antennas separated by λ transmitting to a linear array of M targets separated by $\lambda/2$ located a distance, H, away from the plane of the antennas (Fig. 28). For each target, each antenna delays its time of transmission appropriately in order to ensure coherent summation of all pulses. The time of transmission was selected from the measured phase response data of taps ϕ_7–ϕ_9. Given the quantization of available transmit pulse positions, the pulse from the ith antenna will arrive at the mth target with some error ε_{im} with respect to ideal. The RMS error at each target was computed and the maximum across all targets was recorded for a given H. A plot of this maximum RMS error as a function of the distance H is shown in Fig. 28. Given the measured delay programmability of our system, the maximum RMS error is below 1.3 ps. This equates to less than 0.39 mm RMS error in voxel size.

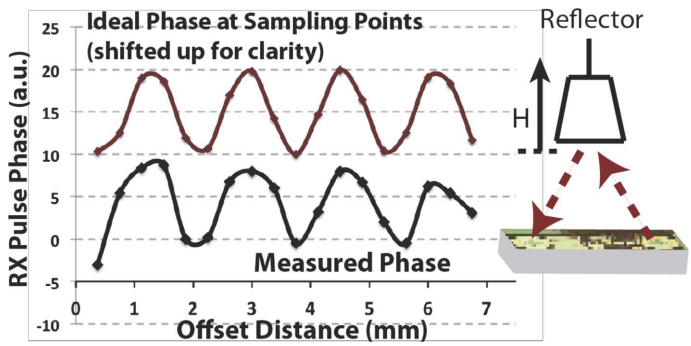


Fig. 29. Interferometric range measurements for a single target.

As previously discussed, phase coherency allows for interferometric range measurements [40]. This has direct applications in the gesture detection system in which position of hand and fingers are mapped in real time. For these measurements, a reflector is moved vertically (steps of 375 μm) above the radar element and Q channel phase of the pulse is observed (Fig. 29).

TABLE II
TRX PERFORMANCE SUMMARY

94GHz Pulsed Radar Transceiver Performance Summary		
Technology		0.13 μm SiGe BiCMOS
Area		4.4mm X 1.4mm
System Specifications	Radar Operation Mode	Pulse, variable PRF and pulse position (through DLL), Direct-Conversion (I/Q)
	PRF (nominal)	1.47 GHz (94 GHz/64)
	PRF Range	1.364 -1.519 GHz
	Min. Pulse Width	36ps (50%-50%)
	Total TRX RMS Jitter	1.2ps
	BB I/Q BW	26 GHz
	Total DC Power (including biasing)	Continuous (1.9W*), Duty-Cycle TX at 20% (1.4W)
LNA (Distributed Amplifier)	BW (-3dB)	15-110 GHz (**), (up to 125 GHz in sim)
	Gain	24 dB
	DC Power	75mA (3.3V)
I-Q Mixer/ Broadband Single to Diff.	Amp/ Phase error (Single-ended to diff)	70-110GHz: 1.2dB/ 5-7° (sim)
	Conversion loss	5-7dB (70-120GHz) (sim)
	DC Power	4mA (3.3V)
Antenna	Type	Tapered loop antenna with metal reflector
	Peak Broadside Gain	-1dB (sim)
PLL/ LO distribution	Lock Range	87.3- 97.2GHz
	CLK Spur	<-60dBc
	DC Power	152mA (3.3V), 23mA (2.5V), 17mA (1.2V)
DLL/ Pulser/ Pulse Driver	Max coarse delay	Full PRI (680ps)
	Max delay span for fine steps	290ps (avg. step=2.28ps, max step=6ps)
	DC Power	94mA (2.5V)
PA	Gain, P_{-1dB}, P_{sat}	16dB, +8dBm, +13dBm
	DC Power	80mA (4V)

* Pulse measurements performed with no duty cycling of DC power
** Measurements limited by VNA frequency range
*** All DC currents of major blocks are programmable by combination of 4-bit DACs

For reference, calculated phase is also shown (moved up vertically for clarity). Single-target range resolution of better than 375 μm is observed (limited by mechanical stepper resolution). Table II summarizes the performance of the radar transceiver.

IX. CONCLUSION

A fully integrated mm-wave-to-baseband pulsed-radar is integrated in 0.13 μm SiGe BiCMOS technology. Phase-coherency, obtained with a DLL-PLL combination, allows for interferometry and long-term averaging before digitization and I/Q combination. TX-beamforming is supported using a DLL structure with embedded phase interpolation inside the loop. The receiver front-end, including a distributed amplifier, active balun, quadrature mixer, and baseband gain stages, provides the highest reported bandwidth for coherent mm-wave receivers in silicon. System measurements include the complete transmit-receive chain and show pulse position tunability across the PRI, center frequency lock range of 87–97 GHz, and phase coherency for interferometric range measurements with better than 375 μm resolution (limited by mechanical stepper). The proposed array architecture eliminates any RF or IF phase shifting or combining and simplifies scaling to larger number of nodes. The future steps include pulsed array measurements with larger number of elements integrated on the board.

ACKNOWLEDGMENT

The authors thank Bagher Afshar, Jun-Chau Chien, Juan Yaquian, and Yasin Aalipour for their contributions. The contributions of the sponsors of the Berkeley Wireless Research Center (BWRC), the National Science Foundation, Intel Foundation, Qualcomm Inc., and the foundry donation of STMicroelectronics is acknowledged. Special thanks go to E. Adabi, A. Wu, A. Pai, D. Gloria, B. Richards, S. Mellers, A. Tassoudji, B. Sun, and N. Saiz.

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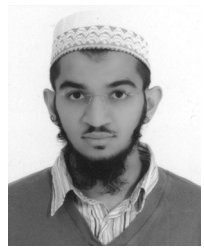

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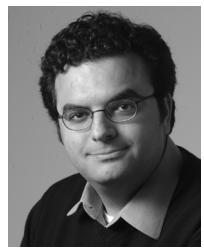

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