60-GHz Four-Element Phased-Array Transmit/Receive System-in-Package Using Phase Compensation Techniques in 65-nm Flip-Chip CMOS Process

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***Abstract*—AThe 60-GHz four-element phased-array transmit/receive (TX/RX) system-in-package antenna modules with phase-compensated techniques in 65-nm CMOS technology are presented. The design is based on the all-RF architecture with 4-bit RF switched *LC* phase shifters, phase compensated variable gain amplifier (VGA), 4:1 Wilkinson power combining/dividing network, variable-gain low-noise amplifier, power amplifier, 6-bit unary digital-to-analog converter, bias circuit, electrostatic discharge protection, and digital control interface (DCI). The 2×2 TX/RX phased arrays have been packaged with four antennas in low-temperature co-fired ceramic modules through flip-chip bonding and underfill process, and phased-array beam steering have been demonstrated. The entire beam-steering functions are digitally controllable, and individual registers are integrated at each front-end to enable beam steering through the DCI. The four-element TX array results in an output $P_{1\,\mathrm{dB}}$ of 5 dBm per channel. The four-element RX array results in an average gain of 25 dB per channel. The four-element array consumes 400 mW in TX and 180 mW in RX and occupies an area of 3.74 mm^2 in the TX integrated circuit (IC) and 4.18 mm^2 in the RX IC. The beam-steering measurement results show acceptable agreement of the synthesized and measured array pattern.**

***Index Terms*—Beamforming, CMOS, flip-chip, phased array, phase-compensated techniques, 60 GHz, system-in-package (SiP), variable gain amplifier (VGA), wireless communication.**

I. Introduction

PHASED-ARRAY systems play an important role in 60-GHz wireless applications, such as WirelessHD, WiGig (The Wireless Gigabit Alliance Website. [Online]. Available: http://wirelessgigabitalliance.org/), IEEE 802.15.3c, and IEEE 802.11ad standards [1]–[3] due to the benefits of improvement in signal-to-noise ratio (SNR), equivalent isotropically radiated power (EIRP), spatial interference cancellation, and wider channel bandwidth. There are several different types of phased arrays, also called beamformers, which can be classified into time, frequency, and spatial domains, as shown in Fig. 1. Each of them has distinct features. Time-domain beamformers perform the desired functions by time-based operations [4]–[10]. In narrowband systems, the "phase shift" is equivalent to a time delay, but unfortunately phase scanned arrays are not suitable for broadband operation. At different frequencies, the same phase shift corresponds to different time delays and causes different angles of wave propagation. Therefore, the same phase shift across the desired frequency band results in the beam direction to vary with frequency. The electrical spacing (d/λ) between array elements also increases with frequency, and therefore, phase scanning is frequency sensitive. In order to keep the group delay over such a wide bandwidth, the phase compensated variable gain amplifier (VGA) can be used to compensate this phenomenon. Frequency-domain beamformers steer the beam directions by controlling the frequency [11]. At one particular frequency, the radiated waves of all sub-elements are in phase at the desired direction. Such frequency-scanning systems are relatively simple and inexpensive to implement. The frequency, rather than the phase, may be adjusted by the control circuits to bring the frequency-sensitive characteristics of phase scanning. The frequency is very important in scanning. Spatially orthogonal

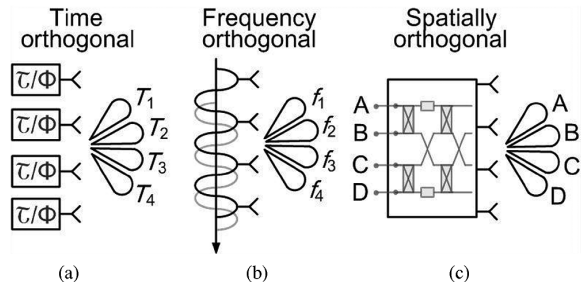

Fig. 1. Classification of scanning techniques. (a) Time-domain beamformer. (b) Frequency-domain beamformer. (c) Spatial-domain beamformer.

Manuscript received October 18, 2011; accepted October 27, 2011. Date of publication January 17, 2012; date of current version March 02, 2012. This work was supported in part by the National Science Council of Taiwan under Contract NSC 99-2219-E-002-005, Contract NSC 99-2219-E-002-010, and Contract NSC 98-2221-E-002-059-MY3, under Excellent Research Projects of National Taiwan University (99R80302), and under the MediaTek-NTU 60-GHz Project (98-S-C12).

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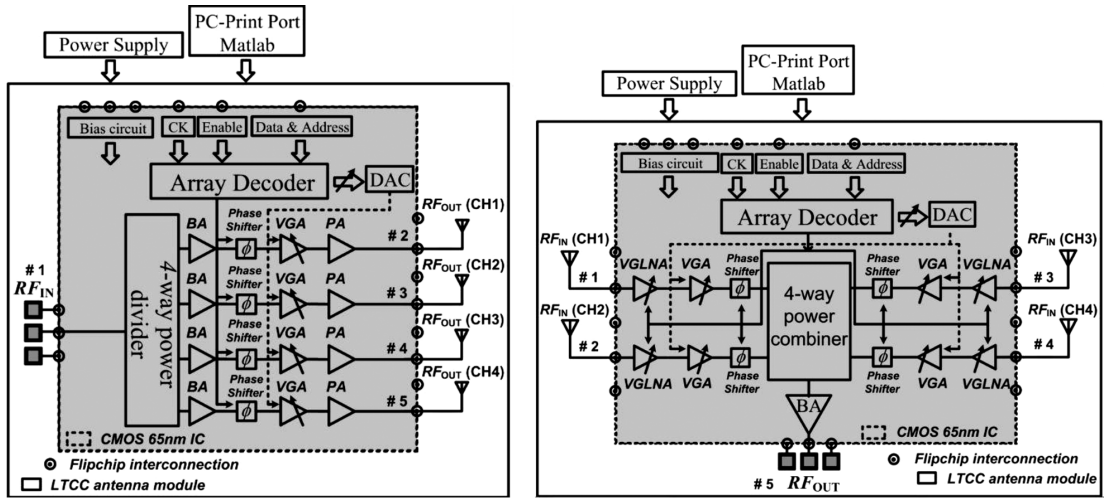
Digital Object Identifier 10.1109/TMTT.2011.2176508



(a) (b)

Fig. 2. Four-element phased-array transmitter/receiver module architecture. (a) Transmitter. (b) Receiver.

beamforming techniques generate multiple fixed directional beams by using the Butler matrix [12]–[14]. The Butler matrix is generally composed of passive components such that it consumes zero dc power consumption, but it suffers from the low spatial resolution due to only discrete beams generated by the Butler matrix.

In this paper, we develop a pair of wideband phased-array transmit/receive (TX/RX) SiP antenna modules. The mechanism of the phase compensated technique is described in detail. The system-level design considerations and the overall TX/RX architecture are also addressed. To the authors' knowledge, this is the first V-band phased-array TX/RX SiP antenna modules with phase compensated VGA technique. Using the switched LC phase shifter and phase compensated VGA, the beam direction of the phased array can be controlled. The beam-steering measurement results show acceptable agreement of synthesized and measured array pattern.

II. System-Level Design Considerations

Fig. 2 shows the block diagram of the proposed 60-GHz four-element phased-array TX/RX SiP antenna modules with phase-compensated techniques. The TX/RX SiP modules were designed and implemented in TSMC 65-nm 1P9M CMOS technology [15]. The Wilkinson power divider/combiner is used to divide/combine signals to/from one/four paths, but it suffers from the high loss of the CMOS substrate. Therefore, buffer amplifiers (BAs) are added to provide enough gain and power. However, more paths of digital control lines and dc bias are required in larger phased-array systems, which are complicated, and more metal layers are needed. The reported Wilkinson power divider/combiners consist of lumped-element [16], which is used to replace the quarter-wavelength for reducing chip size, but suffers from dc and digital control line routing. Therefore, we have modified the traditional design in our work. Fig. 3 shows the metal-stack layers of the TSMC 65-nm 1P9M CMOS process that is used for the Wilkinson power divider/combiner. Because of using the thin-film microstrip (TFMS) lines, it is easier to modify the ground plane

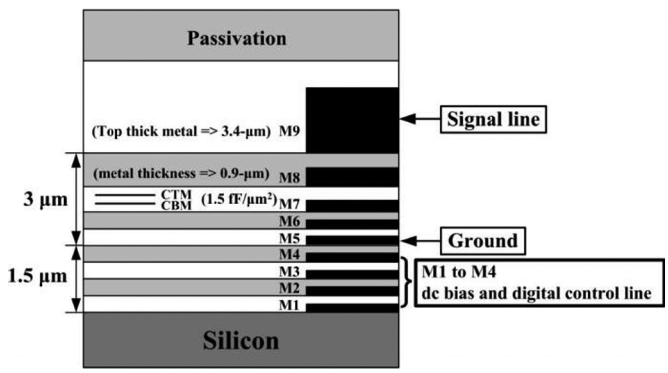


Fig. 3. Metal-stack layers of the TSMC 65-nm 1P9M CMOS process, which is used in a Wilkinson power divider/combiner.

from metal 1 to metal 5. The metal layers 1 to 4 can be used in the dc routes and digital control, and thus the complicated routes of dc bias and digital control can be simplified. The TFMS line loss (500-μm long) is below 0.5 dB at 60 GHz, and the quality factor is about 10 at 60 GHz.

The switched LC phase shifter is frequently used in a phased-array system due to the advantage of digital control [17]. Since the switch on/off is controlled by digital voltage 1/0 V, it does not need a digital-to-analog converter (DAC). Moreover, it has a wider frequency range of constant phase shift than other passive phase shifters, such as reflection-type phase shifter and tunable artificial transmission line phase shifter. However, the switched LC phase shifter suffers from large switching loss at high frequencies. The losses in different phase states are not the same, and thus cause the amplitude imbalance. To minimize the amplitude imbalance of the switched LC phase shifter, a VGA can be cascaded with the phase shifter to compensate the different loss in each state. When the VGA provides different gain to compensate for the loss, the insertion phases of the VGA will also be changed. Therefore, it is difficult to achieve low root-mean-square (rms) phase error and low rms gain error simultaneously. In this design, a switched LC phase shifter using a VGA with a new phase compensation technique is presented.

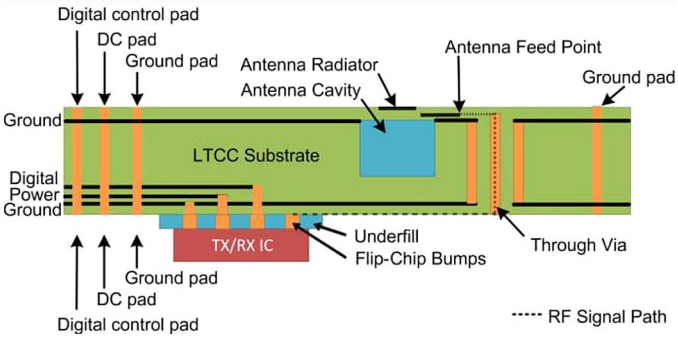


Fig. 4. Layer profile for the 60-GHz LTCC SiP module.

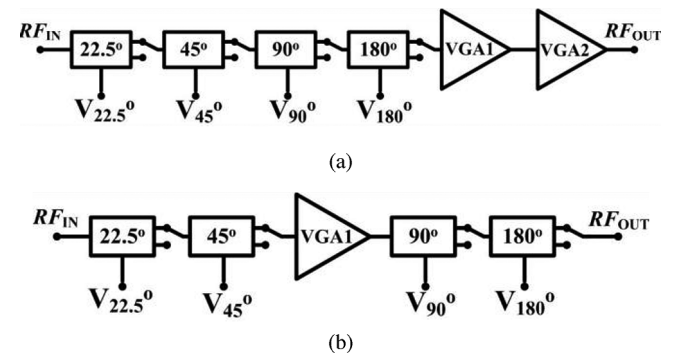


Fig. 5. Block diagram of the switched *LC* phase shifter with VGA. (a) Switched *LC* phase shifter and VGA in transmitter. (b) Switched *LC* phase shifter and VGA in receiver.

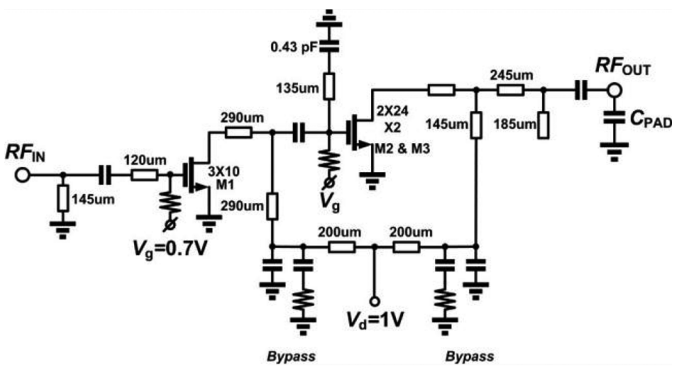


Fig. 6. Schematic of the PA.

Six-bit unary DACs are used to control the gain setting of the VGA. The bias circuits are partitioned into global and local bias, which is to minimize the number of interconnected nets between the bias circuits and circuit blocks in the chip. The digital control interface (DCI) is used to control the bias, DAC, gain setting of variable gain low noise amplifier (VGLNA), and the state of the phase shifter for all circuits in the array. Even the power-down controls at each element are also controlled by the DCI. The DCI provides configuration and control of the chip operation through a set of registers. The external access (reset, writing, and reading) of these registers are through a serial to parallel bus.

Fig. 4 shows the layer profile for the 60-GHz LTCC SiP module. An integrated circuit (IC) and antenna are placed on the opposite sides of the LTCC substrate. The RF signal is transmitted from the IC through the LTCC substrate to the antenna. The chip is first bonded to a multilayer LTCC substrate through flip-chip bonding. Liquid underfill is then dispensed into the gap among the solder bumps. As the dispensed underfill is cured, the solder bumps can be protected from being overstressed during thermal loading, thus increasing solder bump reliability [18].

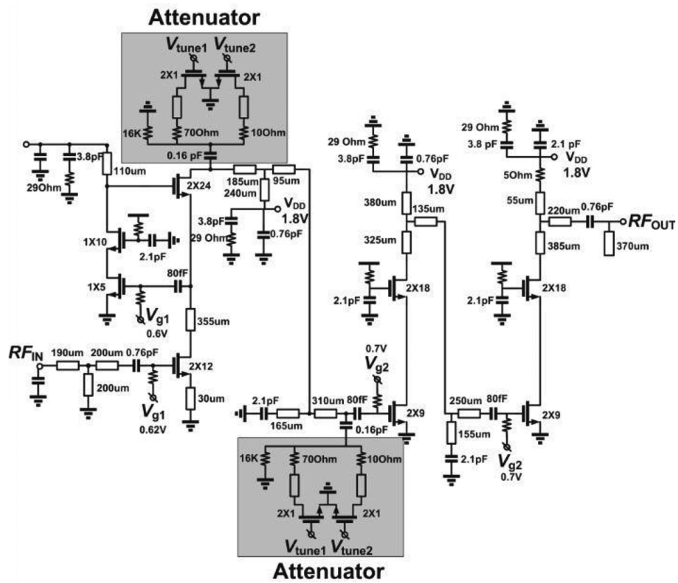


Fig. 7. Schematic of the VGLNA.

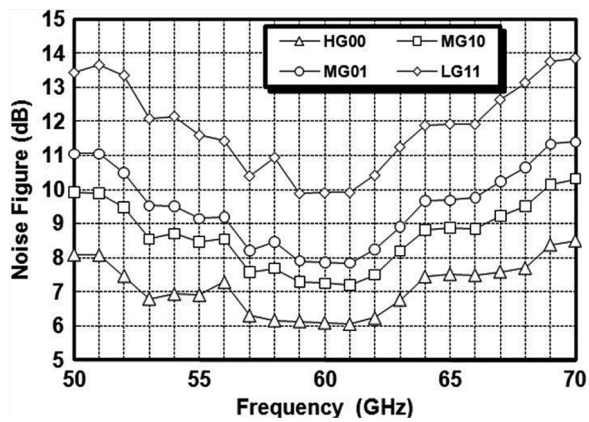


Fig. 8. Measured NF of the VGLNA.

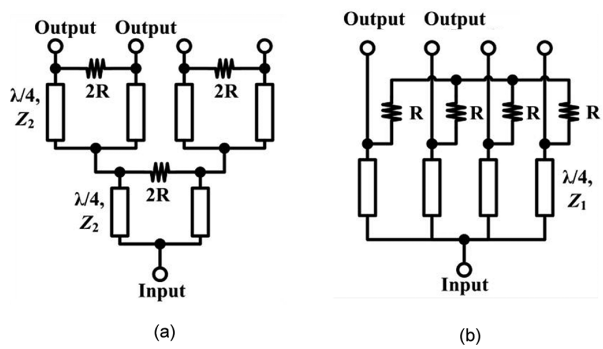


Fig. 9. Topologies of Wilkinson power distribution network. (a) Three of 1-to-2 Wilkinson power dividers are used and cascaded. (b) Directly 1-to-4 Wilkinson power divider.

A. Transmitter Module

As shown in Fig. 2(a), the four-element 60-GHz CMOS phased-array transmitter consists of a 1:4 Wilkinson power

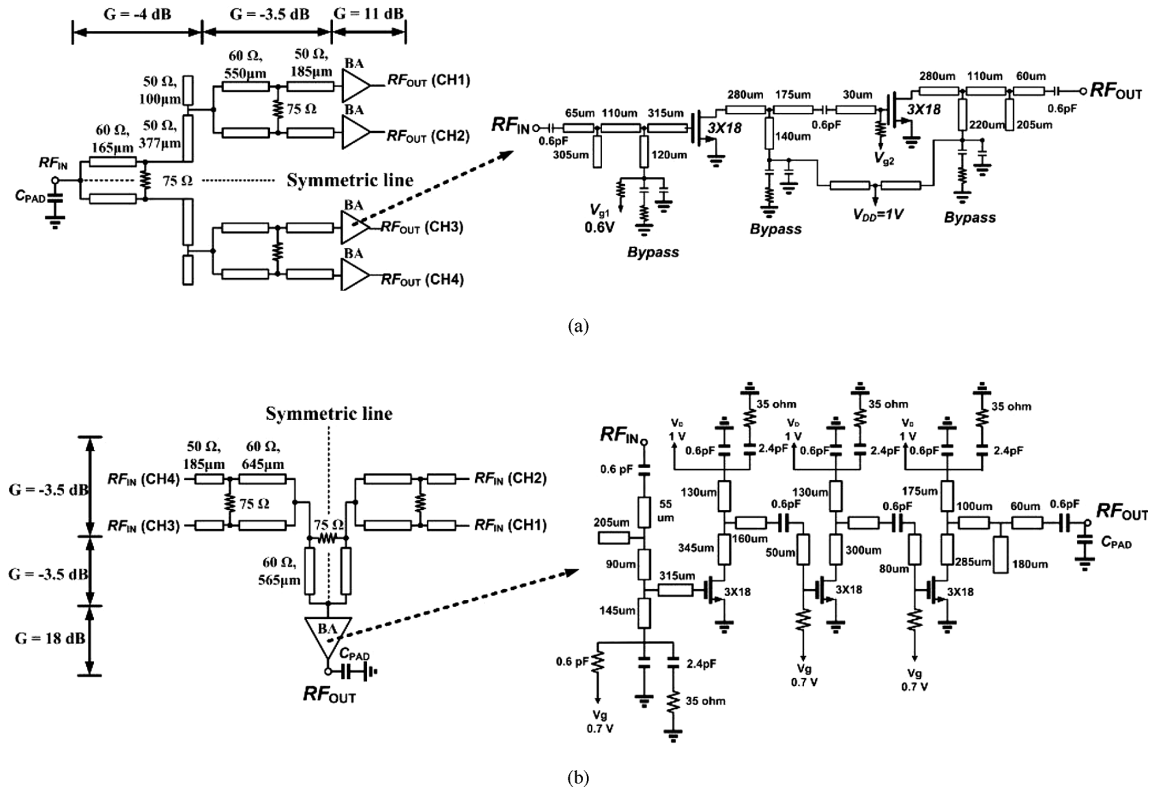


Fig. 10. Schematic of the Wilkinson power distribution network. (a) Transmitter. (b) Receiver.

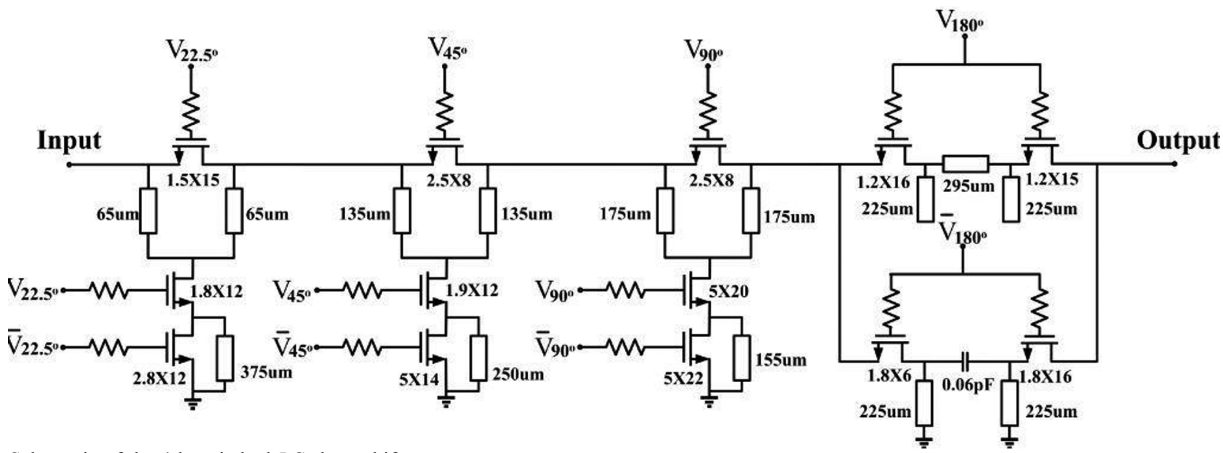


Fig. 11. Schematic of the 4-b switched *LC* phase shifter.

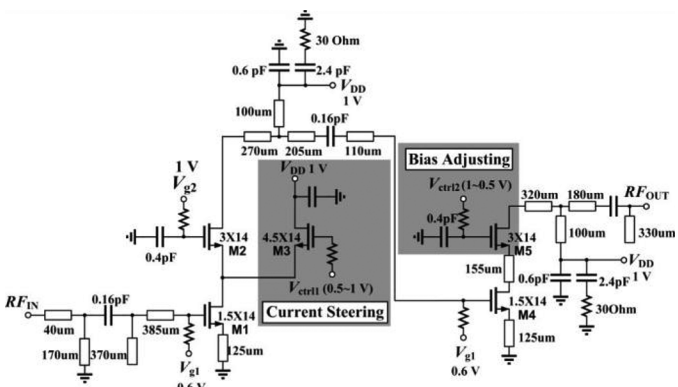


Fig. 12. Schematic of the phase-compensated VGA1.

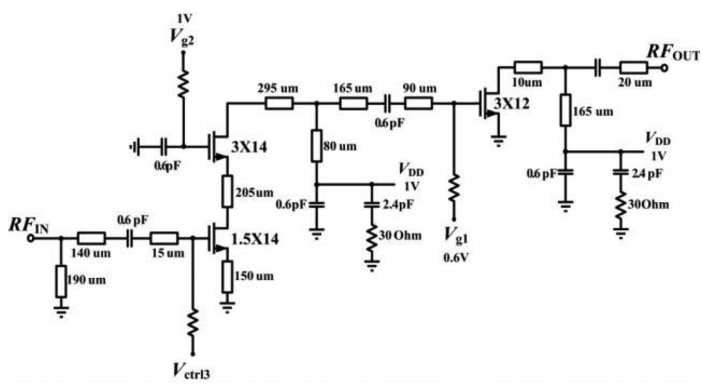


Fig. 13. Schematic of the VGA2.

dividing network, 4-bit RF switched *LC* phase shifter, phase compensated VGA, power amplifier (PA), 6-bit unary DAC, bias circuit, and DCI. They have been packaged through the flip-chip technique with four antennas in a low-temperature co-fired ceramic (LTCC) module. Fig. 5(a) shows the block diagram of the switched *LC* phase shifter with VGA. Due to

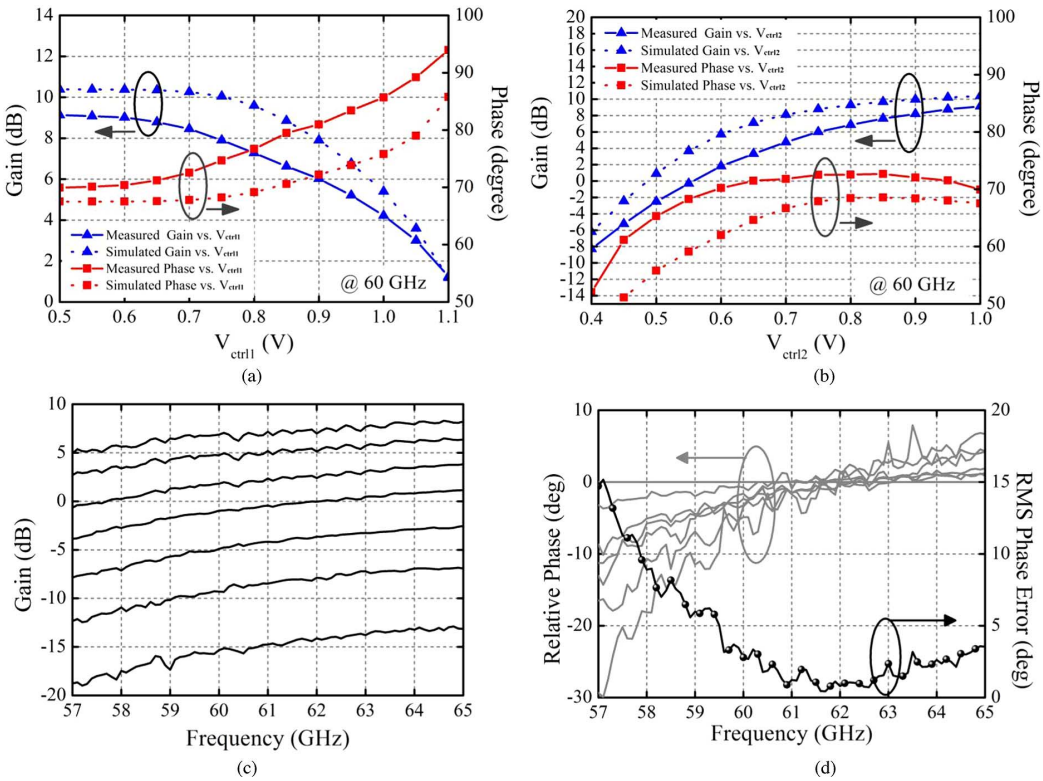


Fig. 14. Gain and phase performance of the phase-compensated VGA. (a) In current steering stage versus $V_{\mathrm{ctrl}1}$. (b) In bias adjusting stage versus $V_{\mathrm{ctrl}2}$. (c) Measured gain in different gain state. (d) Measured relative phase and rms phase error in different gain state.

the RF phase-shifting architecture, the loss is high for each RF path. Therefore, four BAs, which are located between the Wilkinson power divider and phase shifter, are used to provide enough gain and output power. The four BAs and Wilkinson power splitter are co-designed together since the BAs are cascaded to the output of the power divider. After adjusting the phase in each path with the phase shifters, the four signal paths are combined at RF frequency. This architecture takes advantage of low power consumption and small chip size since the RF phase-shifting phased array has a minimum number of components. A VGA cascaded with the phase shifter to compensate the different loss in each state is also co-designed. The PA is placed as the last stage of the front-end in the transmitter. Using the phased-array system can improve EIRP and reduce the output power requirement in the transmitter [19].

B. Receiver Module

As shown in Fig. 2(b), the phase shifting circuit of the receiver is the same in the transmitter. The RX chip consists of a VGLNA, 4-bit RF switched *LC* phase shifter, phase compensated VGA, 4:1 Wilkinson power combining network, 6-bit unary DAC, bias circuit, and DCI. They are also packaged using flip-chip techniques with four antennas in an LTCC module. A low-noise amplifier (LNA) incorporated with a variable gain stage is used in the receiver system to improve the sensitivity and dynamic range of the receiver, and thus the total chip size and power consumption can be minimized at the same time. A switched *LC* phase shifter and phase compensated VGA are also used in the RX design. Fig. 5(b) shows the block diagram of the switched *LC* phase shifter with the VGA. Since the VGLNA has enough gain, the switched *LC* phase shifter and VGA are swapped to enhance the RX linearity without degrading the noise performance. A BA at the output of Wilkinson power combiner is added to provide enough gain and output power.

III. Individual Functional Block Design

In the TX/RX SiP modules, all of the on-chip matching networks, including the metal–insulator–metal (MIM) capacitors, pad parasitic capacitance, and TFMS lines were simulated using a full-wave electromagnetic (EM) simulator (Sonnet 11.52) [20]. The via transition, flip-chip compensation, and four-element antenna array on LTCC were simulated using the High-Frequency Structure Simulator (HFSS) [21]. The complete circuit was then simulated using the Advanced Design System (ADS 2010) [22].

A. TX PA

Fig. 6 shows the schematic diagram of the PA, which is designed to deliver the maximum power from the device with a power consumption of 50 mW [23]. The amplifier consists of two stages of common source devices with input, output, and inter-stage matching networks. In order to achieve maximum output power, the transistors (M2, M3) directly combined in the second stage are selected as 24 fingers with each finger length of 2 μm. In order to achieve higher power-added efficiency (PAE), the transistors (M1) in the first stage are ten fingers with each finger width of 3 μm. Since the CMOS PA operates in a high voltage swing, the output matching network is designed for maximum output power, and the inter-stage and input matching networks are designed for gain and input return loss. All of the

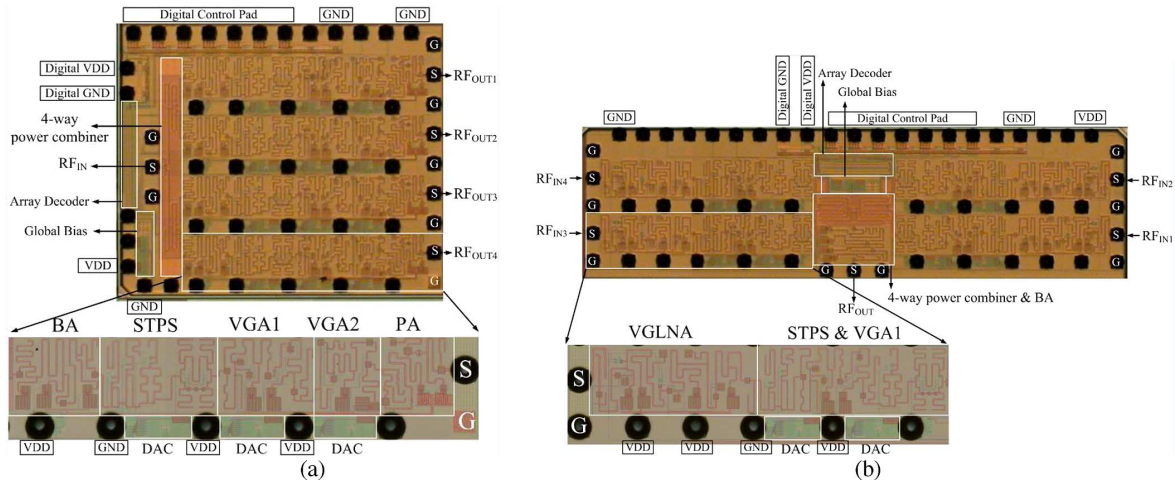


Fig. 15. Die photograph of the four-element CMOS phased array IC. (a) Transmitter (area = 3.74 mm^2). (b) Receiver (area = 4.18 mm^2).

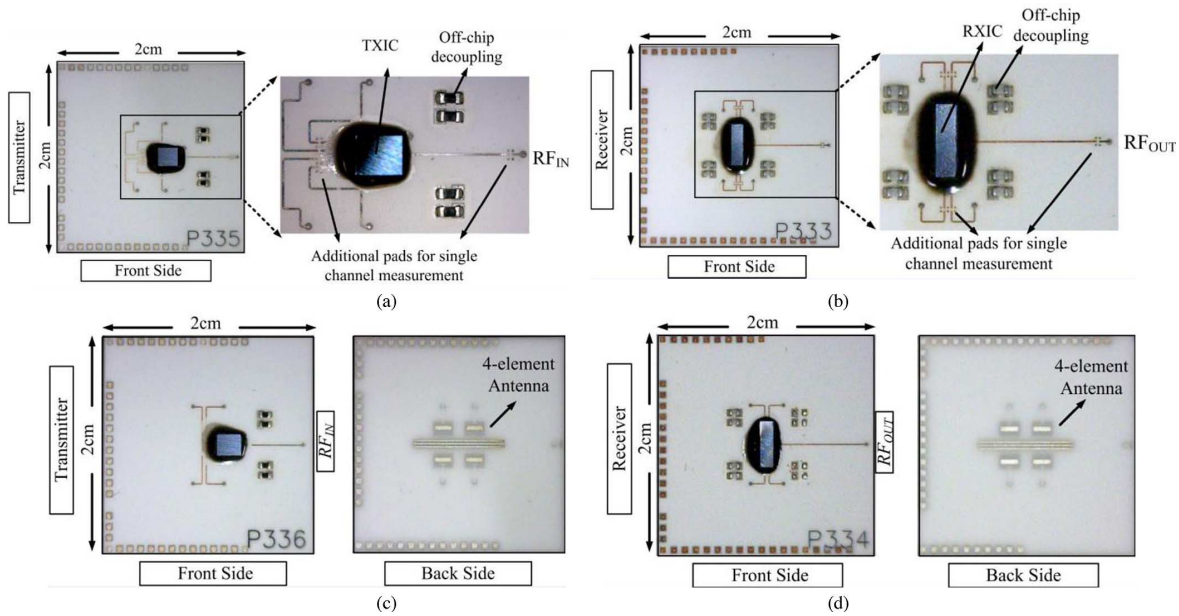


Fig. 16. Photograph of the LTCC SiP module with TX/RX IC and four antennas. (a) For single-channel TX measurement. (b) For single-channel RX measurement. (c) For TX array pattern measurement. (d) For RX array pattern measurement.

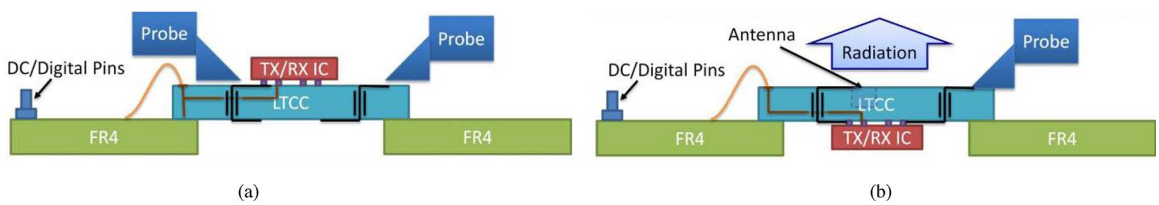


Fig. 17. Experimental setup. (a) Single-channel and (b) array pattern measurement of the TX/RX module.

gates are biased via local bias circuit. This PA is operated at class-A to compromise with output power and linearity. The PA consumes 50 mA from 1-V supply.

B. RX VGLNA

Fig. 7 shows the schematic of the VGLNA circuit. The design methodology of the CMOS VGLNA in [24] is applied here. In the high gain mode, the noise figure (NF) and power consumption are as low as possible. It also needs acceptable NF, better third-order intermodulation intercept point (IIP3), and return loss for the dynamic-range specification in the low gain mode operation. To achieve a higher gain with a minimum NF for the cascaded LNA, a cascode amplifier with a positive feedback [25] is employed as the first stage in this design. In order not to degrade the noise performance, two identical attenuator cells with two digital control bits are incorporated in the matching network between the first and the second stage rather than in the input of the VGLNA. On the other hand, the attenuators effectively suppress the incident power level for the second and the third stages, leading to the improvement of linearity in the

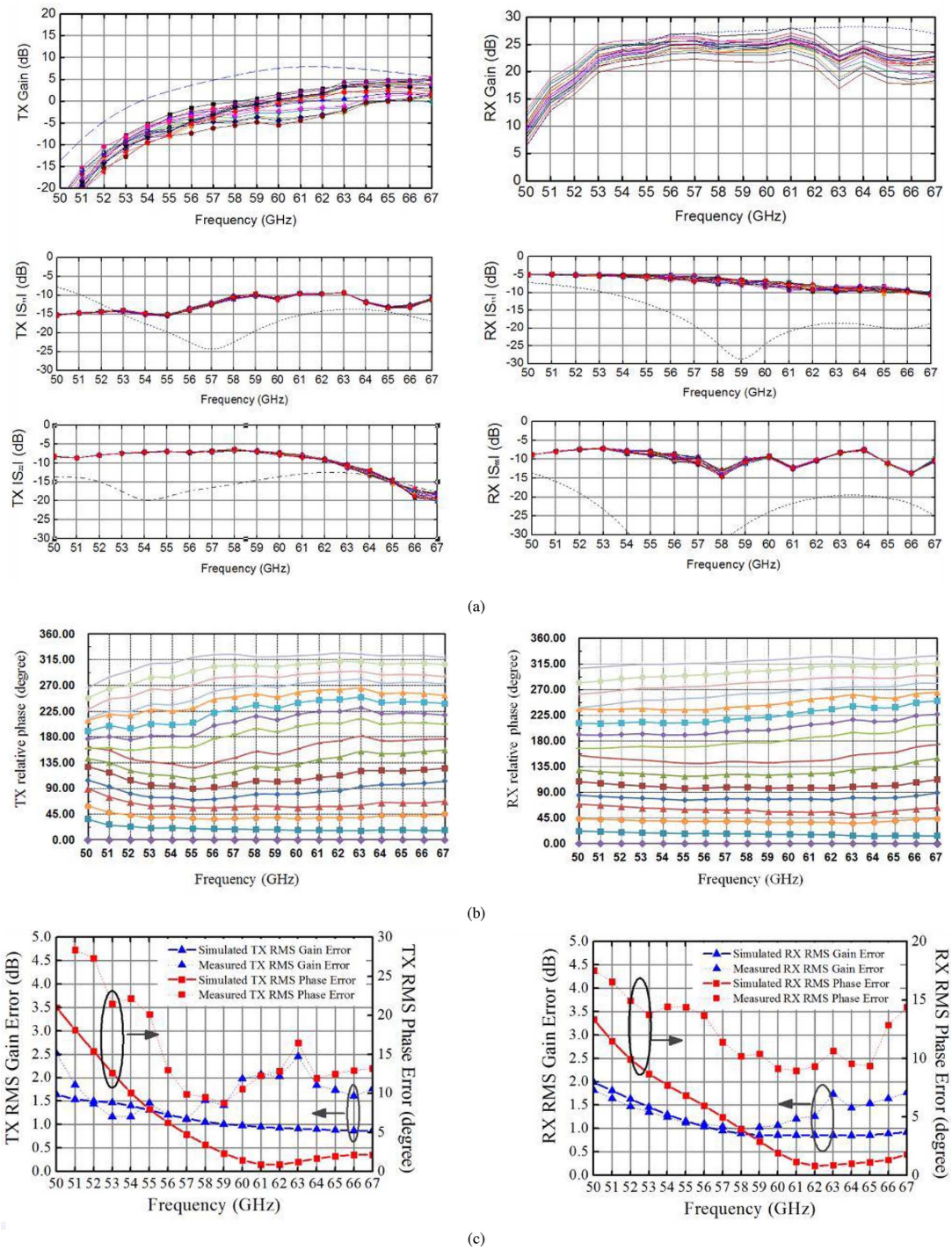


Fig. 18. Simulated (dashed lines) and measured (solid lines) TX/RX single path (CH-1) characteristics for the 16 states. (a) S-parameters. (b) Relative phases. (c) RMS gain/phase error (reference: 0°-bit phase state).

medium- and low-gain mode. The matching networks are also realized by the thin-film microstrip (TFMS) lines, which are routed compactly to minimize the chip area. The measured NF is shown in Fig. 8. In the high-gain mode, the LNA exhibits a measured minimum NF of 6 dB at 61 GHz. The VGLNA consumes 20 mA from 1.8-V supply.

C. Four-Way Wilkinson Power Dividers/Combiners and BA

Fig. 9 shows two topologies that can be used to implement the Wilkinson power distribution network [26]. One is cascading three 1-to-2 Wilkinson power dividers [see Fig. 9(a)]. The other directly implements a 1-to-4 Wilkinson power divider [see Fig. 9(b)]. When characteristic impedance is 50 Ω, Z_1 is equal to 100 Ω. However, according to design rules of the minimum 2-μm-wide line, the maximum available characteristic impedance is 72 Ω. Hence, the directly 1-to-4 Wilkinson power divider cannot be implemented in the 65-nm CMOS process. Although the characteristic impedance with 72 Ω can be implemented with a 2-μm-wide line, the minimum line width should be avoided in the design. Therefore, 4-μm-wide TFMS line is

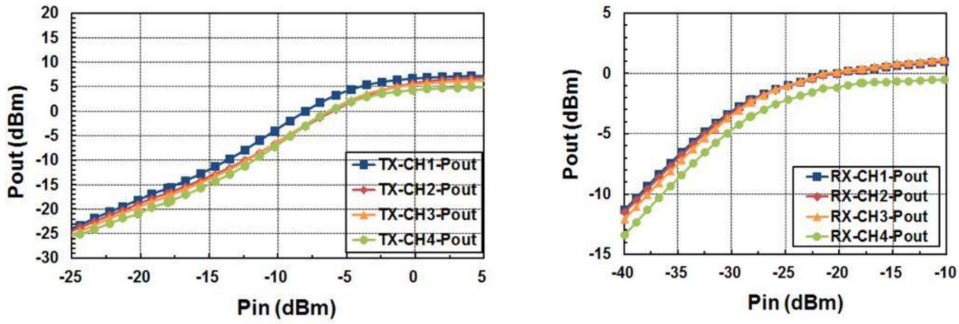


Fig. 19. Measured TX and RX single path power performance (CH1-CH4).

selected for the quarter-wavelength lines. The Wilkinson power divider/combiner is designed for the 42-Ω system in order that the characteristic impedance of the quarter-wavelength line is 60 Ω. Since the system impedance of RF circuits is usually 50 Ω, a simple matching network is used to transform 42 Ω to 50 Ω. Besides, the size of the Wilkinson power divider can be reduced by using capacitive loading. Therefore, the matching network utilizes an open stub to reduce the size and insertion loss of the power divider/combiner.

Fig. 10(a) shows the schematic of 1-to-4 Wilkinson power divider with a buffer. The 1-to-4 power divider with a two-stage common source amplifier operates across a wide frequency range from 57 to 66 GHz. The simulated gain of each RF path of the 1-to-4 power distribution network is higher than 3 dB, and the simulated isolation between two adjacent output ports is better than 35 dB. The 1-to-4 power distribution network consumes 40 mA from a 1-V supply voltage. Fig. 10(b) shows the schematic of 4-to-1 Wilkinson power combiner with a buffer. The 4-to-1 power combiner with a three-stage BA has a bandwidth of 57–66 GHz. The simulated gain of each RF path of the power distribution network is better than 11 dB, and the simulated isolation between the two adjacent input ports is better than 24 dB. The 4-to-1 power distribution network consumes 20 mA from 1-V supply.

D. 4-bit Switched LC Phase Shifter and Phase-Compensated VGA

Fig. 11 is the block diagram of switched *LC* phase shifter, which can be controlled by digital signals and has been often used in phased-array systems. A 4-bit switched *LC* phase shifter contains four stages since the switch on/off can be controlled by the DCI. Switching the high- and low-pass networks by the switch pair can accomplish phase shift; however, the area will be large due to the high- and low-pass networks. In addition, the on resistance of the switching pair will cause high loss. In order to reduce the area, the high-/low-pass networks are combined together. Since the four stages are cascaded, the impedance mismatch may result in the reflection between each stage, and thus the phase variation. In order to prevent the impedance mismatch from each other, all stages are matched to Z_0. Fig. 12 shows the proposed phase compensated VGA1. The 6-bit unary DAC is used to control the gain setting ($V_{\mathrm{ctrl}\,1}$ and $V_{\mathrm{ctrl}\,2}$) of the VGA. Fig. 13 shows the schematic of VGA2. Again, VGA2 is added to provide enough gain and output power. The current steering

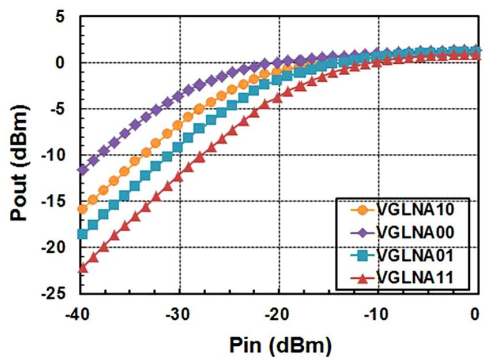


Fig. 20. Measured power performance of the CH-1 RX at four different modes of VGLNA. (“10”: medium gain, “00”: high gain, “01”: medium gain, “11”: low gain).

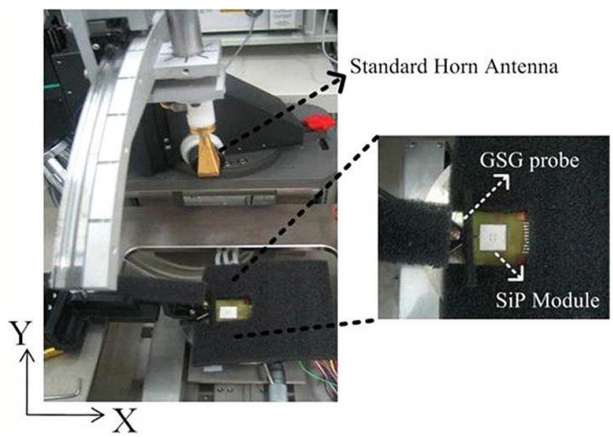
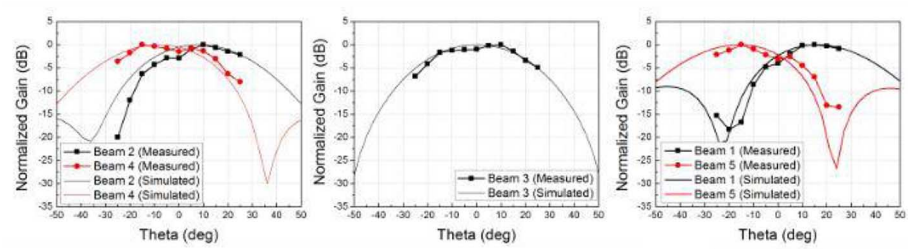


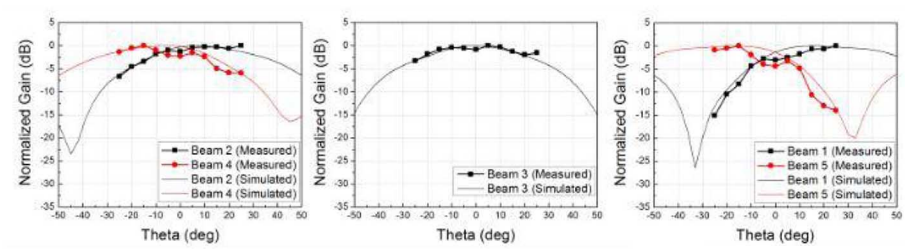
Fig. 21. Photograph of pattern measurements.

circuit [27] is composed of a cascode device (M1, M2) and a current steering device (M3). In the highest gain operation, $V_{\mathrm{ctrl}\,1}$ is set to 0 V, so M3 is turned off, so that the current in M3 is zero and in M2 is maximum. When $V_{\mathrm{ctrl}\,1}$ is increased, the current of M3 increases and the current of M2 decreases. The g_m in the cascode device decreases accordingly, and thus causes an increase in phase. The bias adjusting circuit [28] includes another cascode device (M4, M5). When $V_{\mathrm{ctrl}\,2}$ is decreased, the current of M4 and M5 drop. The gain will decrease and result in a decreasing phase. Using the proposed phase-compensated VGA, the gain imbalance of the switched *LC* phase shifter can be minimized without increasing the phase error.



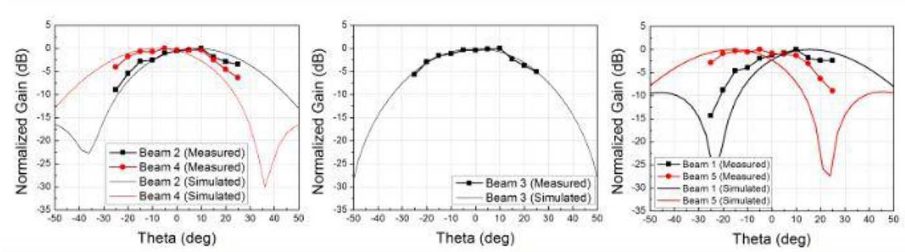
Beam	Scan Angle θ	CH-1	CH-2	CH-3	CH-4
#1	+25°	180°	90°	270°	0°
#2	+12°	180°	135°	315°	0°
#3	0°	180°	180°	0°	0°
#4	-12°	180°	225°	45°	0°
#5	-25°	180°	270°	90°	0°

(a)



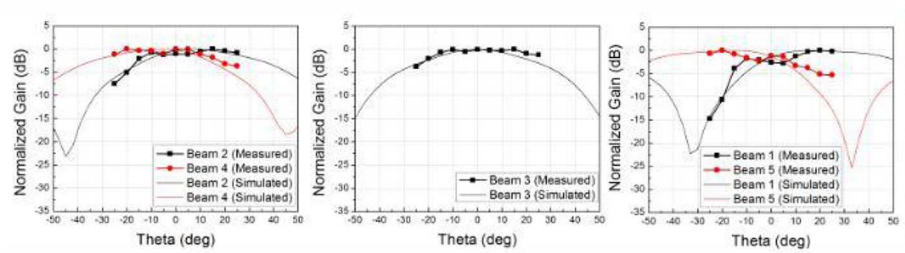
Beam	Scan Angle θ	CH-1	CH-2	CH-3	CH-4
#1	+25°	180°	180°	90°	90°
#2	+12°	180°	180°	45°	45°
#3	0°	180°	180°	0°	0°
#4	-12°	180°	180°	315°	315°
#5	-25°	180°	180°	270°	270°

(b)



Beam	Scan Angle θ	CH-1	CH-2	CH-3	CH-4
#1	+25°	0°	270°	180°	90°
#2	+12°	0°	315°	180°	135°
#3	0°	0°	0°	180°	180°
#4	-12°	0°	45°	180°	225°
#5	-25°	0°	90°	180°	270°

(c)



Beam	Scan Angle θ	CH-1	CH-2	CH-3	CH-4
#1	+25°	90°	90°	180°	180°
#2	+12°	45°	45°	180°	180°
#3	0°	0°	0°	180°	180°
#4	-12°	315°	315°	180°	180°
#5	-25°	270°	270°	180°	180°

(d)

Fig. 22. Measured and synthesized beam patterns at 61 GHz. (a) TX–XZ-plane. (b) TX–YZ-plane. (c) RX–XZ-plane. (d) RX–YZ-plane.

Fig. 14 presents the mechanism of the phase-compensation VGA. Fig. 14(a) and (b) shows the simulated and measured gain and phase of the VGA at 60 GHz versus $V_{\mathrm{ctrl}1}$ and $V_{\mathrm{ctrl}2}$, respectively. From the measurement results, the phase change by sweeping $V_{\mathrm{ctrl}1}$ and $V_{\mathrm{ctrl}2}$ will cancel each other unless $V_{\mathrm{ctrl}2}$ is larger than 0.7 V since the phase will be decreased, as shown in Fig. 14(b). It is observed that the phase of the current steering stage and bias adjusting stage are varying oppositely when the gain is decreased. Therefore, the phase compensation is achieved by the current steering and bias adjusting technique simultaneously.

Fig. 14(c) shows the measured gain of the phase-compensated VGA in different gain state and Fig. 14(d) shows the corresponding phase response and the rms phase error. The measured gain in the highest gain state is 7 dB from 60 to 65 GHz. The measured gain variation range is from -15 to 7 dB at 60 GHz with the absolute phase error is under 7.5°, and the rms phase error is less than 3.5°. Therefore, the phase-compensated VGA can achieve low phase variation in different gain state.

IV. Experimental Setup and Beam-Steering Measurement

The phased-array TX/RX IC is realized in TSMC 65-nm 1P9M flip-chip CMOS technology. It has an area of 3.74 mm^2 for TX and 4.18 mm^2 for RX, and the photographs of the ICs are shown in Fig. 15. The ground–signal–ground (GSG) dimensions for RF I/O is 200 μm. The bump height after flip-chip bonding is 55 μm and the dielectric constant of the underfill is 3.5. A flip-chip interface and underfill process are used to reduce the loss and variation compared with wire bondings. Four cavity-backed rectangular slot loop antenna are implemented on an LTCC process. Fig. 16(a) and (b) are the TX and RX SiP modules with additional testing pads to investigate the single-channel TX and RX performance. We also added

TABLE I
CURRENT STATE OF THE ART PHASED-ARRAY TRANSMITTER AND RECEIVER AROUND 60 GHz

Ref.	A. Valdes-Garcia JSSC2010 [20]	A. Natarajan JSSC2011 [10]	S. Emami, ISSCC2011 [5]	M. Tabesh, ISSCC2011 [6]	E. Cohen, TMTT2010 [9]	W. L. Chan, ISSCC2010 [31]	S. Kishimoto, RFIC2009 [33]	This work	
Technology	120nm SiGe BiCMOS	120nm SiGe BiCMOS	65nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	
Function	TX	RX	TRX	TRX	TRX	TX	TX	TX	RX
# of elements	16	16	32+4/32+8	4	4	4	6	4	4
phase shifting	Passive RF	Passive RF	RF	Active BB	Passive RF	Active LO	Passive BB	Passive RF	Passive RF
freq. (GHz)	51-65	57-66	60	59-62.5	56.6-59.5	56	60.48	57-66	57-62
Gain (dB)	30-34	68-71	N.A	24	7/7.5	20	15	0	25
P_{sat}/element (dBm)	N.A.	N.A.	N.A	-2	3.5/N.A	11	6	7	1.8
P_{1dB}/element (dBm)	9-13.5.	-1	9/N.A	N.A	-0.5/N.A	7.5	0	5	0
IP_{1dB} (dBm)	N.A.	-16	N.A	-29	N.A/-19	-10	N.A	-1	-21.5
P_{dc} (mW)	3800-6400	1800-2000	2160/1540	137/137	52/78	590	960	400	180
RMS Phase error (deg)	N.A	N.A	N.A	N.A	<2°*	N.A	N.A	<1°*	<1°*
Chip size (mm^2)	43.875	37	72.67/77.16	8.75	1.6	4.1	12.5	3.74	4.18
Package	organic BGA	organic BGA	Ceramic	NO	Alumina	NO	LTCC	LTCC	LTCC
Integration level	Beamformer Up mixer Synthesizer MSK modulator IQ calibration	Beamformer Down mixer Synthesizer	Beam former Up/down mixer Synthesizer	Beam former Up/down mixer PLL	Bidirectional Beamformer Up mixer	Beamformer Up mixer Synthesizer	Beamformer Up mixer PLL	Beam former	Beam former
Pattern measurement	YES	YES	NO	NO	NO	NO	YES	YES	YES

*measured from the unit cell.

off-chip decoupling capacitors to improve the stability of the circuit. Note that the TX and RX flip-chip IC and antenna array are designed on the opposite sides of the LTCC substrate. Fig. 16(c) and (d) are the TX/RX SiP modules for TX and RX pattern measurement, and the RF signal is transmitted from the IC through the LTCC substrate to the antenna radiators on the other side. The interconnect lines are realized with 50-Ω microstrip lines to the probe pads on the LTCC substrate. The design and characterization details of this package and antenna will be reported in [18] and [30]. The four-element array consumes 400 mW (100 mW per array element) in the TX from 1-V supply and 180 mW (45 mW per array element) in the RX from 1.8-V and 1-V supply.

A. Single-Channel TX/RX Module Characterizations

Fig. 17(a) shows the single-channel experimental setup of the TX/RX module, with a module size of 2×2 cm^2, including all of the testing pads. The single-channel beamformer characterization is measured on a testing LTCC module after a standard short-open-load-thru (SOLT) calibration with a vector network analyzer (Agilent Technologies, PNA-E8361C) and 200-μm ground-signal-ground probes. Fig. 18(a) presents the simulated and measured TX/RX single path (CH-1) scattering parameters. The dashed lines show the simulated results, which are the average value calculated from all 16 phase states. The solid lines show the measured TX/RX small-signal scattering parameter of all 16 phase states. The measured TX average gain per channel is 0 dB from 57 to 66 GHz. The measured RX small-signal gains for all 16 phase states are also presented and the average gain per channel is about 25 dB at 61 GHz. Fig. 18(a) also shows the simulated and measured I/O return loss. The simulated and measured I/O return losses are all better than 6 dB from 57 to 66 GHz and are independent of the different phase states. Fig. 18(b) shows TX/RX relative phases versus frequency, which achieve full 360° phase range with 22.5° resolution from 57 to 66 GHz. The measured rms gain error was calculated from the average gain of each frequency. The measured TX rms gain/phase error is below 1.5 dB/9° on 4-bit performance at 59 GHz, while the measured RX rms gain/phase error is below 1 dB/9° at 60 GHz [see Fig. 18(c)]. The calculated TX and RX group delay from the measured phase are 220 ± 20 ps and 255 ± 30 ps, respectively, over 57–66 GHz for all phase states. The power performance of the TX is evaluated by a 60-GHz one-tone test, as shown in Fig. 19. This TX achieves a measured $P_{\rm sat}$ of 5 dBm from all four channels. The power performance of the RX is shown in Figs. 19 and 20. The linearity improves as the gain decreases and the highest input 1-dB compression point is -21.5 dBm as the RX is operated in its low-gain mode.

B. TX/RX Array Beam-Steering Characterizations

Fig. 17(b) shows the probe-based measurement setup for the realized gain measurements. The TX/RX array beam-steering characterizations are also measured on an LTCC module.

The TX/RX IC has been packaged with four antennas in an LTCC package and placed on an printed circuit board (PCB). The photograph of the measurement setup for the pattern measurements is shown in Fig. 21. The transmitted and received standard gain horn antenna is placed on a sliding track, which covers an azimuthal a range of only $\pm 25°$ for the broadside gain measurement.

The TX/RX antenna module is placed on a probe station and a probe contacts to a GSG pad apart from antennas to prevent the interference. The probe and a standard gain horn antenna are connected to a vector network analyzer Agilent E8361A for S_{21} measurement. A Friis transmission equation is employed to obtain the realized gain. Fig. 22 shows the normalized TX/RX

array gains as a function of signal incident angles at four different RF phase settings (CH-1 to CH-4), which demonstrates the beam scanned to different angles of $\pm 25^\circ$, $\pm 12^\circ$, and 0°. The synthesized array pattern for a four-element array is based on the simulated scattering parameter including all RF signal traces from IC to antenna array on an LTCC. The measured array patterns at different angles (No. 1–No. 5) are plotted by the dotted lines for comparison. Fig. 22 also shows that 2-D beam-steering patterns are achieved by this 2×2 array through the measured TX/RX XZ-plane and YZ-plane normalized gain patterns. It clearly demonstrates the programmable spatial selectivity of the TX and RX SiP modules. Using the switched LC phase shifter and phase-compensated VGA, the deviation of radiated beam versus frequency can be easily corrected in free space. Moreover, the beam-steering measurement results show acceptable agreement of synthesized and measured array pattern.

V. Conclusion

The 60-GHz four-element phased-array transmitter and receiver SiP antenna modules with phase-compensated techniques in 65-nm CMOS technology have been presented. Table I summarizes the current state-of-the-art phased-array transmitters and receivers at 60 GHz. The 60-GHz four-element phased-array TX and RX SiP modules can achieve wide-bandwidth 2-D beam steering and low power consumption. Based on phase-compensation techniques, the change of radiated beam versus frequency can be corrected in free space. Acceptable agreement between the synthesized and measured beam-steering pattern is demonstrated with a packaged IC.

Acknowledgment

The authors would like to thank A. Chiou, H.-C. Chen, R. Wu, J.-H. C. Zhan, Y. C. Lin, C. L. Tsai, O. Huang, S. Chuang, S. B. Chen, J. Chen, C.-H. Lien, C.-S. Lin, Y.-C. Hsu, M.-C. Chuang, K.-J. Tsai, C.-C. Hung, J.-F. Yeh, W.-T. Li, T.-Y. Ho, B.-J. Huang, D.-J. Haung, Z.-M. Tsai, J.-H. Tsai, P.-C. Huang, J.-J. Kuo, P.-H. Chiang, and C.-C. Kuo for their helpful suggestions.

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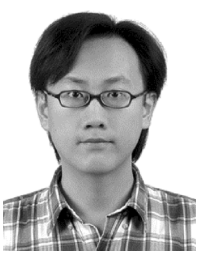

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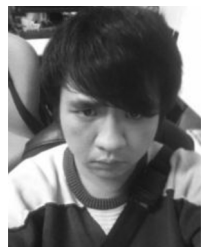

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