60-GHz 5-bit Phase Shifter With Integrated VGA Phase-Error Compensation

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***Abstract*—A 57–64-GHz low phase-error 5-bit switch-type phase shifter integrated with a low phase-variation variable gain amplifier (VGA) is implemented through TSMC 90-nm CMOS low-power technology. Using the phase compensation technique, the proposed VGA can provide appropriate gain tuning with almost constant phase characteristics, thus greatly reducing the phase-tuning complexity in a phased-array system. The measured root mean square (rms) phase error of the 5-bit phase shifter is 2° at 62 GHz. The phase shifter has a low group-delay deviation (phase distortion) of $+/-8.5$ ps and an excellent insertion loss flatness of ± 0.8 dB for a specific phase-shifting state, across 57–64 GHz. For all 32 states, the insertion loss is 14.6 $\pm$ 3 dB, including pad loss at 60 GHz. For the integrated phase shifter and VGA, the VGA can provide 6.2-dB gain tuning range, which is wide enough to cover the loss variation of the phase shifter, with only 1.86° phase variation. The measured rms phase error of the 5-bit phase shifter and VGA is 3.8° at 63 GHz. The insertion loss of all 32 states is 5.4 dB, including pad loss at 60 GHz, and the loss flatness is ± 0.8 dB over 57–64 GHz. To the best of our knowledge, the 5-bit phase shifter presents the best rms phase error at center frequency among the *V*-band switch-type phase shifter.**

***Index Terms*—CMOS, low phase variation, millimeter wave (MMW), phase shifter, variable gain amplifier (VGA).**

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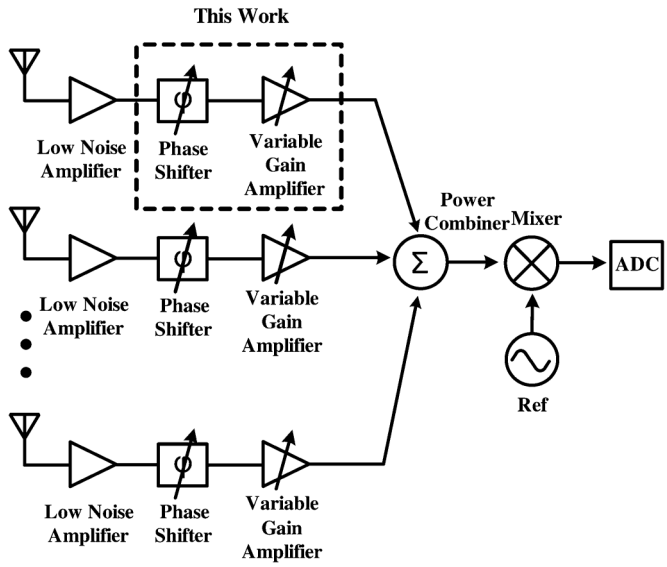

Fig. 1. Block diagram of a receiver front-end for an RF phased-array system.

I. Introduction

RECENTLY, 60-GHz phased array is an attractive technique in the application of high data-rate wireless communications, such as WirelessHD[1] and WiGig[2] due to the advantage of enhancement of the signal-to-noise ratio (SNR) under atmospheric attenuation. In order to accommodate such high-speed data rate for the purpose of improving bandwidth efficiency, a 3–4-bit, or even up to 5-bit phase shifter is essential to reduce error vector magnitude (EVM) for the requirement of a 16-QAM or 64-QAM modulation scheme [1].

Fig. 1 shows a block diagram of a typical phased-array system. The main challenge associated with RF phase shifting is the accuracy of phase control. The 4-bit switch-type phase shifter with low phase variation has been demonstrated in [2]. To further achieve a low phase-variation phased-array system, the gain-compensated variable gain amplifier (VGA) with the integrated phase-compensated technique must be considered for both phase shifter and VGA design.

When the phase shifter provides different phase-shifting states, the loss will be different for each state. Consequently, the VGA must provide different gain compensation for different phase-shifting states. Nevertheless, the gain tuning of the

[1][Online]. Available: http://www.wirelessHD.org

[2][Online]. Available: http://wirelessgigabitalliance.org/

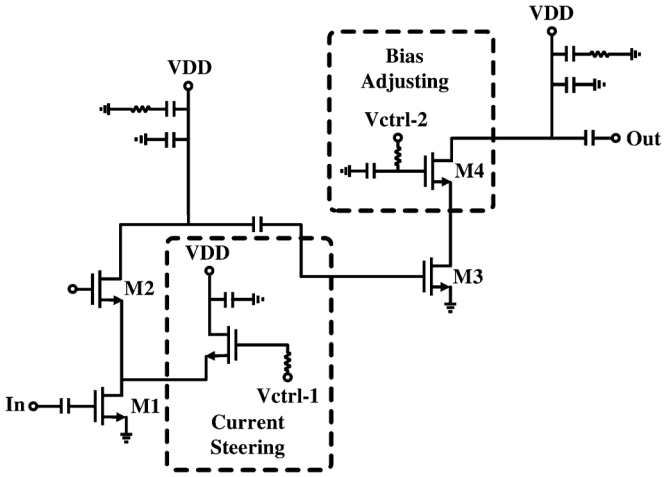

Fig. 2. Schematic of the conventional 60-GHz phase-compensated VGA [3].

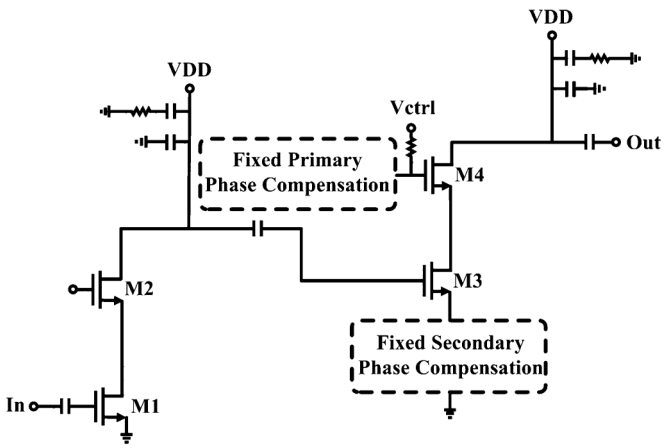

Fig. 3. Schematic of the proposed 60-GHz phase-compensated VGA.

VGA will introduce additional phase variations for the whole phased-array system. Hence, phase-compensated VGA is designed in [3] to compensate the phase variation for different gain-compensation states. However, the conventional approach requires complicated bias tuning for each phase-shifting state to achieve low phase and low gain variation, simultaneously.

For example, gain control can be adjusted through $V_{\mathrm{ctrl}-1}$ in Fig. 2, but the phase adjustment of $V_{\mathrm{ctrl}-2}$ will generate another gain error, which needs $V_{\mathrm{ctrl}-1}$ to be fine tuned interactively.

Thus, the conventional phase compensation in [3] requires a lookup table of $V_{\mathrm{ctrl}-1}$ and $V_{\mathrm{ctrl}-2}$ to achieve accurate gain control with minimum phase error. For the future self-calibration phased-array system, both auto gain control and auto phase control are required for the conventional phase compensation in [3].

In this paper, for a low phase-variation VGA, a simplified phase-compensation technique has been proposed in Fig. 3. In contrast with [3], the proposed technique requires only one auto gain control in the self-calibration phased-array system, which is using fixed phase-compensation blocks to simplify the control complexity. For a high-resolution phase shifter, a previous study of switch-type phase shifter [2] has been improved from 4 to 5 bit, allowing the phased-array system to deliver an ultra-high accurate phase tuning. With the low phase-variation VGA and the high-resolution phase shifter, the proposed phased array is suitable for the applications of satellite communications and radar systems [4].

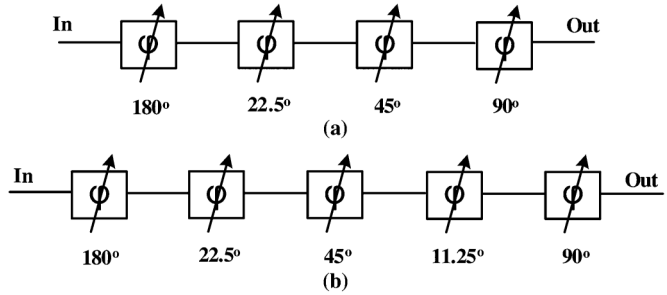

Fig. 4. (a) Schematic of the 4-bit switch-type phase shifter in [2]. (b) Schematic of the proposed 5-bit switch-type phase shifter.

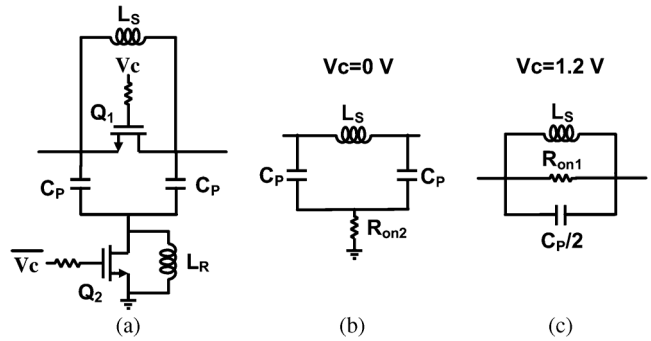

Fig. 5. (a) π-type switch-type phase shifter. (b) Equivalent circuit when $Vc = 0$ V. (c) Equivalent circuit when $Vc = 1.2$ V.

II. 5-bit Low Phase-Variation Phase Shifter

A. Sequence of Phase-Shifting Stages

According to the previous study of the 4-bit switch-type phase shifter [2], as shown in Fig. 4(a), a low phase-variation of 2° is successfully demonstrated. The sequence of phase-shifting stages is an important design consideration for the low phase-variation phase shifter. In order to achieve better EVM performance [1], the multiple phase-shifting stages has been increased from 4 to 5 bit, as shown in Fig. 4(b). However, individual stage performance could be affected by adjacent stages due to loading effects [5]. The small phase-shifting stage (i.e., 11.25° or 22.5°) has more mismatch and loading effect than the large phase-shifting stage. Hence, the small phase-shifting stage (i.e., 11.25° or 22.5°) is placed in between the large phase-shifting stages to reduce loading effects from adjacent stages and to achieve high phase linearity, as shown in Fig. 4.

B. π-Type Versus T-Type Switch-Type Phase-Shifting Stage

There are several ways to realize a switch-type phase shifter. Fig. 5(a) shows the schematic of a single-stage π-type switch-type phase shifter and its equivalent circuits when the control bias Vc is biased at 0 and 1.2 V, respectively [4]. A large resistor (R_G) is added to the gate of the transistor switch to isolate the RF signal from the control bias, as shown in Fig. 5(a). When

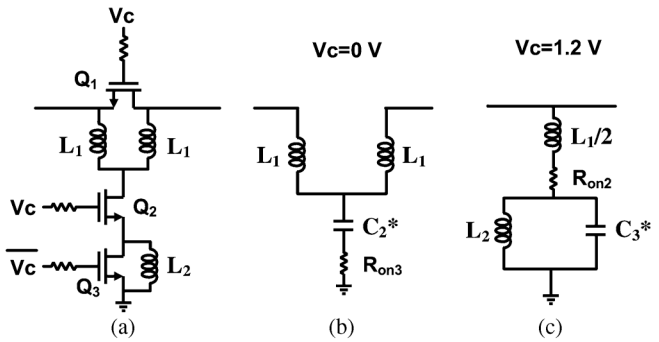

Fig. 6. (a) T-type switch-type phase shifter. (b) Equivalent circuit when $Vc = 0$ V. (c) Equivalent circuit when $Vc = 1.2$ V. (* C_2 and C_3 are the parasitic capacitors of transistors Q_2 and Q_3.)

Vc is 0 V, transistor Q1 is turned off and Q2 is turned on, its equivalent circuit is shown in Fig. 5(b), which is a low-pass filter. Ls and Cp can be obtained from (1) [4]

$$Ls = \frac{Z_0 \sin\varphi}{\omega_0} \qquad Cp = \frac{\tan\frac{\varphi}{2}}{\omega_0 Z_0}. \tag{1}$$

φ is the desired phase shift, Z_0 is the characteristic impedance, and ω_0 is the center frequency. When Vc is 1.2 V, transistor Q1 is turned on and Q_2 is turned off; its equivalent circuit is shown in Fig. 5(c). When Q_2 is turned off, transistor Q_2 will have a parasitic capacitor $C_{\rm OFF}$ due to the nonideal parasitic effects in high frequency. $C_{\rm OFF}$ and L_R form an LC resonator, and L_R can be obtained from (2) [4]

$$L_R = \frac{1}{\omega_0^2 C_{\rm OFF}}. \tag{2}$$

ω_0 is the resonant frequency and $C_{\rm OFF}$ is the parasitic capacitor of transistor Q_2 when it is turned off. The resonant frequency is designed to be the center frequency so $C_{\rm OFF}$ and L_R act like an open circuit at ω_0. Therefore, these two equivalent circuits in Fig. 5(b) and (c) will have a phase difference of φ at ω_0.

Fig. 6 shows the T-type single-stage switch-type phase shifter [6]. The operating principle is similar to the π-type switch-type phase shifter introduced previously. Utilizing transistors as switches, the single-stage switch-type phase shifter has two operating modes: $Vc = 0$ V and $Vc = 1.2$ V, and their equivalent circuits are shown in Fig. 6(b) and (c), respectively. By switching these two bias conditions, the desired phase shift is obtained

$$L_1 = \frac{Z_0}{\omega_0}\tan\left(\frac{\varphi}{2}\right) \qquad L_2 = \frac{1}{\omega_0^2 C_3} \tag{3}$$

$$C_2 = \frac{\sin(\varphi)}{\omega_0 Z_0} \qquad C_3 = \frac{2L_1}{Z_0^2}. \tag{4}$$

The inductances L_1 and L_2 and the capacitances C_2 and C_3 can be calculated from (3) and (4) [6], where φ is the desired phase shift, Z_0 is the characteristic impedance, and ω_0 is the operating frequency.

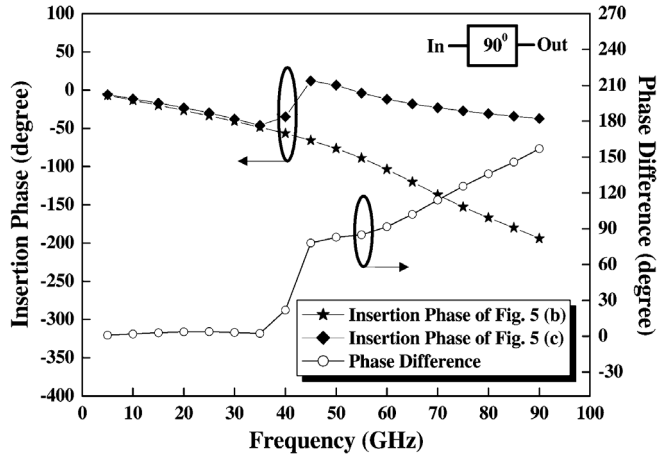

Fig. 7. Insertion phases and phase difference of the two operation modes of the π-type switch-type phase shifter.

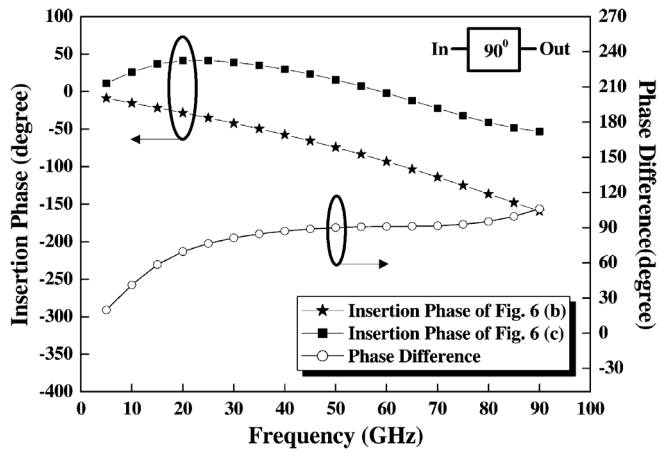

Fig. 8. Insertion phases and phase difference of the two operation modes of the T-type switch-type phase shifter.

The topologies in Figs. 5 and 6 are popular for the switch-type phase-shifter design and we will compare them in terms of phase linearity and group delay in the following sections.

C. Phase Linearity of Switch-Type Phase-Shifting Stage

Group delay [7] is an important parameter that describes the phase linearity of transfer networks. For the phased-array systems, low phase variation, or low group-delay deviation, is required over the entire bandwidth to ensure the signal integrity during transmission.

To choose the appropriate topology for designing a low group-delay deviation phase shifter, the insertion phase and group-delay deviation of the π- and T-type switch-type phase shifter for a 90° phase-shifting stage are compared in Figs. 7 and 8.

In Fig. 7, the two insertion phases of the equivalent circuits in Fig. 5(b) and (c) have different slopes, resulting in a narrow bandwidth of 90° phase shift. Fig. 8 shows the insertion phase and the phase difference of the T-type switch-type phase shifter. The two insertion phases of the equivalent circuits in Fig. 6(b) and (c) have nearly the same slope at 50–70 GHz, which results in a relatively broadband constant phase shift.

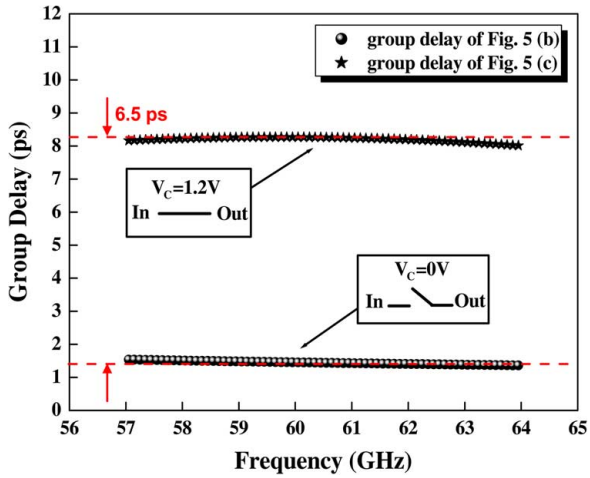

Fig. 9. Group delay of the π-type switch-type phase shifter.

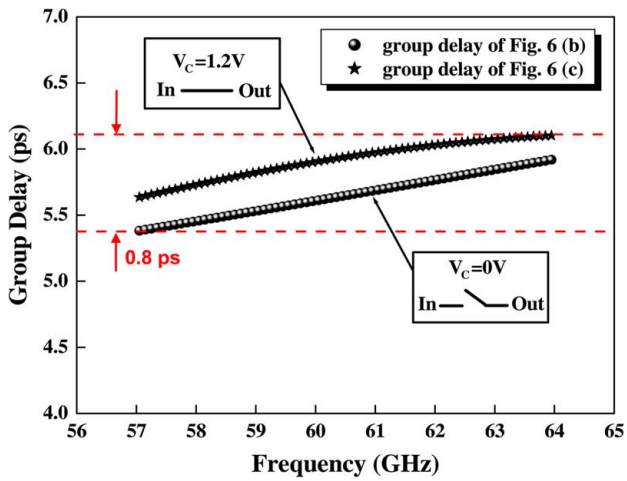

Fig. 10. Group delay of the T-type switch-type phase shifter.

The group delay of the π- and T-type switch-type phase shifter are shown in Figs. 9 and 10, respectively. The group-delay deviation of the π-type phase shifter is 6.5-ps and the group-delay deviation of the T-type phase shifter is 0.8 ps between two operating modes: $Vc = 0$ V and $Vc = 1.2$ V, as shown in Figs. 5(b), 6(b) and Figs. 5(c), 6(c), respectively. Therefore, the T-type switch-type phase shifter has low group delay and low phase deviation.

D. Body-Source Connected MOS Switches

A MOS switch is the key component of the switch-type phase shifter. In order to reduce the insertion loss of a switch-type phase shifter, body-grounded and body-source connected MOS switches are compared in Fig. 11(a) and (b). If the body is connected to ground in the MOS switch, the insertion loss will arise from coupling of drain and source nodes through $C_{\rm db}$ and $C_{\rm sb}$ to ground, as shown in Fig. 11(a). Therefore, to reduce the insertion loss, the body is connected to the source, as shown in Fig. 11(b). Fig. 12 shows the simulated results of two transistor switches with body connected to ground and source. It can be observed that the insertion loss has 0.6-dB improvement when body is connected to source. On the other hand, for the body–source connected MOS in Fig. 11(b), the drain and source nodes are directly connected through $C_{\rm db}$, which degrades the

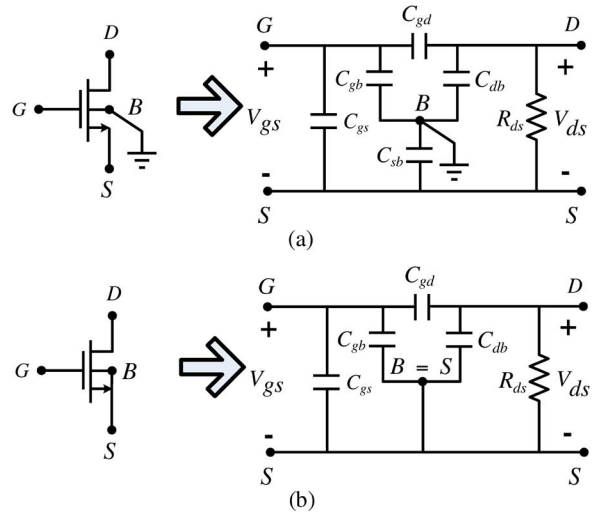

Fig. 11. (a) Equivalent circuit of the body-grounded MOS switch. (b) Equivalent circuit of the body-source connected MOS switch.

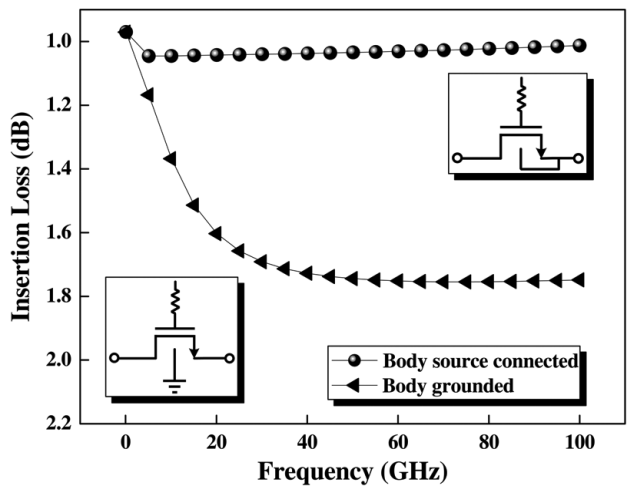

Fig. 12. Simulated insertion loss of transistors when body is connected to ground or source. (* The size of transistor is 40 μm/0.1 μm.)

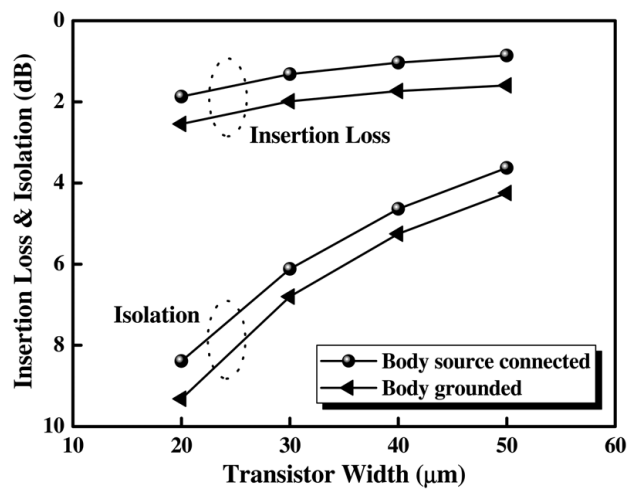

Fig. 13. Simulated insertion loss and isolation of transistors versus different transistor sizes at 60 GHz.

isolation between these two nodes [6]. Finally, Fig. 13 indicates the simulated insertion loss and isolation of transistors versus different transistor sizes. It shows that the transistor switch with

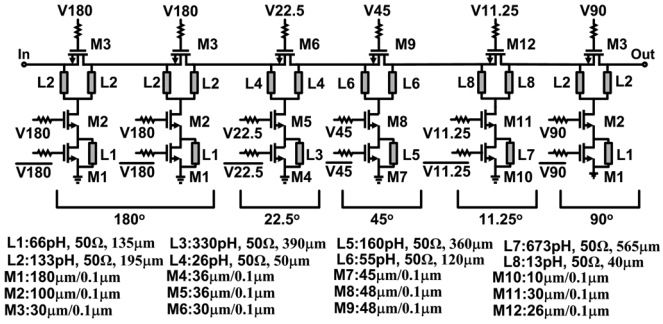

Fig. 14. Schematic of the proposed 5-bit 60-GHz switch-type phase shifter.

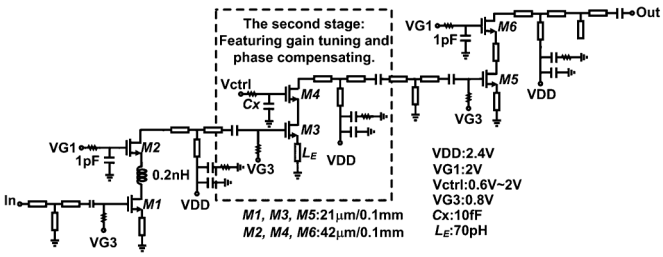

Fig. 15. Schematic of the proposed three-stage 60-GHz low phase-variation VGA.

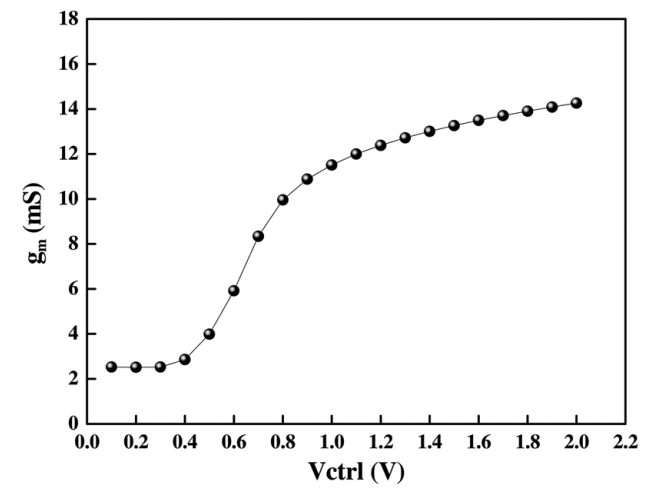

Fig. 16. g_m versus $V_{\rm ctrl}$ of the gain tuning stage of the proposed VGA.

body–source connection can improve the insertion loss at the cost of the isolation.

E. Proposed 5-bit Phase Shifter

Fig. 14 shows the schematic of the proposed switch-type phase shifter. To reduce loading effects from adjacent stages, a 360° phase shift is implemented by cascading 180°, 22.5°, 45°, 11.25°, and 90°, respectively. For low insertion loss, the transistor switches (M3, M6, M9, and M12) have body connected to source. To achieve a compact chip area and to minimize the influence caused by process variation, the inductors are implemented with microstrip lines.

III. Low Phase-Variation VGA

In this paper, the proposed three-stage VGA with low phase variation using TSMC 90-nm CMOS technology is depicted in

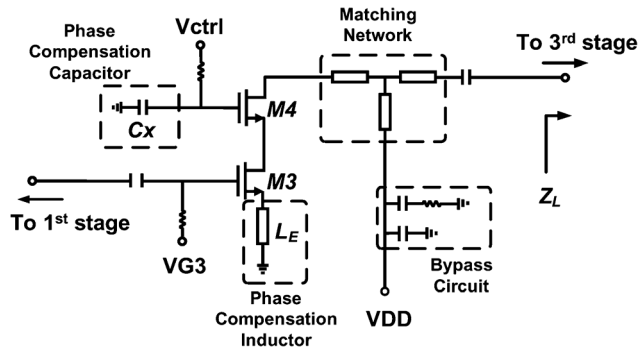

Fig. 17. Schematic of 60-GHz gain-tuning and phase-compensation stage.

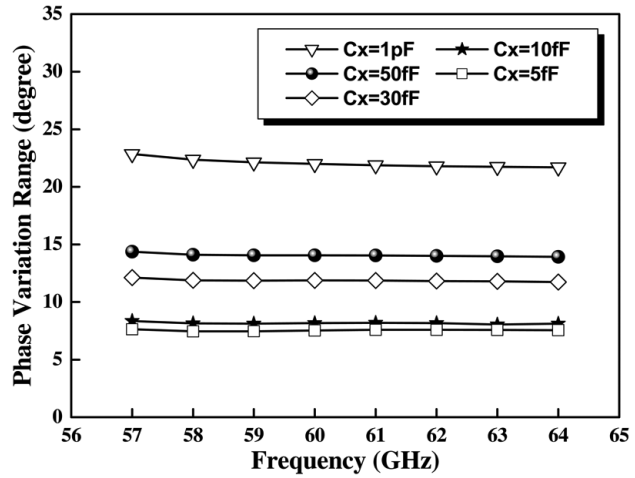

Fig. 18. Different values of C_X versus phase-variation range while $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V. ($L_E = 0$ pH.)

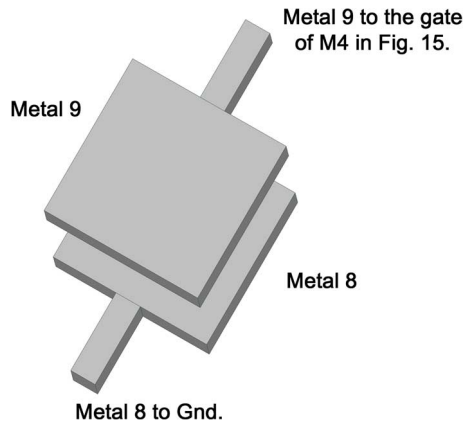

Fig. 19. Custom-designed metal9–oxide–metal8 capacitor with a capacitance of 10 fF for the implementation of C_X at 60 GHz.

Fig. 15. The phase-compensation technique is achieved by utilizing the phase-compensation capacitor (C_X) and source degeneration inductor (L_E). Due to the millimeter-wave (MMW) frequency, all the CMOS parasitic effects of C_X and L_E need to be considered carefully, which has more design challenges than the 5-GHz SiGe bipolar juntion transistor (BJT) compensation technique in [8]. From 5 to 60 GHz, to have well-controlled parasitics, a parallel-plate capacitor and a short transmission line will be selected for the implementation of C_X and L_E in the proposed 60-GHz CMOS VGA. C_X has a primary effect on

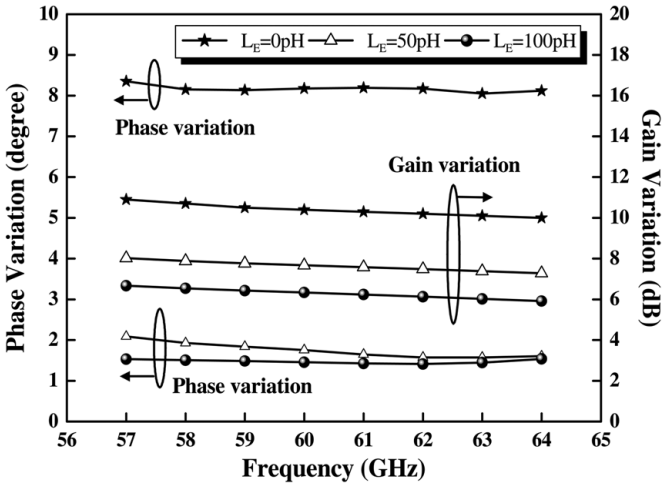

Fig. 20. Different values of L_E versus phase variation and gain variation while C_X is 10 fF, and $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V.

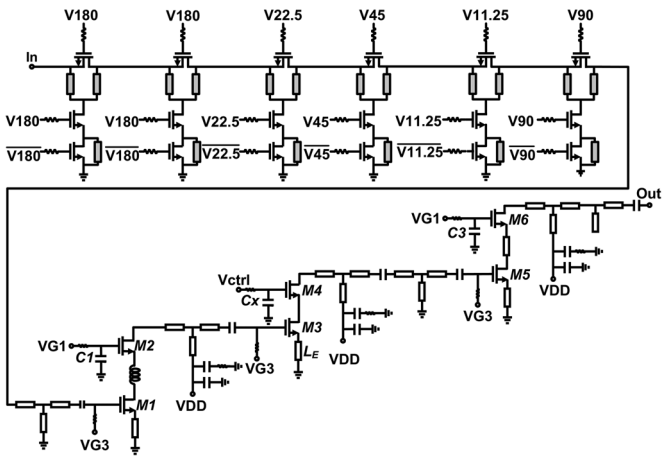

Fig. 21. Schematic of the proposed 60-GHz 5-bit phase shifter and low phase-variation VGA.

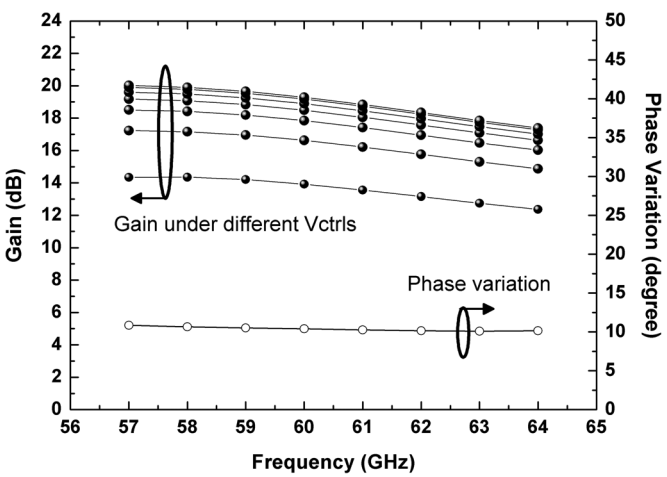

Fig. 22. Simulation results of *phase and gain variations of 60-GHz VGA without phase-variation compensation ($C_X = 1$ pF and $L_E = 70$ pH.) (*Phase variation denotes the difference between the maximum and the minimum phase when the $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V.)

phase-variation compensation, while L_E helps to reduce phase variation.

When the control voltage, $V_{\rm ctrl}$, of the VGA is adjusted, the transconductance (g_m) and matching conditions will also be

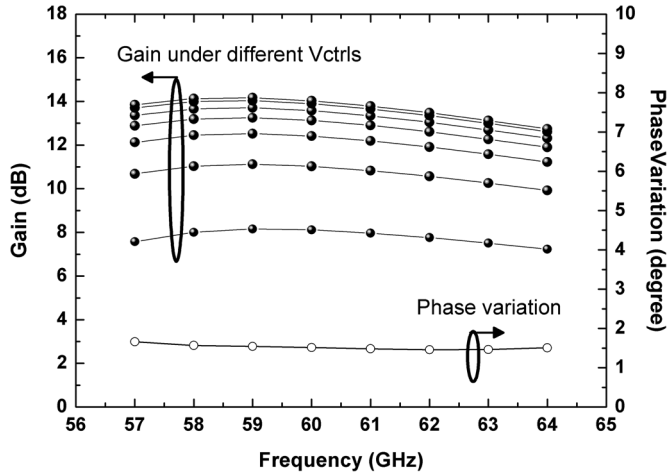

Fig. 23. Simulation results of *phase and gain variations of 60-GHz VGA with phase-variation compensation ($C_X = 10$ fF and $L_E = 70$ pH.) (*Phase variation denotes the difference between the maximum and the minimum phase when the $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V.)

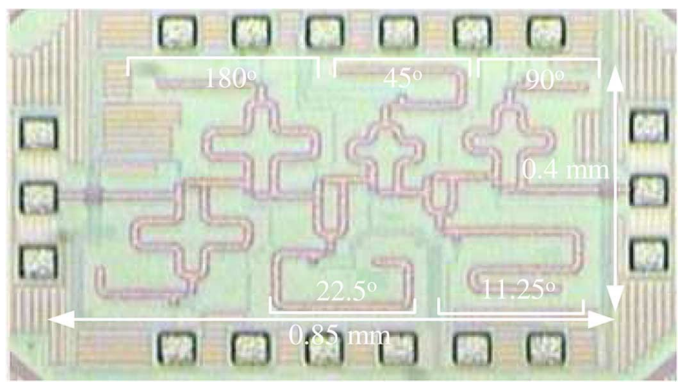

Fig. 24. Chip photograph of the proposed 5-bit 60-GHz switch-type phase shifter. (Chip size: 0.34 mm^2 without pads.)

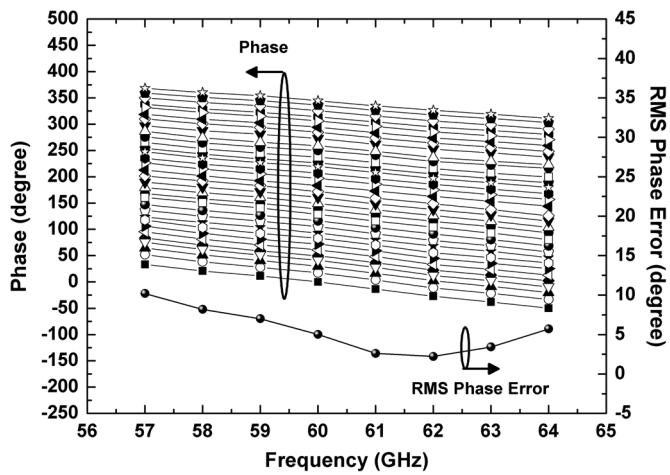

Fig. 25. Measured phase and rms phase error of the proposed phase shifter.

varied accordingly, as shown in Fig. 16; therefore, the gain tuning stage is designed in the second stage to minimize the impact on input and output return loss. The gain tuning and phase compensation stage is composed of a common-source (CS) and a common-gate (CG) cascode topology, as shown in Fig. 17. The equations of maximum S_{21} and minimum S_{21} are given by (5) and (6), respectively. The gain tuning range of a VGA is given by (7). It is worth noted that the gain tuning

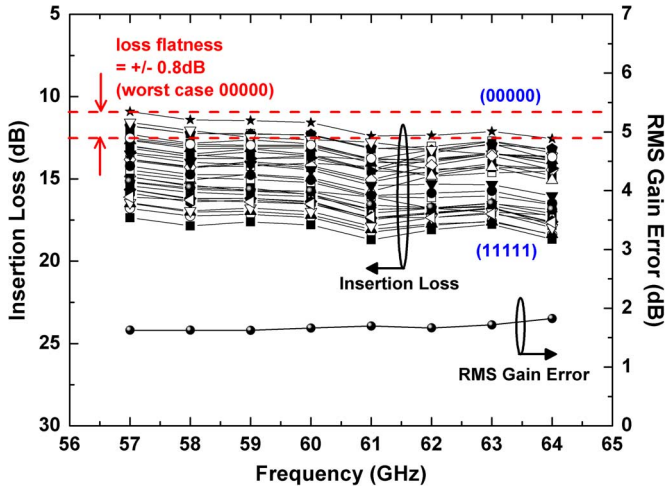

Fig. 26. Measured insertion loss and rms gain error of the proposed phase shifter.

range in (7) is determined by transconductance (g_m), which is independent of load impedance

$$S_{21,\max} = 20\log(g_{m,\max} \cdot Z_L) \quad \text{(dB)} \tag{5}$$

$$S_{21,\min} = 20\log(g_{m,\min} \cdot Z_L) \quad \text{(dB)} \tag{6}$$

$$\Delta S_{21} = 20\log\left(\frac{g_{m,\max}}{g_{m,\min}}\right) \quad \text{(dB)}. \tag{7}$$

Since a constant gain at different phase-shifting states is required in the phased-array system, the gain tuning of the VGA should be wide enough to cover the loss variation of a phase shifter, which is about 6 dB. From (7) and Fig. 16, the gain tuning can be calculated as 6.3 dB as $V_{\rm ctrl}$ is varied from 0.6 ($g_m = 6$ mS) to 1.2 V ($g_m = 12.4$ mS).

However, the tuning of g_m means the variation of node impedance, which also results in phase variation of VGA. To minimize phase variation, the *RC* time constant of a node has to be minimized. By decreasing C_X, effective source node capacitance of M4 in Fig. 17 will be decreased, resulting in less phase variation in Fig. 18.

The phase-variation range versus frequency and C_X is shown in Fig. 18. Phase-variation range denotes the difference between the maximum and the minimum phase when the $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V. According to Fig. 18, a better phase compensation is accomplished by a smaller value of C_X. Since 5 fF of C_X is easily affected by process variation, 10 fF of C_X is chosen to have low phase variation.

To implement C_X, the metal–insulator–metal (MIM) capacitors are utilized; however, foundry provided MIM capacitors suffer from higher process variation, especially for small size capacitors. Therefore, a custom-designed metal9–oxide–metal8 capacitor is used to reduce the capacitance error caused by process variation, as shown in Fig. 19, but the cost is the increased capacitance area. In addition, notice that there is a tradeoff between phase variation and gain. By choosing a small value of C_X, a good phase variation can be obtained while gain will be sacrificed since a small value of C_X cannot provide a good RF short.

L_E also has an effect on phase variation. Fig. 20 shows the phase and gain variations under different values of L_E. Gain

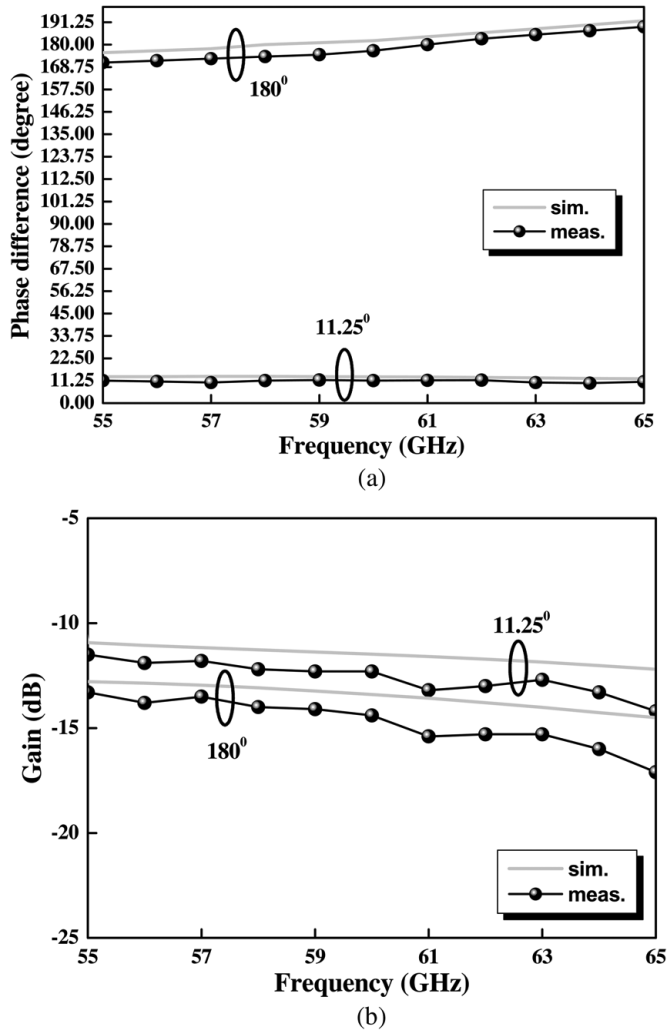

Fig. 27. Measured and simulated: (a) phase difference and (b) gain of 180° and 11.25° phase shifter test-cells.

variation indicates the difference between the maximum and the minimum gain when $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V. The optimized phase variation of 1.5° occurs when L_E is 100 pH. However, the gain variation is decreased by 1.5 dB compared to 50 pH of L_E. Obviously, the improvement of phase variation causes the reduction of gain variation due to the source degeneration inductor. Since the phased array should have a constant gain at different phase-shifting states, the gain tuning range of the VGA is only required to cover the loss variation of a phase shifter. Therefore, instead of choosing L_E for the optimized phase variation, we choose L_E to be 70 pH, between 50–100 pH, to acquire low phase variation while maintaining enough gain tuning range for the loss compensation of the switch-type phase shifter in Section II.

Finally, the schematic of the proposed phase shifter and VGA is shown in Fig. 21. The simulated gain- and phase-variation figures without and with the phase-variation compensation are shown in Figs. 22 and 23, respectively. If the phase-variation compensation capacitor C_X is 10 fF and the source degeneration inductor L_E is 70 pH, the phase variation can be significantly reduced from 10.5° to 1.5°, thus a total of 9° phase-variation reduction.

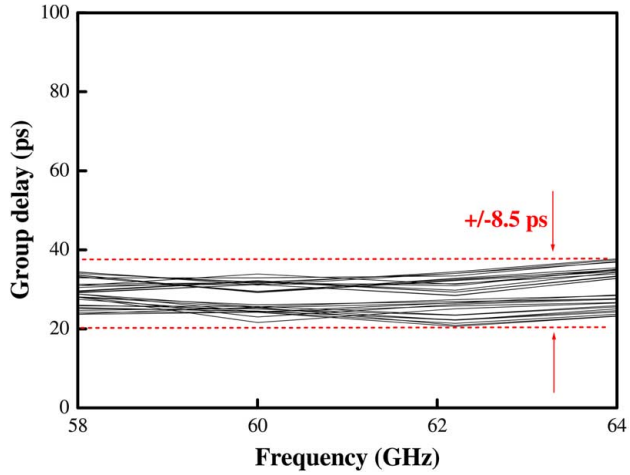

Fig. 28. Measured group delay of the proposed 5-bit 60-GHz phase shifter.

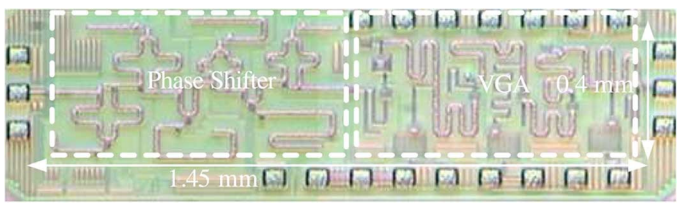

Fig. 29. Chip photograph of the proposed 5-bit 60-GHz switch-type phase shifter and VGA. (Chip size: 0.58 mm^2 without pads.)

IV. Experimental Results

The proposed 5-bit switch-type phase shifter and the integrated phase shifter and VGA are both implemented in TSMC 90-nm low-power 1P9M CMOS technology. Two-port on-wafer S-parameter measurements were conducted in a frequency range from 57 to 64 GHz using vector network analyzer Agilent E8361A.

Root mean square (rms) phase error and rms gain error are two important parameters that indicate the phase control precision and the loss variation, respectively. The following equations give the definition of rms phase error and rms gain error [7]:

$$\text{rms phase error} = \sqrt{\frac{1}{N-1} \times \sum_{i=2}^{N} |\varphi_{\text{error},i}|^2} \tag{8}$$

$$\text{rms gain error} = \sqrt{\frac{1}{N} \times \sum_{i=1}^{N} |A_i - A_{\text{average}}|^2}. \tag{9}$$

A. 5-bit 60-GHz Switch-Type Phase Shifter

Fig. 24 shows a chip photograph of the proposed 5-bit switch-type phase shifter with a chip size of 0.34 mm^2, excluding RF and dc pads. Five control biases (V180, V22.5, V45, V11.25, V90) gives 32 phase-shifting states, and the measured phase and rms phase error are shown in Fig. 25. The phase shifter provides 360° phase shift with a rms phase error of 2.2° at 62 GHz and $<$ 10° across 57–64 GHz. Fig. 26 indicates the measured insertion loss and rms gain error of the 32 phase-shifting states. The insertion losses are designed to achieve excellent loss flatness of ±0.8 dB throughout 57–64 GHz. The

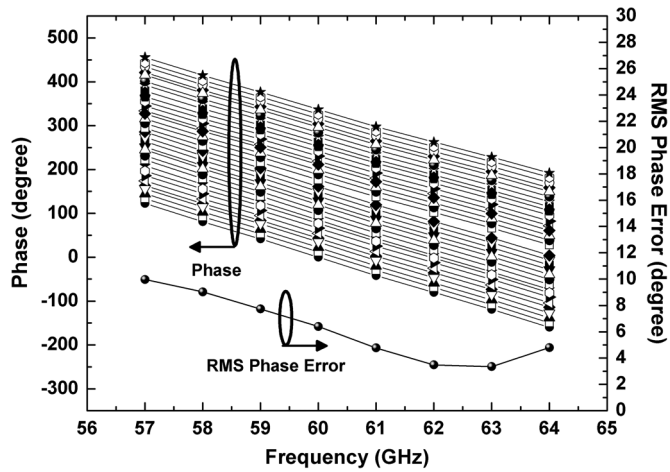

Fig. 30. Measured phase and rms phase error of the proposed phase shifter and VGA.

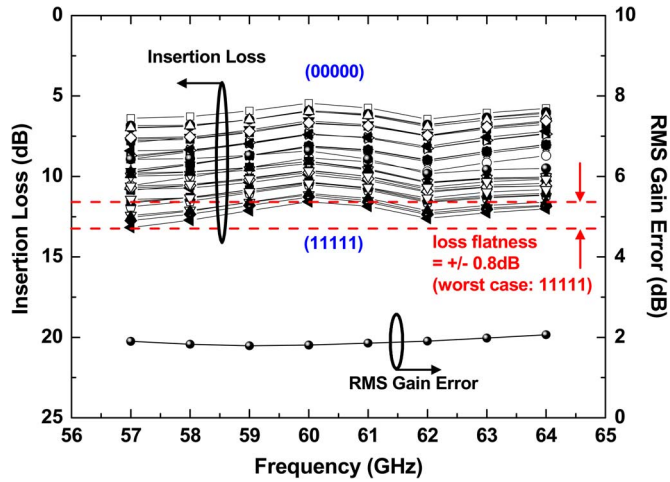

Fig. 31. Measured insertion loss and rms gain error of the proposed phase shifter and VGA.

measured insertion loss is 14.6 ± 3 dB and the rms gain error $<$1.8 dB over 57–64 GHz. Fig. 27 presents the simulated and measured phase difference and insertion loss of individual 180° and 11.25° phase-shifting cells. The measured insertion loss of the 180° and 11.25° phase shifters are 14.4 and 12.3 dB, respectively, at 60 GHz. Fig. 28 shows the measured group delay of the 32 phase-shifting states. The measured group-delay deviation of the 32 states is $+/-8.5$ ps over 58–64 GHz.

B. 5-bit 60-GHz Phase Shifter and Low Phase-Variation VGA

Fig. 29 shows a chip photograph of the proposed 5-bit switch-type phase shifter and low phase-variation VGA with a chip size of 0.58 mm^2, excluding RF and dc pads. To verify the function of phase shifter, a total of 32 combinations of the bias conditions (V180, V22.5, V45, V11.25, V90) were set to measure the 32 phase-shifting states with the bias condition (V_{ctrl}) of the VGA fixed to 0.6 V, as shown in Fig. 21. The measured phase and rms phase error of the 32 phase-shifting states are shown in Fig. 30. The measured rms phase error is 3.3° at 63 GHz and $<$ 9.9° across 57–64 GHz. Fig. 31 shows the measured insertion loss is 8.4 ± 3 dB and the rms gain error $<$2 dB over 57–64 GHz. The worst case of the measured insertion loss flatness occurs when the phase shifter is set to 11111 and the measured loss

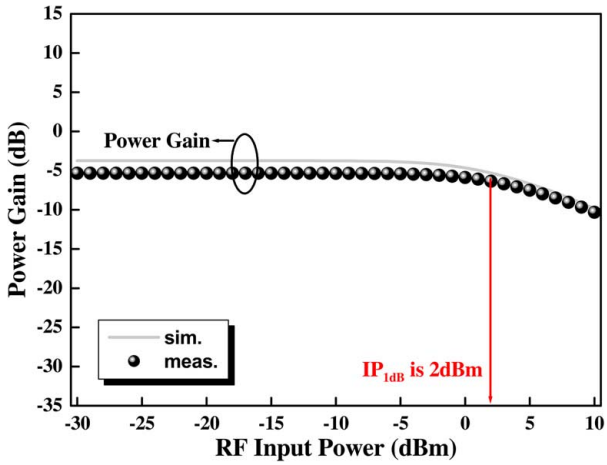

Fig. 32. Simulated and measured gain versus input power at 60 GHz of the proposed phase shifter and VGA.

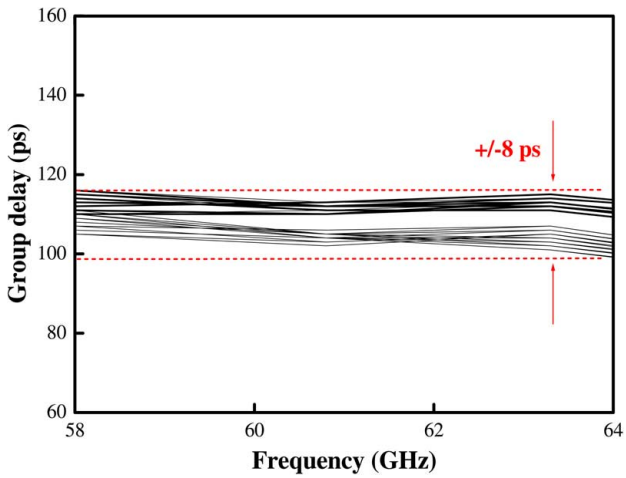

Fig. 33. Measured group delay of the proposed phase shifter and VGA.

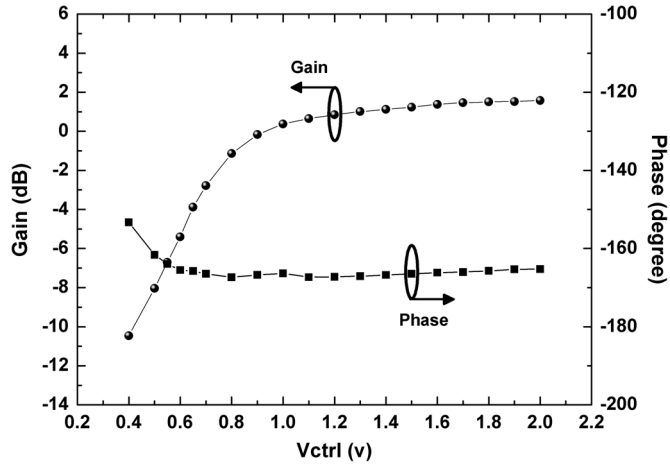

Fig. 34. Measured gain and phase under different $V_{\rm ctrl}$ with phase shifter set to the "00000" state of 0° phase shifting.

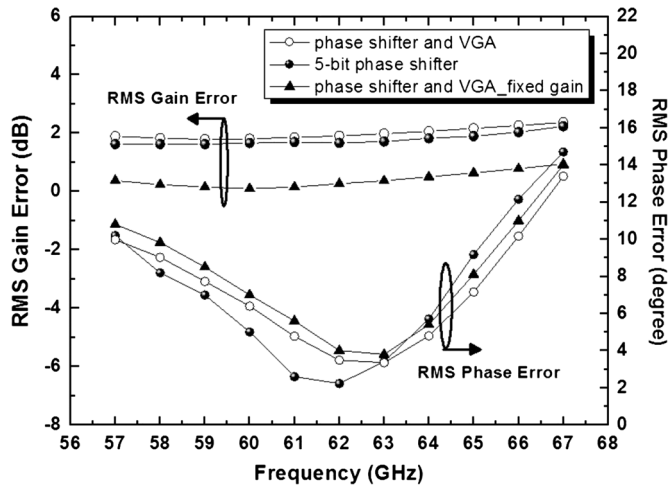

Fig. 35. RMS gain error and rms phase error of the proposed 5-bit phase shifter and VGA.

flatness of the phase shifter and VGA is ±0.8 dB, as shown in Fig. 31. The simulated and measured gain versus swept RF input is shown in Fig. 32. The measured input 1-dB compression point of the proposed phase shifter and VGA is 2 dBm. Fig. 33 shows the measured group delay of the 32 phase-shifting states. The measured group-delay deviation of the 32 states is $+/-8$ ps over 58–64 GHz.

The function of the low-phase VGA was verified by fixing the bias conditions of the phase shifter to 00000 and tuning the bias $V_{\rm ctrl}$ of the VGA. Fig. 34 shows the measured result of the low phase-variation function of the proposed phase shifter and VGA. The optimized bias is to acquire maximum gain variation while maintaining minimum phase variation. Here we need to obtain about 6 dB of gain variation for compensating the loss variation of the 5-bit phase shifter to deliver a constant gain in a phased-array system. Therefore, from Fig. 35, it can be observed that when $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V, gain changes most rapidly while phase remains almost the same due to the phase-variation compensation. The measured gain variation is 6.2 dB with only 1.86° phase variation. The rms gain error and the rms phase error of the proposed 5-bit switch-type phase shifter and the phase shifter integrated with the VGA are shown in Fig. 35. The rms phase error and the rms gain error of the phase shifter integrated with the VGA with the constant gain of -5.4 dB are 3.8° at 63 GHz and 0.5 dB, respectively. The rms phase error of the phase shifter integrated with the VGA without and with the constant gain are almost the same. As a result, it proves that the proposed VGA has minimum impact on the phase variation of the phase shifter.

Table I summarizes the circuit performances and makes comparisons with the recently published above 30-GHz RF phase shifters. Compared with the other RF phase shifters, the proposed 5-bit phase shifter has high phase-shifting states, 32 states for 5 bit, and the best rms phase error of 2° at center frequency among these switch-type phase shifters.

Finally, for phased-array applications in satellite communications and radar systems, a phase shifter with at least 22.5° phase resolution is essential [4]. Consequently, Table II summarizes the circuit performances and makes comparisons with the recently published high-resolution phased arrays. Compared with the other phased arrays, the proposed phase shifter integrated with the VGA has high phase resolution, low phase error, and is able to control gain with only one $V_{\rm ctrl}$, thus simplified the control complexity. Finally, from Table II, this work presents the best phase variation of 3.8° under the same gain of -5.4 dBm. This property enables the VGA to operate gain tuning with a minimum effect on the phase error of the phase shifter.

TABLE I
COMPARISON TABLE OF RF PHASE SHIFTERS

Ref./ Technology	Freq. (GHz)	Topology	Phase Range (°)	Resolution (°)	Max. Loss (dB)	Loss Flatness (dB)	Max. Phase Error (°)	Min. Phase Error (°)	Gain Deviation (dB)*	P_{DC} (mW)	Area (mm^2)
[4]/0.13μm SiGe BiCMOS	32-36	STPS	360	22.5	15	±2.5	24	4@35GHz	1	0	0.21
[9]/ SiGe BiCMOS	34-39	STPS	360	11.25	n/a	±2.75	16	2@36.5 GHz	1	0	n/a
[10]/ 0.18μm SiGe BiCMOS	40-45	VS	360	n/a	12.5	n/a	9	6.5@40 GHz	n/a	40	0.11
[11]/ 0.13μm SiGe BiCMOS	57-64	RTPS	180	n/a	8	±1.5	n/a	n/a	n/a	0	0.56
[12]/ 0.13μm SiGe BiCMOS	60	RTPS	156	n/a	7.2	±1	n/a	n/a	1.1	0	0.33
[13]/ 65nm CMOS	55-65	STPS	360	22.5	16	±2	9.2	5.5@55 GHz	n/a	0	0.2
[14]/ 0.12μm SiGe BiCMOS	67-78	STPS	360	22.5	22.5	±3.7	11.25	3.75@71 GHz	4.5	0	0.28
This work/ 90nm CMOS	**57-64**	**STPS**	**360**	**11.25**	**18**	**±0.8**	**10**	**2@62 GHz**	**1.8**	**0**	**0.34**

TABLE II
COMPARISON TABLE OF HIGH-RESOLUTION PHASED ARRAYS

Ref/ Technology	Freq. (GHz)	Phase range (°)	Reso-lution (°)	Return loss (dB)	Gain (dB)	Loss flatness (dB)	Max. Phase Error (°)	Min. Phase Error (°)	VGA control bias	VGA phase variation (°)	VGA gain tuning range (dB)	P_{DC} (one channel) (mW)
[3] / 65nm CMOS	57-62	360	22.5	>10	24.2± 3.3	±2.5	11.5(Rx)	9@61 GHz(Rx)	Analog 2 bias port	*V_{ctrl1}:20 V_{ctrl2}:2	6	45
[9]/ 0.13μm SiGe BiCMOS	34-39	360	11.25	>15	-1.5 ±1.5	±0.5	15	5@36.5 GHz	Digital 5bit	15-20	7.5	35.5
[15] / 0.18μm SiGe BiCMOS	32.8-44	360	22.5	>8	10.4± 2	±2.5	8.3	7.2@44 GHz	n/a	n/a	n/a	147.5
[16] / 65nm CMOS	58.2-63.7	360	22.5	>5	12±2	±1.5	9	6@58.2 GHz	Digital 2bit	n/a	n/a	156
[17]/ 0.18μm SiGe BiCMOS	13-15	360	22.5	>6	3.4± 3.6	±1.6	12	8.1@13 GHz	Digital 4bit	2.4	7.2	455
This work/ 90nm CMOS	**58-65**	**360**	**11.25**	**>10**	**-5.4**	**±0.8**	**9.8**	**3.8@63 GHz**	**Analog 1 bias port**	**1.86**	**6.2**	**31.2**

* V_{ctrl1} and V_{ctrl2} tuned, respectively.

V. Conclusion

A 57–64-GHz low phase-error 5-bit switch-type phase shifter with an integrated low phase-variation VGA using TSMC 90-nm LP CMOS technology has been presented in this paper. Using the phase-variation compensation technique, the proposed VGA can provide gain tuning of 6.2 dB with only 1.86° phase variation, which agrees well with the theoretical calculation of 6.3 dB and software simulation results of 7 dB when $V_{\rm ctrl}$ is tuned from 0.6 to 1.2 V in Fig. 15. For the phase shifter, the measured rms phase error of the 5-bit phase shifter is 2° at 62 GHz. The insertion loss of all 32 states is 14.6 ± 3 dB including pad loss at 60 GHz, and the loss flatness is ± 0.8 dB over 57–64 GHz.

For the phase shifter integrated with the VGA, the measured rms phase error is 3.8° at 63 GHz. The insertion loss of all 32 states is 5.4 dB including pad loss at 60 GHz, and the loss flatness is ± 0.8 dB over 57–64 GHz. The phase shifter integrated with the VGA draws 13 mA from a 2.4-V supply and consumes a total dc power of 31.2 mW.

As mentioned above, the low phase-variation VGA has a minimum impact on the phase variation of the phase shifter, which is suitable for high-resolution phased arrays.

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