16.9-mW 33.7-dB Gain mmWave Receiver Front-End in 65 nm CMOS

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***Abstract*—This work presents a low power receiver front-end design for the 77 GHz radar application. The theoretical maximum achievable gains in the LNA and the mixer are derived by using energy conservation principle. It is shown that the maximum gain can be increased by raising the impedance ratio between stages. The impedance transformation is able to provide high passive gain without any power consumption. Moreover, the quality of the passive components plays a critical role to approach the maximum gain condition. Accordingly a low power receiver front-end is designed in 65 nm CMOS. The measured results show the highest gain of 33.7 dB at 73 GHz with 3 dB bandwidth from 67 GHz to 75 GHz. The input return loss, P1dB, IIP3, and NF at IF frequency of 8 MHz, are 16.4 dB, -32 dBm, -19 dBm, and 12.2 dB, respectively. The power consumption is only 16.9 mW from a 1 V supply. To the best of our knowledge, this work shows the highest gain while consumes the lowest power as compared to the prior works.**

I. INTRODUCTION

The car anti-collision radar system can improve driving safety by emitting an alarm signal in advance to notice the driver to prevent accidents. The radar system used to be installed in luxury cars. Recently it has been implemented by SiGe technology [1], [2]. With the rapid progress of CMOS technology, the transistor speed raises up dramatically to make it possible to design such a system with low cost and high integration. It is thus feasible to apply this system to every car to improve human life.

The 77 GHz band is specified for the radar system, which usually uses the ranging method of frequency modulated continuous wave (FMCW) radar as shown in Fig. 1. The frequency of the LO signal sweeps over time. As this modulated signal is bounced back from the obstacle, or the target, the received signal has a time delay relative to the transmitted one. When the signal is converted to IF band, the spectrum has a beat frequency component related to the distance between the radar and the target. Hence the distance can be known after signal processing.

Those previous CMOS receivers at 77 GHz show low gain while consume high power [3]-[5]. Few insights are given and no detailed analysis is provided to explain how to optimize the circuit. Instead, in this work, the receiver front-end is designed based on the derived compact formulas for the maximum achievable voltage gain and voltage conversion gain in the LNA and the mixer, respectively. Much insight is given to help optimize the receiver. The proposed receiver front-end not only presents the highest gain, it also consumes the lowest power. This approves that the proposed design methodology is valuable for millimeter-wave circuit designs.

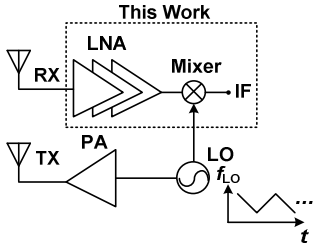

Fig. 1. The FMCW radar system. This work mainly focuses on the receiver front-end design consisting of an LNA and a mixer.

II. RF FRONT-END CIRCUIT DESIGN

As illustrated in Fig. 1, the receiver architecture consists of an LNA and a mixer. The LNA needs to carry out high gain in order to suppress the noise from the following stages while the mixer is required to down-convert the RF signal into intermediate frequency with high linearity. The following subsections exhibit the design principle.

A. LNA Design

For the narrowband application, the LNA can be modeled as cascades of an input matching network, an active device, and an output matching network, as depicted in Fig. 2. The output impedance of the active device can be simply modeled as *RC* in parallel. As the input is power matched, the effective transconductance of the input stage at the frequency of interest ω_o can be simply approximated as

$$G_{M@\omega_o} = \frac{\omega_T}{2\omega_o R_S} \quad (1)$$

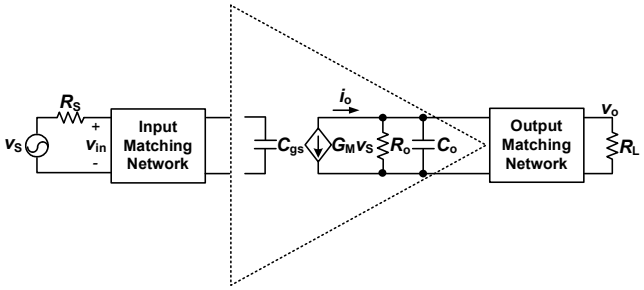

Fig. 2. The equivalent model of a narrowband LNA.

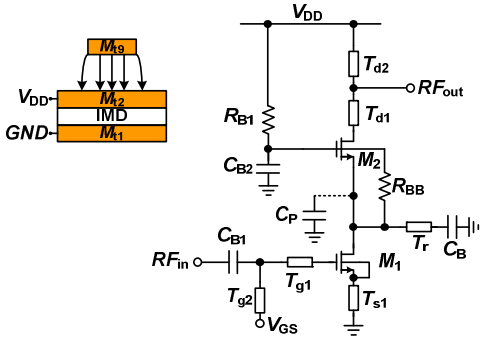

Fig. 3. The proposed LNA design. The inset shows the transmission line structure. IMD means intermediate dielectric.

where ω_T is the unit current gain frequency [6]. By using the energy conservation principle, the maximum power acquired at R_L is equal to the maximum available power delivered from the active device. Under such a condition, the maximum achievable trans-impedance gain can be derived as

$$\left|\frac{v_o}{i_o}\right|_{Max@\omega_0} = \frac{1}{2}\sqrt{\frac{R_o}{R_L}}R_L. \qquad (2)$$

All of possible parasitic capacitances can be absorbed into the matching networks without degrading LNA gain. From (1), (2), and $i_o=G_M v_S$, the maximum achievable voltage gain of the LNA is thus shown as

$$\left|\frac{v_o}{v_{in}}\right|_{Max@\omega_0} = \frac{1}{2}\frac{\omega_T}{\omega_o}\frac{R_L}{R_S}\sqrt{\frac{R_o}{R_L}} = \frac{1}{2}\sqrt{\frac{R_o}{R_S}}\left(\frac{\omega_T}{\omega_o}\right) \propto \frac{1}{\sqrt{L}}, \qquad (3)$$

where R_S and R_L are generally 50 Ω and L is the channel length of the transistor. The same equation is shown in [7] but no detailed explanation is given. Furthermore, we demonstrate (3) is the "maximum" gain that the LNA can provide. High R_o is desired in analog IC design to have high gain. This is usually realized by using longer channel length. However, shorter length is required in high frequency design to have a high speed device. The compromise between these two choices still longs for shorter length for the purpose of high gain in millimeter-wave frequency. This explains that the technology scaling is actually beneficial for RF circuit design.

Fig. 3 shows the proposed LNA design. As illustrated in (3), high impedance ratio R_o/R_L and high ω_T are desired to have high gain. The passive gain provided by the impedance transformation can be high without any power consumption. The channel length is chosen as 60 nm to have high ω_T while the impedance ratio is boosted by using the cascode topology.

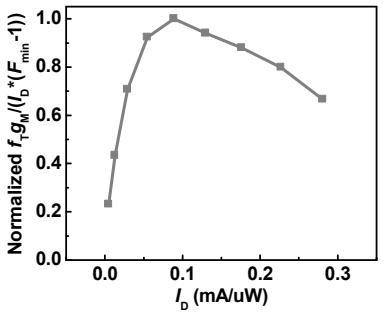

Fig. 4. The simulated normalized FOM versus current density.

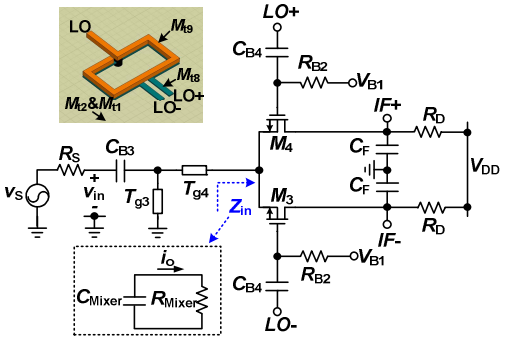

Fig. 5. The proposed mixer design. The inset indicates the structure of the Marchand balun.

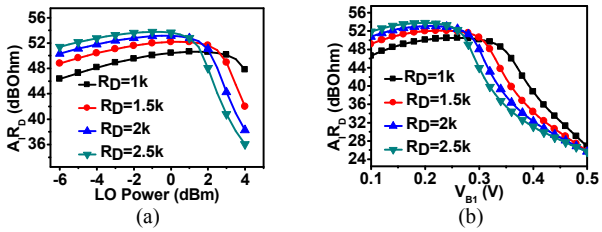

Fig. 6. The simulated voltage conversion gain versus (a) LO power (b) gate bias of V_{B1} under different R_D values.

The cascode topology also benefits in high reverse isolation between the input and output. A bulk-to-source resistor R_{BB} is added to further improve the isolation. In order to make M_2 serve as a good current buffer, the parasitic capacitance C_P at the drain node of M_1 is resonated out by a short stub T_r. This also helps suppress the noise contribution from M_2. To get good trade-off among the power consumption, the noise figure, and ω_T, the bias of the transistor is designed according to the defined normalized FOM as shown in Fig. 4. Hence the current density of 89 μA/μm is chosen and f_T, NF_{min}, and I_D are 132.9 GHz, 2.8 dB, and 3.7 mA, respectively. The simulated voltage gain of the proposed LNA at 77 GHz with lossless matching networks is 11.3 dB. The calculated value using (3) is 11.8 dB where R_o is extracted as 1.03 kΩ. The possible discrepancy between the realized gain and the theoretical one is due to the approximation in (1).

As long as the maximum achievable gain is known, the design of impedance matching networks becomes very critical. The matching networks should be as lossless as possible. The input and output matching networks are implemented by the transmission lines T_{g1}, T_{g2}, and T_{d1}, T_{d2}, respectively, of which the cross-sectional view is shown in the inset in Fig. 3. The second metal layer M_{t2} in the entire

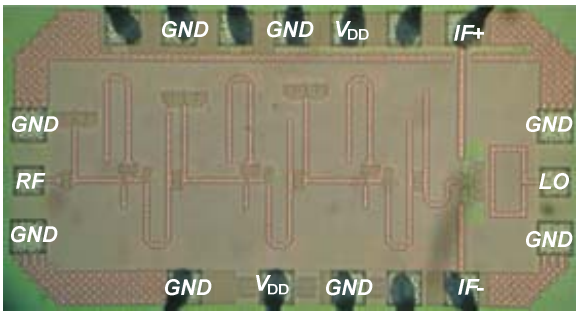

Fig. 7. Chip micrograph

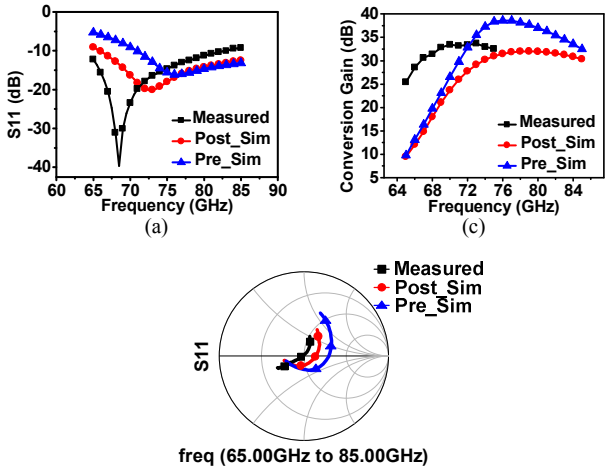

Fig. 8. (a) The measured input return loss. (b)S11 in Smith chart. (c) The measured RF bandwidth. Pre_Sim means that only the transmission lines are replaced by the EM simulated results. Post_Sim represents that EM simulation is conducted on the whole chip, including all the interconnects and the transmission lines.

chip is linked to V_{DD} to reduce the impact of the parasitic path on the transmission line design. Moreover, M_{t2}, ac grounded together with M_{t1}, can also provide better substrate isolation to prevent the field from leaking into the substrate and reduce the induced substrate loss. The post-layout simulated voltage gain of the LNA is 4.9 dB, different from 11.3 dB provided the matching network is lossless. The quality of the transmission lines shall be improved and the layout parasitics need to be reduced further to get closer to the ideal value. The most import implication is that the achievable gain is limited by the quality of the passive components and the layout parasitics, instead of the transistor speed. In order to provide enough gain to suppress the noise from the following stages, cascades of three identical stages are implemented in the final LNA design to provide power gain of 13.8 dB at 77 GHz. The power consumption is only 13.7 mW from a 1 V supply.

B. Mixer Design

The proposed single-balanced mixer is shown in Fig. 5. Since the frequency separation between LO and IF signals has many orders of difference, a simple *RC* low pass filter can effectively remove the LO leakages. A Marchand balun is designed to provide the differential LO signals.

For the mixer design, the maximum voltage conversion gain is also derived in (4) by using the energy conservation

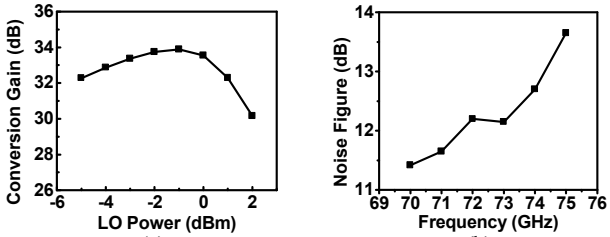

Fig. 9. (a) The measured conversion gain versus LO power when RF frequency is 73 GHz. (b) The measured noise figure versus RF frequency.

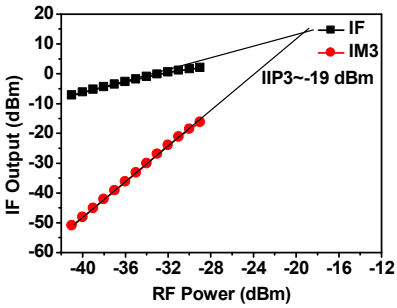

Fig. 10. The measured IIP3.

principle where current gain A_I of an ideal switching stage is assumed to be $2/\pi$.

$$\left|\frac{v_{IF+}-v_{IF-}}{v_{in}}\right|_{max@\omega_o} = \frac{A_I R_D}{\sqrt{R_S R_{Mixer}}} = \frac{2}{\pi}\frac{R_D}{\sqrt{R_S R_{Mixer}}}. \quad (4)$$

R_{Mixer} is not as expected to be low since high loading resistance R_D makes R_{Mixer} to increase. However, higher R_D is still desired to have high gain since R_{Mixer} is inside a square root in (4). To have high conversion gain, the switching stage design becomes very critical. Hence the loading resistance R_D, LO power, and the gate bias should be designed carefully. As depicted in Fig. 6(a), $A_I R_D$ peaks variously at different R_D values. Higher R_D shows higher conversion gain while the required LO power can also be small. Small LO power is appealing since in general it is not easy to generate high LO power in millimeter-wave frequencies. However, the linearity is also degraded when R_D is large. The gain and linearity are also dependent on the gate bias as shown in Fig. 6(b). Therefore, R_D, V_{B1}, and LO power of 2 k , 0.2 V, and -1 dBm, respectively, can enable the mixer to have good trade-off among the linearity and conversion gain. It is to note that the actual achievable $A_I R_D$ shall be higher than the values shown in Fig. 6 since some portion of the input current leaks through C_{Mixer}. In the practical implementation, C_{Mixer} is absorbed into the matching network and will not cause gain degradation. The simulated voltage conversion gain assuming ideal matching network is 22.0 dB. The calculated gain based on (4) is 21.3 dB where R_{Mixer} is extracted as 241.2 Ω using LSSP simulation in Agilent ADS tool. The discrepancy between the simulated gain and the calculated one could be resulted from the accuracy in R_{Mixer} extraction because of large signal operation in the mixer. The input matching network composed of T_{g3} and T_{g4} are designed to achieve the maximum

Table I. Summary of the proposed front-end

Work	[3] ISSCC 2009	[4] JSSC 2010	[5] JSSC 2010	**This Work**
Topology	LNA+Mixer+IF Amp.	LNA+Mixer+TIA+Buffer	LNA+Mixer+IF Amp.	**LNA+Mixer**
f_{RF} (GHz)	73.5~77.1	78.1~78.8	75.6~76.3	**67~75**[(d)]
V_{DD} (V)	0.8	1.2	1.2	**1**
Conversion Gain (dB)	8	23.1	38.7[(a)]	**33.7**
NF (dB)	6.8[(c)]	12.6	30[(b)]	**12.2**
IIP3 (dBm)	N/A	N/A	-12.5[(c)]	**-19**
P1dB (dBm)	-17[(c)]	N/A	-22[(c)]	**-32**
Power (mW)	260	111	55	**16.9**
Technology (CMOS)	90 nm	90 nm	65 nm	**65 nm**

(a) IF amplifier provides 16 dB gain. (b) NF of the LNA is 7.4 dB. (c) LNA only. (d) only measured up to 75 GHz.

conversion gain condition. The realized voltage gain is 17.8 dB at 77 GHz. The power consumption is only 0.1 mW.

III. Measurement Results

The proposed receiver front-end is implemented in 65 nm CMOS technology. The chip micrograph is shown in Fig. 7. The chip size is 0.99×0.53 mm^2. The measurement is conducted by chip-on-board setup. The RF and LO signals are applied to the chip by high frequency probes. The DC and IF pads are wire-bonded to the PCB. An on board operational amplifier with unit gain is employed to convert the differential IF signals to the single-ended form. The power consumption is only 16.9 mW from a 1 V supply.

Fig. 8(a) and 8(b) show the measured input return loss. The measured and simulated results show similar trends with a frequency drift. This drift may be caused by unexpected parasitics in the transistor model. The foundry only guarantees model accuracy up to 30 GHz. To accurately predict the transistor parasitics, the modeling methodology proposed in [8] can be used. Even with such a frequency offset, the input return loss is still kept below 10 dB from 65 GHz to 82 GHz. The measured conversion gain showing the RF bandwidth is illustrated in Fig. 8(c) when the IF frequency is set to 8 MHz and the LO power is -2 dBm. The highest gain is 33.7 dB at the frequency of 73 GHz. The peak gain frequency is around 5 % shift from the target of 77 GHz. The 3 dB bandwidth covers from 67 GHz to 75 GHz. The conversion gain is only measured up to 75 GHz. It is believed that the 3 dB bandwidth can be even wider. The experimental results show higher gain than those of the post-simulation, but lower than those of the pre-simulation. This may implies that the post-simulation over-estimates the parasitic loss. It may be also due to the reason that the peak gain frequency shifts to lower band so the gain is higher. Higher power consumption in the measurement may be another reason. The consumed power in the simulation is only 14.7 mW.

Fig. 9(a) shows the conversion gain versus LO power at 73 GHz. The highest gain is achieved when the LO power is near -2 dBm. Fig. 9 (b) illustrates the measured noise figure with respect to the RF frequency at IF frequency of 8 MHz. The noise figure is 12.2 dB when the RF frequency is 73 GHz. Fig. 10 depicts the measured IIP3. The IIP3 and P1dB are around -19 dBm and -32 dBm, respectively. Table I summarizes this work and makes comparison with other works. It is clear that the proposed receiver front-end shows the highest gain while the power consumption is the lowest. The noise performance is also better.

IV. Conclusion

A high gain and low power receiver front-end suitable for the 77 GHz radar application is realized in 65 nm CMOS technology. The receiver is optimized based on the insight acquired from the derived formulas for the maximum achievable gains in the LNA and the mixer. The measured conversion gain is 33.7 dB at 73 GHz RF frequency. The power consumption is only 16.9 mW from a 1 V supply.

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