Double-Balanced 130-180 GHz Passive and Balanced 145-165 GHz Active Mixers in 45 nm CMOS

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***Abstract*- This paper presents wideband passive and active mixers in the 100-200 GHz range. The mixers are built using a 45nm CMOS SOI process with an ft of 220 GHz when referenced to the top metal layer. The passive double-balanced mixer results in a conversion loss of 12-13 dB from 130-180 GHz (including balun, transmission line and GSG pad losses) and achieves optimal performance with 3 dBm of LO power (referenced to the GSG LO pads). The active mixer achieves a conversion loss of 4.5 dB with a 3-dB bandwidth of 145-165 GHz, and consumes only 10 mW of DC power from a 1.5 V supply. The application areas are in wideband Gbps communications, imaging arrays with large IF bandwidths, and mm-wave spectrometers. To our knowledge, this work represents the first demonstration of high performance CMOS mixers in the 130-180 GHz frequency range.**

I. Introduction

Advanced CMOS nodes such as 65, 45 and 32nm, have the potential for > 100 GHz operation due to their high ft and thick-metal back-end layers which are compatible with low-loss mm-wave transmission-lines. Seo et al. and Xu et al. demonstrated 65nm CMOS amplifiers at 140 GHz [1,2], while Cetinoneri et al. showed a 45nm CMOS doubler at 170-190 GHz with 0.5-1 mW of output power [3]. Laskin et al. presented the first 140 GHz CMOS downconveter with 20 dB conversion loss in 65nm CMOS [4]. In this work, the mixer was operated using a 102 GHz local oscillator which resulted in an IF of 38 GHz and added insertion loss.

There are few CMOS building blocks available above 100 GHz due to the limited ft of the current CMOS transistors. In fact, most of the silicon circuits above 100 GHz have been dominated by SiGe due to its higher gain, lower noise figure and lower 1/f noise [5]. However, SiGe technology is not yet co-integrated with advanced CMOS nodes, which makes it challenging to build system-on-chip solutions using both analog and high-speed digital circuit blocks. This paper presents state-of-the-art wideband passive and active mixers in 45nm CMOS which are essential for wideband BPSK and QPSK receivers (and upconverters), and imaging arrays with a wide IF-bandwidth (radiometers or spectrometers).

II. Circuit Design

The technology used in the IBM 12SOI 45nm CMOS, which is built on a partially depleted 225nm SOI layer and a 13.5 Ω-cm substrate [6]. The metal back-end is given in Fig. 1 and consists of 11 metal layers where all layers are copper with tungsten vias except the top metal which is an aluminum layer. This technology does not offer an MIM capacitor. The design kit provides MOM capacitors using already available metal layers and an interdigital layout to increase the capacitance per unit area. The transistor *ft* is specified as 480 GHz when referenced to M1 [6], but S-parameter measurements at UCSD using the interconnects up to the top metal results in an *ft* of 220 GHz for a 30x1 µm transistor [3].

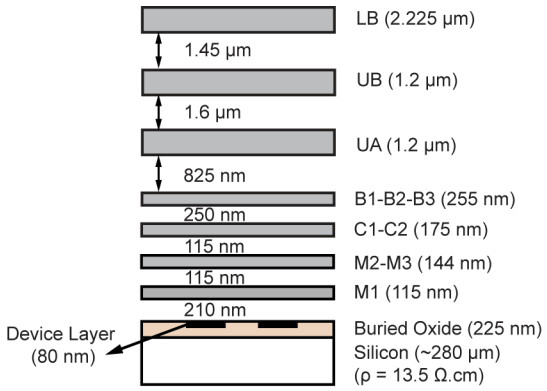

Fig. 1. Metal stack-up of the IBM 12SOI 45 nm CMOS process. All metals are copper except for the aluminum top layer (not to scale).

A. Passive Mixer

The passive mixer is based on a double balanced resistive-mixer topology (Fig. 2a), and is designed using the transistor models provided by design kit as a starting point. The transistor and interconnect parasitics with the first four layers of the metal stack-up (M1 to C1) are first extracted using Calibre [7], and the higher interconnect levels (C2 to LB) are modeled using Sonnet, a full-wave EM-simulator [8]. The 50 Ω matching networks are built using 9/8/9 µm CPW lines in the top metal layers with a simulated loss of 1.1 dB/mm. The input and output baluns are also simulated using Sonnet and show a wideband loss of 2 dB at 140-180 GHz. In this case, the primary coil is defined in the top metal layer (LB) and secondary coil uses the second metal layer (UB).

The transistor size is then optimized in order to result in a wide impedance match and a low conversion loss at 130-190 GHz. Due to the low parasitic capacitance of the 45nm SOI transistor, a W/L=400 is chosen (16x1µm/40nm) which results in a turn-on resistance of 16 Ω and a simulated conversion loss of ~12-13 dB at 130-180 GHz (including the 2 dB balun loss and GSG pad loss). The CMOS transistors are biased at Vg=0.3 V (~Vth) in order to reduce the LO power required to turn-on the devices. The transistor layout is shown in Fig. 2b. Two CMOS devices, which are differentially driven by LO signals, are interdigitated together to reduce the parasitics and to enhance mixer performance.

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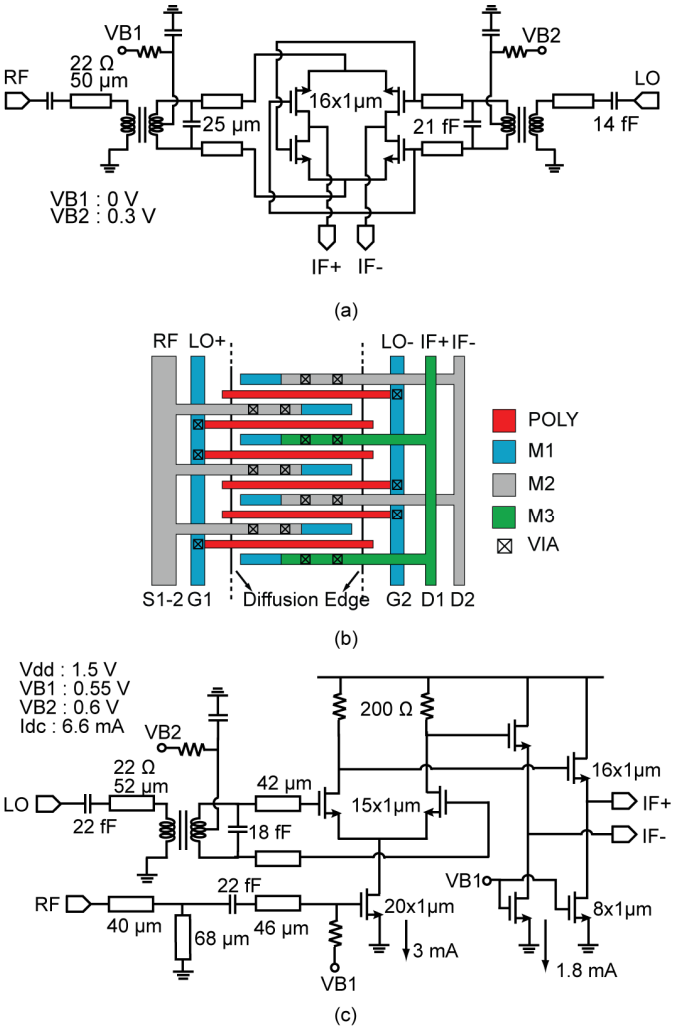

Fig. 2. (a) Schematic of passive mixer. (b) Implemented differential transistor layout (not to scale). (c) Schematic of active mixer. All transmission lines are 50 Ω unless marked. All transistors have a 40 nm gate length.

B. Active Mixer

The active mixer is based on a standard single balanced mixer topology (Fig. 2b). The RF and LO transistor sizes and current density (0.15 mA/µm) are simultaneously optimized to achieve the highest conversion gain. The mixer is resistively loaded for wideband IF operation, and the output is buffered using a source follower to achieve a 100 Ω differential output impedance. All three transistors are modeled using Calibre extraction (up to C1) and EM simulations (C2 to LB), and the same balun is used to generate the differential LO signal. The RF transistor is biased using a 1 kΩ resistor and the LO transistor pair bias is applied at the balun secondary coil so as to minimize the number of capacitors needed (series and shunt) and thus improve the conversion loss. The simulated conversion loss is 0.7 dB at 145 GHz, with a 3-dB bandwidth of 137-154 GHz.

III. MEASUREMENTS

The 50 Ω transmission line and back-to-back balun test cells are first characterized by using S-parameter measurements using a 140-220 GHz vector network analyzer. The system is first calibrated using an SOLT probe-tip calibration and a GGB CS-15 cal-substrate. A "Thru" measurement is first done, and the transmission-line losses obtained using 200, 400, and 600 µm line measurements. The measured loss is ~2.1 dB/mm which is higher than the simulated value of 1.2 dB/mm (Fig. 3). M. Seo et al. found the same results on a 65nm CMOS, and the additional loss is not yet explained [1]. The measured back-to-back balun loss is 4 dB at 160 GHz with an acceptable impedance match (S_{11} < -8 dB).

The CMOS mixers are shown in Fig. 5. The RF port return loss is measured using S-parameters, and the conversion gain is characterized using the setup shown in Fig. 6. In order to generate the RF and LO signals, a x12 multiplier chain on the RF port and a x2 multiplier on the LO port are used. The RF and LO signals are measured using waveguide couplers and power meters simultaneously during DUT characterization. One of the IF differential outputs is terminated off-chip and the IF measurements are done using a 26 GHz spectrum analyzer. A 3 dB value is added to the measured conversion loss to account for the power loss in the terminated port.

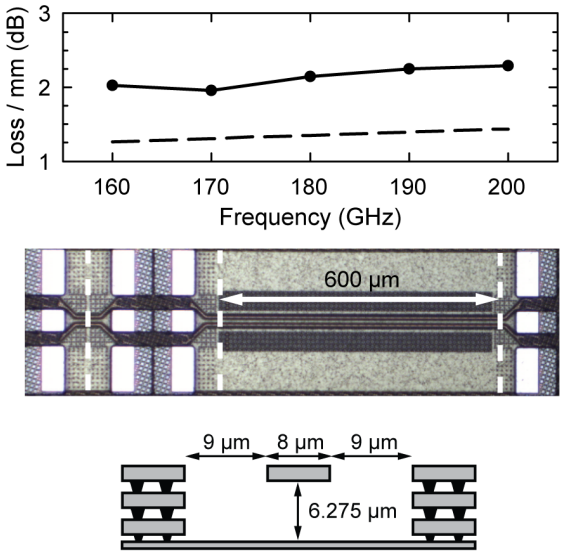

Fig. 3. Measured (solid) and simulated (dashed) 50Ω line (top). GSG "Thru" and 600 µm –long transmission line used for line loss measurements (middle). 50 Ω transmission line cross-section (bottom).

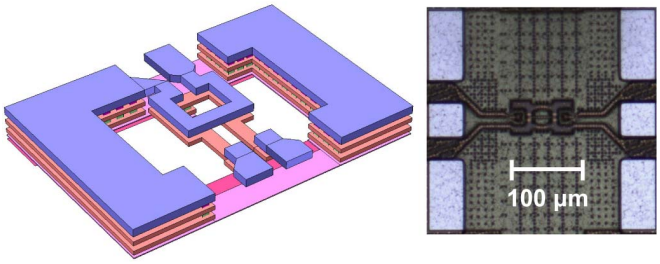

Fig. 4. Balun 3D view (left) and back to back balun test cell (right). Spirals have a side dimension of 20 µm with a 4 µm trace width.

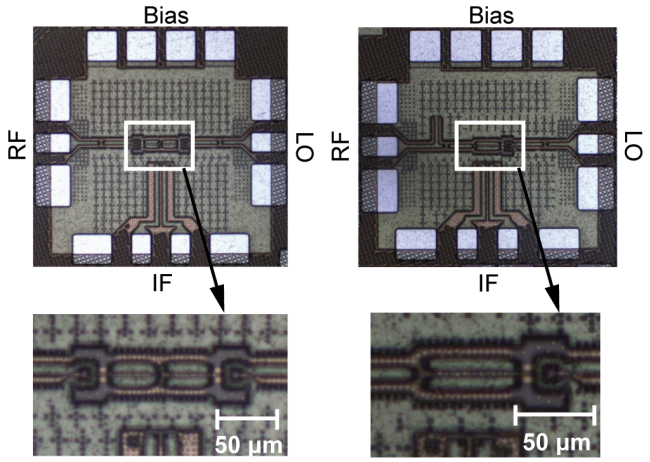

Fig. 5. Chip microphotographs of passive (left) and active (right) mixers. Both mixers occupy an area of 568x580 µm^2 including all pads.

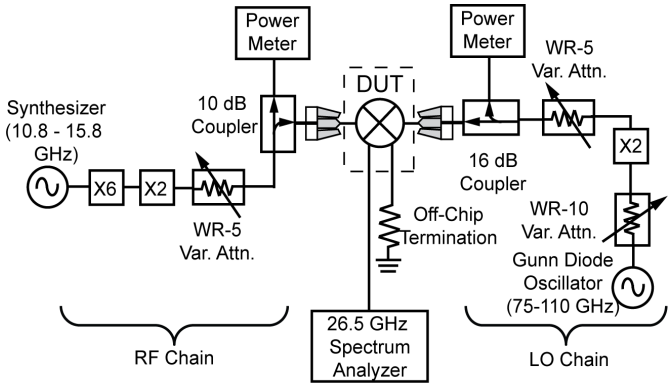

Fig. 6. Measurement setup for the passive and active mixers.

The measured passive mixer return loss agrees well with simulations and is < -8 dB at 140-180 GHz (Fig. 7a). Fig. 7b presents the mixer conversion gain vs. RF frequency with a fixed LO frequency at 156.3 GHz. Note the very wide USB and LSB IF bandwidth achieved of 26 GHz (limited by the spectrum analyzer). Measurements show a conversion gain of 12-13 dB at 130-185 GHz at an LO power of 2.8 dBm (~0 dBm at the mixer transistor pair which is quite low for a passive mixer). The conversion gain vs. LO power is shown in Fig. 7c, and +3 dBm of LO power is required at the GSG pads for best mixer performance. The RF power is also swept up to

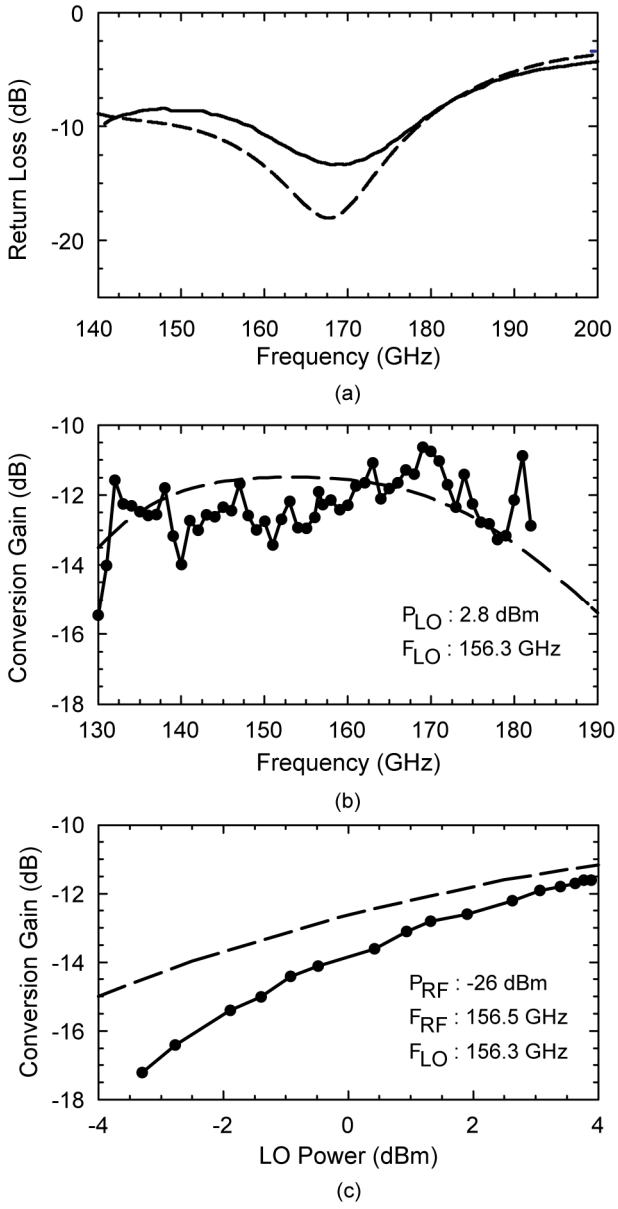

Fig. 7. Passive Mixer: (a) Measured (solid) and simulated (dashed) return loss, (b) conversion gain vs. frequency, and (c) conversion gain vs. LO power. Measurements include RF and LO input balun loss of ~2 dB and are referenced to the GSG pads.

-16 dBm (limited by measurement setup), and no compression was observed. The passive mixer does not consume any DC power.

A similar set of measurements were done on the active mixer, which consumes 6.6 mA from a 1.5 V supply voltage including the IF buffers. The measured return loss at the RF port is < -9 dB at 140-200 GHz (Fig. 8a). The conversion gain vs. RF frequency is shown in Fig. 8(b) and is > -5 dB at 148-158 GHz, with a 3-dB bandwidth of 145-164 GHz, and is such better than published results. A shift in the center frequency is observed from 145 GHz to 155 GHz and is most probably due to transistor models. The active mixer requires 2 dBm of LO

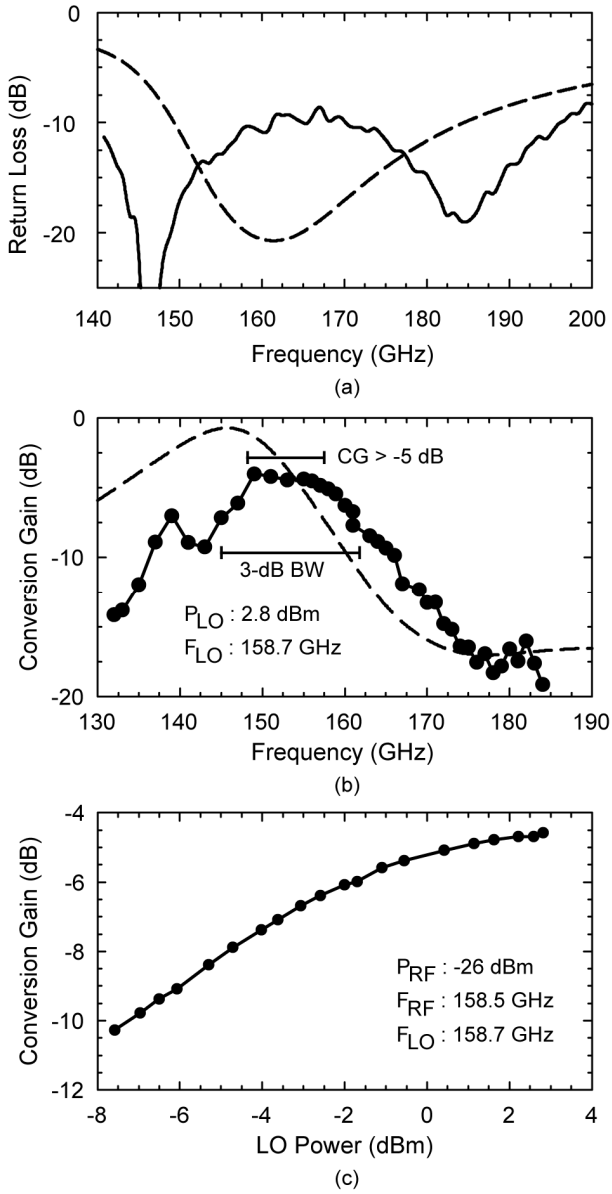

Fig. 8. Active Mixer: (a) Measured (solid) and simulated (dashed) return loss, (b) conversion gain vs. frequency, and (c) conversion gain vs. LO power. Measurements include LO input balun loss of ~2 dB and are referenced to the GSG RF and LO pads.

power at the GSG pads (~-1 dBm at the transistor pair) to achieve a conversion gain of -4.5 dB (Fig. 8c). Again,no compression is observed with -16 dBm of RF power (limited by the measurement set-up).

ACKNOWLEDGEMENTS

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REFERENCES

[1] M. Seo, et al., "A 1.1V 150 GHz amplifier with 8dB gain and +6dBm saturated output power in standard digital 65nm CMOS using dummy-prefilled microstrip lines," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig.*, Feb. 2009, pp.484-485.

[2] Z. Xu, Q.J. Gu, I. Ku, M.F. Chang, "A compact, fully differential D-band CMOS amplifier in 65nm CMOS," *Solid State Circuits Conference (A-SSCC), 2010 IEEE Asian* , vol., no., pp.1-4, 8-10 Nov. 2010.

[3] B. Cetinoneri, Y. Atesal and G. M. Rebeiz, "Low Noise W-Band Amplifiers and mW-Level 170-190 GHz Doublers in 45-nm CMOS," Submitted for publication in *IEEE Trans. Microwave Theory and Techn.*, April 2011.

[4] E. Laskin, et al., "Nanoscale CMOS Transceiver Design in the 90–170-GHz Range," *IEEE Trans. Microwave Theory and Techn.*, vol.57, no.12, pp.3477-3490, Dec. 2009.

[5] B. Heinemann *et al.*, "SiGe HBT technology with ft/fmax of 300GHz/500 GHz and 2.0 ps CML gate delay," in *IEEE Int. Electron Devices Meeting*, Dec. 2010, pp. 688–691.

[6] S. Lee, et al., "Record RF performance of 45-nm SOI CMOS Technology," *IEEE Intl. Electron Devices Meeting*, pp.255-258, 10-12 Dec. 2007.

[7] Calibre PEX. [Online]. Available: http://www.mentor.com/products/ic_nanometer_design/bl_phy_design/calibre_xrc/

[8] Sonnet, ver. 12, Sonnet Software Inc., Syracuse, NY, 1986-2008.